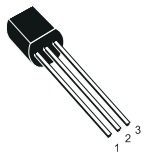
N-CHANNEL MOSFET
600V - 13Ω - 0.8A

General features

Type	V_{DSS}	$R_{DS(on)}$	I_D	Pw
L1N60A	600V	<15Ω	0.3A	3W

- 100% avalanche tested
- Extremely high dv/dt capability
- Gate charge minimized
- New high voltage benchmark

L1N60A

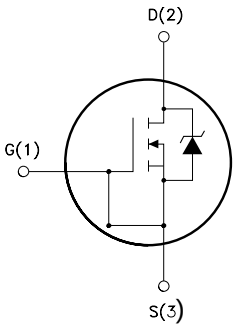


TO-92

Description

The L1N60A is a high voltage MOSFET and is designed to have better characteristics,such as fast switching time,low gate charge,low on-state restance.

Internal schematic diagram



Applications

- Switching application

Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
		TO-92	
V_{DS}	Drain-Source Voltage (V_{GS} = 0)	600	V
V_{DGR}	Drain-Gate Voltage (R_{GS} = 20KΩ)	600	V
V_{GS}	Gate-Source Voltage	± 30	V
I_D	Drain Current (continuous) at T_C = 25°C	0.3	A
I_D	Drain Current (continuous) at T_C=100°C	0.189	A
I_{DM}(1)	Drain Current (pulsed)	1.2	A
P_{TOT}	Total Dissipation at T_C = 25°C	3	W
	Derating Factor	0.25	W/°C
$V_{ESD(G-D)}$	Gate source ESD(HBM-C=100pF, R=1.5KΩ)	800	V
dv/dt(2)	Peak Diode Recovery voltage slope	4.5	V/ns
T_J T_{stg}	Operating Junction Temperature Storage Temperature	-55 to 150	°C

1. Pulse width limited by safe operating area
2. I_{SD} ≤0.3A, di/dt ≤200A/μs, V_{DD} =80%$V_{(BR)DSS}$

Table 2. Thermal resistance

Symbol	Parameter	Value	Unit
		TO-92	
$R_{thj\text{-}case}$	Thermal resistance junction-case Max	--	°C/W
$R_{thj\text{-}a}$	Thermal resistance junction-ambient Max	120	°C/W
$R_{thj\text{-}lead}$	Thermal resistance junction-lead Max	40	°C/W
T_l	Maximum lead temperature for soldering purpose	260	°C

1. When mounted on 1 inch² FR-4 board, 2 Oz Cu

Table 3. Avalanche data

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche Curent, Repetitive or Noy-Repetitive (pulse width limited by Tj Max)	0.8	A
E_{AS}	Single pulse avalanche Energy (starting Tj=25°C, Id=Iar, Vdd=50V)	60	mJ

Electrical characteristics

(T_{CASE}=25°C unless otherwise specified)

Table 4. On/off states

Symbol	Parameter	Test Condictions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	I_D = 1mA, V_{GS}= 0	600			V
I_{DSS}	Zero Gate Voltage Drain Current (V_{GS} = 0)	V_{DS} = Max Rating, V_{DS} = MaxRating @125°C			1 50	μA μA
I_{GSS}	Gate Body Leakage Current (V_{DS} = 0)	V_{GS} = ±20V			±10	μA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}= V_{GS}, I_D = 50μA	3	3.75	4..5	V
$R_{DS(on)}$	Static Drain-Source On Resistance	V_{GS}= 10V, I_D= 0.4A		13	15	Ω

Table 5. Dynamic

Symbol	Parameter	Test Condictions	Min.	Typ.	Max.	Unit
g_{fs} (1)	Forward Transconductance	V_{DS} =15V, I_D = 0.4A		0.5		S
C_{iss} C_{oss} C_{rss}	Input Capacitance Output Capacitance Reverse Transfer Capacitance	V_{DS} =25V, f=1 MHz, V_{GS}=0		94 17.6 2.8		pF pF pF
$C_{oss\ eq}$ (2).	Equivalent Output Capacitance	V_{GS}=0, V_{DS} =0V to 480V		11		pF
Q_g Q_{gs} Q_{gd}	Total Gate Charge Gate-Source Charge Gate-Drain Charge	V_{DD}=480V, I_D = 0.8A V_{GS} =10V (see Figure 11)		4.9 1 2.7	6.9	nC nC nC

1. Pulsed: pulse duration=300μs, duty cycle 1.5%
2. $C_{oss\ eq.}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} inceases from 0 to 80% V_{DSS}

Table 6. Switching times

Symbol	Parameter	Test Condictions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r $t_{d(off)}$ t_f	Turn-on Delay Time Rise Time Turn-off Delay Time Fall Time	V_{DD}=300 V, I_D= 0.4A, R_G=4.7Ω, V_{GS}=10V (see Figure 19)		5.5 5 13 28		ns ns ns ns

Table 7. Source drain diode

Symbol	Parameter	Test Condictions	Min	Typ.	Max	Unit
I_{SD}	Source-drain Current				0.8	A
I_{SDM}(1)	Source-drain Current (pulsed)				2.4	A
V_{SD}(2)	Forward on Voltage	I_{SD}=0.8A, V_{GS}=0			1.6	V
t_{rr} Q_{rr} I_{RRM}	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	I_{SD}=0.8A, di/dt = 100A/μs, V_{DD}=20V, Tj=25°C		135 216 3.2		ns nC A
t_{rr} Q_{rr} I_{RRM}	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	I_{SD}=0.8A, di/dt = 100A/μs, V_{DD}=20V, Tj=150°C		140 224 3.2		ns nC A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration=300μs, duty cycle 1.5%

Table 8. Gate-source zener diode

Symbol	Parameter	Test Condictions	Min.	Typ.	Max.	Unit
BV_{GSO}(1)	Gate-source Braekdown Voltage	Igs=±1mA (Open Drain)	30			V

L1N60A

Electrical characteristics (curves)

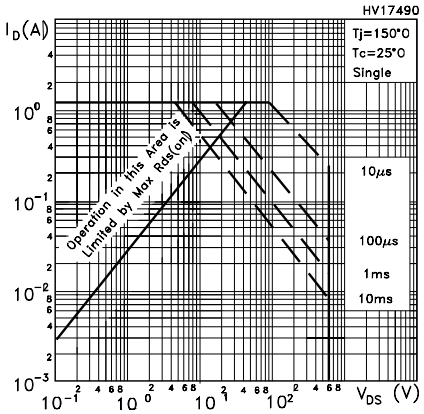


Figure 1. Safe operating area for TO-92

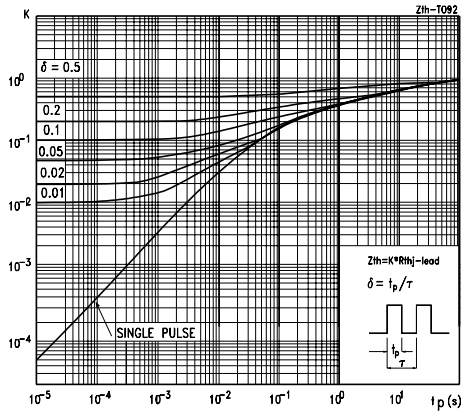


Figure 2. Thermal impedance for TO-92

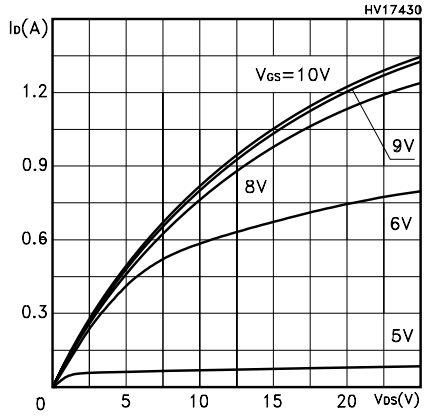


Figure 3. Output characterisics

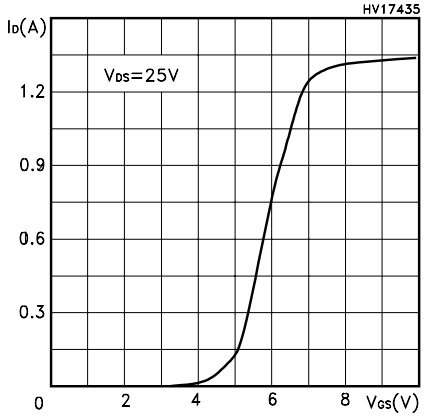


Figure 4. Transfer characteristics

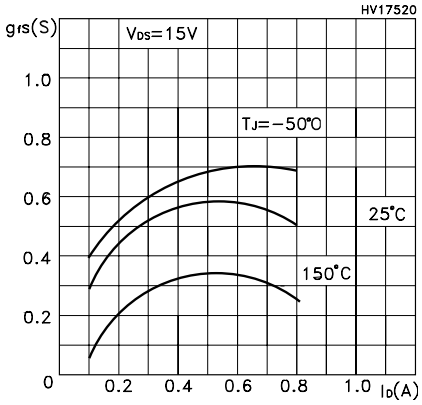


Figure 5. Transconductance

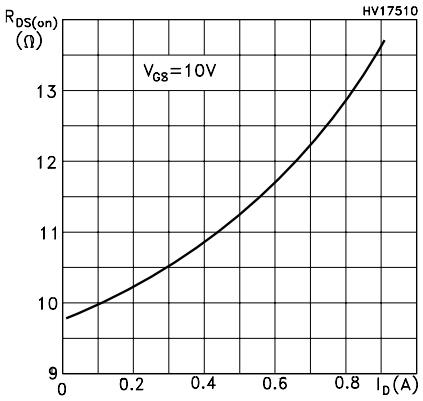


Figure 6. Static drain-source on resistance

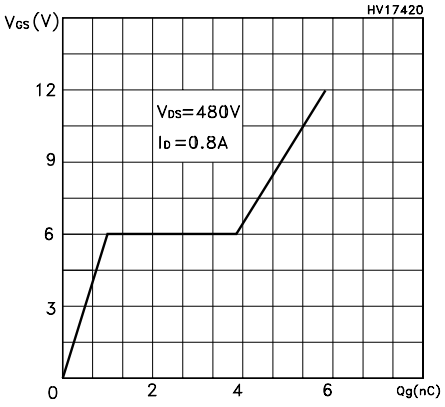


Figure 7. Gate charge vs gate-source voltage

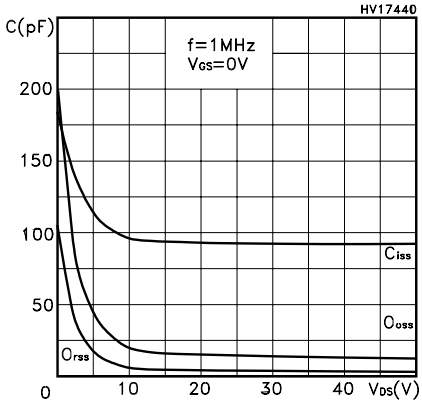


Figure 8. Capacitance variations

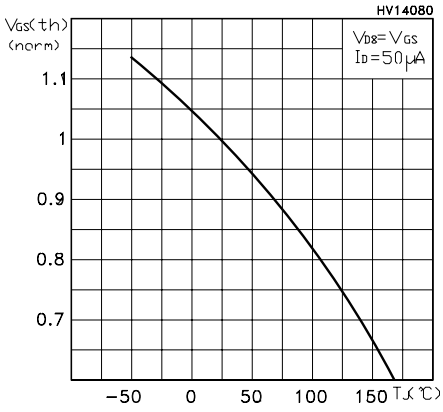


Figure 9. Normalized gate threshold voltage vs temperature

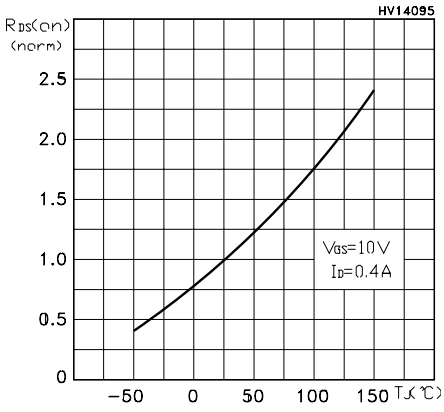


Figure 10. Normalized on resistance vs temperature

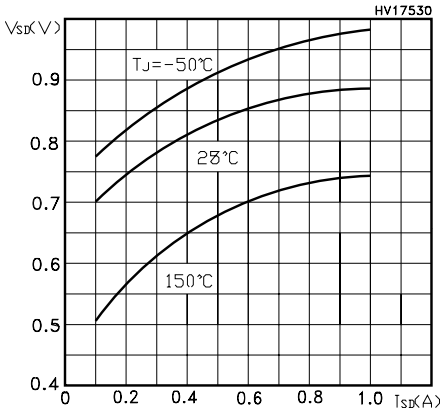


Figure 11. Source-drain diode forward characteristics

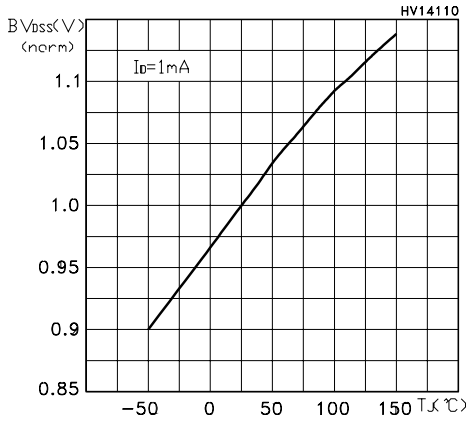


Figure 12. Normalized B_{VDSS} vs temperature

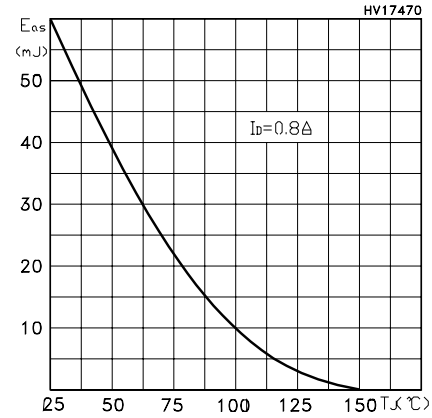


Figure 13. Maximum avalanche energy vs temperature

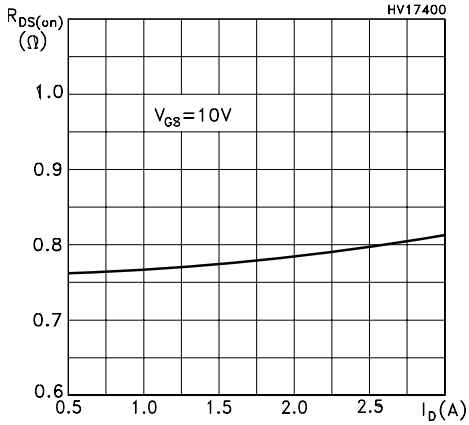


Figure 14. Max Id Current vs Tc

Test circuit

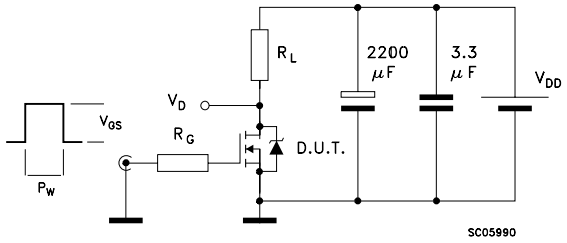


Figure 15. Switching times test circuit for resistive load

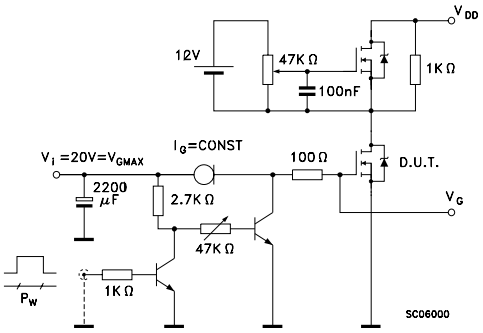


Figure 16. Gate charge test circuit

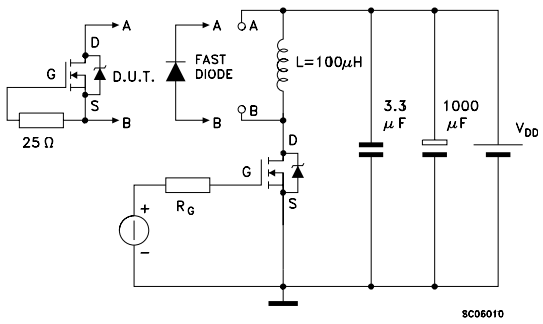


Figure 17. Test circuit for inductive load switching and diode recovery times

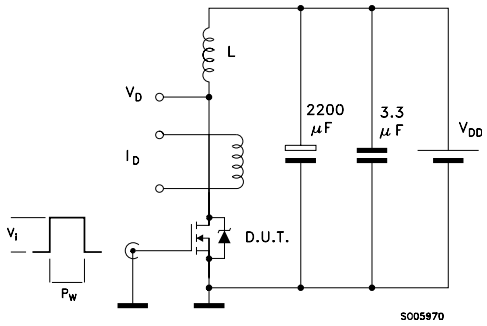


Figure 18. Unclamped Inductive load test circuit

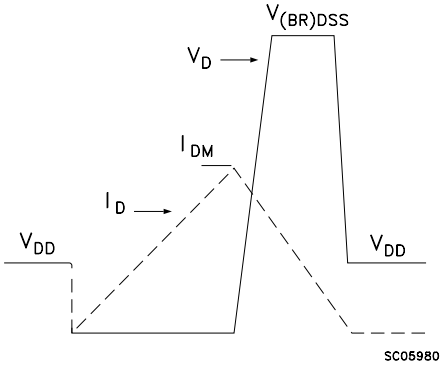


Figure 19. Unclamped inductive waveform

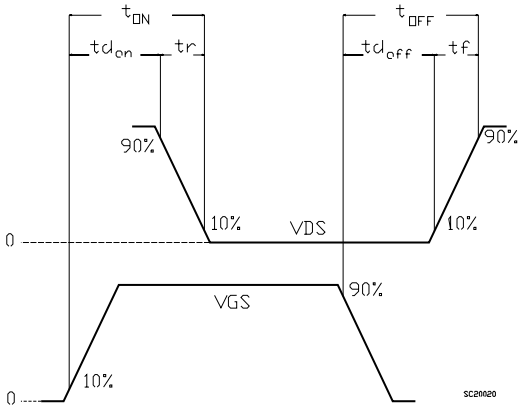


Figure 20. Switching time waveform

L1N60A

TO-92 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	4.32		4.95	0.170		0.194
b	0.36		0.51	0.014		0.020
D	4.45		4.95	0.175		0.194
E	3.30		3.94	0.130		0.155
e	2.41		2.67	0.094		0.105
e1	1.14		1.40	0.044		0.055
L	12.70		15.49	0.50		0.610
R	2.16		2.41	0.085		0.094
S1	0.92		1.52	0.036		0.060
W	0.41		0.56	0.016		0.022
V		5°			5°