Ordering number : ENA2003

SANYO Semiconductors
DATA SHEET

An ON Semiconductor Company

Bi-CMOS IC

LV5065VB — Built-in 2-channels DC/DC Converter Controller

Overview

The LV5065VB is a high efficiency DC/DC converter controller with 2-channels IC adopting a synchronous rectifying system. Incorporating numerous functions on a single chip with easy external setting, it can be used for a wide variety of applications. This device is optimal for use in internal power supply systems which are used in electronic devices, LCD-TVs, DVD recorders, etc.

Functions

- Step-down DC/DC converter controller with 2-channel
- Built-in input UVLO circuit, Over current detection function, soft-start/soft-stop function and Start-up delay circuit
- Built-in output voltage monitor function (Under voltage protection with power good and timer latch)
- 180 degree interleaving operation during 1-phase to 2-phase
- Synchronized operation is possible (Master-slave operation is possible when using plural devices)

Specifications

Absolute Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{CC} max		20	V
Output peak current	I_{OUT}		±1.0	A
Allowable power dissipation	Pd max	Mounted on a specified board *	0.95	W
Operating temperature	Topr		-20 to 85	°C
Storage temperature	Tstg		-55 to +150	°C

*: Specified board: 114.3mm × 76.1mm ×1.6mm, glass epoxy board.

Caution 1) Absolute maximum ratings represent the value which cannot be exceeded for any length of time.

Caution 2) Even when the device is used within the range of absolute maximum ratings, as a result of continuous usage under high temperature, high current, high voltage, or drastic temperature change, the reliability of the IC may be degraded. Please contact us for the further details.

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Parameter		Symbol	Conditions	Ratings	Unit
Allowable terminal voltage					
1	Between HDRV1,2, CBOOT1,2 and PGND			25	V
2	Between HDRV1,2, CBOOT1,2 and SW			6.5	V
3	V_{IN}, ILIM1,2, RSNS1,2, SW1,2, PGOOD1,2			20	V
4	VLIN5, V_{DD}, LDRV1,2			6.5	V
5	COMP1,2, FB1,2, SS1,2, UV_DELAY,TD1,2, CT, CLKO			VLIN5+0.3	V

Recommended Operating Condition at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Recommended supply voltage range	V_{IN}		9.5 to 18	V

Electrical Characteristics at Ta = 25°C, V_{IN}=12V, Unless especially specified.

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
System						
Reference voltage for comparing	V_{REF}	V_{IN} = 15	1%	0.633	+1%	V
Supply current 1	$I_{CC}1$	TD1,2 = 5V, V_{IN} = 15 (Except for the Ciss charge)	4	6	8	mA
Supply current 2	$I_{CC}2$	TD1,2 = 0V, V_{IN} = 15	0.8	1.4	2.0	mA
5V supply voltage	VLIN5	V_{IN} = 15, IVIN5 = 0 to 10mA	5.10	5.30	5.50	V
Over-current sense comparator offset	$V_{CL}OS$		-5		+5	mV
Over-current sense reference current source	I_{CL}	V_{IN} = 12 to 15V *1	60.45	65.00	69.55	μA
Soft start source current	$I_{SS}SC$	TD = 5V	-1.8	-3.5	-7.0	μA
Soft start sink current	$I_{SS}SK$	TD = 0V	0.2	1.0		mA
Soft start clamp voltage	$V_{SS}T0$		1.2	1.6	2.0	V
UV_DELAY source current	$I_{SC}UVD$	UV_DELAY = 2V	-4.3	-8.6	-17.2	μA
UV_DELAY sink current	$I_{SK}UVD$	UV_DELAY = 2V	0.2	1.0		mA
UV_DELAY threshold voltage	V_{UVD}		1.5	2.4	3.5	V
UV_DELAY operating voltage	V_{UVP}	100% at VFBx = V_{REF}	77	82	87	%
VUVP detection hysteresis	ΔV_{UVP}			8		%
Over-voltage detection	$V_{O}VP$	100% at VFBx = V_{REF}	113	118	123	%
Output discharge transistor ON resistance	$V_{SW}ON$		5	10	20	Ω
Output part						
CBOOT leakage current	I_{CBOOT}	VCBOOT = VSW + 6.5V			10	μA
HDRVx LDRVx source current	$I_{SC}DRV$			1.0		A
HDRVx LDRVx sink current	$I_{SK}DRV$			1.0		A
HDRVx lower ON resistance	$R_{H}DRV$	I_{OUT} = 500mA		1.5	2.5	Ω
LDRVx lower ON resistance	$R_{L}DRV$	I_{OUT} = 500mA		1.5	2.5	Ω
Synchronous ON prevention dead time 1	$T_{dead}1$	LDRV OFF→HDRV ON		50		ns
Synchronous ON prevention dead time 2	$T_{dead}2$	HDRV OFF→LDRV ON		50		ns
LDRV_ON delay time	Mdead	HDRV OFF→LDRV ON at MAX_Duty		50		ns
Oscillator						
Oscillation frequency	f_{osc}	V_{IN} = 15, CT=270pF	170	200	230	kHz
Oscillation frequency range	$f_{osc}op$	V_{IN} = 15	100		500	kHz
Maximum ON duty	D_{ON} max	V_{IN} = 15, CT=270pF	90		95	%
Minimum ON time	T_{ON} min	V_{IN} = 15, CT=270pF		120		ns
Upper-side voltage saw- tooth wave	$V_{saw}H$	f_{OSC}=200kHz, RSNS=V_{IN}(0Ω)		2.75	3.2	V
Lower-side voltage saw-tooth wave	$V_{saw}L$	f_{OSC}=200kHz		1	1.2	V
ON time difference between CH1 to CH2	ΔTdead			5		%

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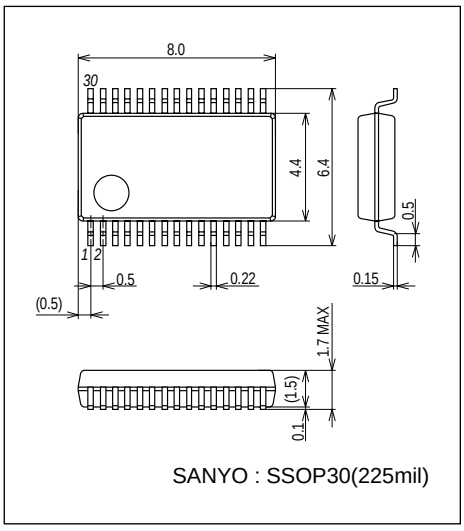
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Error Amplifier						
Error amplifier input current	I_{FB}		-200	-100	200	nA
COMP pin source current	$I_{COMP}SC$			-100	-18	μA
COMP pin sink current	$I_{COMP}SK$		18	100		μA
Error amplifier gm	gm		500	700	900	umho
Current detection amplifier gain	GISNS		3	4	5	
Logic output						
Power Good low level source current	$I_{pwrgd}L$	V_{PGOOD} = 0.4V	0.5	1.0		mA
Power Good high level leakage current	$I_{pwrgd}H$	V_{PGOOD} = 15V			10	μA
TP pin threshold voltage	$V_{ON}TD$	When the voltage of the TD pin rises	1.5	2.6	3.5	V
TP pin high impedance voltage	$V_{TD}H$	When V_{IN} and VLIN5 pins are set to open	4.5	5.2	5.5	V
TD pin charge source current	$I_{TD}SC$		-1.8	-3.5	-7.0	μA
TD pin discharge sink current	$I_{TD}SK$		0.2	1.0		mA
CLKO high level voltage	$V_{CLKO}H$	I_{CLKO} = 1mA	0.7V5LIN			V
CLKO low level voltage	$V_{CLKO}L$	I_{CLKO} = 1mA			0.3V5LIN	V
Protection function						
V_{IN} UVLO Release voltage	V_{UVLO}		3.5	4.1	4.3	mA
UVLO Hysteresis	ΔV_{UVLO}			0.4		μA

*1: The overcurrent detection standard current source assumes it a measurement standard

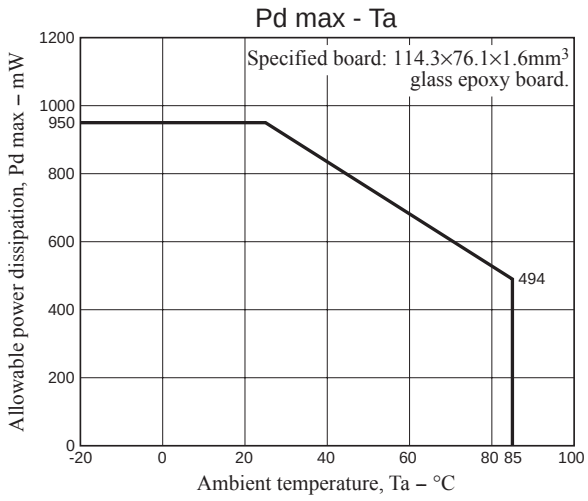
Package Dimensions

unit : mm (typ)

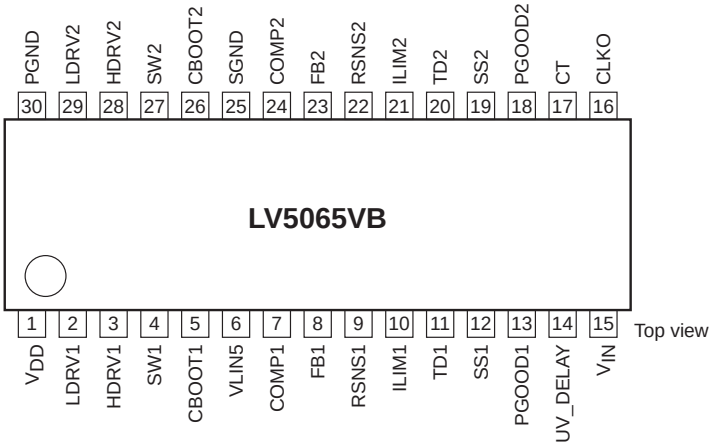
3421



SANYO : SSOP30(225mil)

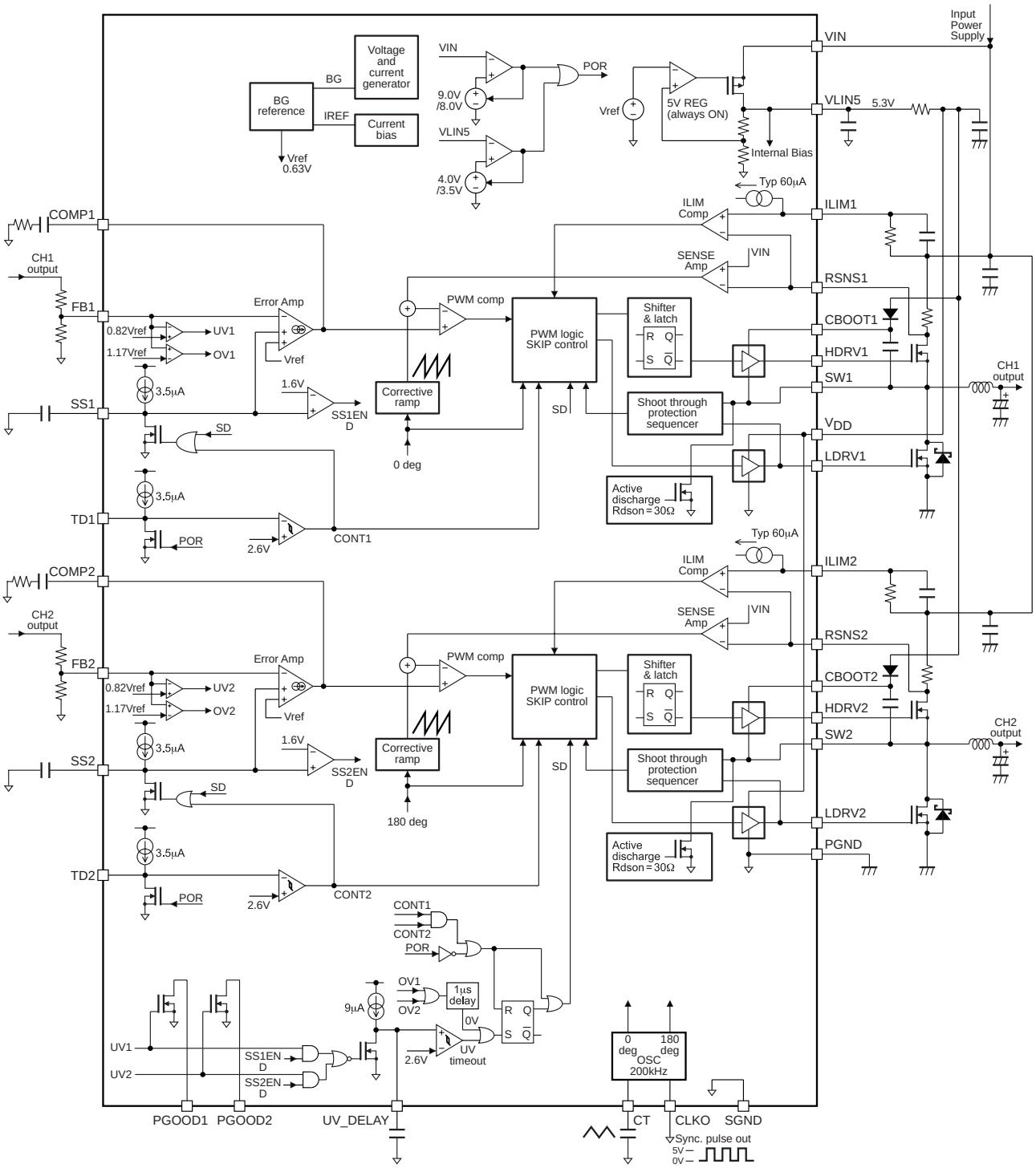


Pin Assignment



Top view

Block Diagram



Pin Functions

Pin No.	Pin name	Description
1	V_{DD}	Power supply pin for the gate drive of an external lower-side MOS-FET. This pin is connected to the VLIN5 pin through a filter.
2	LDRV	The gate drive pin of an external lower-side MOS-FET of channel 1. This pin has the signal input part for prevention of short-through of both the upper and lower MOS-FETs. When the voltage of this pin becomes less than 2V, the HDRV pin is turned on.
3	HDRV1	The gate drive pin for an external upper side MOS-FET of channel 1.
4	SW1	This pin is connected with the switching node of channel 1. A source of an external upper side MOSFET and a drain of an external lower side MOS-FET are connected with this pin. This pin becomes the return current path of the HDRV pin. This pin is connected with a transistor drain of the discharge MOS-FET for SOFT STOP in the IC (typical 30Ω). Also, this pin has the signal output part for the short through prevention of both the upper and lower MOS-FETs. When this terminal voltage becomes 2V or less for PGND, the LDRV pin is turned on.
5	CBOOT1	The bootstrap capacity connection pin of channel 1. The gate drive power of upper MOSFET is provided by this pin. This pin is connected to the V_{DD} pin through a diode and is connected to the SW pin through the bootstrap capacity.
6	VLIN5	The output pin of an internal regulator of 5V. The current is provided by the V_{IN} pin. Also, power supply of the control circuit in the IC is provided by this pin. Connect an output capacitor of 1μF between this pin and SGND. A regulator of 5V operates, even if the IC is in the standby state. This pin is monitored by an UVLO function and the IC starts by the voltage of 4.0V or more (the IC is off by the voltage of 3.5V or less.)
7	COMP1	The phase compensation pin of channel 1. The output of an internal transformer conductance amplifier is connected. Connect an external phase compensation circuit between this pin and SGND.
8	FB1	Feed back input pin of channel 1. The minus terminal (-) of the trans conductance amplifier is connected. The voltage generated when the output voltage was divided by a resistor is input into this pin. The converter operates so that this pin becomes an internal reference voltage (V_{REF}=0.63V). Also, this pin is monitored by the comparators UVP and OVP. When the voltage of this pin becomes less than 82% of the set voltage, the PGOOD pin is low level. A timer of the UV_DELAY function operates. Also, when the voltage of this pin becomes more than 118% of the set voltage, the IC latches off.
9	RSNS1	Channel 1 side input pin of the over current detection comparator / the current detection amplifier. To detect resistance, this pin is connected to the under side of a resistor for the current detection between the V_{IN} pin and the DRAIN of the upper MOS-FET. Also, to use the ON resistance of MOS-FET for the current detection, connect this pin to the SOURCE of the upper MOS-FET. To prevent the common impedance of main current to the detection-voltage, this pin is connected by independent wiring.
10	ILIM	The pin to set the trip point for over current detection of channel 1. Since the SINK current source of 65μA (ILIM) is connected in the IC, the over-current detection voltage (ILIM × RLIM) is generated by connecting a resistor RLIM between this pin and the V_{IN} pin. The over-current is detected by comparing the voltage between the V_{IN} pin and the ILIM pin to the current detection resistance RSNS or both end voltage of the upper MOSFET.
11	TD	Start-up delay pin of channel 1. The time until the IC starts after releasing POR is set by connecting a capacitor between this pin and SGND. After releasing POR, an external capacitor is charged up by the constant current source of 3.5μA in the IC. When this terminal voltage becomes 2.6V or more, The IC starts. Also, when this terminal voltage becomes 2.6V or less, The IC becomes the standby state. If external capacitor is not connected, the IC instantly starts after releasing POR.
12	SS1	The pin to connect a capacitor for soft start of channel 1. After releasing POR, when the voltage of the TD pin becomes 2.6V or more, the SS1 pin is charged by an internal constant current source of 3.5μA. Since this pin is connected to the positive (+) input of the transformer conductance amplifier, the ramp-up wave form of the SS pin becomes the ramp-up wave form of the output. During POR operations and after the UV_DELAY time-out, the SS1 pin is discharged
13	PGOOD	The power good pin of channel 1. The open drain MOS-FET of the withstand of 18V is connected in the IC. When the output voltage of channel 1 is less than -13% for the setup voltage, the low level is output. This pin has hysteresis of about (V_{REF} × 8.0%).
14	UV_DELAY	Common UVP DELAY pin to channel 1 and channel 2. By connecting a capacitor between this pin and SGND, the time until the IC latches off after detecting the UVP state can be set. Also, after channel 1 or channel 2 terminated the soft-start function, when the output voltage becomes 82% or less for the setup voltage, an external capacitor is charged by the constant current source of 8.6μA in the IC. When this terminal voltage becomes 2.6V or more, the IC is latched off. If an external capacitor is not connected, the IC is instantly latched off after detecting the UVP state. Also, when this pin is shorted to GND, the UV_DELAY function is not operated.

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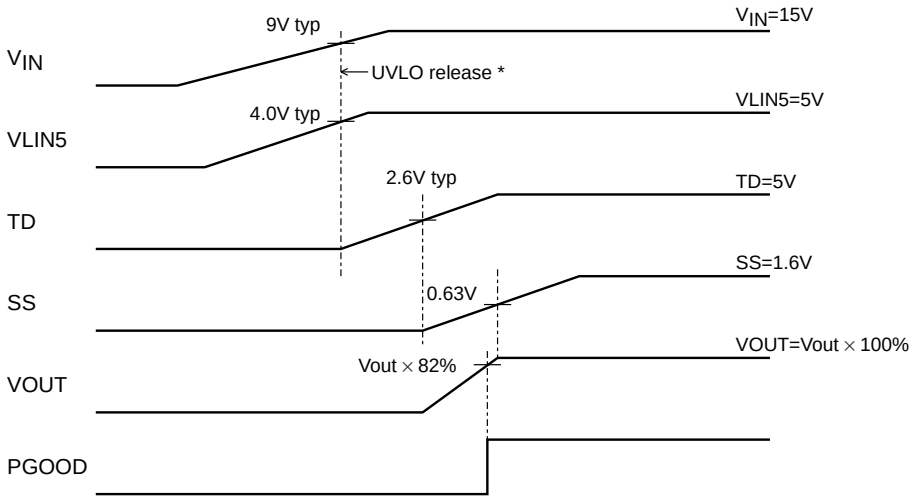
Pin No.	Pin name	Description
15	V_{IN}	Power supply pin of the IC. This pin is observed by the UVLO function and IC starts by 9.0V or more. (After starts, stop by 8.0V or less.)
16	CLKO	The clock output pin. The clock that synchronized to the oscillation waveform of the CT pin is output. To synchronize two or more LV5052Vs, the CLKO pin of the device that becomes a master is connected to the CT pin of the device that becomes a slave. When two or more the devices are synchronized and the start-up timing is changed by using the TD pin between each device, the earliest start-up device is determined as the master.
17	CT	The pin to connect an external capacitor for the oscillator. Connect a capacitor between this pin and SGND. When a capacitor of 270pF is connected between this pin and GND, the oscillation frequency can be set up by 200kHz. Also, this pin is applied by an external clock signal. The PWM operation is performed by the frequency of applied clock signal. When an external clock signal is applied, the rectangular wave of 0V in low level and from 0V / 3.3V to 5V in high level is applied. The rectangular wave source needs the fan-out of 1mA or more.
18	PGOOD2	The power good pin of channel 2.
19	SS2	The pin to connect a capacitor for soft start of channel 2.
20	TD2	Start-up delay pin of channel 2.
21	ILIM2	The pin to set the trip point for over current detection of channel 2.
22	RSNS2	Channel 2 side input pin of the over current detection comparator / the current detection amplifier.
23	FB2	Feed back input pin of channel 2.
24	COMP2	The phase compensation pin of channel 2.
25	SGND	The system ground of the IC. The reference voltage is generated based on this pin. This pin is connected to the power supply system ground.
26	CBOOT2	The bootstrap capacity connection pin of channel 2.
27	SW2	This pin is connected with the switching node of channel 2.
28	HDRV2	The gate drive pin for an external upper side MOS-FET of channel 2.
29	LDRV2	The gate drive pin of an external lower-side MOS-FET of channel 2.
30	PGND	Power ground pin. This pin becomes the return current path of the LDRV pin.

Start-up Sequence

Each signal control timing at power supply ON is as below.

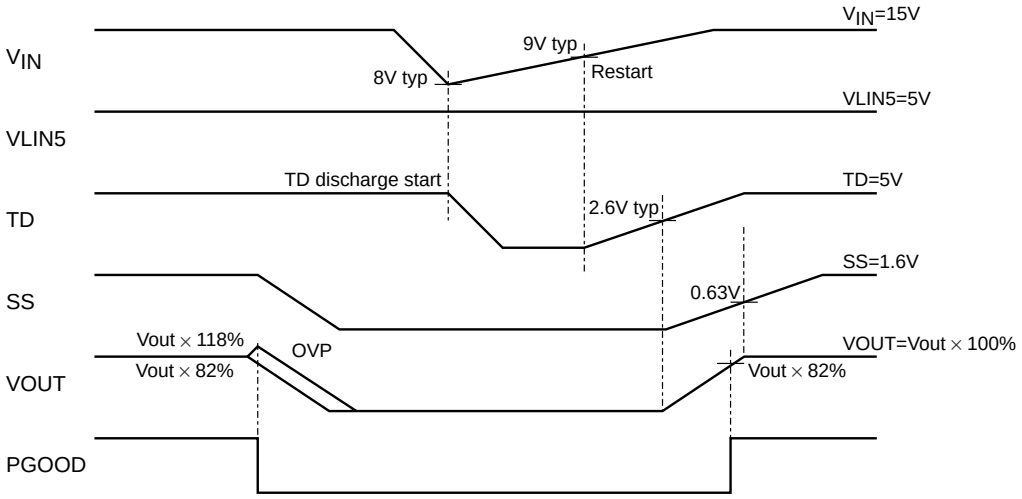


***** Starts charging the TD at the trigger point of either VIN > 9V(typ) or VLIN5 > 4.5V(typ), whichever is later.

Protection Operate Sequence

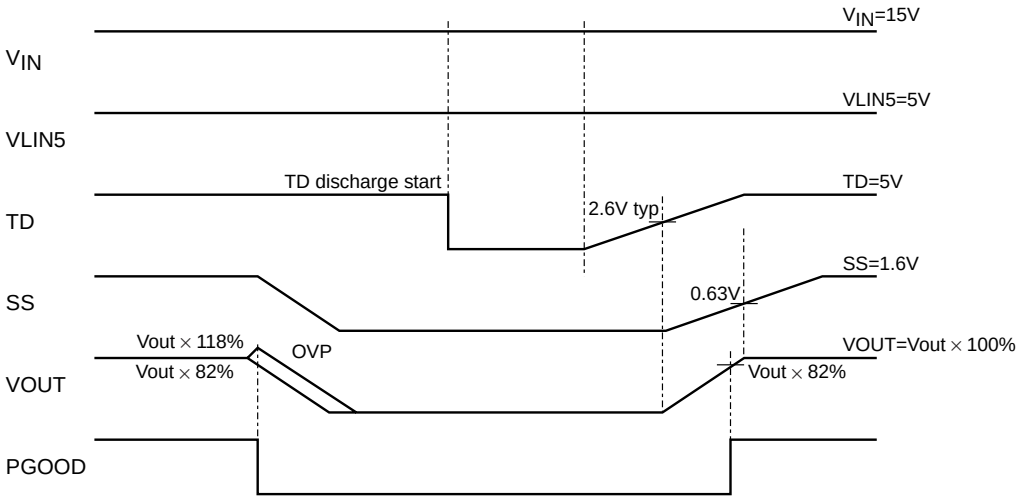
(1) Latch-off release by UVLO

The signal control timing diagram for resetting the latch-off condition using UVLO is shown below.



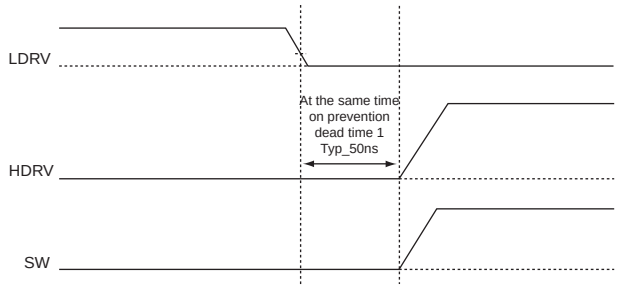
(2) Latch off release by TD

The signal control timing diagram for resetting the latch-off condition using UVLO is shown below.



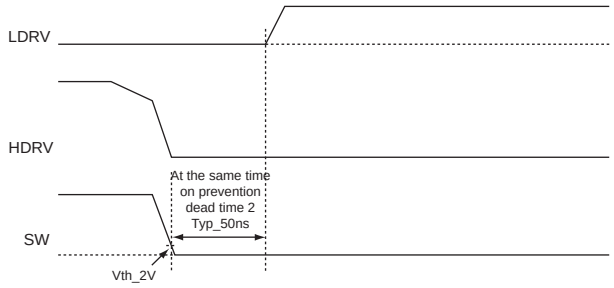
Shoot through protection

At the same time on prevention dead time1 (Tdead1): LDRV OFF → HDRV ON



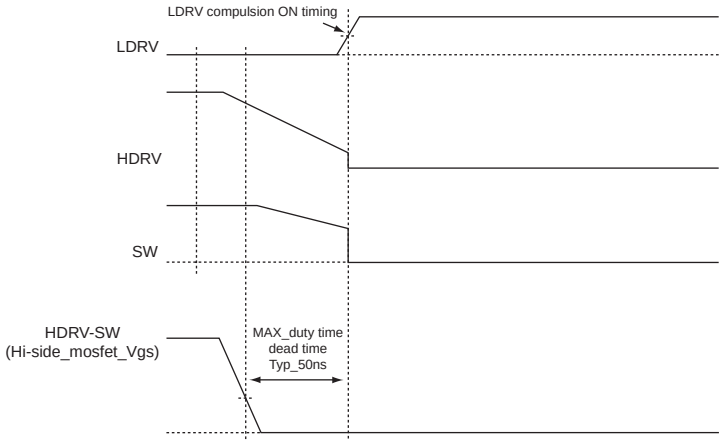
- HDRV is turned on after typ_50ns after LDRV became 2V in the LDRV off → HDRV on.

At the same time on prevention dead time2 (Tdead2): HDRV OFF → LDRV ON



- LDRV is turned on after typ_50ns after SW became 2V in the HDRV off → LDRV on.

LDRV compulsion ON delay time



- Even if SW does not reach 2V when HDRV reaches MAX_duty, LDRV is performed ON of forcibly after about 50ns. This price changes by Ciss of the external MOSFET.

Synchronized operation

A recommended circuit for synchronizing the LV5056VB is shown below.