



SANYO Semiconductors

# DATA SHEET

## LV5106FN — Bi-CMOS IC For cell phone system Power supply

### Overview

The LV5106FN is a power supply for a cell phone system that integrates four series regulators, two de-writers, and an LED driver (with 5V output) on a single chip.

### Functions

- REG×4 (CMOS output)
- DET circuit (one for REG1, one for VBAT (with reset output))
- Thermal shutdown circuit (150°C)
- Three-color LED driver (charge pump 5V output incorporated)
- FRONT LED driver
- Mic bias output

### Features

- Low power consumption 4μA when REG4 and VBATDET operate  
30μA when REG1, REG2, REG3, and REG4 + DET1 and VBATDET operate
- Built-in charge pump circuit VBAT : 3.2V to 4.5V, 5V constant output with a load of 80mA
- Built-in 3-color LED drive circuit Three independent colors, 128-step PWM intensity control

### Specifications

#### Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V <sub>CC</sub> max		7	V
Allowable power dissipation	P <sub>d</sub> max	Ta ≤ 75°C *Mounted on a board.	440	mW
Operating temperature	T <sub>opr</sub>		-30 to +75	°C
Storage temperature	T <sub>stg</sub>		-40 to +125	°C

\* Mounted on a 50.0mm×50.0mm×0.8mm, glass epoxy board.

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# LV5106FN

## Operating Conditions at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage 1	VBAT	29, 33pin	3.2 to 4.5	V
Supply voltage 2	VBATCP	3pin	3.2 to 5.9	V

## Electrical Characteristics Ta = 25°C, VBAT = 3.6V, VCHARGE = 0V, unless otherwise specified.

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
<b>Analog :</b>						
<b>Current dissipation</b>						
Current dissipation 1	I <sub>CC1</sub>	REG4, VBATDET : ON REG1, 2, 3, charge pump, DET1 : OFF no-load VBAT = 3.2V to 4.2V		4	10	μA
Current dissipation 2	I <sub>CC2</sub>	REG1, 2, 4, DET1, VBATDET : ON REG3, charge pump : OFF no load		25	35	μA
Current dissipation 3	I <sub>CC3</sub>	REG3, 4, VBATDET : ON REG1, 2, DET1, charge pump : OFF no load		20	28	μA
Current dissipation 4	I <sub>CC4</sub>	REG1, 2, 3, 4, DET1, VBATDET : ON charge pump : OFF no load		30	42	μA
Current dissipation 5	I <sub>CC5</sub>	REG1, 2, 3, 4, DET1, VBATDET : ON charge pump : OFF no load ECO : L		15	21	μA
Current dissipation 6	I <sub>CC6</sub>	REG1, 2, 3, 4, charge pump, DET1, VBATDET : ON no load		5	8	mA
<b>REG1</b>						
Output voltage 1	V <sub>O1</sub>	I <sub>O</sub> = 30mA, ECO = H	2.74	2.8	2.86	V
Output voltage 2	V <sub>O1E</sub>	I <sub>O</sub> = 30mA, ECO = L	2.71	2.8	2.89	V
Output voltage 3	ΔV <sub>O1</sub>	(I <sub>O</sub> = 30mA, REG1 output voltage at ECO = H) - (I <sub>O</sub> = 10mA, REG1 output voltage at I <sub>O</sub> = 10 mA and ECO = L)	0	15	35	mV
Output voltage 4	ΔV <sub>O2</sub>	I <sub>O</sub> = 30mA (charge-pump on-time REG1 output voltage) – (charge-pump off-time REG1 output voltage)	-35		35	mV
Drop out voltage	VDR1	VBAT = 2.7V, I <sub>O</sub> = 30mA		0.04	0.06	V
Load regulation	ΔV <sub>OLO1</sub>	I <sub>O</sub> = 1 to 150mA		10	50	mV
Line regulation	ΔV <sub>OLN1</sub>	VBAT = 3.3 to 4.5V, I <sub>O</sub> = 1mA		10	60	mV
Output voltage temperature coefficient	ΔV <sub>O1</sub> /ΔTj	Ta = -25 to 75°C, I <sub>O</sub> = 30mA		±100		ppm/°C
Ripple rejection	V <sub>R1</sub>	VBAT = 3.6V, I <sub>O</sub> = 30mA, VRR = -20dBV, f <sub>RR</sub> = 1kHz		65		dB
Output noise voltage	V <sub>ON1</sub>	I <sub>O</sub> = 30mA, 20Hz < f < 20kHz		75		μVrms
<b>REG2</b>						
Output voltage 1	V <sub>O2</sub>	I <sub>O</sub> = 30mA, ECO = H	2.55	2.6	2.65	V
Output voltage 2	V <sub>O2E</sub>	I <sub>O</sub> = 30mA, ECO = L	2.53	2.6	2.67	V
Drop out voltage	VDR1	VBAT = 2.5V, I <sub>O</sub> = 30mA		0.06	0.12	V
Load regulation	ΔV <sub>OLO2</sub>	I <sub>O</sub> = 1 to 100mA		10	100	mV
Line regulation	ΔV <sub>OLN2</sub>	VBAT = 3.3 to 4.5V, I <sub>O</sub> = 1mA		10	60	mV
Output voltage temperature coefficient	ΔV <sub>O2</sub> /ΔTj	Ta = -25 to 75°C, I <sub>O</sub> = 30mA		±100		ppm/°C
Ripple rejection	V <sub>R2</sub>	VBAT = 3.6V, I <sub>O</sub> = 30mA, VRR = -20dBV, f <sub>RR</sub> = 1kHz		65		dB
Output noise voltage	V <sub>ON2</sub>	I <sub>O</sub> = 30mA, 20Hz < f < 20kHz		75		μVrms

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Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
<b>REG3</b>						
Output voltage 1	V <sub>O3</sub>	I <sub>O</sub> = 30mA, ECO = H	2.45	2.5	2.55	V
Output voltage 2	V <sub>O3E</sub>	I <sub>O</sub> = 30mA, ECO = L	2.43	2.5	2.57	V
Drop out voltage	VDR3	V <sub>BAT</sub> = 2.4V, I <sub>O</sub> = 30mA		0.06	0.12	V
Load regulation	ΔV <sub>OLO3</sub>	I <sub>O</sub> = 1 to 50mA		10	50	mV
Line regulation	ΔV <sub>OLN3</sub>	V <sub>BAT</sub> = 3.3 to 4.5V, I <sub>O</sub> = 1mA		10	60	mV
Output voltage temperature coefficient	ΔV <sub>O3</sub> /ΔT <sub>j</sub>	T <sub>a</sub> = -25 to 75°C, I <sub>O</sub> = 30mA		±100		ppm/°C
Ripple rejection	V <sub>R3</sub>	V <sub>BAT</sub> = 3.6V, I <sub>O</sub> = 30mA, VRR = -20dBV, f <sub>RR</sub> = 1kHz		65		dB
Output noise voltage	V <sub>ON3</sub>	I <sub>O</sub> = 30mA, 20Hz < f < 20kHz		75		μVrms
<b>REG4</b>						
Output voltage	V <sub>O4</sub>	I <sub>O</sub> = 30mA	2.91	3	3.09	V
Drop out voltage	VDR3	V <sub>BAT</sub> = 2.9V, I <sub>O</sub> = 30mA		0.06	0.12	V
Load regulation	ΔV <sub>OLO4</sub>	I <sub>O</sub> = 1 to 50mA		10	50	mV
Line regulation	ΔV <sub>OLN4</sub>	V <sub>BAT</sub> = 3.3 to 4.5V, I <sub>O</sub> = 1mA		10	60	mV
Output voltage temperature coefficient	ΔV <sub>O4</sub> /ΔT <sub>j</sub>	T <sub>a</sub> = -25 to 75°C, I <sub>O</sub> = 30mA		±100		ppm/°C
Ripple rejection	V <sub>R4</sub>	V <sub>BAT</sub> = 3.6V, I <sub>O</sub> = 30mA, VRR = -20dBV, f <sub>RR</sub> = 1kHz		55		dB
Output noise voltage	V <sub>ON4</sub>	I <sub>O</sub> = 30mA, 20Hz < f < 20kHz		75		μVrms
<b>DET1</b>						
Detection voltage	VD1	H→L	2.45	2.5	2.55	V
Hysteresis width	ΔV <sub>H1</sub>		75	125	175	mV
Detection voltage temperature coefficient	ΔVD1/ΔT <sub>j</sub>	T <sub>a</sub> = -25 to 75°C		±100		ppm/°C
<b>VBATDET</b>						
Detection voltage	VDB	H→L	3.04	3.1	3.16	V
Hysteresis width	ΔVHB		93	155	217	mV
Output pull-up resistance	RPDETB		1.4	1.8	2.2	MΩ
Detection voltage temperature coefficient	ΔVDB/ΔT <sub>j</sub>	T <sub>a</sub> = -25 to 75°C		±100		ppm/°C
<b>Charge pump</b>						
Output voltage 1	VCPO1	V <sub>BAT</sub> = 3.2 to 5.9V, Load current 80mA	4.8	5	5.2	V
Oscillation frequency	CPOSC		0.7	1	1.3	MHz
Output ripple	VRCP	V <sub>BAT</sub> = 3.6, Load current 80mA		±200		mVp-p
Efficiency	η	V <sub>BAT</sub> = 3.2, Load current 80mA		72		%
<b>LED driver</b>						
LEDR output voltage	VLR	I <sub>O</sub> = 40mA	0	0.1	0.2	V
LEDG output voltage	VLG	I <sub>O</sub> = 40mA	0	0.1	0.2	V
LEDB output voltage	VLB	I <sub>O</sub> = 40mA	0	0.1	0.2	V
LEDF output voltage	VLF	I <sub>O</sub> = 40mA	0	0.15	0.3	V
LEDR OFF leak	ILR			0	1	μA
LEDG OFF leak	ILG			0	1	μA
LEDB OFF leak	ILB			0	1	μA
LEDF OFF leak	ILF			0	1	μA
<b>Mic bias</b>						
Output ON resistance	RMO	I <sub>O</sub> = 10mA		10		Ω
OFF leakage current	ILM			0	1	μA
<b>Output voltage (GP_0, 1)</b>						
Output H level	V <sub>OH</sub>	I <sub>O</sub> = 1mA	REG10 -0.3		REG10	V
Output L level	V <sub>OL</sub>	I <sub>O</sub> = 1mA	0		0.3	V

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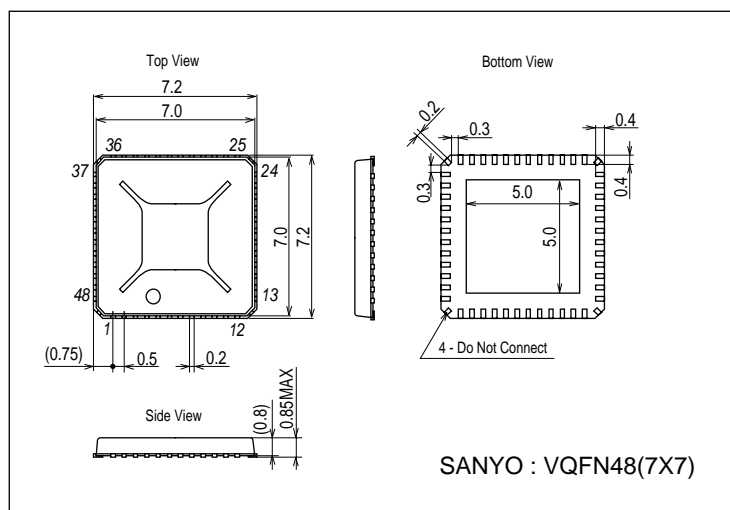
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Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
<b>Input voltage 1 (SDATA, SEN, SCLK)</b>						
H level	V <sub>INH1</sub>	Input H level	REG10 ×0.8		REG10	V
L level	V <sub>INL1</sub>	Input L level	0		REG10 ×0.2	V
<b>Input voltage 2 (T_CNT, TCXOCNT, ECO, REG3CTL, REG12CTL, PWRON, RTCINT, MSSELO, MSSELOC, KEYSENSE4, HWRESET)</b>						
H level	V <sub>INH2</sub>	Input H level	REG40 ×0.8		REG40	V
L level	V <sub>INL2</sub>	Input L level	0		REG40 ×0.2	V
<b>Input voltage 3 (RESOUT_N)</b>						
H level	V <sub>INH3</sub>	Input H level	REG40 ×0.8		REG40	V
L level	V <sub>INL3</sub>	Input L level	0		REG40 ×0.2	V
<b>Input voltage 4 (CHG_G)</b>						
H level	V <sub>INH4</sub>	Input H level	REG40 ×0.8		6	V
L level	V <sub>INL4</sub>	Input L level	0		REG40 ×0.2	V
<b>Input voltage 5 (Vcharge)</b>						
H level	V <sub>INH5</sub>	Input H level	4.4		6	V
L level	V <sub>INL5</sub>	Input L level	0		3.6	V
<b>Input voltage 6 (VBATBK)</b>						
H level	V <sub>INH6</sub>	Input H level	REG40 ×0.8		VBAT	V
L level	V <sub>INL6</sub>	Input L level	0		REG40 ×0.2	V
<b>Serial bus :</b>						
<b>Serial transfer timing</b>						
Cycle time	tcy1	SCLK clock cycle	300			ns
Data setup time 1	ts0	SDEN setup time for rise of SCLK	150			ns
Data setup time 2	ts1	SDATA setup time for rise of SCLK	150			ns
Data hold time 1	th0	SDEN hold time for fall of SCLK	150			ns
Data hold time 2	th1	SDATA hold time for rise of SCLK	150			ns
Pulse width 1	tw1L	SCLK L-period pulse width	150			ns
Pulse width 2	tw1H	SCLK H-period pulse width	150			ns
Pulse width 3	tw2L	SDEN L-period pulse width	1			μs

## Package Dimensions

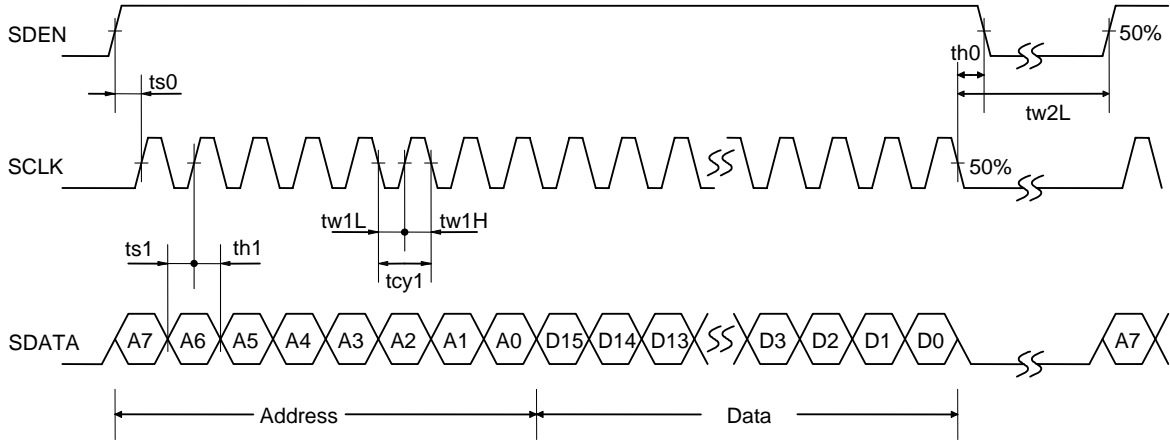
unit : mm (typ)

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## Serial transfer timing conditions



Data length : 24bit

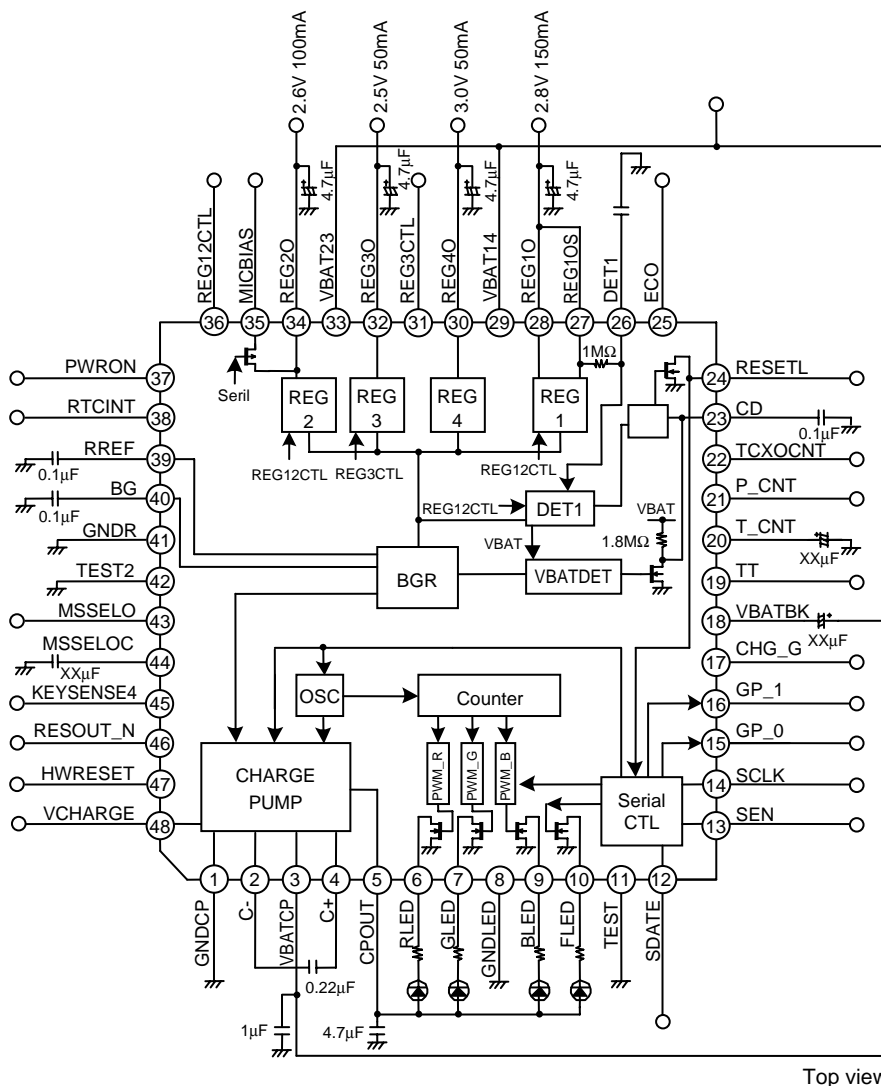
Clock frequency : 3MHz or less

"SDATA" is taken in at fall of "SDEN" when "SCLK" of 24 clock is entered during H period of "SDEN."

(Note) "SDATA" is not taken in when "SCLK" is 23 clock or less during H period of "SDEN."

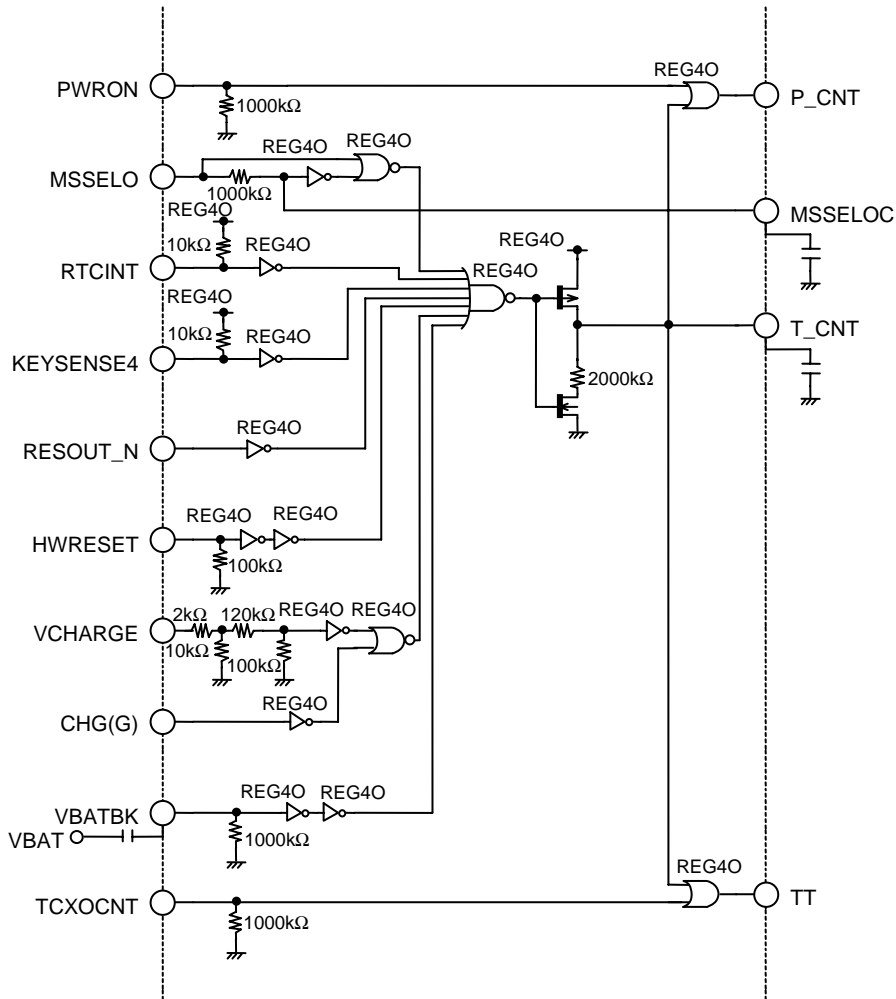
When "SCLOCK" exceeds 25 clock, "SDATA" is taken in at the 24th clock, and subsequent "SDATA" is ignored.

## Block Diagram



Top view

Power Control Block Diagram



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