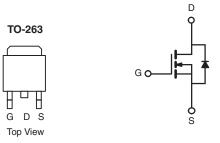


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Vishay Siliconix

# Automotive N-Channel 60 V (D-S) 175 °C MOSFET

PRODUCT SUMMARY					
V <sub>DS</sub> (V)	60				
$R_{DS(on)}(\Omega)$ at $V_{GS} = 10 \text{ V}$	0.015				
I <sub>D</sub> (A)	56				
Configuration	Single				



#### N-Channel MOSFET

#### **FEATURES**

- Halogen-free According to IEC 61249-2-21 Definition
- TrenchFET® Power MOSFET
- Package with Low Thermal Resistance
- AEC-Q101 Qualified<sup>d</sup>
- 100 % R<sub>a</sub> and UIS Tested
- Characterization Ongoing
- Compliant to RoHS Directive 2002/95/EC



HALOGEN

FREE

ORDERING INFORMATION				
Package	TO-263			
Lead (Pb)-free and Halogen-free	SQM60N06-15-GE3			

ABSOLUTE MAXIMUM RATINGS (T <sub>C</sub> = 25 °C, unless otherwise noted)						
PARAMETER	SYMBOL	LIMIT	UNIT			
Drain-Source Voltage		$V_{DS}$	60	- V		
Gate-Source Voltage	$V_{GS}$	± 20				
Continuous Drain Current	T <sub>C</sub> = 25 °C	1	56			
Continuous Drain Current	T <sub>C</sub> = 125 °C	- I <sub>D</sub>	32			
Continuous Source Current (Diode Conduction) <sup>a</sup>	Continuous Source Current (Diode Conduction) <sup>a</sup>			Α		
Pulsed Drain Current <sup>b</sup>	I <sub>DM</sub>	227				
Single Pulse Avalanche Current	L = 0.1 mH	I <sub>AS</sub>	29			
Single Pulse Avalanche Energy	L=0.11IIII	E <sub>AS</sub>	42	mJ		
Maximum Power Dissipation <sup>b</sup>	T <sub>C</sub> = 25 °C	- P <sub>D</sub>	107	W		
Maximum Fower Dissipation-	T <sub>C</sub> = 125 °C		35	VV		
Operating Junction and Storage Temperature Range		T <sub>J</sub> , T <sub>stg</sub>	- 55 to + 175	°C		

THERMAL RESISTANCE RATINGS					
PARAMETER		SYMBOL	LIMIT	UNIT	
Junction-to-Ambient P	PCB Mount <sup>c</sup>	$R_{thJA}$	40	°C/W	
Junction-to-Case (Drain)		$R_{thJC}$	1.4	C/VV	

#### Notes

- a. Package limited.
- b. Pulse test; pulse width  $\leq$  300  $\mu$ s, duty cycle  $\leq$  2 %.
- c. When mounted on 1" square PCB (FR-4 material).
- d. Parametric verification ongoing.



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PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT	
Static	1				·	ı		
Drain-Source Breakdown Voltage	V <sub>DS</sub>	$V_{GS} = 0$ , $I_D = 250 \mu A$		60	-	-	V	
Gate-Source Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> =	$V_{DS} = V_{GS}, I_D = 250 \mu\text{A}$		-	3.5	V	
Gate-Source Leakage	I <sub>GSS</sub>	V <sub>DS</sub> =	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 20 \text{ V}$		-	± 100	nA	
		V <sub>GS</sub> = 0 V	V <sub>DS</sub> = 60 V	-	-	1.0		
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>GS</sub> = 0 V	V <sub>DS</sub> = 60 V, T <sub>J</sub> = 125 °C	-	-	50	μA	
		V <sub>GS</sub> = 0 V	V <sub>DS</sub> = 60 V, T <sub>J</sub> = 175 °C	-	-	250		
On-State Drain Current <sup>a</sup>	I <sub>D(on)</sub>	V <sub>GS</sub> = 10 V	$V_{DS} \ge 5 V$	75	-	-	Α	
		V <sub>GS</sub> = 10 V	I <sub>D</sub> = 30 A	-	0.012	0.015	Ω	
Drain-Source On-State Resistance <sup>a</sup>	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V	I <sub>D</sub> = 30 A, T <sub>J</sub> = 125 °C	-	-	0.027		
	, ,	V <sub>GS</sub> = 10 V	I <sub>D</sub> = 30 A, T <sub>J</sub> = 175 °C	-	-	0.033		
Forward Transconductanceb	9 <sub>fs</sub>	V <sub>DS</sub> = 15 V, I <sub>D</sub> = 30 A		-	61	-	S	
Dynamic <sup>b</sup>								
Input Capacitance	C <sub>iss</sub>			-	1983	2480		
Output Capacitance	C <sub>oss</sub>	$V_{GS} = 0 V$	V <sub>DS</sub> = 25 V, f = 1 MHz	-	314	395	pF	
Reverse Transfer Capacitance	C <sub>rss</sub>			-	125	160		
Total Gate Charge <sup>c</sup>	Qg			-	33	50		
Gate-Source Charge <sup>c</sup>	Q <sub>gs</sub>	V <sub>GS</sub> = 10 V	$V_{DS} = 30 \text{ V}, I_{D} = 60 \text{ A}$	-	8.9	-	nC	
Gate-Drain Charge <sup>c</sup>	$Q_{gd}$			-	7.4	-		
Gate Resistance	R <sub>g</sub>		f = 1 MHz	0.8	1.6	2.4	Ω	
Turn-On Delay Time <sup>c</sup>	t <sub>d(on)</sub>			-	11	17		
Rise Time <sup>c</sup>	t <sub>r</sub>	$V_{DD} = 30 \text{ V}, R_L = 0.5 \Omega$ $I_D \cong 60 \text{ A}, V_{GEN} = 10 \text{ V}, R_g = 1 \Omega$		-	12	18	ns	
Turn-Off Delay Time <sup>c</sup>	t <sub>d(off)</sub>			-	21	32		
Fall Time <sup>c</sup>	t <sub>f</sub>			-	7	11		
Source-Drain Diode Ratings and Chara	acteristics <sup>b</sup>							
Pulsed Current <sup>a</sup>	I <sub>SM</sub>			-	-	227	Α	
Forward Voltage	$V_{SD}$	$I_F = 30 \text{ A}, V_{GS} = 0$		-	0.9	1.5	V	

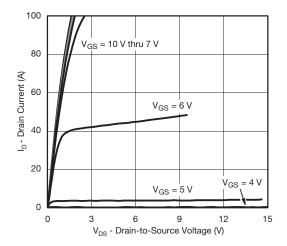
#### Notes

- a. Pulse test; pulse width  $\leq 300~\mu s,$  duty cycle  $\leq 2~\%.$
- b. Guaranteed by design, not subject to production testing.
- c. Independent of operating temperature.

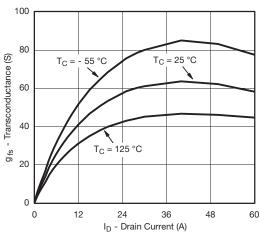
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



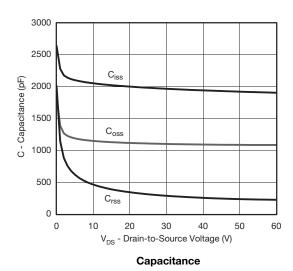
## **TYPICAL CHARACTERISTICS** (T<sub>A</sub> = 25 °C, unless otherwise noted)

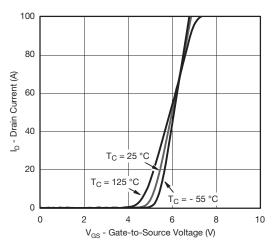


#### **Output Characteristics**

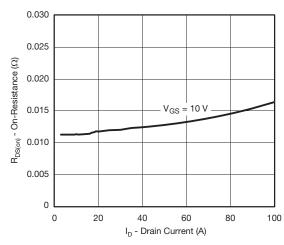


### Transconductance

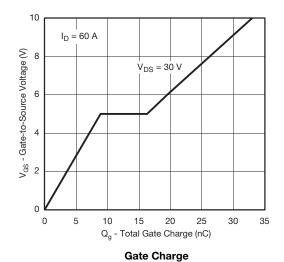




#### **Transfer Characteristics**

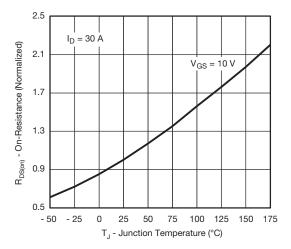


**On-Resistance vs. Drain Current** 

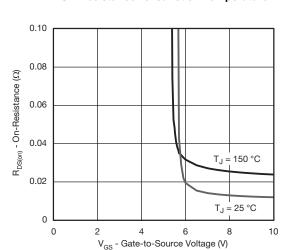




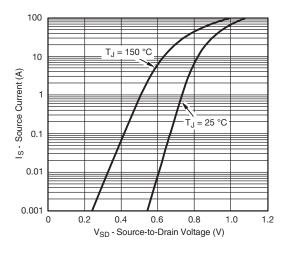
## **TYPICAL CHARACTERISTICS** (T<sub>A</sub> = 25 °C, unless otherwise noted)



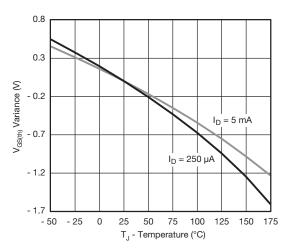




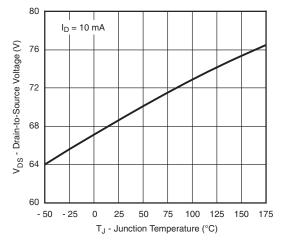
On-Resistance vs. Gate-to-Source Voltage



**Source Drain Diode Forward Voltage** 



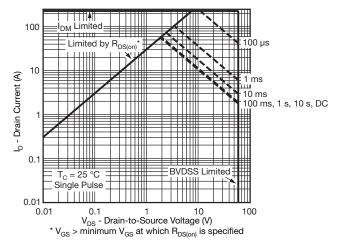
**Threshold Voltage** 



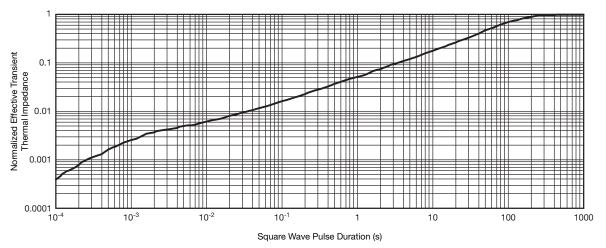
Drain Source Breakdown vs. Junction Temperature



## **THERMAL RATINGS** ( $T_A = 25$ °C, unless otherwise noted)



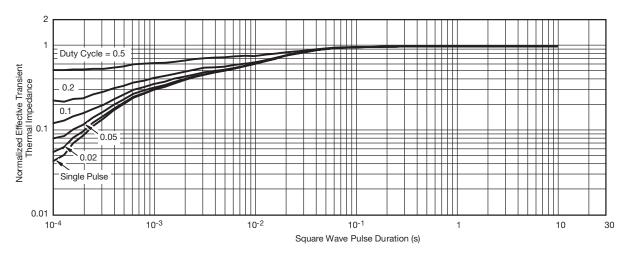
#### **Safe Operating Area**



Normalized Thermal Transient Impedance, Junction-to-Ambient

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## THERMAL RATINGS (T<sub>A</sub> = 25 °C, unless otherwise noted)



#### Normalized Thermal Transient Impedance, Junction-to-Case

#### Note

- The characteristics shown in the two graphs
- Normalized Transient Thermal Impedance Junction-to-Ambient (25 °C)
- Normalized Transient Thermal Impedance Junction-to-Case (25 °C)

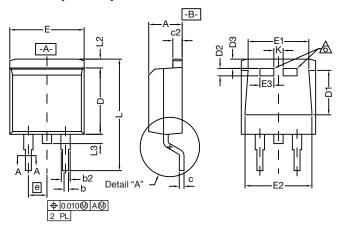
are given for general guidelines only to enable the user to get a "ball park" indication of part capabilities. The data are extracted from single pulse transient thermal impedance characteristics which are developed from empirical measurements. The latter is valid for the part mounted on printed circuit board - FR4, size 1" x 1" x 0.062", double sided with 2 oz. copper, 100 % on both sides. The part capabilities can widely vary depending on actual application parameters and operating conditions.

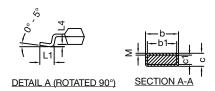
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### TO-263 (D<sup>2</sup>PAK): 3-LEAD





		INCHES		MILLIN	METERS	
DIM.		MIN.	MAX.	MIN.	MAX.	
Α		0.160	0.190	4.064	4.826	
	b	0.020	0.039	0.508	0.990	
	b1	0.020	0.035	0.508	0.889	
	b2	0.045	0.055	1.143	1.397	
c*	Thin lead	0.013	0.018	0.330	0.457	
	Thick lead	0.023	0.028	0.584	0.711	
	Thin lead	0.013	0.017	0.330	0.431	
c1	Thick lead	0.023	0.027	0.584	0.685	
	c2	0.045	0.055	1.143	1.397	
D		0.340	0.380	8.636	9.652	
D1		0.220	0.240	5.588	6.096	
D2		0.038	0.042	0.965	1.067	
D3		0.045	0.055	1.143	1.397	
E		0.380	0.410	9.652	10.414	
E1		0.245	-	6.223	-	
E2		0.355 0.375		9.017	9.525	
E3		0.072	0.078	1.829	1.981	
	е	0.100 BSC		0.100 BSC 2.54 BSC		
	K	0.045	0.055	1.143	1.397	
L		0.575	0.625	14.605	15.875	
L1		0.090	0.110	2.286	2.794	
L2		0.040	0.055	1.016	1.397	
L3		0.050	0.070	1.270	1.778	
L4		0.010 BSC		0.254 BSC		
М		-	0.002	-	0.050	
ECN: T10-0738-Rev. J, 03-Jan-11 DWG: 5843						

### Notes

- 1. Plane B includes maximum features of heat sink tab and plastic.
- 2. No more than 25 % of L1 can fall above seating plane by max.
- 3. Pin-to-pin coplanarity max. 4 mils.
- 4. \*: Thin lead is for SUB, SYB. Thick lead is for SUM, SYM, SQM.





## RECOMMENDED MINIMUM PADS FOR D<sup>2</sup>PAK: 3-Lead



Recommended Minimum Pads Dimensions in Inches/(mm)

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