Never stop thinking

TLE8386EL

Smart Boost Controller

Datasheet

Rev. 1.0, 2009-11-30

Automotive Power

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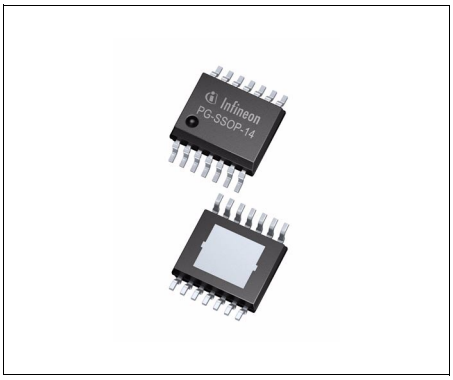
1 Overview



PG-SSOP-14

Features

- Wide Input Voltage Range from 4.75 V to 45 V
- Constant Current or Constant Voltage Regulation
- Very Low Shutdown Current: IQ< 10 µA
- Flexible Switching Frequency Range, 100 kHz to 500 kHz
- Synchronization with external clock source
- Output Open Circuit Diagnostic Output
- Available in a small thermally enhanced PG-SSOP-14 package
- Internal 5 V Low Drop Out Voltage Regulator
- Output Overvoltage Protection
- Internal Soft Start
- Over Temperature Shutdown
- Automotive AEC Qualified
- Green Product (RoHS) Compliant

Description

The TLE8386EL is a boost controller with built in protection and diagnostic features. The main function of this device is step-up (boost) an input voltage to a larger output voltage. The diagnostics are communicated on a status output (pin ST) to indicate a fault conditions such as over temperature, open feedback and open load. The switching frequency is adjustable in the range of 100 kHz to 500 kHz and can be synchronized to an external clock source. The TLE8386EL features an enable function reducing the shut-down current consumption to <10 µA. The current mode regulation scheme of this device provides a stable regulation loop maintained by small external compensation components. The integrated soft-start feature limits the current peak as well as voltage overshoot at start-up. This IC is suited for use in the harsh automotive environments and provides protection functions such as output overvoltage protection and overtemperature shutdown.

Type	Package	Marking
TLE8386EL	PG-SSOP-14	TLE8386

2 Block Diagram

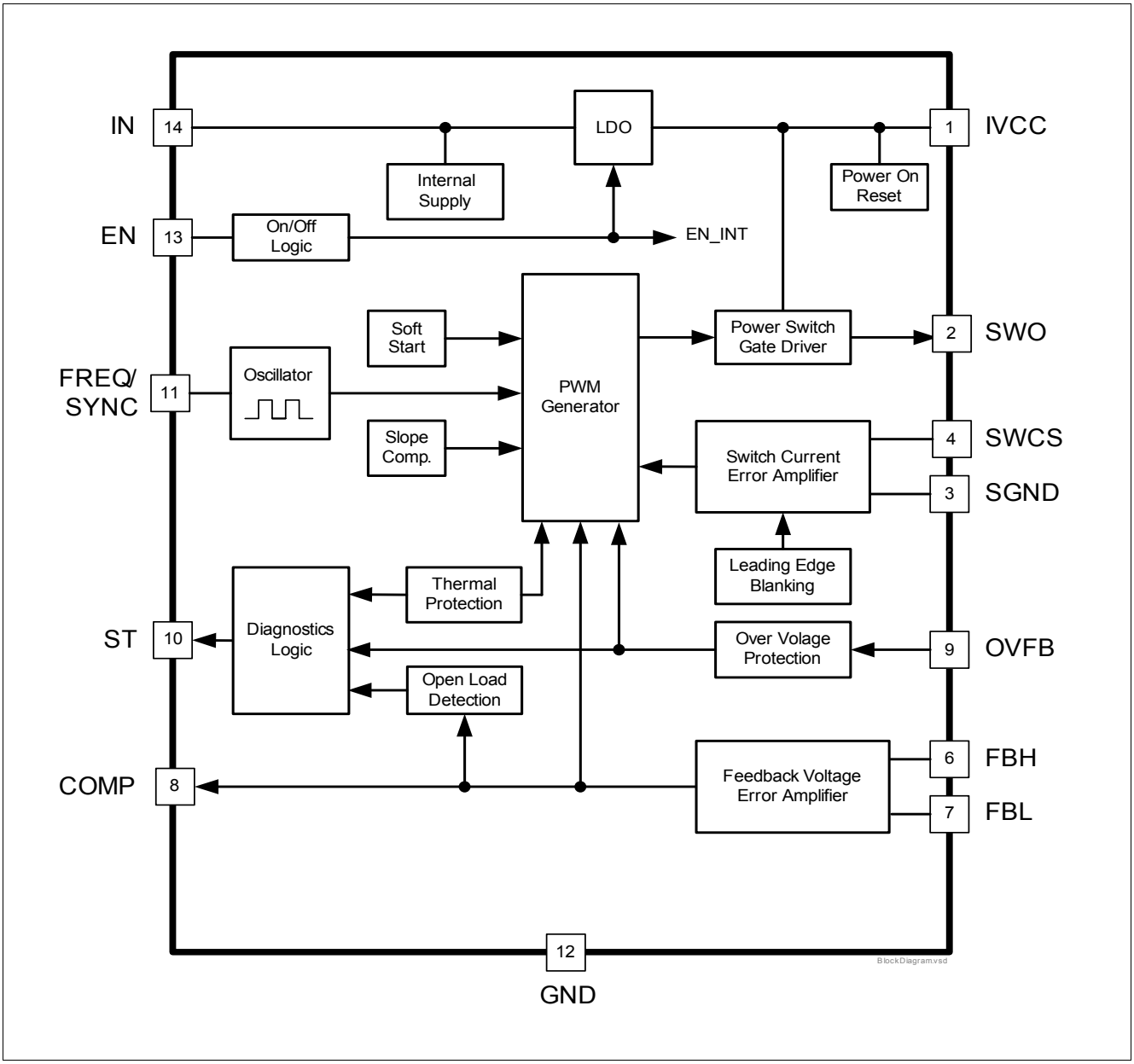


Figure 1 Block Diagram

3 Pin Configuration

3.1 Pin Assignment

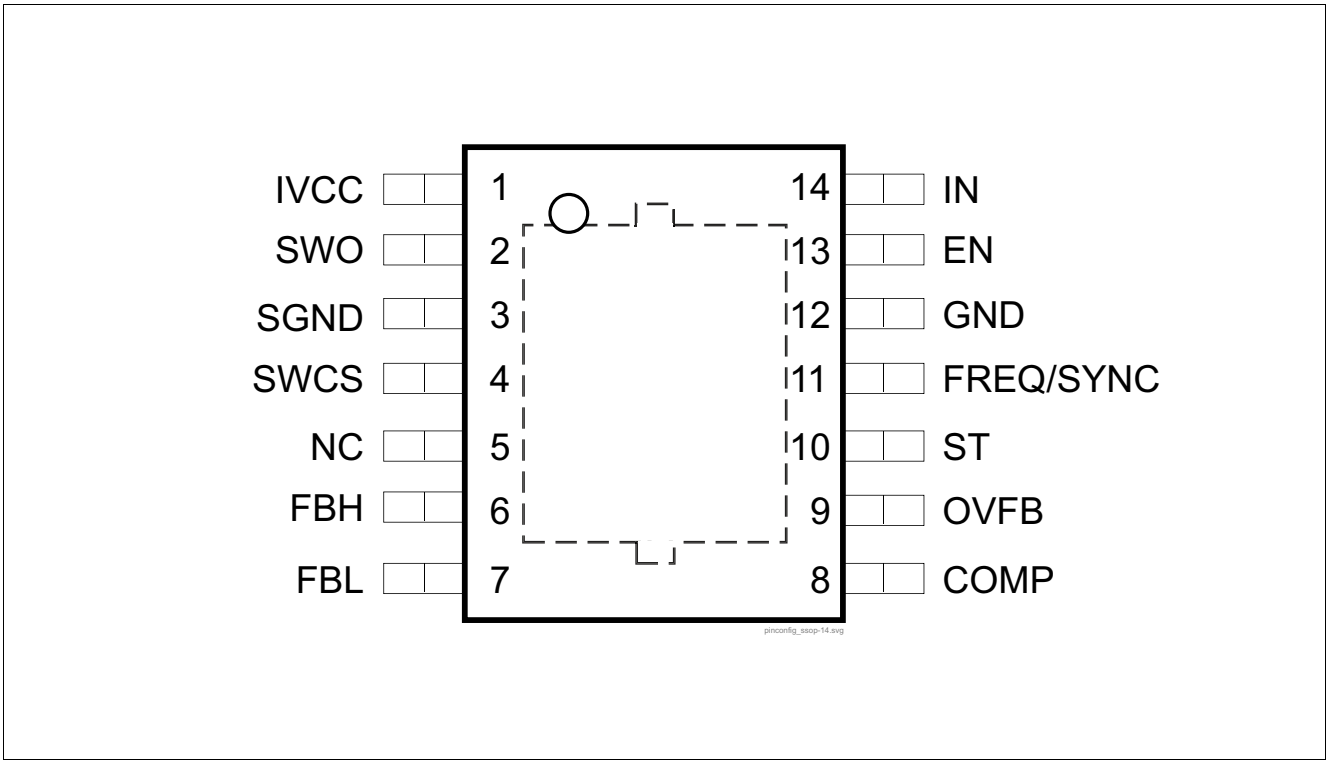


Figure 2 Pin Configuration

3.2 Pin Definitions and Functions

Pin	Symbol	Function
1	IVCC	**Internal LDO Output;** Used for internal biasing and gate drive. Bypass with external capacitor. Do not leave pin IVCC open.
2	SWO	**Switch Output;** Connect to gate of external boost converter switching MOSFET
3	SGND	**Current Sense Ground;** Ground return for current sense switch
4	SWCS	**Current Sense Input;** Detects the peak current through switch
5	NC	**No Connect;**
6	FBH	**Voltage Feedback Positive;** Non inverting Input (+)
7	FBL	**Voltage Feedback Negative;** Inverting Input (-)
8	COMP	**Compensation Input;** Connect R and C network to pin for stability

Pin	Symbol	Function
9	OVFB	**Output Overvoltage Protection Feedback;** Connect to resistive voltage divider to set overvoltage threshold.
10	ST	**Status Output;** Open drain diagnostic output to indicate fault condition. Connect pull up resistor to pin.
11	FREQ / SYNC	**Frequency Select or Synchronization Input;** Connect external resistor to GND to set frequency. Or apply external clock signal for synchronization within frequency capture range.
12	GND	**Ground;** Connect to system ground.
13	EN	**Enable;** Apply logic high signal to enable device.
14	IN	**Supply Input;** Supply for internal biasing.
Exposed Pad		Connect to GND.

4 General Product Characteristics

4.1 Absolute Maximum Ratings

Absolute Maximum Ratings[1)]

T_j = -40 °C to +150 °C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values		Unit	Conditions
			Min.	Max.		
Voltages						
4.1.1	IN Supply Input	V_{IN}	-0.3	45	V	
4.1.2	EN Enable Input	V_{EN}	-40	45	V	
4.1.3	FBH-FBL; Feedback Error Amplifier Differential	V_{FBH}-V_{FBL}	-5.5	5.5	V	
4.1.4	FBH; Feedback Error Amplifier Positive Input	V_{FBH}	-0.3	45	V	
4.1.5	FBL Feedback Error Amplifier Negative Input	V_{FBL}	-0.3	45	V	
4.1.6	OVFB Over Voltage Feedback Input	V_{OVP}	-0.3	5.5	V	
4.1.7			-0.3	6.2	V	t < 10s
4.1.8	SWCS Switch Current Sense Input	V_{SWCS}	-0.3	5.5	V	
4.1.9			-0.3	6.2	V	t < 10s
4.1.10	SWO Switch Gate Drive Output	V_{SWO}	-0.3	5.5	V	
4.1.11			-0.3	6.2	V	t < 10s
4.1.12	SGND Current Sense Switch GND	V_{SGND}	-0.3	0.3	V	
4.1.13	COMP Compensation Input	V_{COMP}	-0.3	5.5	V	
4.1.14			-0.3	6.2	V	t < 10s
4.1.15	FREQ / SYNC; Frequency and Synchronization Input	$V_{FREQ / SYNC}$	-0.3	5.5	V	
4.1.16			-0.3	6.2	V	t < 10s
4.1.17	ST	V_{ST}	-0.3	45	V	
4.1.18	Diagnostic Status Output	I_{ST}	-5	5	mA	
4.1.19	IVCC Internal Linear Voltage Regulator Output	V_{IVCC}	-0.3	5.5	V	
4.1.20			-0.3	6.2	V	t < 10s
Temperatures						
4.1.21	Junction Temperature	T_j	-40	150	°C	–
4.1.22	Storage Temperature	T_{stg}	-55	150	°C	–

Absolute Maximum Ratings[1)]

T_j = -40 °C to +150 °C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values		Unit	Conditions
			Min.	Max.		
ESD Susceptibility						
4.1.23	ESD Resistivity to GND	$V_{ESD,HBM}$	-2	2	kV	HBM[2)]
4.1.24	ESD Resistivity to GND	$V_{ESD,CDM}$	-500	500	V	CDM[3)]
4.1.25	ESD Resistivity Pin 1, 7, 8, 14 (corner pins) to GND	$V_{ESD,CDM,C}$	-750	750	V	CDM[3)]

1) Not subject to production test, specified by design.

2) ESD susceptibility, Human Body Model “HBM” according to EIA/JESD 22-A114B

3) ESD susceptibility, Charged Device Model “CDM” EIA/JESD22-C101 or ESDA STM5.3.1

Note: Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note: Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as “outside” normal operating range. Protection functions are not designed for continuous repetitive operation.

4.2 Functional Range

Pos.	Parameter	Symbol	Limit Values		Unit	Conditions
			Min.	Max.		
4.2.1	Supply Voltage Input	V_{IN}	4.75	45	V	$V_{IVCC} > V_{IVCC,RTH,d}$
4.2.2	Feedback Voltage Input	$V_{FBH;}$ V_{FBL}	4.5	45	V	–
4.2.3	Junction Temperature	T_j	-40	150	°C	–

Note: Within the functional range the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the related electrical characteristics table.

4.3 Thermal Resistance

*Note: This thermal data was generated in accordance with JEDEC JESD51 standards. For more information, go to **www.jedec.org**.*

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
4.3.1	Junction to Case[1)]	R_{thJC}	–	10	–	K/W	–
4.3.2	Junction to Ambient[1) 2)]	R_{thJA}	–	47	–	K/W	2s2p
4.3.3		R_{thJA}	–	54	–	K/W	1s0p + 600 mm^2
4.3.4		R_{thJA}	–	64	–	K/W	1s0p + 300 mm^2

1) Not subject to production test, specified by design.

2) Specified R_{thJA} value is according to JEDEC 2s2p (JESD 51-7) + (JESD 51-5) and JEDEC 1s0p (JESD 51-3) + heatsink area at natural convection on FR4 board;

5 Boost Regulator

5.1 Description

The TLE8386EL boost (step-up) regulator provides a higher output voltage than input voltage. The boost regulator function is implemented by a pulse width modulated (PWM) current mode controller. The PWM current mode controller uses the peak current through the external power switch and error in the output current to determine the appropriate pulse width duty cycle (on time) for constant output current. The current mode controller it provides a PWM signal to an internal gate driver which then outputs the same PWM signal to external n-channel enhancement mode metal oxide field effect transistor (MOSFET) power switch. The current mode controller also has built-in slope compensation to prevent sub-harmonic oscillations which is a characteristic of current mode controllers operating at high duty cycles (>50% duty). An additional built-in feature is an integrated soft start that limits the current through the inductor and external power switch during initialization. The soft start function gradually increases the inductor and switch current over 1 ms (typical) to minimize potential overvoltage at the output.

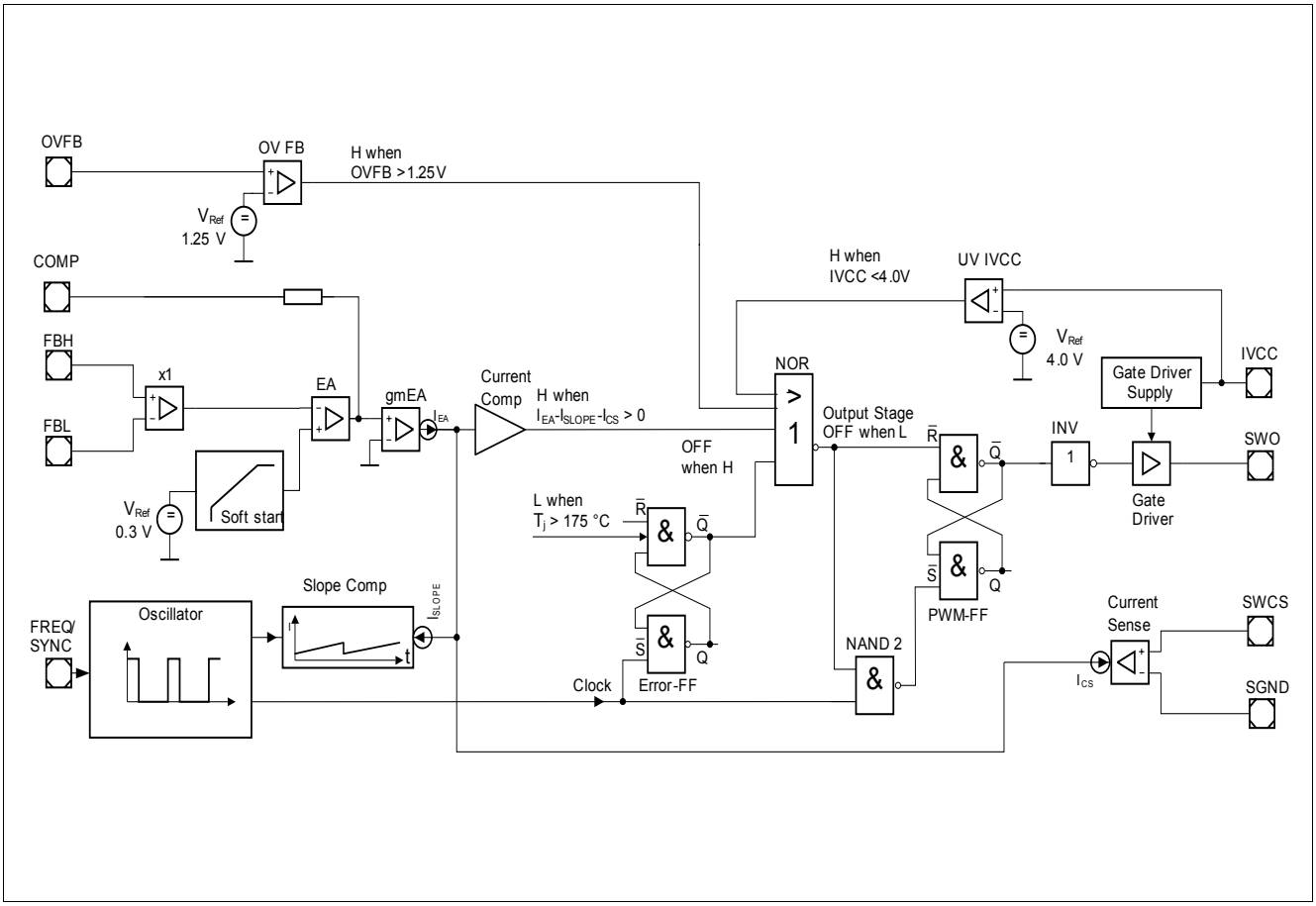


Figure 3 Boost Regulator Block Diagram

5.2 Electrical Characteristics

V_{IN} = 6V to 40V; 4.5V ≤ V_{FBH} ≤ 40V, 4.5V ≤ V_{FBL} ≤ 40V, T_j = -40 °C to +150 °C, all voltages with respect to ground, positive current flowing into pin; (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
Boost Regulator:							
5.2.1	Feedback Reference Voltage	V_{REF}	0.28	0.30	0.32	V	V_{IN} = 19 V; $V_{REF} = V_{FBH} - V_{FBL}$
5.2.2	Voltage Line Regulation	ΔV_{REF} /ΔV_{IN}	–	–	0.15	%/V	V_{IN} = 6 to 19 V; V_{BO}= 30 V; I_{BO} = 100 mA **Figure 13**
5.2.3	Voltage Load Regulation	ΔV_{REF} /ΔI_{BO}	–	–	5	%/A	V_{IN} = 19 V; V_{BO} = 30V; I_{BO} = 100 to 500 mA **Figure 13**
5.2.4	Switch Peak Over Current Threshold	V_{SWCS}	130	150	170	mV	V_{IN} = 6 V V_{FBH} = V_{FBL} = 5 V V_{COMP} = 3.5V
5.2.5	Maximum Duty Cycle	$D_{MAX,fixed}$	90	93	95	%	Fixed frequency mode
5.2.6	Maximum Duty Cycle	$D_{MAX,sync}$	88	–	–	%	Synchronization mode
5.2.7	Soft Start Ramp	t_{SS}	350	1000	1500	µs	V_{FB} rising from 5% to 95% of V_{FB}, typ.
5.2.8	Feedback Input Current	I_{FBx}	-10	-50	-100	µA	V_{FBH} - V_{FBL} = 0.3 V
5.2.9	Switch Current Sense Input Current	I_{SWCS}	10	50	100	µA	V_{SWCS} = 150 mV
5.2.10	Input Undervoltage Shutdown	$V_{IN,off}$	3.75	–	–	V	V_{IN} decreasing
5.2.11	Input Voltage Startup	$V_{IN,on}$	–	–	4.75	V	V_{IN} increasing
Gate Driver for Boost Switch							
5.2.12	Gate Driver Peak Sourcing Current[1)]	$I_{SWO,SRC}$	–	380	–	mA	V_{SWO} = 3.5V
5.2.13	Gate Driver Peak Sinking Current[1)]	$I_{SWO,SNK}$	–	550	–	mA	V_{SWO} = 1.5V
5.2.14	Gate Driver Output Rise Time	$t_{R,SWO}$	–	30	60	ns	$C_{L,SWO}$ = 3.3nF; V_{SWO} = 1V to 4V
5.2.15	Gate Driver Output Fall Time	$t_{F,SWO}$	–	20	40	ns	$C_{L,SWO}$ = 3.3nF; V_{SWO} = 1V to 4V
5.2.16	Gate Driver Output Voltage[1)]	V_{SWO}	4.5	–	5.5	V	$C_{L,SWO}$ = 3.3nF;

1) Not subject to production test, specified by design

6 Oscillator and Synchronization

6.1 Description

R_OSC vs. switching frequency

The internal oscillator is used to determine the switching frequency of the boost regulator. The switching frequency can be selected from 100 kHz to 500 kHz with an external resistor to GND. To set the switching frequency with an external resistor the following formula can be applied.

$$R_{FREQ} = \frac{1}{\left(141 \times 10^{-12}\left[\frac{s}{\Omega}\right]\right) \times \left(f_{FREQ}\left[\frac{1}{s}\right]\right)} - \left(3.5 \times 10^{3}\left[\Omega\right]\right)\ \left[\Omega\right]$$

In addition, the oscillator is capable of changing from the frequency set by the external resistor to a synchronized frequency from an external clock source. If an external clock source is provided on the pin FREQ/SYNC, then the internal oscillator synchronizes to this external clock frequency and the boost regulator switches at the synchronized frequency. The synchronization frequency capture range is 250 kHz to 500 kHz.

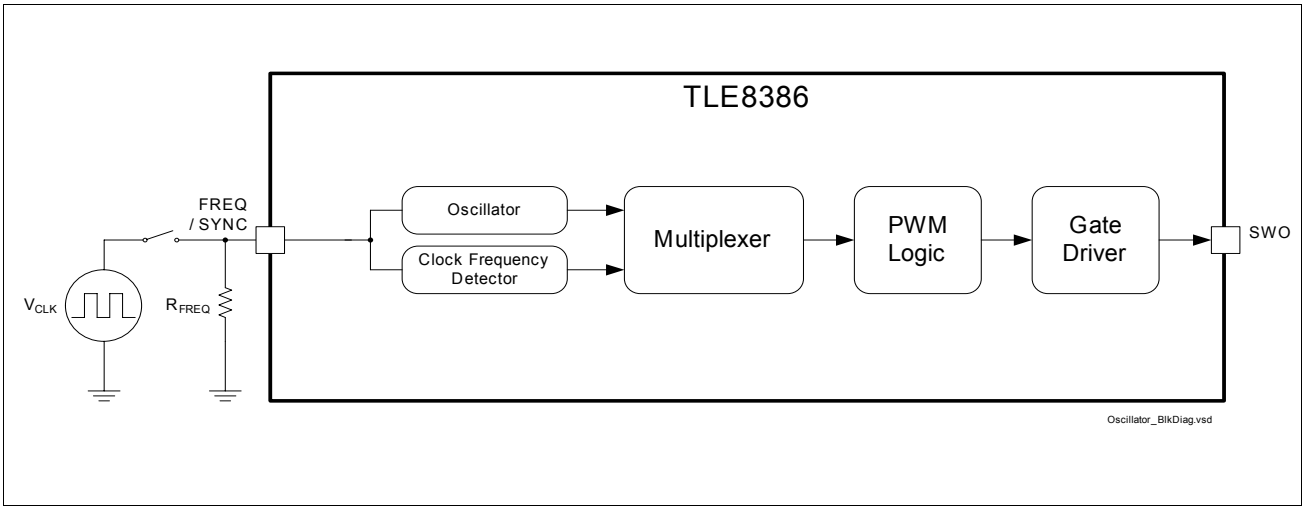


Figure 4 Oscillator and Synchronization Block Diagram and Simplified Application Circuit

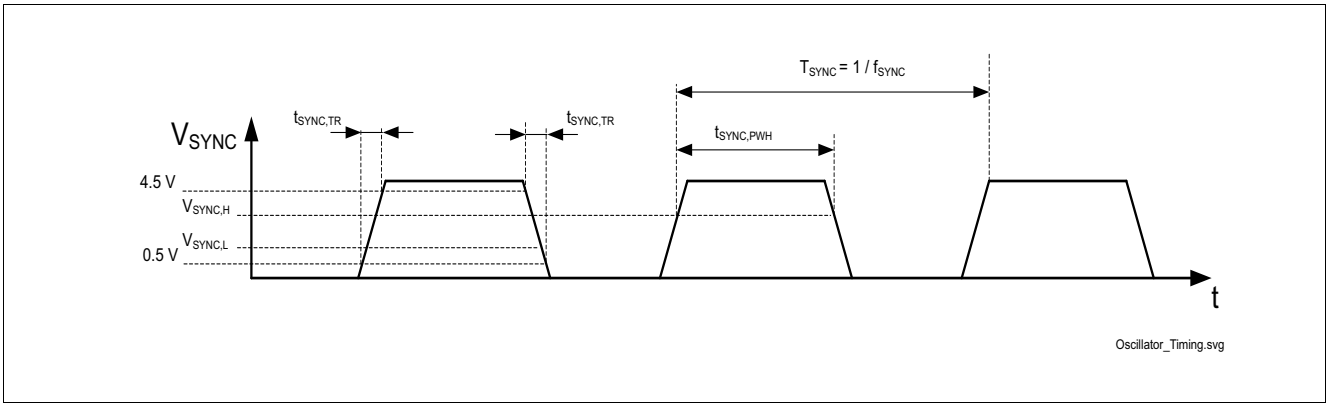


Figure 5 Synchronization Timing Diagram

6.2 Electrical Characteristics

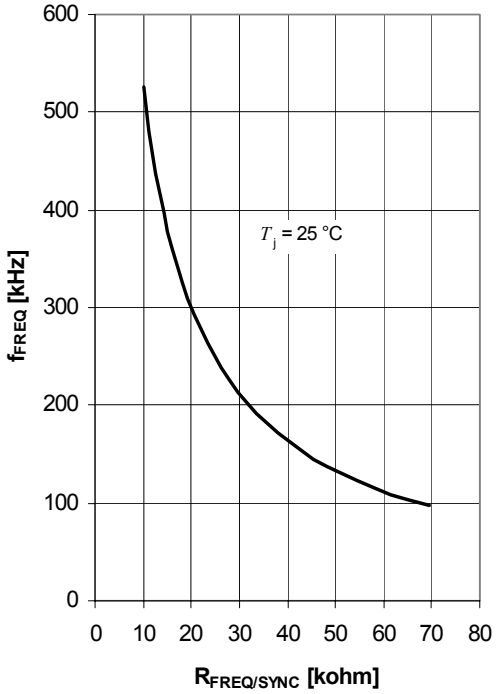
V_{IN} = 6V to 40V; 4.5V ≤ V_{FBH} ≤ 40V, 4.5V ≤ V_{FBL} ≤ 40V, T_j = -40 °C to +150 °C, all voltages with respect to ground, positive current flowing into pin; (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
Oscillator:							
6.2.1	Oscillator Frequency	f_{FREQ}	250	300	350	kHz	R_{FREQ} = 20kΩ
6.2.2	Oscillator Frequency Adjustment Range	f_{FREQ}	100	–	500	kHz	17% internal tolerance + external resistor tolerance
6.2.3	FREQ / SYNC Supply Current	I_{FREQ}	–	–	-700	µA	V_{FREQ} = 0 V
6.2.4	Frequency Voltage	V_{FREQ}	1.16	1.24	1.32	V	f_{FREQ} = 100 kHz
Synchronization							
6.2.5	Synchronization Frequency Capture Range	f_{SYNC}	250	–	500	kHz	–
6.2.6	Synchronization Signal High Logic Level Valid	$V_{SYNC,H}$	3.0	–	–	V	1)
6.2.7	Synchronization Signal Low Logic Level Valid	$V_{SYNC,L}$	–	–	0.8	V	1)
6.2.8	Synchronization Signal Logic High Pulse Width	$t_{SYNC,PWH}$	200	–	–	ns	1)

1) Synchronization of external PWM ON signal to falling edge

Typical Performance Characteristics of Oscillator

Switching Frequency f_{SW} versus Frequency Select Resistor to GND $R_{FREQ/SYNC}$



7 Enable Function

7.1 Description

The enable function powers on or off the device. A valid logic low signal on enable pin EN powers off the device and current consumption is less than 10 µA. A valid logic high enable signal on enable pin EN powers on the device. The voltage at pin IVCC (internal biasing) stays present for the Power Off Delay Time after the the device is switched off by the Enable signal.

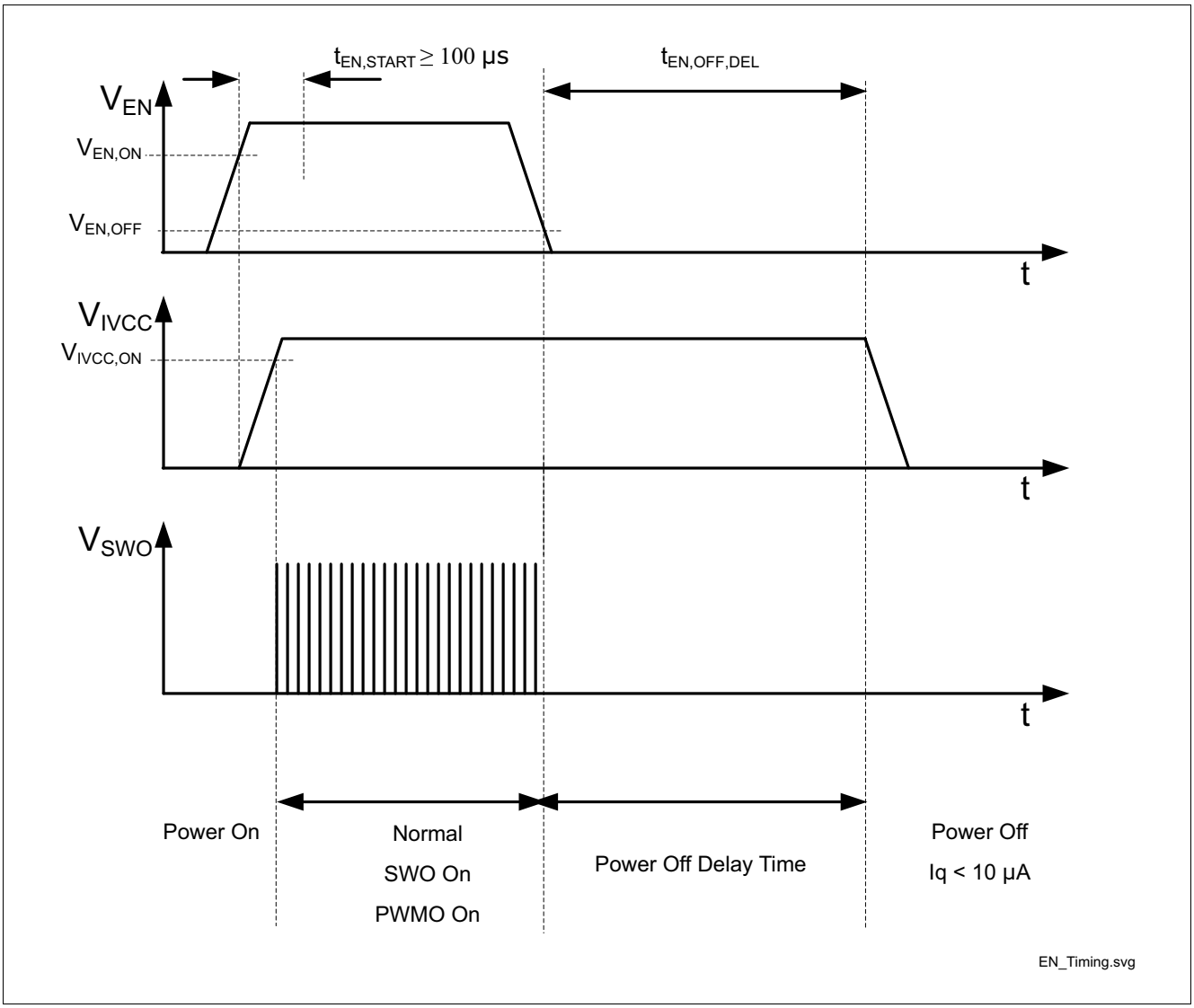


Figure 6 Timing Diagram Enable

7.2 Electrical Characteristics

V_{IN} = 6V to 40V; 4.5V ≤ V_{FBH} ≤ 40V, 4.5V ≤ V_{FBL} ≤ 40V, T_j = -40 °C to +150 °C, all voltages with respect to ground, positive current flowing into pin; (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
Enable Input:							
7.2.1	Enable Turn On Threshold	$V_{EN,ON}$	3.0	–		V	–
7.2.2	Enable Turn Off Threshold	$V_{EN,OFF}$	–	–	0.8	V	–
7.2.3	Enable Hysteresis	$V_{EN,HYS}$	50	200	400	mV	–
7.2.4	Enable High Input Current	$I_{EN,H}$	–	–	30	µA	$V_{EN/PWMI}$ = 16.0 V
7.2.5	Enable Low Input Current	$I_{EN,L}$	–	0.1	1	µA	$V_{EN/PWMI}$ = 0.5 V
7.2.6	Enable Turn Off Delay Time	$t_{EN,OFF,DEL}$	8	10	12	ms	–
7.2.7	Enable Startup Time	$t_{EN,START}$	100	–	–	µs	–
Current Consumption							
7.2.8	Current Consumption, Shutdown Mode	I_{q_off}	–	–	10	µA	$V_{EN/PWMI}$ = 0.8 V; T_j ≤ 105C; V_{IN} = 16V
7.2.9	Current Consumption, Active Mode[1)]	I_{q_on}	–	–	7	mA	$V_{EN/PWMI}$ ≥ 4.75 V; I_{BO} = 0 mA; V_{IN} = 16V V_{SWO} = 0% Duty

1) Dependency on switching frequency and gate charge of boost and dimming switch.

8 Linear Regulator

8.1 Description

The internal linear voltage regulator supplies the internal gate drivers with a typical voltage of 5 V and current up to 50 mA. An external output capacitor with low ESR is required on pin IVCC for stability and buffering transient load currents. During normal operation the external boost MOSFET switche will draw transient currents from the linear regulator and its output capacitor. Proper sizing of the output capacitor must be considered to supply sufficient peak current to the gate of the external MOSFET switch. Please refer to application section for recommendations on sizing the output capacitor. An integrated power-on reset circuit monitors the linear regulator output voltage and resets the device in case the output voltage falls below the power-on reset threshold. The power-on reset helps protect the external switches from excessive power dissipation by ensuring the gate drive voltage is sufficient to enhance the gate of an external logic level n-channel MOSFET.

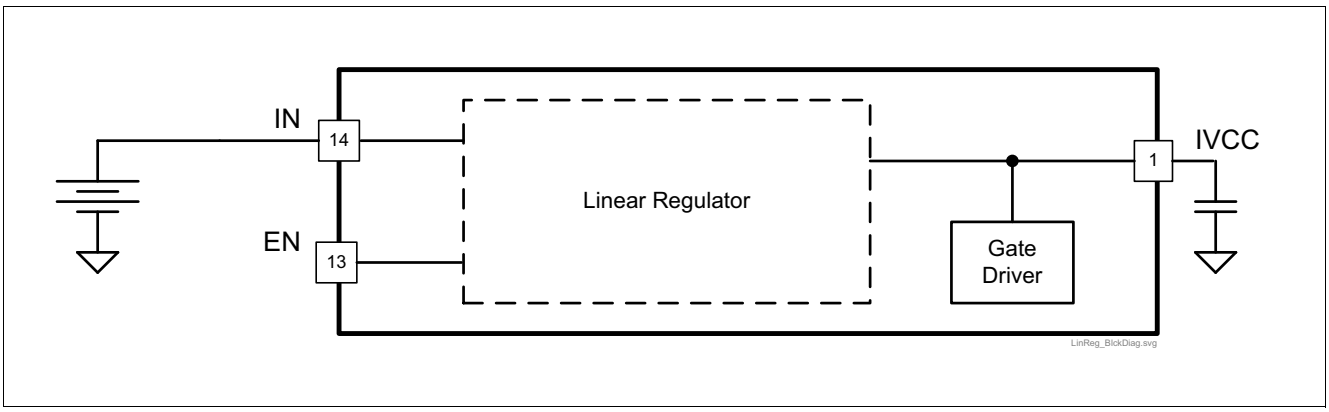


Figure 7 Voltage Regulator Block Diagram and Simplified Application Circuit

8.2 Electrical Characteristics

V_{IN} = 6V to 40V; 4.5V ≤ V_{FBH} ≤ 40V, 4.5V ≤ V_{FBL} ≤ 40V, T_j = -40 °C to +150 °C, all voltages with respect to ground, positive current flowing into pin; (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
8.2.1	Output Voltage	V_{IVCC}	4.6	5	5.4	V	6 V ≤ V_{IN} ≤ 45 V 0.1 mA ≤ I_{IVCC} ≤ 50 mA
8.2.2	Output Current Limitation	I_{LIM}	51		90	mA	V_{IN} = 13.5 V V_{IVCC} = 4.5V
8.2.3	Drop out Voltage	V_{DR}			1400	mV	I_{IVCC} = 50mA [1]
8.2.4	Output Capacitor	C_{IVCC}	0.47		–	µF	[2]
8.2.5	Output Capacitor ESR	$R_{IVCC,ESR}$			0.5	Ω	f = 10kHz
8.2.6	Undervoltage Reset Headroom	$V_{IVCC,HDRM}$	100	–	–	mV	V_{IVCC} decreasing V_{IVCC} - $V_{IVCC,RTH,d}$
8.2.7	Undervoltage Reset Threshold	$V_{IVCC,RTH,d}$	4.0	–	–	V	V_{IVCC} decreasing
8.2.8	Undervoltage Reset Threshold	$V_{IVCC,RTH,i}$	–	–	4.5	V	V_{IVCC} increasing

1) Measured when the output voltage V_{CC} has dropped 100 mV from its nominal value.

2) Minimum value given is needed for regulator stability; application might need higher capacitance than the minimum.

9 Protection and Diagnostic Functions

9.1 Description

The TLE8386EL has integrated circuits to diagnose and protect against output overvoltage, open load, open feedback and overtemperature faults. In case any of the four fault conditions occur the Status output ST will output an active logic low signal to communicate that a fault has occurred. During an overvoltage or open load condition the gate driver outputs SWO will turn off. Figure 11 illustrates the various open load and open feedback conditions. In the event of an overtemperature condition the integrated thermal shutdown function turns off the gate drivers and internal linear voltage regulator. The typical junction shutdown temperature is 175°C. After cooling down the IC will automatically restart operation. Thermal shutdown is an integrated protection function designed to prevent immediate IC destruction and is not intended for continuous use in normal operation.

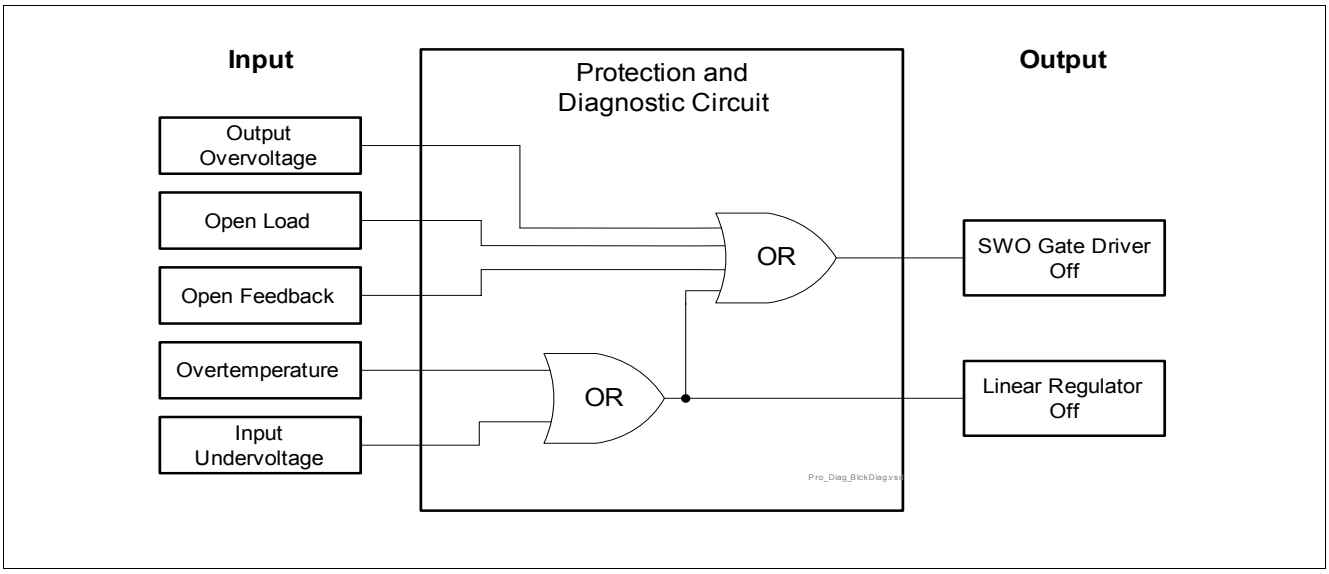
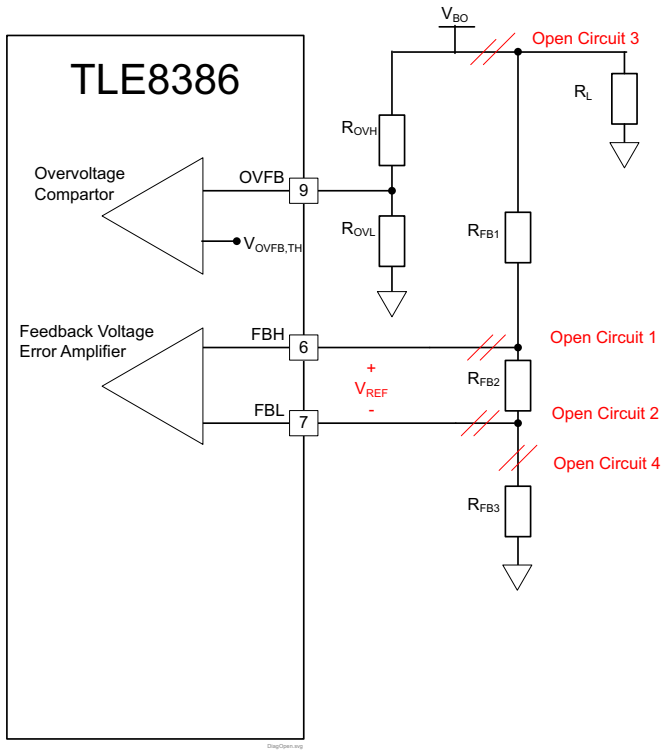


Figure 8 Protection and Diagnostic Function Block Diagram

Input		Output		
Condition	Level*	ST	SWO	IVCC
Overvoltage	False	H	Sw*	Active
	True	L	L	Active
Open Load	False	H	Sw*	Active
	True	L	L	Active
Open Feedback	False	H	Sw*	Active
	True	L	L	Active
Overtemperature	False	H	Sw*	Active
	True	L	L	Shutdown

*Note:
Sw = Switching
False = Condition does not exist
True = Condition does exist

Figure 9 Status Output Truth Table



Output Open Circuit Conditions

Open Circuit Condition	Fault Condition	Fault Threshold Voltage V_{REF}
1	Open FBH	-20 to -100 mV
2	Open FBL	0.5 to 1.0 V
3	Open VBO	$V_{FBx} < V_{FBx,MIN} = 4.5$ V
4	Open FB GND	Detected by overvoltage

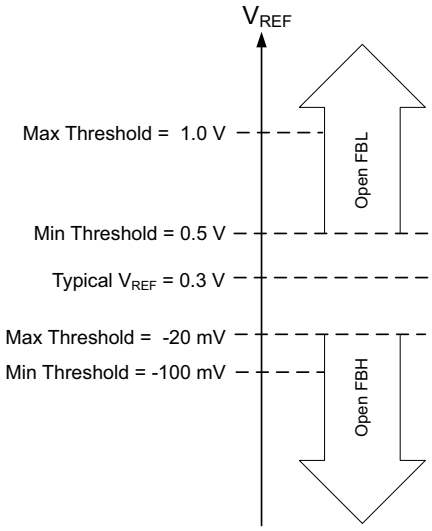


Figure 10 Open Load and Open Feedback Conditions

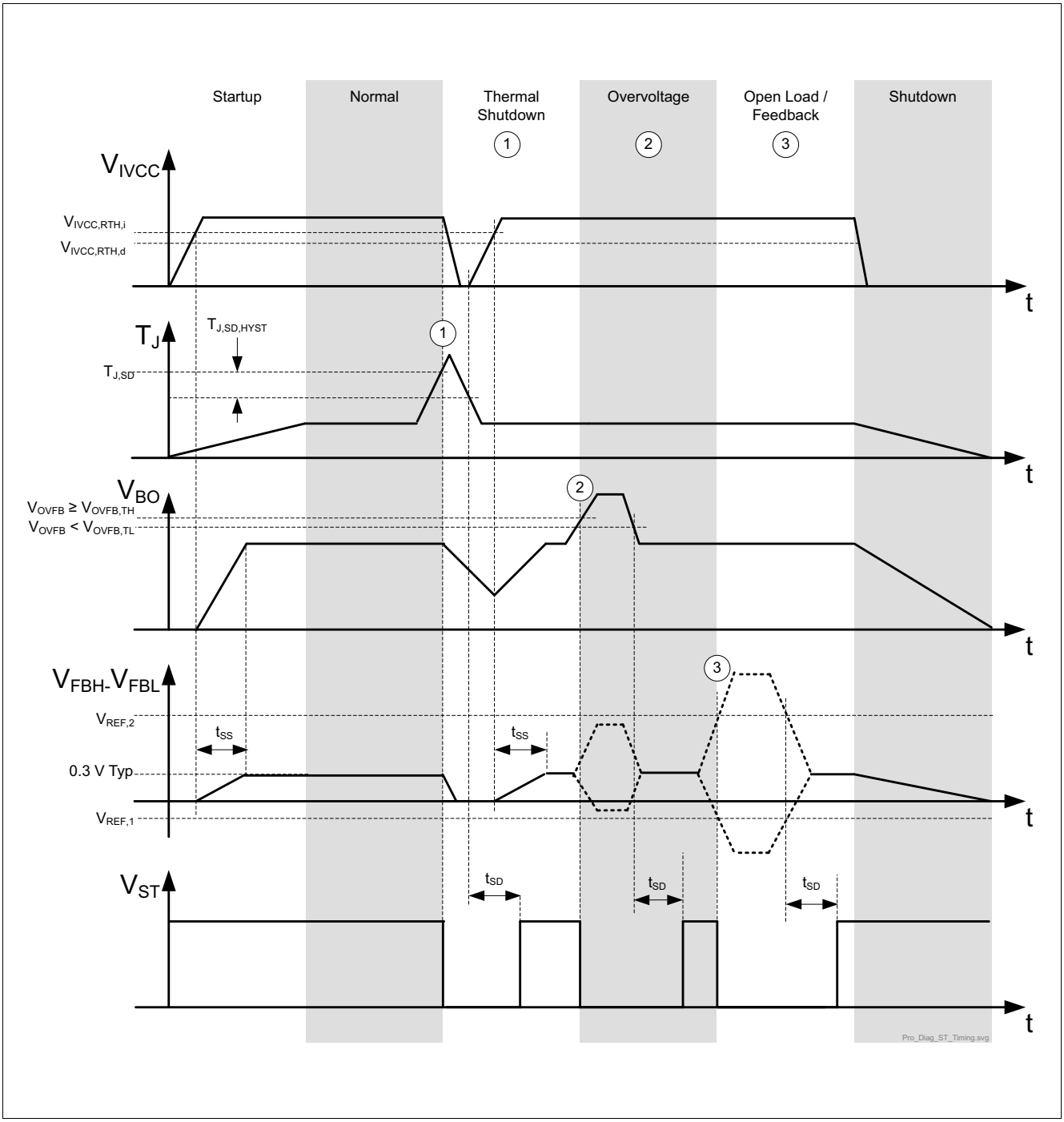


Figure 11 Status Output Timing Diagram

9.2 Electrical Characteristics

V_{IN} = 6V to 40V; 4.5V ≤ V_{FBH} ≤ 40V, 4.5V ≤ V_{FBL} ≤ 40V, T_j = -40 °C to +150 °C, all voltages with respect to ground, positive current flowing into pin; (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
Status Output:							
9.2.1	Status Output Voltage Low	$V_{ST,LOW}$	–	–	0.4	V	I_{ST} = 1mA
9.2.2	Status Sink Current Limit	$I_{ST,MAX}$	2	–	–	mA	V_{ST} = 1V
9.2.3	Status Output Current	$I_{ST,HIGH}$	–	–	1	µA	V_{ST} = 5V
9.2.4	Status Delay Time	t_{SD}	8	10	12	ms	–
Temperature Protection:							
9.2.5	Over Temperature Shutdown	$T_{j,SD}$	160	175	190	°C	–
9.2.6	Over Temperature Shutdown Hystereses	$T_{j,SD,HYST}$	–	15	–	°C	–
Overvoltage Protection:							
9.2.7	Output Over Voltage Feedback Threshold Increasing	$V_{OVFB,TH}$	1.21	1.25	1.29	V	–
9.2.8	Output Over Voltage Feedback Hysteresis	$V_{OVFB,HYS}$	50	–	150	mV	Output Voltage decreasing
9.2.9	Over Voltage Reaction Time	t_{OVPRR}	2	–	10	µs	Output Voltage decreasing
9.2.10	Over Voltage Feedback Input Current	I_{OVFB}	-1	0.1	1	µA	V_{OVFB} = 1.25 V
Open Load and Open Feedback Diagnostics							
9.2.11	Open Load/Feedback Threshold	$V_{REF,1,3}$	-100	–	-20	mV	V_{REF} = V_{FBH} - V_{FBL} Open Circuit 1 or 3
9.2.12	Open Feedback Threshold	$V_{REF,2}$	0.5	–	1	V	V_{REF} = V_{FBH} - V_{FBL} Open Circuit 2

Note: Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as "outside" normal operating range. Protection functions are not designed for continuous repetitive operation.

10 Package Outlines

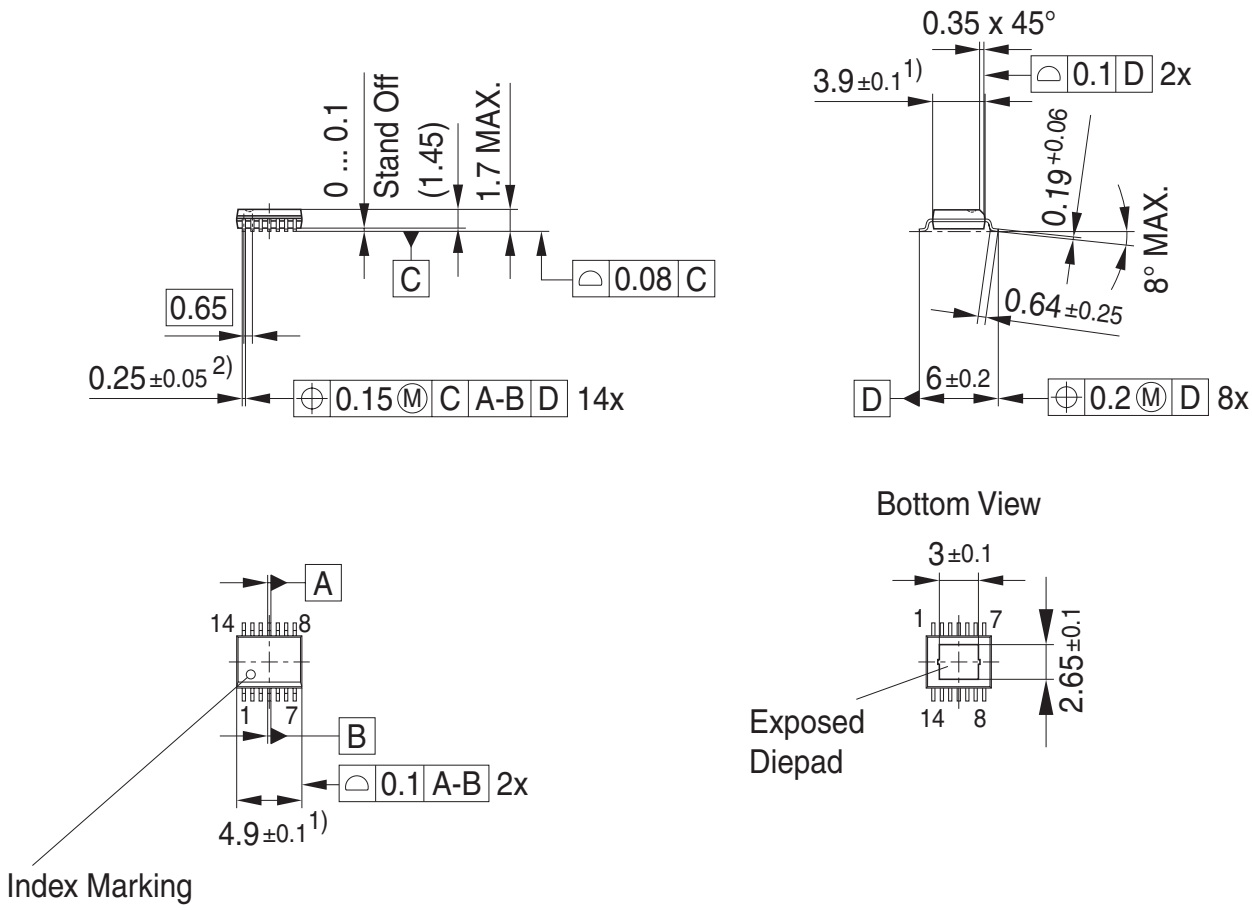


Figure 12 PG-SSOP-14

Green Product (RoHS compliant)

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-Compliant (i.e Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

For further package information, please visit our website:
http://www.infineon.com/packages.

Dimensions in mm

11 Application Information

Note: The following information is given as a hint for the implementation of the device only and shall not be regarded as a description or warranty of a certain functionality, condition or quality of the device.

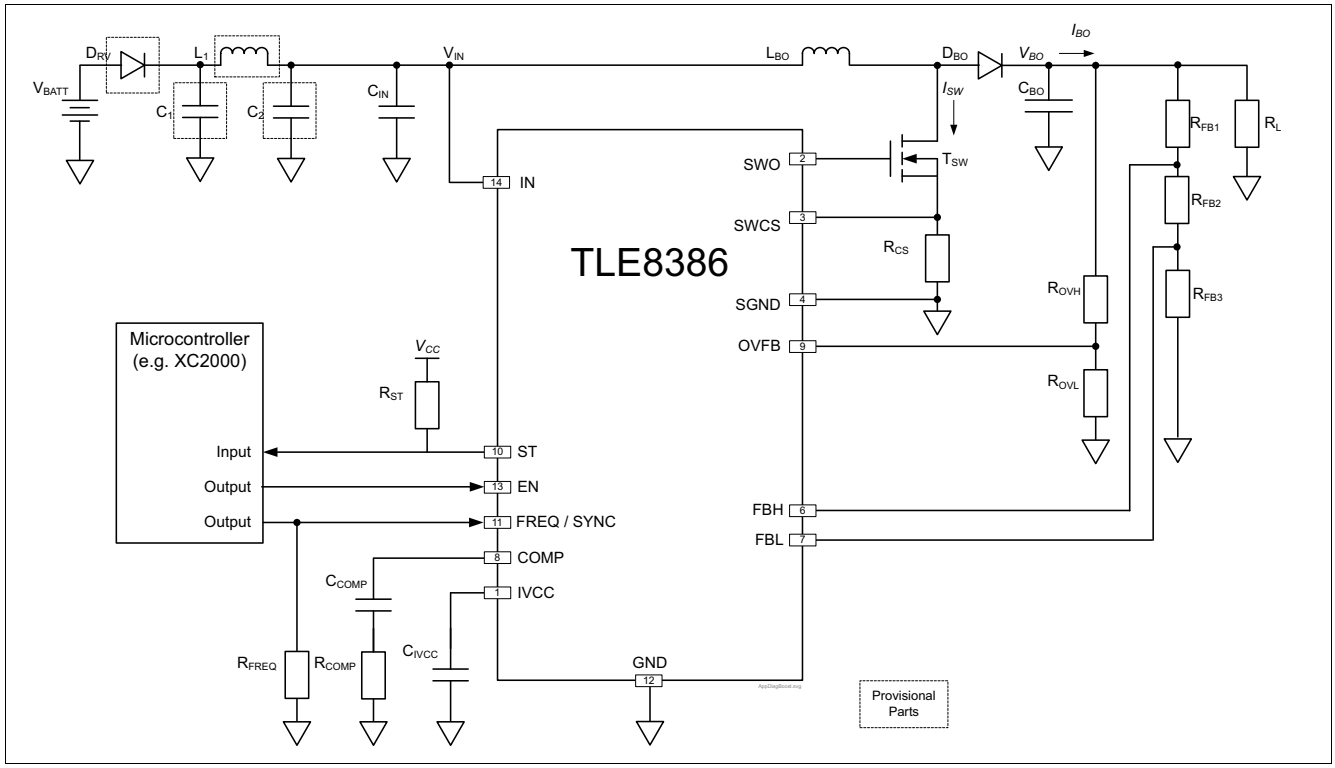


Figure 13 Boost Voltage Application Circuit (Voltage Source)

Reference Designator	Value	Manufacturer	Part Number	Type	Quantity
D_{BO}	Schottky, 3 A, 100 V_R	Vishay	SS3H10	Diode	1
C_{BO}	100 uF, 80V	Panasonic	EEVFK1K101Q	Capacitor	1
C_{IN}	100 uF, 50V	Panasonic	EEEFK1H101GP	Capacitor	1
C_{COMP}	10 nF	--	--	Capacitor	1
C_{IVCC}	1 uF, 6.3V	EPCOS	MLCC CCNPZC105KBW X76	Capacitor	1
IC_1	--	Infineon	TLE8386EL	IC	1
IC_2	--	Infineon	XC886	IC	1
L_{BO}	100 uH	Coilcraft	MSS1278T-104ML_	Inductor	1
R_{COMP}	10 kΩ	--	--	Resistor	1
R_{FB1},R_{FB3}	51 kΩ, 1%	Panasonic	ERJ3EKF5102V	Resistor	1
R_{FB2}	1 kΩ, 1%	Panasonic	ERJ3EKF1001V	Resistor	1
R_{FREQ}, R_{ST}	20 kΩ, 1%	Panasonic	ERJ3EKF2002V	Resistor	2
R_{OVH}	51 kΩ, 1%	Panasonic	ERJP06F5102V	Resistor	1
R_{OVL}	1 kΩ, 1%	Panasonic	ERJ3EKF1001V	Resistor	1
R_{CS}	50 mΩ, 1%	Panasonic	ERJB1CFR05U	Resistor	1
T_{SW}	N-ch, 75 V, 65 mΩ	Infineon	IPD22N08S2L-50	Transistor	1

Figure 14 Bill of Materials for Boost Voltage Application Circuit

Note: This is a simplified example of an application circuit. The function must be verified in the real application.

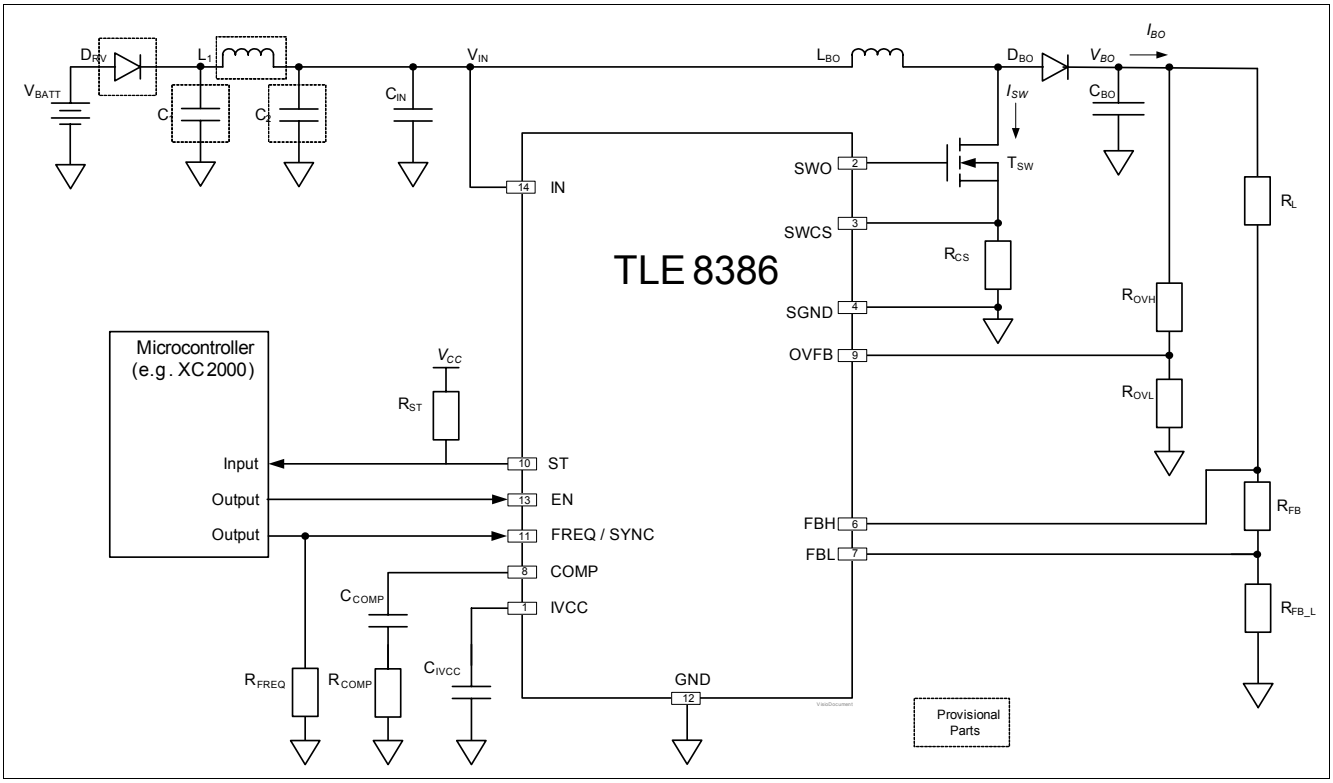


Figure 15 Boost Voltage Application Circuit (Current Source)

11.1 Further Application Information

In fixed frequency mode where an external resistor configures the switching frequency the minimum boost inductor is given by the formula in**Figure 16**.

- L_{MIN} = Minimum Inductacne Required During Fixed Frequency Operation
- V_{BO} = Boost Output Voltage
- R_{CS} = Current Sense Resistor
- f_{FREQ} = Switching Frequency

$$L_{MIN} \geq \frac{V_{BO}[V] \times R_{CS}[\Omega]}{106 \times 10^{-3}[V] \times f_{FREQ}[Hz]}$$

Figure 16 Minimum Inductance Required During Fixed Frequency Operation

In synchronization mode where an external clock source configures the switching frequency the minimum boost inductor is given by the formula in **Figure 17**.

- L_{SYNC} = Minimum Inductacne Required During Synchronization Operation
- V_{BO} = Boost Output Voltage
- R_{CS} = Current Sense Resistor

$$L_{SYNC} \geq \frac{V_{BO}[V] \times R_{CS}[\Omega]}{106 \times 10^{-3}[V] \times 250kHz}$$

Figure 17 Minimum Inductance Required During Synchronization Operation

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12 Revision History

Revision	Date	Changes
1.0	2009-11-30	Initial datasheet

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