V53C665
64K x 16 BIT FAST PAGE MODE
WRITE-PER-BIT CMOS DYNAMIC RAM

V53C665	80 ns	100 ns
Max. $\overline{RAS}$ Access Time, (t_{RAC})	80 ns	100 ns
Max. Column Address Access Time, (t_{CAA})	45 ns	55 ns
Min. Fast Page Mode Cycle Time, (t_{PC})	55 ns	65 ns
Min. Read/Write Cycle Time, (t_{RC})	135 ns	170 ns

Features

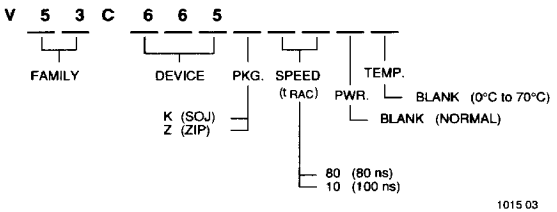
- 65,536 word by 16 bit organization
- Fast access and Cycle times
- Low power
  - 632 mW Max. Operating (80 ns)
  - 495 mW Max. Operating (100 ns)
  - 5.5 mW Max. Standby
- Read-Modify-Write, $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$-only refresh, Hidden refresh, Write-Per-Bit and Fast Page Mode capability
- All inputs and outputs TTL compatible
- 256 refresh cycles/4 ms
- Available in 40 Pin Plastic SOJ and Plastic ZIP packages

Description

The V53C665 is a high speed, 65,536 word x 16 bit CMOS dynamic RAM. Fabricated with Vitelic's CMOS technology, the V53C665 offers Fast Page Mode, Write-Per-Bit for masking of the data bits during memory access, fast usable speed, and low standby current for portable applications. Fast Page Mode operation allows random access of up to 256 x 16 bits within a row with cycle times as short as 55 ns. These features make the V53C665 ideal for graphics and high performance, high bandwidth systems.

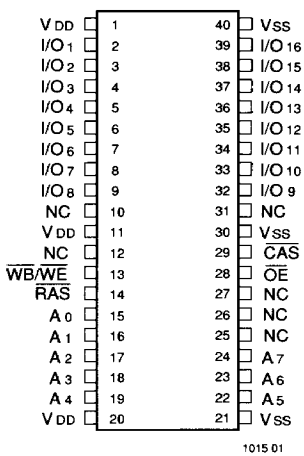
Device Usage Chart

Operating Temperature Range	Package Outline		Access Time (ns)		Power	Temperature Mark
	K	Z	80	100	Std.	
0°C to 70°C	•	•	•	•	•	Blank

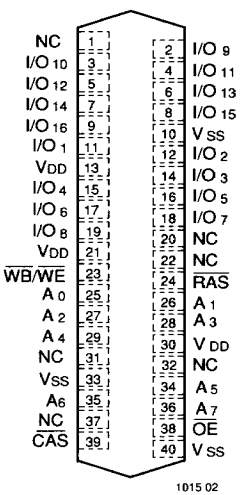


Description	Pkg.	Pin Count
Plastic SOJ	K	40
Plastic ZIP	Z	40

40-Pin Plastic SOJ
PIN CONFIGURATION
Top View



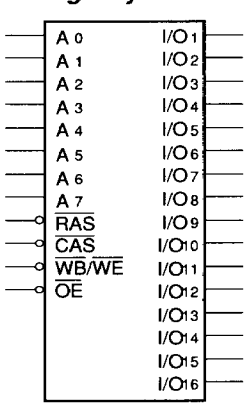
40-Pin Plastic ZIP
PIN CONFIGURATION
Top View



Pin Names

Symbol	Name
A0 – A7	Address Inputs
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WB/WE}$	Write Per Bit/ Read/Write Input
$\overline{OE}$	Output Enable
I/O1 – I/O16	Data Input/Output
V_{DD}	Power (+ 5V)
V_{SS}	Ground
NC	No Connection

Logic Symbol



Absolute Maximum Ratings*

Ambient Temperature
Under Bias ..... −10°C to +80°C
Storage Temperature (plastic) .... −55°C to +125°C
Voltage on any Pin Except V_{DD}
Relative to V_{SS} ..... −1.0 to +7.0 V
Voltage on V_{DD} relative to V_{SS} ..... −1.0 to +7.0 V
Data Out Current ..... 50 mA
Power Dissipation ..... 1.0 W

*Note: Operation above Absolute Maximum Ratings can adversely affect device reliability.

Capacitance*

V_{DD} = 5V ± 10%, V_{SS} = 0V

Symbol	Parameter	Min.	Max.	Unit
C_{IN1}	Input Capacitance (A0 – A7)	3	4	pF
C_{IN2}	Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WB/WE}$, $\overline{OE}$)	4	5	pF
C_{OUT}	Output Capacitance (I/O1 – I/O16)	5	7	pF

*NOTE: Capacitance is sampled and not 100% tested

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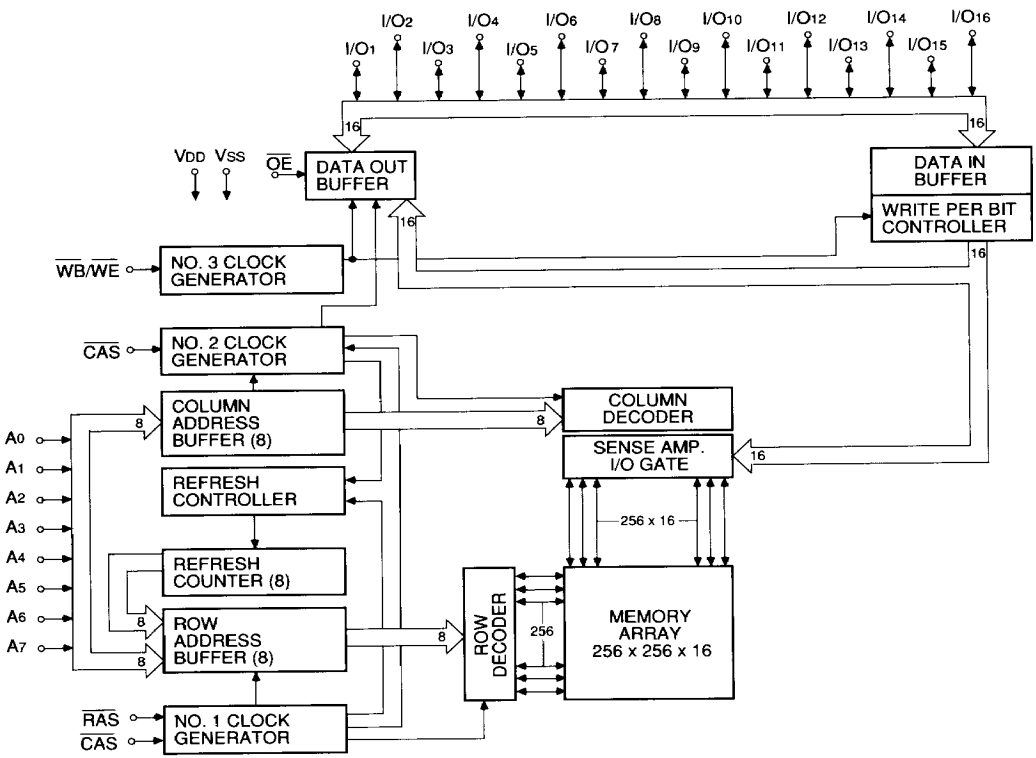
Block Diagram



DC and Operating Characteristics (1,2)

T_A = 0°C to 70°C, V_{DD} = 5V ± 10%, V_{SS} = 0V unless otherwise specified

Symbol	Parameter	Access Time (ns)	Min.	Max.	Unit	Test Conditions	Notes
I_{LI}	Input Leakage Current (any input pin)		-10	10	µA	$V_{SS} \le V_{IN} \le V_{DD}$	
I_{LO}	Output Leakage Current		-10	10	µA	$V_{SS} \le V_{OUT} \le V_{DD}$	
I_{DD1}	V_{DD} Supply Current, Operating	80	—	115	mA	$t_{RC} = t_{RC}$ (Min.)	1, 2, 4
		100	—	90			
I_{DD2}	V_{DD} Supply Current, TTL Standby		—	2	mA	$\overline{RAS} = \overline{CAS} = V_{IH}$ Other Inputs ≥ V_{SS}	
I_{DD3}	V_{DD} Supply Current, $\overline{RAS}$-Only Refresh	80	—	115	mA	$t_{RC} = t_{RC}$ Min.	2, 4
		100	—	90			
I_{DD4}	V_{DD} Supply Current, Fast Page Mode Operation	80	—	70	mA	Minimum Cycle	1, 2, 4
		100	—	60			
I_{DD5}	V_{DD} Supply Current, Standby, Output Enabled		—	1	mA	$\overline{RAS} = V_{IH}$, $\overline{CAS} = V_{IL}$, Other Inputs ≥ V_{SS}	1
I_{DD6}	V_{DD} Supply Current, $\overline{CAS}$ before $\overline{RAS}$ Mode	80	—	115	mA	$\overline{RAS} \ge V_{DD}$ - 0.2 V, $\overline{CAS}$ at V_{IH} All Other Inputs ≥ V_{SS}	
		100	—	90			
V_{IH}	Input High Voltage		-1	0.8	V		3
V_{IL}	Input Low Voltage		2.4	V_{DD}+1	V		3
V_{OH}	Output High Voltage		2.4	—	V	I_{OH} = -5 mA	
V_{OL}	Output Low Voltage		—	0.4	V	I_{OL} = 4.2 mA	

AC Characteristics (5, 6, 7)

T_A = 0°C to 70°C, V_{DD} = 5V ± 10%, V_{SS} = 0V unless otherwise noted
AC Test conditions, input pulse levels 0 to 3 V

#	JEDEC Symbol	Symbol	Parameter	80 Min.	80 Max.	100 Min.	100 Max.	Unit	Notes
1	t_{RL1RH1}	t_{RAS}	$\overline{RAS}$ Pulse Width	80	10K	100	10K	ns	
2		t_{RASP}	$\overline{RAS}$ Pulse Width (Fast Page Mode)	80	100K	100	100K	ns	
3	t_{RL2RL2}	t_{RC}	Read or Write Cycle Time	135	—	170	—	ns	
4	t_{RH2RL2}	t_{RP}	$\overline{RAS}$ Precharge Time	45	—	60	—	ns	
5	t_{RL1CH1}	t_{CSH}	$\overline{CAS}$ Hold Time	80	—	100	—	ns	
6	t_{CL1CH1}	t_{CAS}	$\overline{CAS}$ Pulse Width	35	10K	40	10K	ns	
7	t_{RL1CL1}	t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	20	45	20	60	ns	13
8	t_{WH2CL2}	t_{RCS}	Read Command Set-Up Time	0	—	0	—	ns	
9	t_{AVRL2}	t_{ASR}	Row Address Set-Up Time	0	—	0	—	ns	
10	t_{RL1AX}	t_{RAH}	Row Address Hold Time	10	—	10	—	ns	
11	t_{AVCL2}	t_{ASC}	Column Address Set-Up Time	0	—	0	—	ns	
12	t_{CL1AX}	t_{CAH}	Column Address Hold Time	15	—	15	—	ns	
13	t_{CL1RH1}	t_{RSH}	$\overline{RAS}$ Hold Time	35	—	40	—	ns	
14	t_{CH2RL2}	t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5	—	5	—	ns	
15	t_{CH2WX}	t_{RCH}	Read Command Hold Time referenced to $\overline{CAS}$	0	—	0	—	ns	10
16	t_{RH2WX}	t_{RRH}	Read Command Hold Time referenced to $\overline{RAS}$	0	—	0	—	ns	10
17	$t_{OEL1RH2}$	t_{ROH}	$\overline{RAS}$ Hold Time referenced to $\overline{OE}$	15	—	20	—	ns	
18	t_{GL1QV}	t_{OAC}	Access Time from $\overline{OE}$	—	35	—	40	ns	
19	t_{CL1QV}	t_{CAC}	Access Time from $\overline{CAS}$	—	35	—	40	ns	8,13
20	t_{RL1QV}	t_{RAC}	Access Time from $\overline{RAS}$	—	80	—	100	ns	8,13,14
21	t_{AVQV}	t_{CAA}	Access Time from Column Address	—	45	—	55	ns	5,14
22	t_{CL1QX}	t_{LZ}	$\overline{CAS}$ to Output in Low-Z	0	—	0	—	ns	8
23	t_{RL1AX}	t_{AR}	Column Address Hold Time referenced to $\overline{RAS}$	55	—	65	—	ns	
24	t_{RL1AV}	t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	35	15	45	ns	14
25	t_{WL1CH1}	t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	20	—	20	—	ns	
26	t_{WL1CL2}	t_{WCS}	Write Command Set-Up Time	0	—	0	—	ns	12
27	t_{CL1WH1}	t_{WCH}	Write Command Hold Time	15	—	15	—	ns	
28	t_{WL1WH1}	t_{WP}	Write Command Pulse Width	15	—	15	—	ns	
29	t_{RL1WH1}	t_{WCR}	Write Command Hold Time from $\overline{RAS}$	55	—	65	—	ns	
30	t_{WL1RH1}	t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	20	—	20	—	ns	

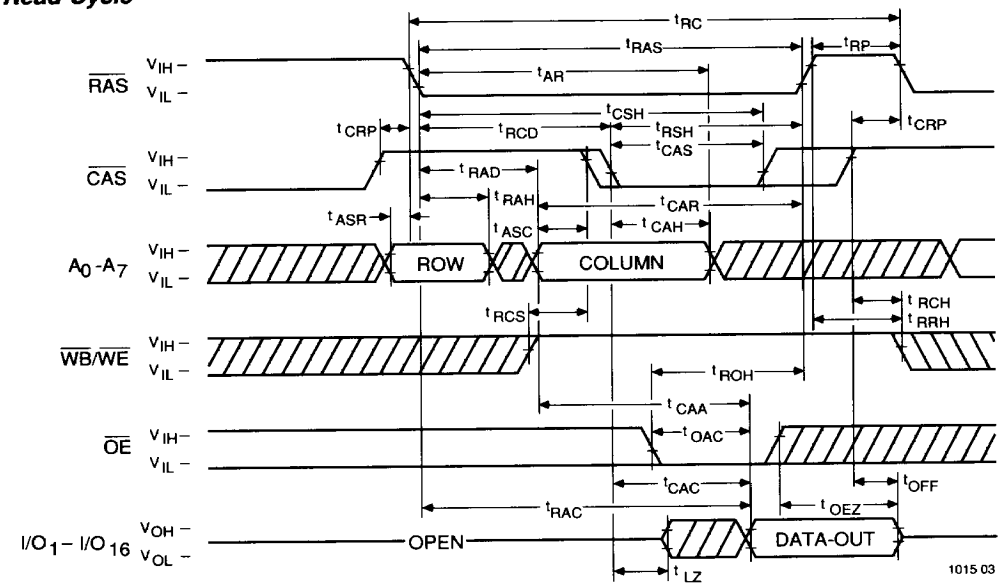
AC Characteristics (continued)

#	JEDEC Symbol	Symbol	Parameter	80		100		Unit	Notes
				Min.	Max.	Min.	Max.		
31	t_{DVWL2}	t_{DS}	Data-In Set-Up Time	0	—	0	—	ns	11
32	t_{WL1DX}	t_{DH}	Data-In Hold Time	15	—	15	—	ns	11
33	t_{GH2DX}	t_{OED}	$\overline{OE}$ to Data Delay Time	10	—	20	—	ns	
34	t_{RL2RL2} (RMW)	t_{RWC}	Read-Modify-Write Cycle Time	180	—	225	—	ns	
35	t_{CL1WL2}	t_{CWD}	$\overline{CAS}$ to $\overline{WE}$ Delay Time	55	—	70	—	ns	12
36	t_{RL1WL2}	t_{RWD}	$\overline{RAS}$ to $\overline{WE}$ Delay Time in Read-Modify-Write Cycle	100	—	130	—	ns	12
37	t_{AVWL2}	t_{AWD}	Column Address to $\overline{WE}$ Delay Time	65	—	85	—	ns	12
38	t_{CL2CL2}	t_{PC}	Fast Page Mode Cycle Time	55	—	65	—	ns	
39	t_{CH2CL2}	t_{CP}	$\overline{CAS}$ Precharge Time	10	—	10	—	ns	
40	t_{AVRH1}	t_{CAR}	Column Address to $\overline{RAS}$ Set-Up Time	45	—	55	—	ns	
41	t_{CH2QV}	t_{CAP}	Access Time from Column Precharge	—	50	—	60	ns	8
42	t_{RL1DX}	t_{DHR}	Data Hold Time referenced to $\overline{RAS}$	55	—	65	—	ns	
43	t_{CL1RL2}	t_{CSR}	$\overline{CAS}$ Set-Up Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh)	5	—	5	—	ns	
44	t_{RH2CL2}	t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	0	—	0	—	ns	
45	t_{RL1CH1}	t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh)	10	—	10	—	ns	
46	t_{CL2CL2} (RMW)	t_{PCM}	Fast Page Mode Read-Modify-Write Cycle Time	100	—	120	—	ns	
47		t_{CPWD}	$\overline{CAS}$ Precharge to $\overline{WE}$ Delay Time (Fast Page Mode)	70	—	90	—	ns	12
48		t_{CPT}	$\overline{CAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$ Counter Test Cycle)	40	—	40	—	ns	
49		t_{OEZ}	Output Buffer Turn Off Delay Time from $\overline{OE}$	0	10	0	20	ns	
50		t_{OEH}	$\overline{OE}$ Command Hold Time	10	—	20	—	ns	
51		t_{WBS}	Write-Per-Bit Set-Up Time	0	—	0	—	ns	
52		t_{WBH}	Write-Per-Bit Hold Time	10	—	10	—	ns	
53		t_{WDS}	Write-Per-Bit Selection Set-Up Time	0	—	0	—	ns	
54		t_{WDH}	Write-Per-Bit Selection Hold Time	10	—	10	—	ns	
55		t_{OFF}	Output Buffer Turn-off Delay	0	20	0	20	ns	9
56		t_T	Transition Time (Rise and Fall)	3	50	3	50	ns	7
57		t_{RI}	Refresh Interval	—	4	—	4	ms	

NOTES:

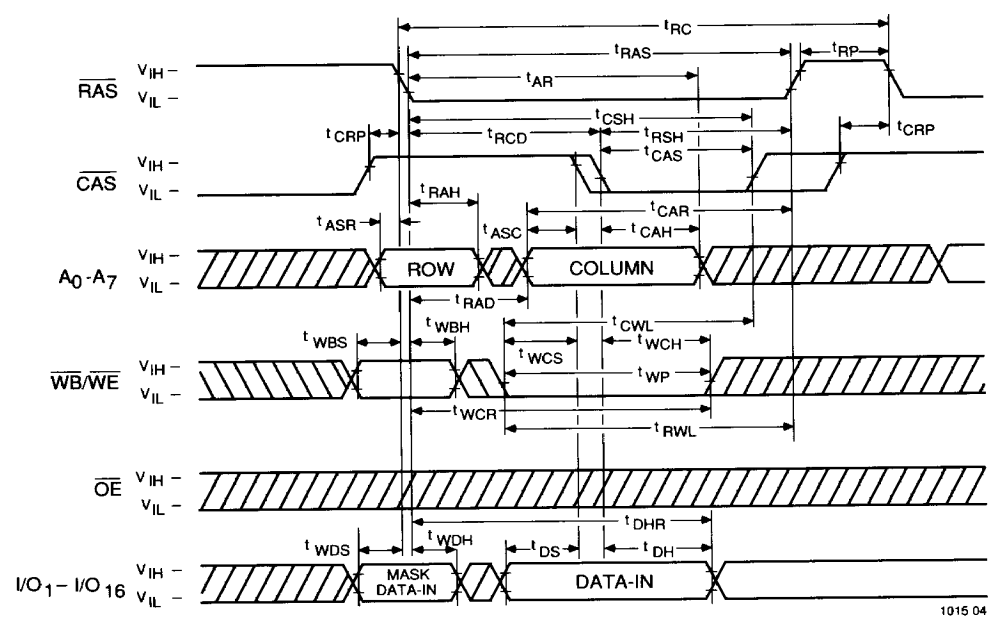
1. I_{DD} is dependent on output loading when the device output is selected. Specified I_{DD} (max.) is measured with the output open.
2. I_{DD} is dependent upon the number of address transitions. Specified I_{DD} (max.) is measured with a maximum of two transitions per address cycle in Fast Page Mode.
3. Specified V_{IL} (min.) is steady state operating. During transitions, V_{IL} (min.) may undershoot to -1.0 V for a period not to exceed 20 ns. All AC parameters are measured with V_{IL} (min.) $\geq V_{SS}$ and V_{IH} (max.) $\leq V_{DD}$.
4. Column Address can be changed once or less while $\overline{RAS} = V_{IL}$ and $\overline{CAS} = V_{IH}$
5. An initial pause of 200 µs is required after power-up followed by 8 $\overline{RAS}$ only refresh cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ refresh cycles instead of 8 $\overline{RAS}$ only refresh cycles is required.
6. AC measurements assume $t_T = 5$ ns.
7. V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring timing of output signals. Also, transition times are measured between V_{IH} and V_{IL}.
8. Measured with a load equivalent to one TTL load and 50 pF.
9. t_{OFF} (max.) and t_{OEZ} (max.) define the time at which the outputs achieve the open circuit condition and are not referenced to output voltage levels.
10. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
11. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WB}$/ $\overline{WE}$ leading edge in read-modify-write cycles.
12. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD} and t_{CPWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$ (min.) the cycle is an early write cycle and data out pins will remain open circuit (high impedance) through the entire cycle. If $t_{RWD} \geq t_{RWD}$ (min.), $t_{CWD} \geq t_{CWD}$ (Min.), $t_{AWD} \geq t_{AWD}$ (min.) and $t_{CPWD} \geq t_{CPWD}$ (min.), the cycle is a read-modify-write cycle and the data out will contain data read from the selected cell. If neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
13. Operation within the t_{RCD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RCD} (max.) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (Max.) limit, then access time is controlled by t_{CAC}.
14. Operation within the t_{RAD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RAD} (max.) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max.) limit, then access time is controlled by t_{CAA}.

Read Cycle



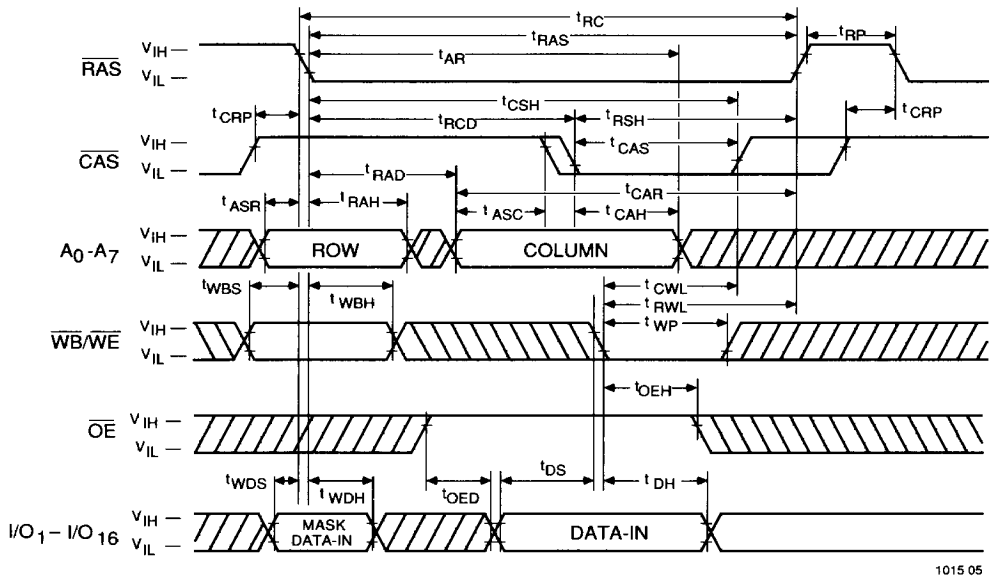
NOTE: D_{IN} = OPEN

Write Cycle (Early Write)



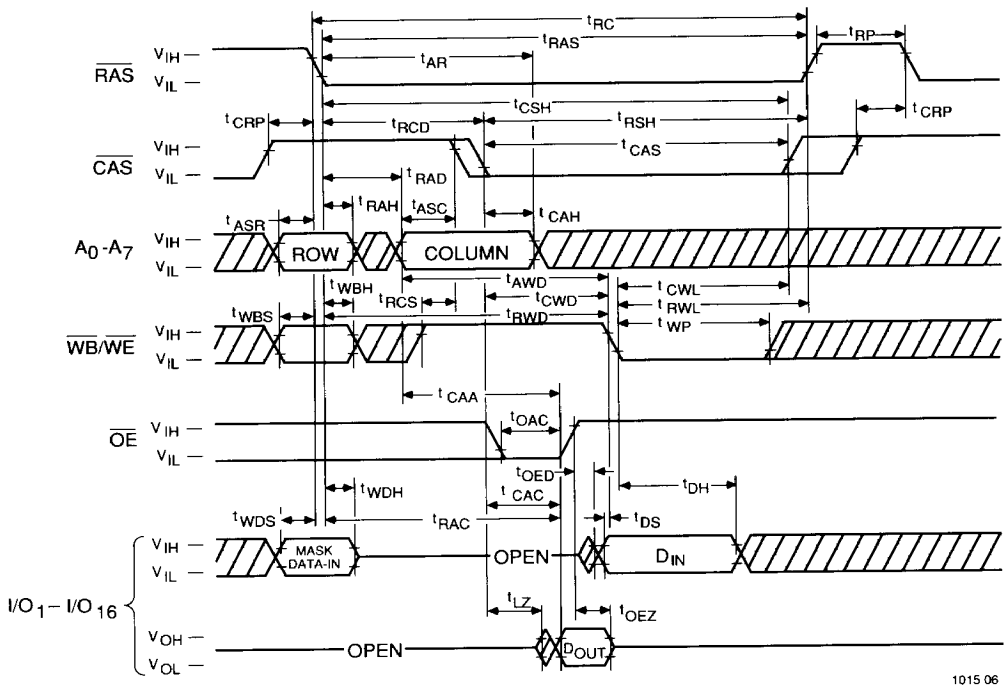
NOTE: D_{OUT} = OPEN

Write Cycle ($\overline{OE}$-Controlled Write)

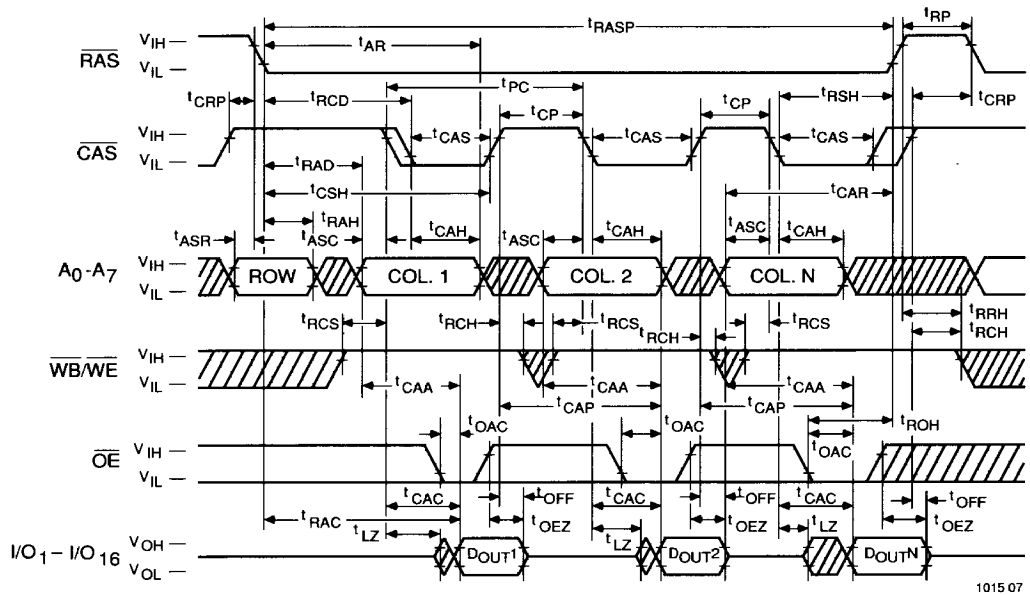


NOTE: D_{OUT} = OPEN

Read-Modify-Write Cycle

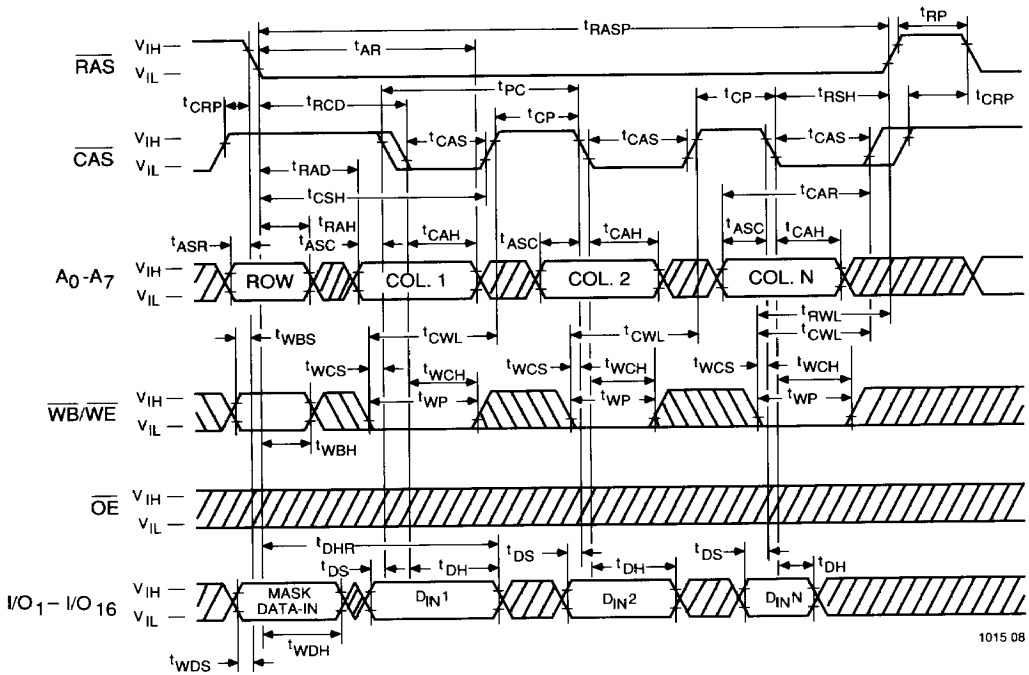


Fast Page Mode Read Cycle



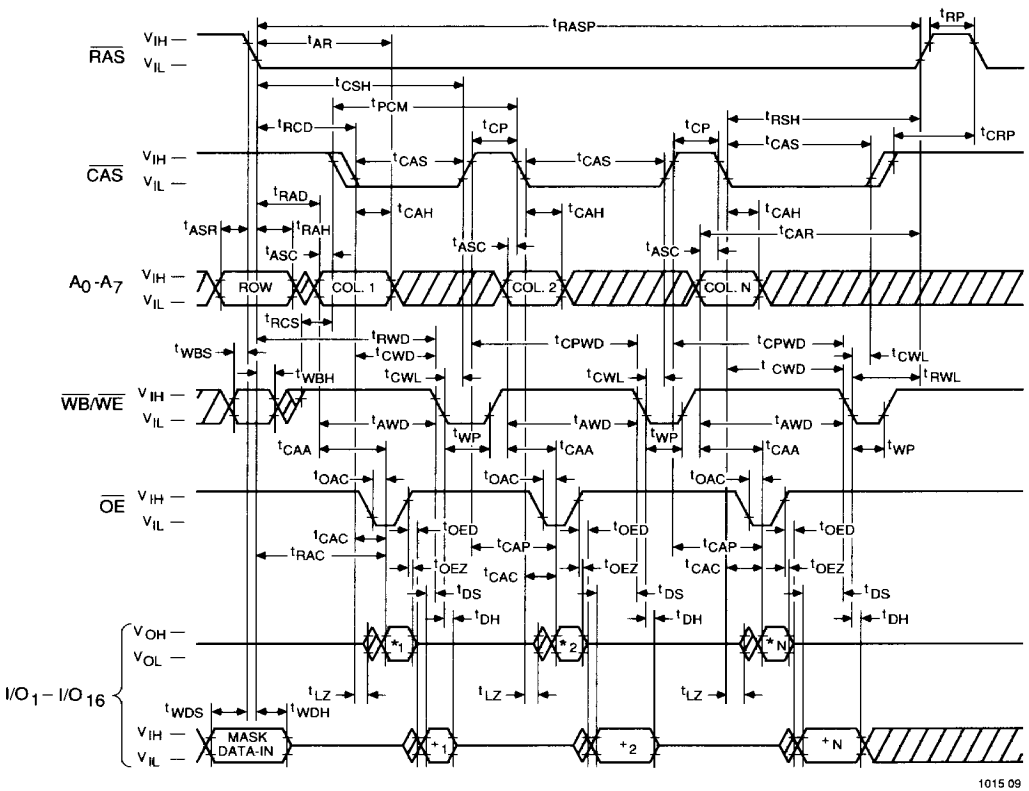
NOTE: D_{IN} = OPEN

Fast Page Mode Write Cycle



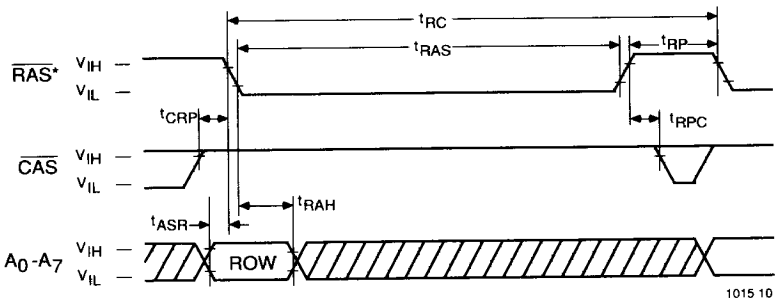
NOTE: D_{OUT} = OPEN

Fast Page Read-Modify-Write Cycle



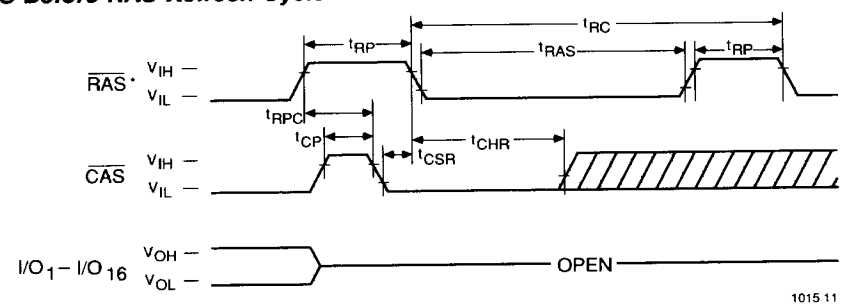
NOTE: * = D_{OUT}, + = D_{IN}

$\overline{RAS}$-Only Refresh Cycle



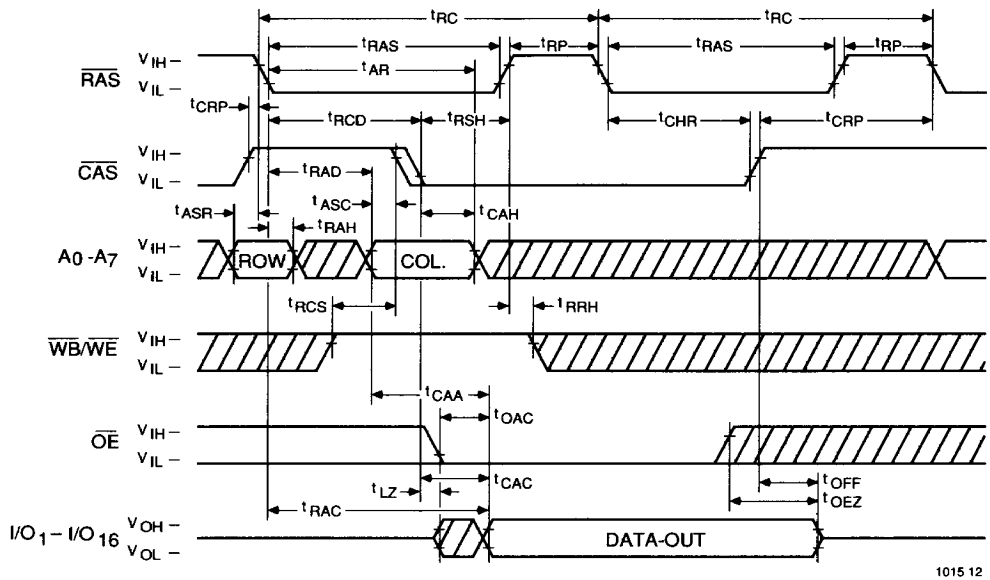
NOTE: $\overline{WB}/\overline{WE}$, $\overline{OE}$ = "H" or "L"

$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Cycle



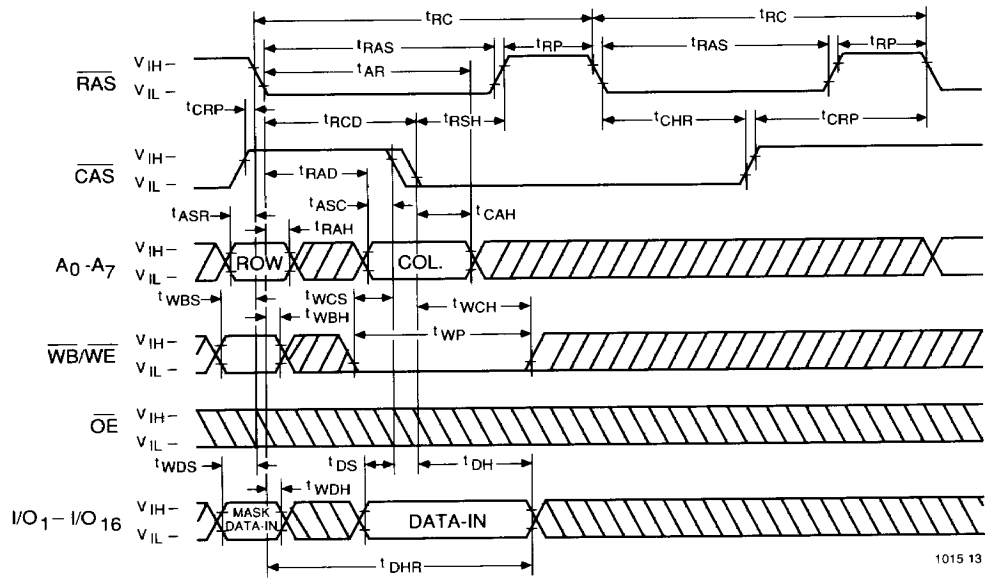
NOTE: D_{IN}, $\overline{WB}/\overline{WE}$, $\overline{OE}$, A0 – A7 = "H" or "L"

Hidden Refresh Cycle (Read)



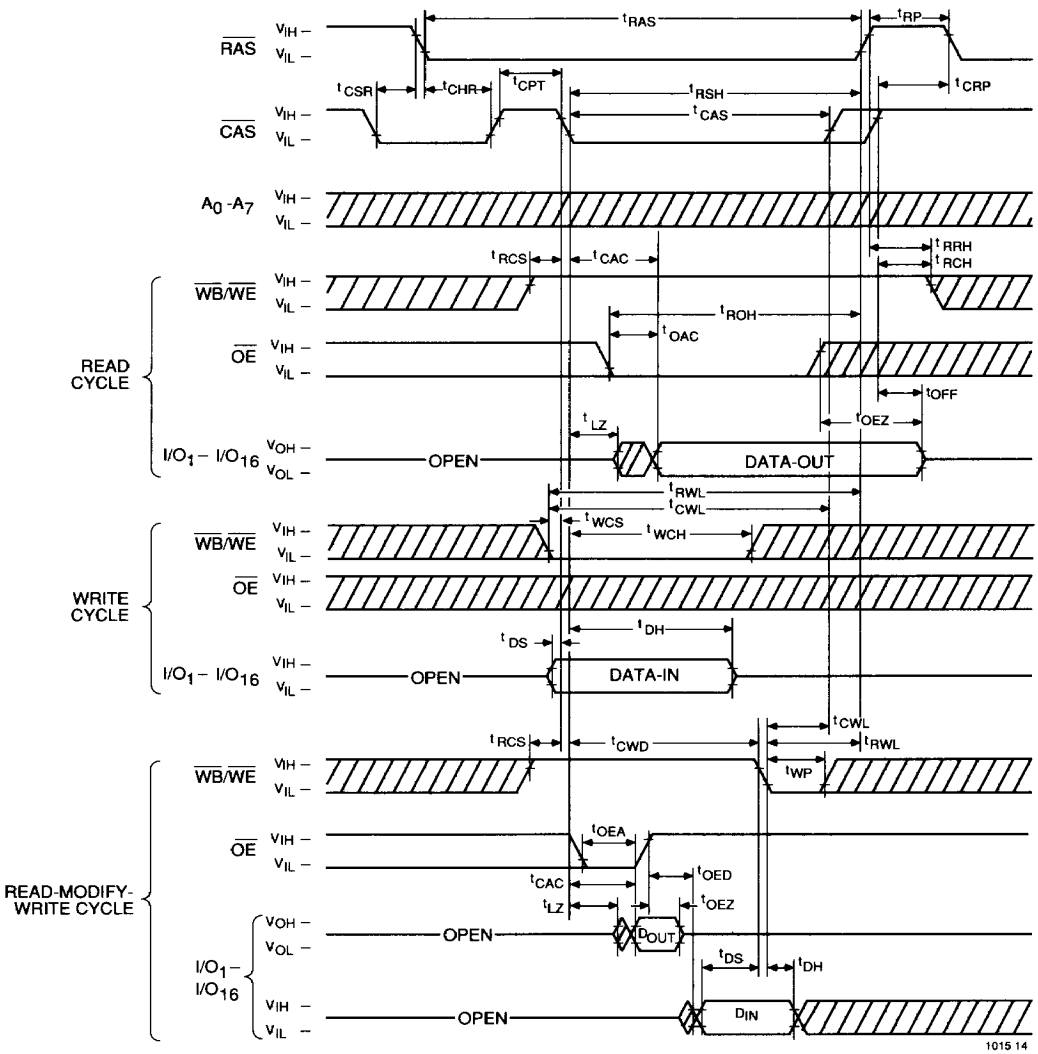
NOTE: D_{IN} = OPEN

Hidden Refresh Cycle (Write)



NOTE: D_{OUT} = OPEN

CAS-Before-RAS Refresh Counter Test Cycle



Application Information

Addressing

The 16 address bit required to decode 1 of the 65,536 cell locations within the V53C665 are multiplexed onto the 8 address inputs and latched into the on-chip address latches by externally applying two negative going TTL-level clocks.

The first clock, the Row Address Strobe ($\overline{RAS}$), latches the 8 row address bits into the chip. The second clock, the Column Address Strobe ($\overline{CAS}$), subsequently latches the 8 column address bits into the chip. Each of these signals, $\overline{RAS}$ and $\overline{CAS}$, triggers a sequence of events which are controlled by different delayed internal clocks.

The two clock chains are linked together logically in such a way that the address multiplexing operation is done outside of the critical path timing sequence for read data access. The later events in the $\overline{CAS}$ clock sequence are inhibited until the occurence of a delayed signal derived from the $\overline{RAS}$ clock chain. The "gated $\overline{CAS}$" feature allows the $\overline{CAS}$ clock to be externally activated as soon as the Row Address Hold Time specification (t_{RAH}) has been satisfied and the address inputs have been changed from Row address to Column address information.

Data Inputs

A write cycle is performed by bringing ($\overline{WB}$/) $\overline{WE}$ low during the $\overline{RAS}$/$\overline{CAS}$ operation. The falling edge of $\overline{CAS}$ or ($\overline{WB}$/) $\overline{WE}$ strobes data on (Wi) IOi into the on-chip data latch. To make use of the write-per-bit capability ($\overline{WB}$/) $\overline{WE}$ must be low as $\overline{RAS}$ falls. In this case data bits to which the write operation is applied can be specified by keeping Wi (IOi) high with set-up and hold times referenced to the $\overline{RAS}$ negative transition. For those data bits of Wi (IOi) that are kept low as $\overline{RAS}$ falls the write operation is inhibited on the chip. If ($\overline{WB}$/) $\overline{WE}$ is high as $\overline{RAS}$ falls, the write-per-bit capability does not work and the write operation is performed for all four data bits.

Data Outputs

The three-state output buffers provide direct TTL compatibility with a fan-out of a standard TTL load. Data-out is the same polarity as data-in. The outputs are in the high-impedance state until $\overline{CAS}$ is brought low. In a read cycle the outputs go active after the access time interval t_{RAC} and t_{OAC} are satisfied.

The outputs become valid after the access time has elapsed and remain valid while $\overline{CAS}$ and $\overline{OE}$ are low. $\overline{CAS}$ or $\overline{OE}$ going high returns them to a high impedance state. In an early-write cycle, the outputs are always in the high impedance state. In a delayed-write or read-modify-write cycle, the outputs will follow the sequence for the read cycle.

The $\overline{OE}$ controls the impedance of the output buffers. In the logic high position the buffers will remain in a high impedance state.

When the $\overline{OE}$ input is brought to a logical low level, the output buffers are enabled. Both $\overline{CAS}$ and $\overline{OE}$ can control the outputs. Thus, in a read operation, either $\overline{OE}$ or $\overline{CAS}$ returning high forces the outputs into the high impedance state.

$\overline{RAS}$ Only Refresh

Refresh of the dynamic cell matrix is accomplished by performing a memory cycle at each of the 256 row addresses (A0 – A7) within each 4 millisecond time interval. Although any normal memory cycle will perform the refresh operation, this function is most easily accomplished with "$\overline{RAS}$-only" cycles—$\overline{RAS}$-only refresh results in a substantial reduction in operating power. This reduction in power is reflected in the I_{CC3} specification.

$\overline{CAS}$ Before $\overline{RAS}$ Refresh

$\overline{CAS}$ before $\overline{RAS}$ refreshing available on the V53C665 offers an alternate refresh method. If $\overline{CAS}$ is held on low for the specified period (t_{CSR}) before $\overline{RAS}$ goes to low, on-chip refresh control clock generations and the refresh address counter are enabled, and an internal refresh operation takes place. After the refresh operation is performed, the refresh address counter is automatically incremented in preparation for the next $\overline{CAS}$ before $\overline{RAS}$ refresh operation.

Fast Page Mode

The "Fast Page Mode" feature of the V53C665 allows for successive memory operations at multiple column locations of the same row address with increased speed without an increase in power. This is done by strobing the row address into the chip and maintaining the $\overline{RAS}$ signal at a logic 0 throughout all successive memory cycles in which the row address is common. This "Fast Page Mode" of operation will not dissipate the power associated with the negative going edge of $\overline{RAS}$. Also, the time required for strobing in a new address is eliminated, thereby increasing the access and cycle times.

Hidden Refresh

An optional feature of the V53C665 is that refresh cycles may be performed while maintaining valid data at the output pins. This is referred to as Hidden Refresh. Hidden Refresh is performed by holding $\overline{CAS}$ at V_{IL} and taking $\overline{RAS}$ high and after a specified precharge period (t_{RP}), executing a $\overline{CAS}$ before $\overline{RAS}$ refresh cycle. (See figure below.)

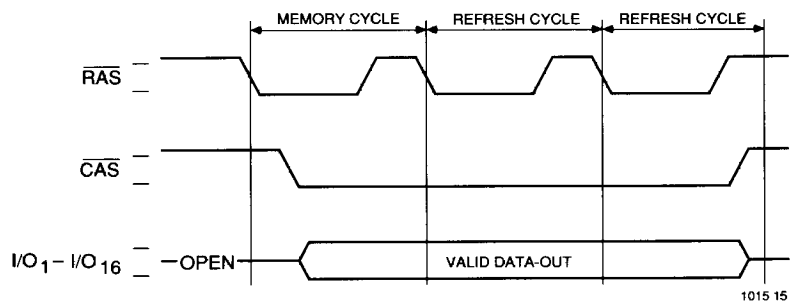
This feature allows a refresh cycle to be "Hidden" among data cycles without affecting the data availability.

$\overline{CAS}$ Before $\overline{RAS}$ Refresh Counter Test

The internal refresh operation of the V53C665 can be tested by the "$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST." This cycle performs READ/WRITE operation taking the internal counter address as row address and the input address as column address.

The test is performed after a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ cycles as initialization cycles. The test procedure is as follows:

1. Write "0" into all the memory cells at normal write mode.
2. Select one certain column address and read "0" out and write "1" in each cell by performing "$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST (READ-MODIFY-WRITE Cycle)". Repeat this operation 256 times.
3. Check "1" out of 256 bits at normal read mode, which was written in step 2.
4. Using the same column as in step 2, read "1" out and write "0" in each cell performing "$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST." Repeat this operation 256 times.
5. Check "0" out of 256 bits at normal mode, which was written in step 4.
6. Perform the above steps 1 to 5 to the complement data.



Hidden Refresh Cycle