

DATA SHEET



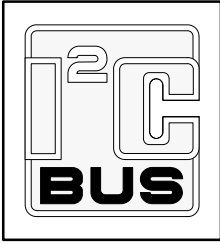
PCA9531 8-bit I²C LED dimmer

Product data

2003 Nov 10

8-bit I²C LED dimmer

PCA9531



FEATURES

- Eight LED drivers (on, off, flashing at a programmable rate)
- Two selectable, fully programmable blink rates (frequency and duty cycle) between 0.625 and 160 Hz (1.6 and 6.25 milliseconds)
- 256 brightness steps
- Input/outputs not used as LED drivers can be used as regular GPIOs
- Internal oscillator requires no external components
- I²C interface logic compatible with SMBus
- Internal power-on reset
- Noise filter on SCL/SDA inputs
- Active low reset input
- Eight open drain outputs directly drive LEDs to 25 mA
- Edge rate control on outputs
- No glitch on power-up
- Supports hot insertion
- Low stand-by current
- Operating power supply voltage range of 2.3 V to 5.5 V
- 0 to 400 kHz clock frequency
- ESD protection exceeds 2000 V HBM per JESD22-A114, 150 V MM per JESD22-A115 and 1000 V CDM per JESD22-C101
- Latch-up testing is done to JEDEC Standard JESD78 which exceeds 100 mA
- Package offer: SO16, TSSOP16, HVQFN16

ORDERING INFORMATION

| PACKAGES | TEMPERATURE RANGE | ORDER CODE | TOPSIDE MARK | DRAWING NUMBER |
|----------------------|-------------------|------------|--------------|----------------|
| 16-pin plastic SO | -40 to +85 °C | PCA9531D | PCA9531D | SOT109-1 |
| 16-pin plastic TSSOP | -40 to +85 °C | PCA9531PW | PCA9531 | SOT403-1 |
| 16-pin plastic HVQFN | -40 to +85 °C | PCA9531BS | 9531 | SOT629-1 |

Standard packing quantities and other packaging data is available at www.philipslogic.com/packaging.

I²C is a trademark of Philips Semiconductors Corporation.

DESCRIPTION

The PCA9531 is an 8-bit I²C & SMBus I/O expander optimized for dimming LEDs in 256 discrete steps for Red/Green/Blue (RGB) color mixing and back light applications.

The PCA9531 contains an internal oscillator with two user programmable blink rates and duty cycles coupled to the output PWM. The LED brightness is controlled by setting the blink rate high enough (> 100 Hz) that the blinking can not be seen and then using the duty cycle to vary the amount of time the LED is on and thus the average current through the LED.

The initial setup sequence programs the two blink rates/duty cycles for each individual PWM. From then on, only one command from the bus master is required to turn individual LEDs ON, OFF, BLINK RATE 1 or BLINK RATE 2. Based on the programmed frequency and duty cycle, BLINK RATE 1 and BLINK RATE 2 will cause the LEDs to appear at a different brightness or blink at periods up to 1.6 second. The open drain outputs directly drive the LEDs with maximum output sink current of 25 mA per bit and 100 mA per package.

To blink LEDs at periods greater than 1.6 second the bus master (MCU, MPU, DSP, chipset, etc.) must send repeated commands to turn the LED on and off as is currently done when using normal I/O Expanders like the Philips PCF8574 or PCA9554. Any bits not used for controlling the LEDs can be used for General Purpose Parallel Input/Output (GPIO) expansion which provides a simple solution when additional I/O is needed for ACPI power switches, sensors, push-buttons, alarm monitoring, fans, etc.

The active low hardware reset pin (RESET) and Power On Reset (POR) initializes the registers to their default state causing the bits to be set high (LED off).

Three hardware address pins on the PCA9531 allow eight devices to operate on the same bus.

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PIN CONFIGURATION — SO, TSSOP

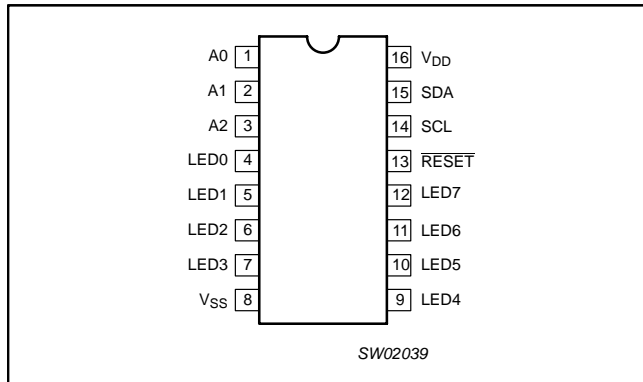


Figure 1. Pin configuration — SO, TSSOP

PIN CONFIGURATION — HVQFN

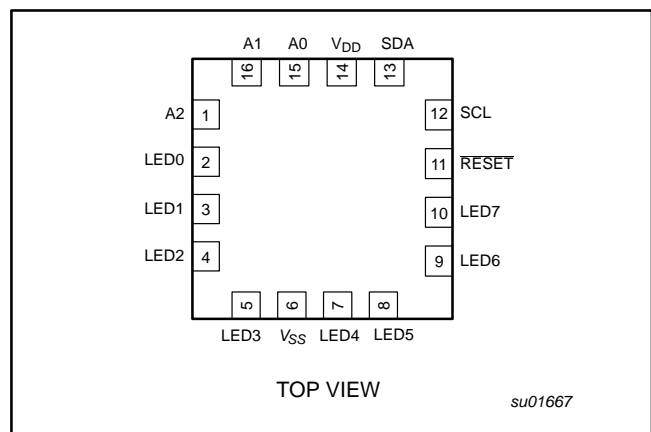


Figure 2. Pin configuration — HVQFN

PIN DESCRIPTION

| SO, TSSOP PIN NUMBER | HVQFN PIN NUMBER | SYMBOL | FUNCTION |
|----------------------------|------------------------|-----------------|------------------------|
| 1 | 15 | A0 | Address input 0 |
| 2 | 16 | A1 | Address input 1 |
| 3 | 1 | A2 | Address input 2 |
| 4, 5, 6, 7 | 2, 3, 4, 5 | LED0-3 | LED drivers 0-3 |
| 8 | 6 | V _{SS} | Supply ground |
| 9, 10, 11, 12 | 7, 8, 9, 10 | LED4-7 | LED drivers 4-7 |
| 13 | 11 | RESET | Active low reset input |
| 14 | 12 | SCL | Serial clock line |
| 15 | 13 | SDA | Serial data line |
| 16 | 14 | V _{DD} | Supply voltage |

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BLOCK DIAGRAM

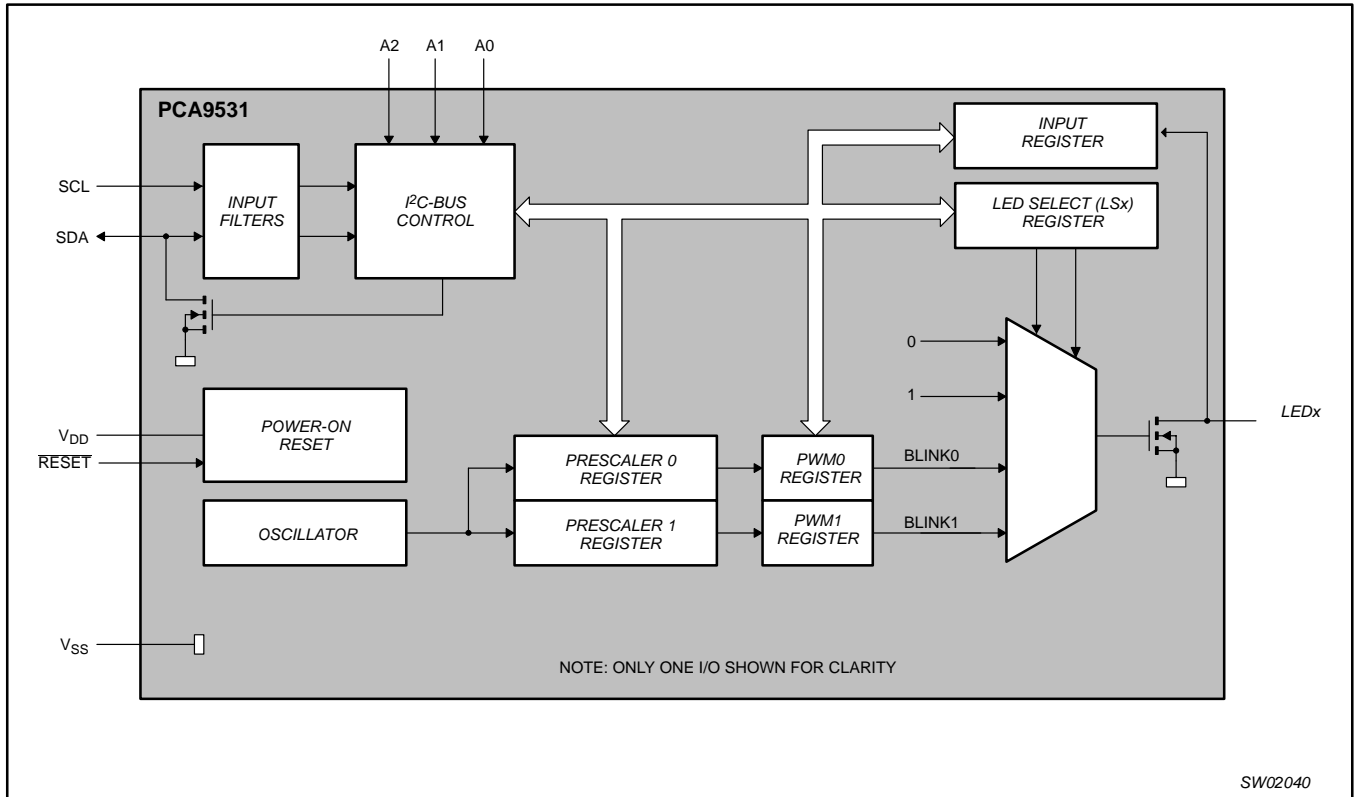


Figure 3. Block diagram

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DEVICE ADDRESSING

Following a START condition the bus master must output the address of the slave it is accessing. The address of the PCA9531 is shown in Figure 4. To conserve power, no internal pullup resistors are incorporated on the hardware selectable address pins and they must be pulled HIGH or LOW.

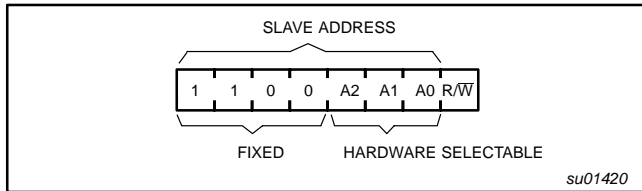


Figure 4. Slave address

The last bit of the address byte defines the operation to be performed. When set to logic 1 a read is selected while a logic 0 selects a write operation.

CONTROL REGISTER

Following the successful acknowledgement of the slave address, the bus master will send a byte to the PCA9531 which will be stored in the Control Register.

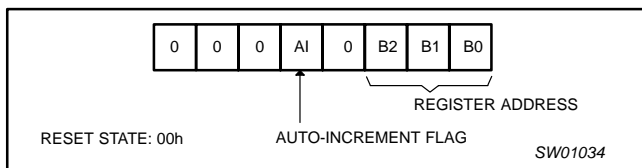


Figure 5. Control register

CONTROL REGISTER DEFINITION

| B2 | B1 | B0 | REGISTER NAME | TYPE | REGISTER FUNCTION |
|----|----|----|---------------|-------------|-----------------------|
| 0 | 0 | 0 | INPUT | READ | INPUT REGISTER |
| 0 | 0 | 1 | PSC0 | READ/ WRITE | FREQUENCY PRESCALER 0 |
| 0 | 1 | 0 | PWM0 | READ/ WRITE | PWM REGISTER 0 |
| 0 | 1 | 1 | PSC1 | READ/ WRITE | FREQUENCY PRESCALER 1 |
| 1 | 0 | 0 | PWM1 | READ/ WRITE | PWM REGISTER 1 |
| 1 | 0 | 1 | LS0 | READ/ WRITE | LED0-LED3 SELECTOR |
| 1 | 1 | 0 | LS1 | READ/ WRITE | LED4-LED7 SELECTOR |

REGISTER DESCRIPTION

The lowest 3 bits are used as a pointer to determine which register will be accessed.

If the auto-increment flag is set, the three low order bits of the Control Register are automatically incremented after a read or write. This allows the user to program the registers sequentially. The contents of these bits will rollover to '000' after the last register is accessed.

When auto-increment flag is set (AI = 1) and a read sequence is initiated, the sequence must start by reading a register different from the input register (B2 B1 B0 ≠ 0 0 0).

Only the 3 least significant bits are affected by the AI flag.

Unused bits must be programmed with zeroes.

INPUT — INPUT REGISTER

| bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---|---|---|---|---|---|---|---|
| Default | X | X | X | X | X | X | X | X |

The INPUT register reflects the state of the device pins. Writes to this register will be acknowledged but will have no effect.

PSC0 — FREQUENCY PRESCALER 0

| bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---|---|---|---|---|---|---|---|
| default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

PSC0 is used to program the period of the PWM output.

$$\text{The period of BLINK0} = \frac{(\text{PSC0} + 1)}{152}$$

PWM0 — PWM REGISTER 0

| bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---|---|---|---|---|---|---|---|
| default | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

The PWM0 register determines the duty cycle of BLINK0. The outputs are LOW (LED on) when the count is less than the value in PWM0 and HIGH (LED off) when it is greater. If PWM0 is programmed with 00h, then the PWM0 output is always HIGH (LED off).

$$\text{The duty cycle of BLINK0 is: } \frac{\text{PWM0}}{256}$$

PSC1 — FREQUENCY PRESCALER 1

| bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---|---|---|---|---|---|---|---|
| default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

PSC1 is used to program the period of PWM output.

$$\text{The period of BLINK1} = \frac{(\text{PSC1} + 1)}{152}$$

PWM1 — PWM REGISTER 1

| bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---|---|---|---|---|---|---|---|
| default | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

The PWM1 register determines the duty cycle of BLINK1. The outputs are LOW (LED on) when the count is less than the value in PWM1 and HIGH (LED off) when it is greater. If PWM1 is programmed with 00h, then the PWM1 output is always HIGH (LED off).

$$\text{The duty cycle of BLINK1 is: } \frac{\text{PWM1}}{256}$$

LS0 — LED0-3 SELECTOR

| | LED 3 | LED 2 | LED 1 | LED 0 | | | | |
|---------|-------|-------|-------|-------|---|---|---|---|
| bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

LS1 — LED4-7 SELECTOR

| | LED 7 | LED 6 | LED 5 | LED 4 | | | | |
|---------|-------|-------|-------|-------|---|---|---|---|
| bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

The LSx LED select registers determine the source of the LED data.

00 = Output is set Hi-Z (LED off - default)

01 = Output is set low (LED on)

10 = Output blinks at PWM0 rate

11 = Output blinks at PWM1 rate

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POWER-ON RESET

When power is applied to V_{DD}, an internal Power On Reset holds the PCA9531 in a reset state until V_{DD} has reached V_{POR}. At this point, the reset condition is released and the PCA9531 registers are initialized to their default states, all the outputs in the off state.

EXTERNAL RESET

A reset can be accomplished by holding the **RESET** pin low for a minimum of t_W. The PCA9531 registers and I²C state machine will be held in their default state until the **RESET** input is once again high.

This input requires a pull-up resistor to V_{DD}.

CHARACTERISTICS OF THE I²C-BUS

The I²C-bus is for 2-way, 2-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as control signals (see Figure 6).

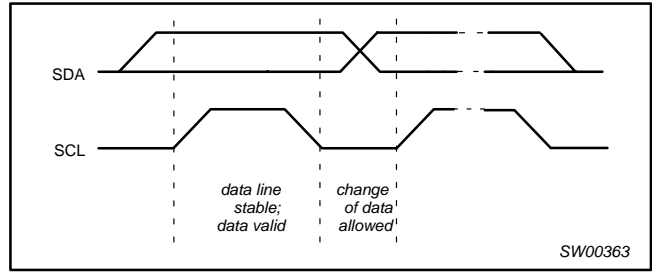


Figure 6. Bit transfer

Start and stop conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the start condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the stop condition (P) (see Figure 7).

System configuration

A device generating a message is a transmitter: a device receiving is the receiver. The device that controls the message is the master and the devices which are controlled by the master are the slaves (see Figure 8).

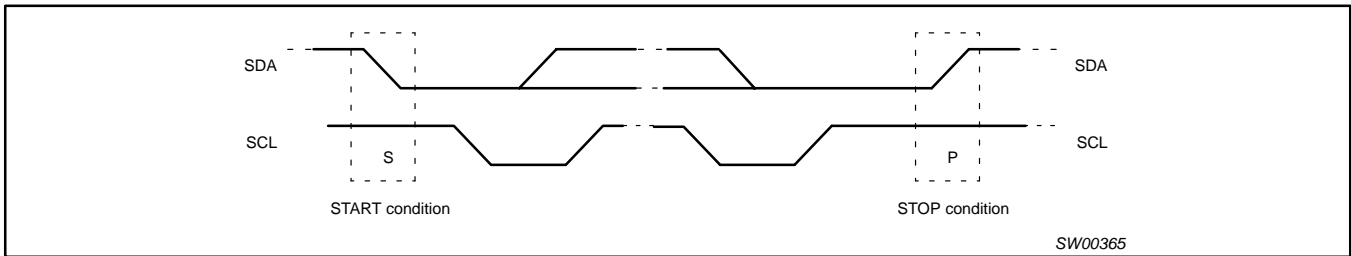


Figure 7. Definition of start and stop conditions

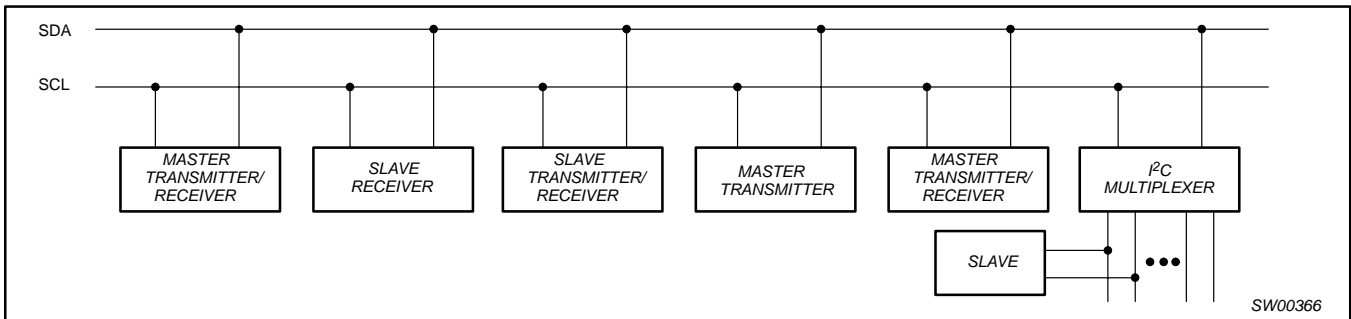


Figure 8. System configuration

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Acknowledge

The number of data bytes transferred between the start and the stop conditions from transmitter to receiver is not limited. Each byte of eight bits is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter whereas the master generates an extra acknowledge related clock pulse.

A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse, set-up and hold times must be taken into account.

A master receiver must signal an end of data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event, the transmitter must leave the data line HIGH to enable the master to generate a stop condition.

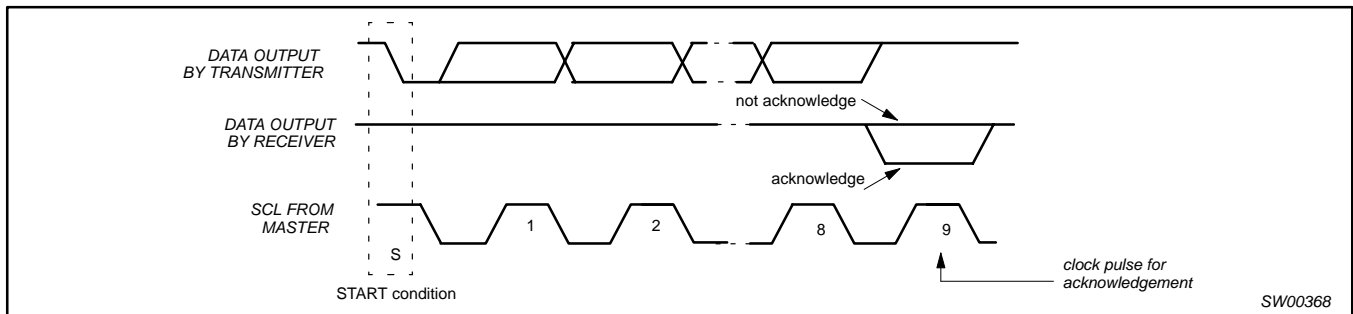


Figure 9. Acknowledgement on the I²C-bus

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Bus transactions

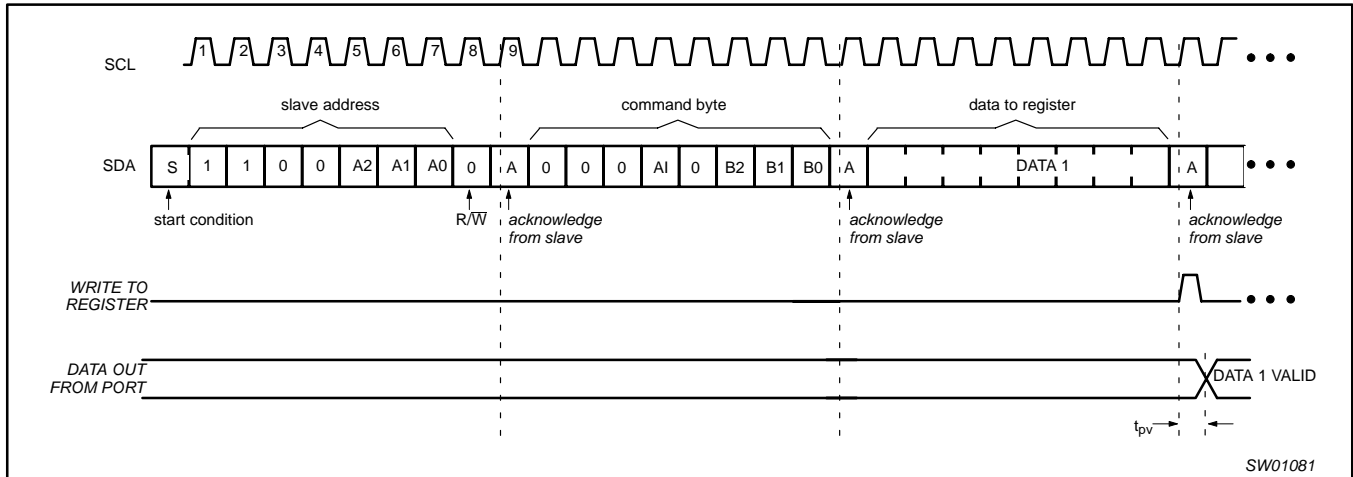


Figure 10. WRITE to register

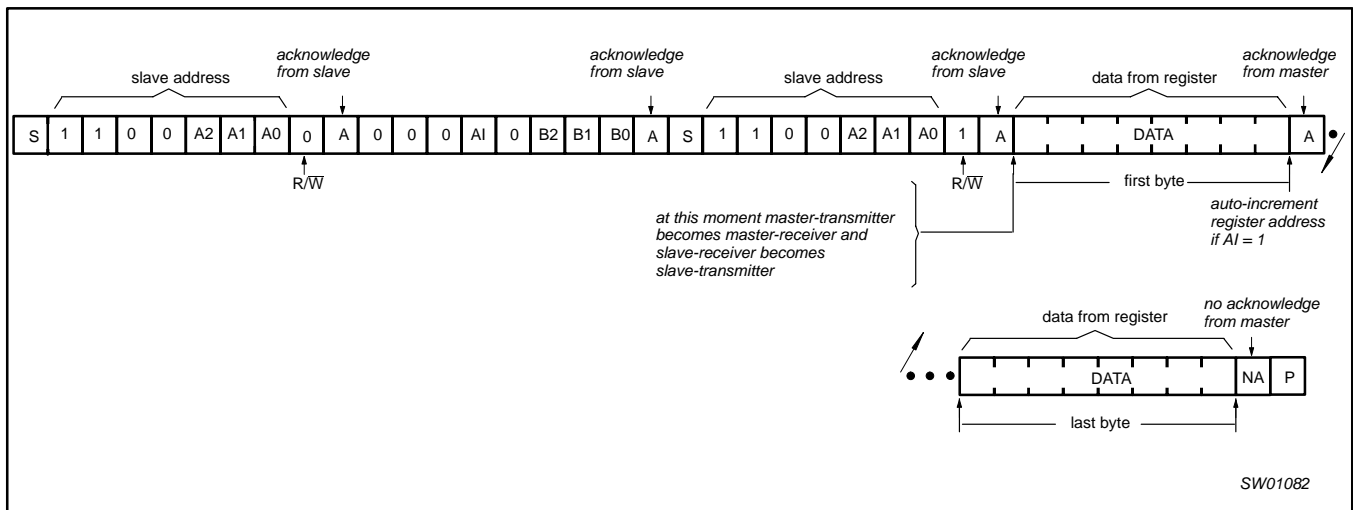
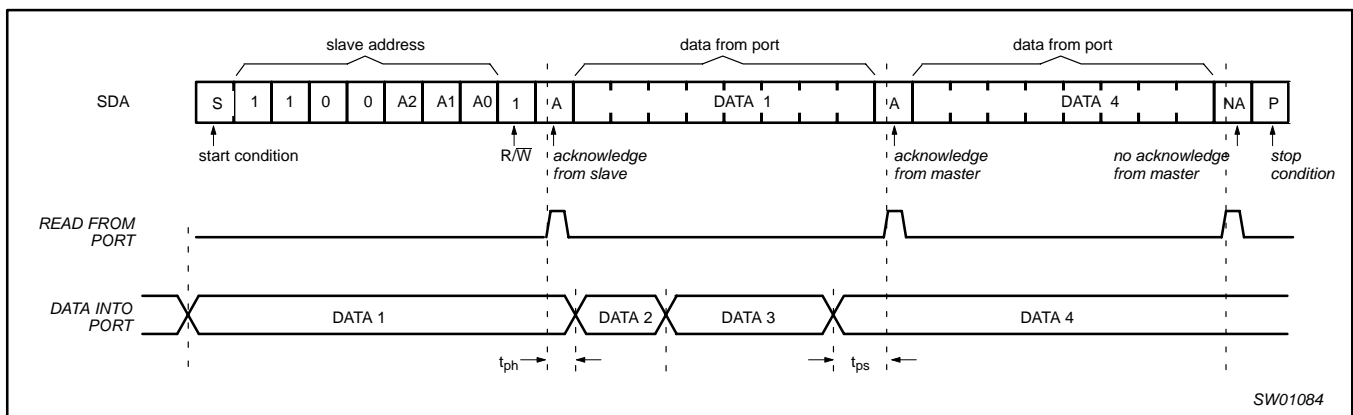


Figure 11. READ from register



NOTES:

1. This figure assumes the command byte has previously been programmed with 00h.

Figure 12. READ input port register

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APPLICATION DATA

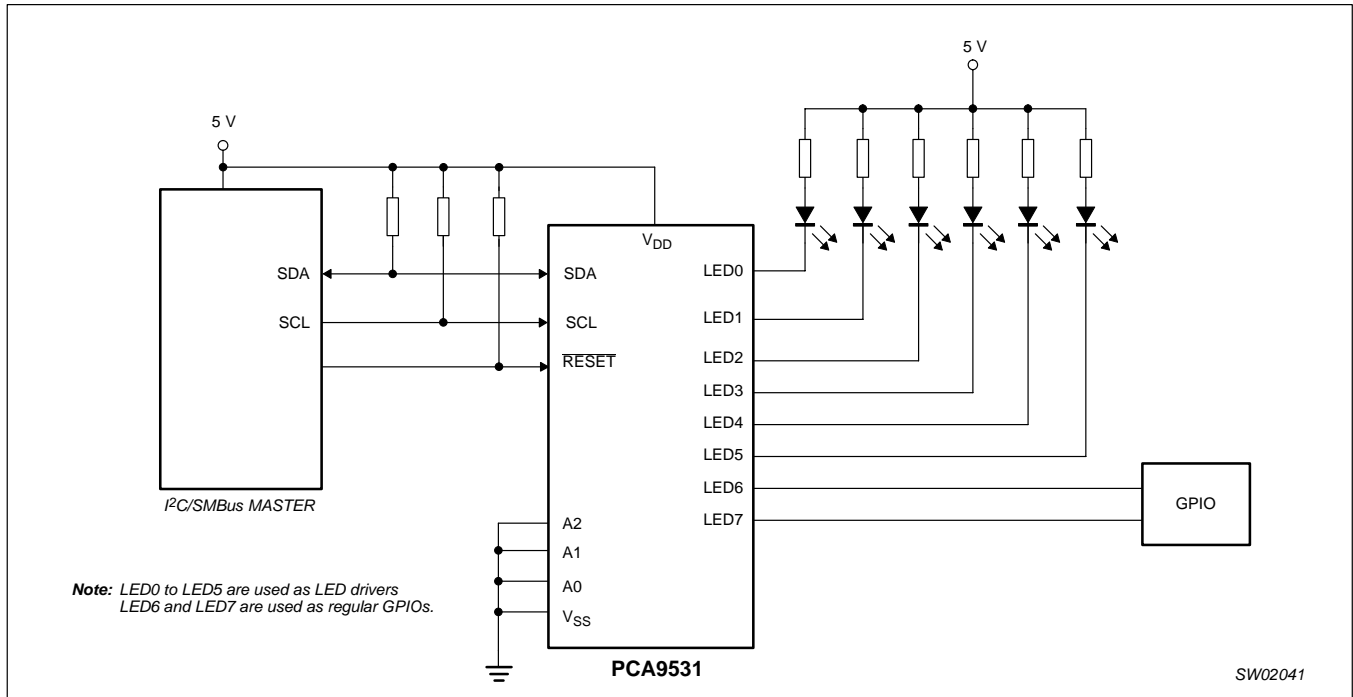


Figure 13. Typical application

Minimizing I_{DD} when the I/O is used to control LEDs

When the I/Os are used to control LEDs, they are normally connected to V_{DD} through a resistor as shown in Figure 13. Since the LED acts as a diode, when the LED is off the I/O V_{IN} is about 1.2 V less than V_{DD}. The supply current, I_{DD}, increases as V_{IN} becomes lower than V_{DD} and is specified as ΔI_{DD} in the DC characteristics table.

Designs needing to minimize current consumption, such as battery power applications, should consider maintaining the I/O pins greater than or equal to V_{DD} when the LED is off. Figure 14 shows a high value resistor in parallel with the LED. Figure 15 shows V_{DD} less than the LED supply voltage by at least 1.2 V. Both of these methods maintain the I/O V_{IN} at or above V_{DD} and prevents additional supply current consumption when the LED is off.

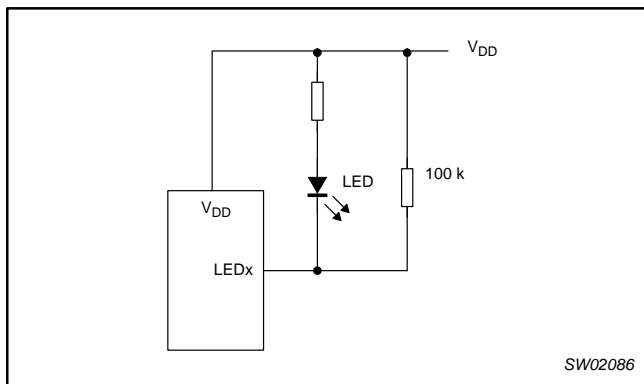


Figure 14. High value resistor in parallel with the LED

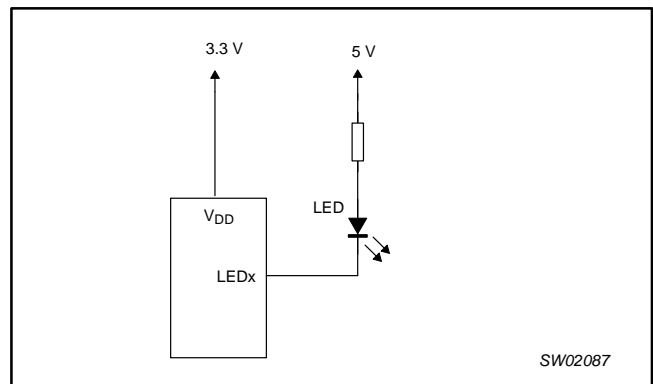


Figure 15. Device supplied by a lower voltage

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Programming example

The following example will show how to set LED0 to LED3 on. It will then set LED4 and LED5 to blink at 1 Hz at a 50% duty cycle. LED6 and LED7 will be set to be dimmed at 25% of their maximum brightness (duty cycle = 25%).

Table 1.

| | I ² C-bus |
|---|----------------------|
| Start | S |
| PCA9531 address with A0-A2 = low | C0h |
| PSC0 subaddress + auto-increment | 11h |
| Set prescaler PSC0 to achieve a period of 1 second: $\text{Blink period} = 1 = \frac{\text{PSC0} + 1}{152}$ PSC0 = 151 | 97h |
| Set PWM0 duty cycle to 50%: $\frac{\text{PWM0}}{256} = 0.5$ PWM0 = 128 | 80h |
| Set prescaler PCS1 to dim at max frequency: Blink period = max PSC1 = 0 | 00h |
| Set PWM1 output duty cycle to 25%: $\frac{\text{PWM1}}{256} = 0.25$ PWM1 = 64 | 40h |
| Set LED0 to LED3 on | 55h |
| Set LED4 and 5 to PWM0, and LED6 or 7 to PWM1 | FAh |
| Stop | P |

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ABSOLUTE MAXIMUM RATINGS

In accordance with the Absolute Maximum Rating System (IEC 134)

| SYMBOL | PARAMETER | CONDITIONS | MIN | MAX | UNIT |
|------------------|-------------------------------|------------|-----------------------|------|------|
| V _{DD} | Supply voltage | | -0.5 | 6.0 | V |
| V _{I/O} | DC voltage on an I/O | | V _{SS} - 0.5 | 5.5 | V |
| I _{I/O} | DC output current on an I/O | | — | +25 | mA |
| I _{SS} | Supply current | | — | 200 | mA |
| P _{tot} | Total power dissipation | | — | 400 | mW |
| T _{stg} | Storage temperature range | | -65 | +150 | °C |
| T _{amb} | Operating ambient temperature | | -40 | +85 | °C |

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take precautions appropriate to handling MOS devices. Advice can be found in Data Handbook IC24 under "Handling MOS devices".

DC CHARACTERISTICSV_{DD} = 2.3 to 5.5 V; V_{SS} = 0 V; T_{amb} = -40 to +85 °C; unless otherwise specified. TYP at 3.3 V and 25 °C.

| SYMBOL | PARAMETER | CONDITIONS | MIN | TYP | MAX | UNIT |
|---|--------------------------------------|--|---------------------|-----|-----------------------|------|
| Supplies | | | | | | |
| V _{DD} | Supply voltage | | 2.3 | — | 5.5 | V |
| I _{DD} | Supply current | Operating mode; V _{DD} = 5.5 V; V _I = V _{DD} or V _{SS} ; f _{SCL} = 100 kHz | — | 350 | 500 | μA |
| I _{stb} | Standby current | Standby mode; V _{DD} = 5.5 V; V _I = V _{DD} or V _{SS} ; f _{SCL} = 0 kHz | — | 1.9 | 3.0 | μA |
| ΔI _{DD} | Additional standby current | Standby mode; V _{DD} = 5.5 V; Every LED I/O at V _{IN} = 4.3 V; f _{SCL} = 0 kHz | — | — | 800 | μA |
| V _{POR} | Power-on reset voltage | No load; V _I = V _{DD} or V _{SS} | — | 1.7 | 2.2 | V |
| Input SCL; input/output SDA | | | | | | |
| V _{IL} | LOW level input voltage | | -0.5 | — | 0.3 V _{DD} | V |
| V _{IH} | HIGH level input voltage | | 0.7 V _{DD} | — | 5.5 | V |
| I _{OL} | LOW level output current | V _{OL} = 0.4V | 3 | 6.5 | — | mA |
| I _L | Leakage current | V _I = V _{DD} = V _{SS} | -1 | — | +1 | μA |
| C _I | Input capacitance | V _I = V _{SS} | — | 3.7 | 5 | pF |
| I/Os | | | | | | |
| V _{IL} | LOW level input voltage | | -0.5 | — | 0.8 | V |
| V _{IH} | HIGH level input voltage | | 2.0 | — | 5.5 | V |
| I _{OL} | LOW level output current | V _{OL} = 0.4 V; V _{DD} = 2.3 V; Note 1 | 9 | — | — | mA |
| | | V _{OL} = 0.4 V; V _{DD} = 3.0 V; Note 1 | 12 | — | — | mA |
| | | V _{OL} = 0.4 V; V _{DD} = 5.0 V; Note 1 | 15 | — | — | mA |
| | | V _{OL} = 0.7 V; V _{DD} = 2.3 V; Note 1 | 15 | — | — | mA |
| | | V _{OL} = 0.7 V; V _{DD} = 3.0 V; Note 1 | 20 | — | — | mA |
| | | V _{OL} = 0.7 V; V _{DD} = 5.0 V; Note 1 | 25 | — | — | mA |
| I _L | Input leakage current | V _{DD} = 3.6 V; V _I = 0 or V _{DD} | -1 | — | 1 | μA |
| C _{IO} | Input/output capacitance | | — | 2.5 | 5 | pF |
| Select Inputs A0, A1, A2 / RESET | | | | | | |
| V _{IL} | LOW level input voltage | | -0.5 | — | 0.8 | V |
| V _{IH} | HIGH level input voltage; A0 / RESET | | 2.0 | — | 5.5 | V |
| V _{IH} | HIGH level input voltage; A1 / A2 | | 2.0 | — | V _{DD} + 0.5 | V |
| I _{LI} | Input leakage current | | -1 | — | 1 | μA |
| C _I | Input capacitance | V _I = V _{SS} | — | 2.3 | 5 | pF |

NOTE:

1. Each I/O must be externally limited to a maximum of 25 mA and the device must be limited to a maximum current of 100 mA.

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AC SPECIFICATIONS

| SYMBOL | PARAMETER | STANDARD MODE I ² C BUS | | FAST MODE I ² C BUS | | UNITS |
|-----------------------------------|--|------------------------------------|------|--------------------------------------|-----|-------|
| | | MIN | MAX | MIN | MAX | |
| f _{SCL} | Operating frequency | 0 | 100 | 0 | 400 | kHz |
| t _{BUF} | Bus free time between STOP and START conditions | 4.7 | — | 1.3 | — | μs |
| t _{HD;STA} | Hold time after (repeated) START condition | 4.0 | — | 0.6 | — | μs |
| t _{SU;STA} | Repeated START condition setup time | 4.7 | — | 0.6 | — | μs |
| t _{SU;STO} | Setup time for STOP condition | 4.0 | — | 0.6 | — | μs |
| t _{HD;DAT} | Data in hold time | 0 | — | 0 | — | ns |
| t _{VD;ACK} | Valid time for ACK condition ² | — | 600 | — | 600 | ns |
| t _{VD;DAT (L)} | Data out valid time ³ | — | 600 | — | 600 | ns |
| t _{VD;DAT (H)} | Data out valid time ³ | — | 1500 | — | 600 | ns |
| t _{SU;DAT} | Data setup time | 250 | — | 100 | — | ns |
| t _{LOW} | Clock LOW period | 4.7 | — | 1.3 | — | μs |
| t _{HIGH} | Clock HIGH period | 4.0 | — | 0.6 | — | μs |
| t _F | Clock/Data fall time | — | 300 | 20 + 0.1 C _b ¹ | 300 | ns |
| t _R | Clock/Data rise time | — | 1000 | 20 + 0.1 C _b ¹ | 300 | ns |
| t _{SP} | Pulse width of spikes that must be suppressed by the input filters | — | 50 | — | 50 | ns |
| Port Timing | | | | | | |
| t _{PV} | Output data valid | — | 200 | — | 200 | ns |
| t _{PS} | Input data setup time | 100 | — | 100 | — | ns |
| t _{PH} | Input data hold time | 1 | — | 1 | — | μs |
| Reset | | | | | | |
| t _W | Reset pulse width | 6 | — | 6 | — | ns |
| t _{REC} | Reset recovery time | 0 | — | 0 | — | ns |
| t _{RESET} ^{4,5} | Time to reset | 400 | — | 400 | — | ns |

NOTES:

1. C_b = total capacitance of one bus line in pF.
2. t_{VD;ACK} = time for Acknowledgement signal from SCL low to SDA (out) low.
3. t_{VD;DAT} = minimum time for SDA data out to be valid following SCL low.
4. Resetting the device while actively communicating on the bus may cause glitches or errant STOP conditions.
5. Upon reset, the full delay will be the sum of t_{RESET} and the RC time constant of the SDA bus.

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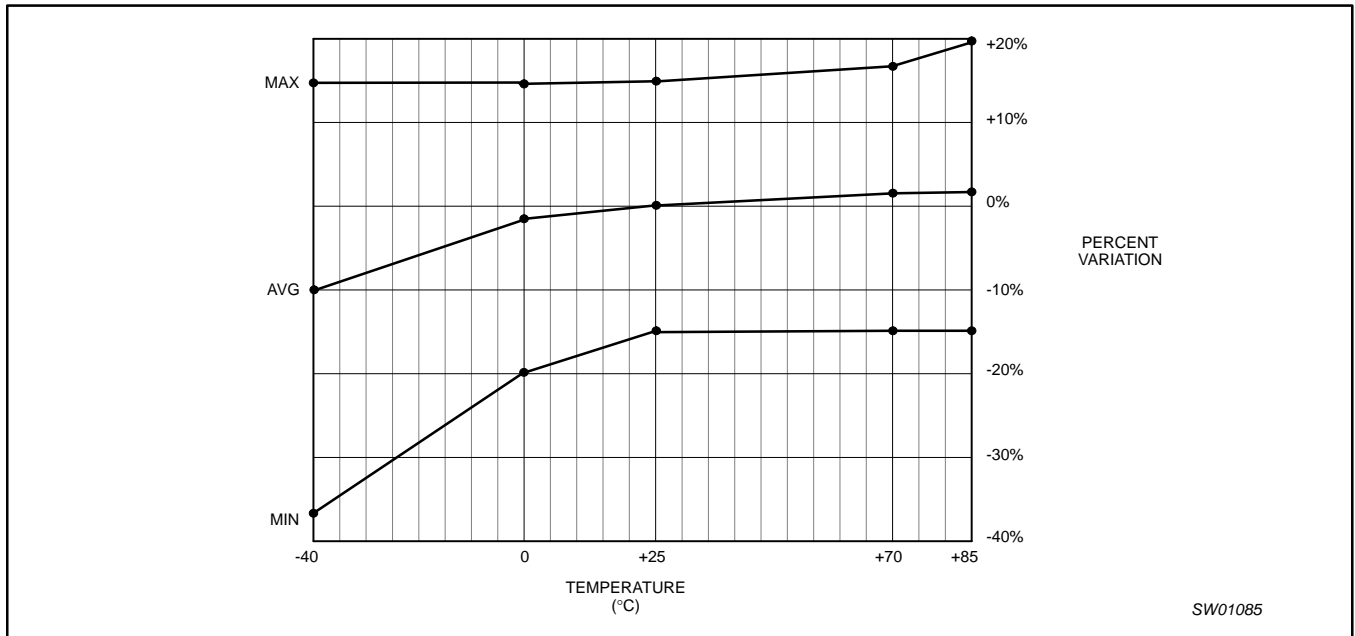


Figure 16. Typical frequency variation over process at V_{DD} = 2.3 V to 3.0 V

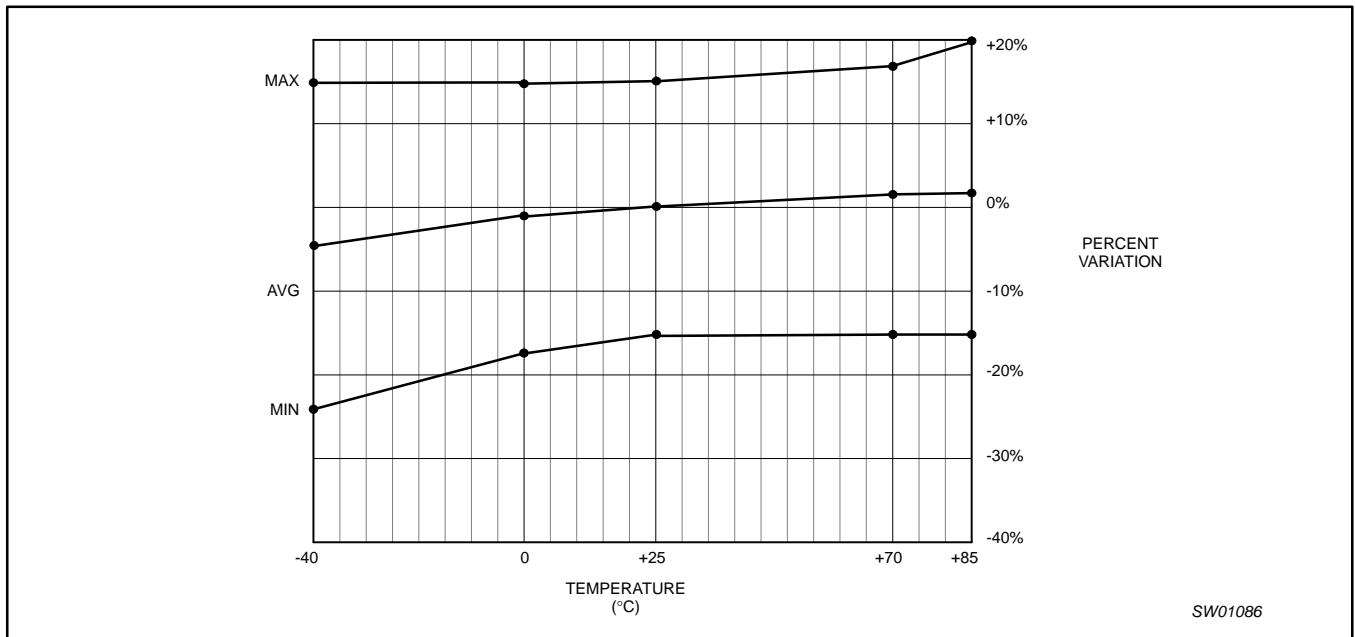


Figure 17. Typical frequency variation over process at V_{DD} = 3.0 V to 5.5 V

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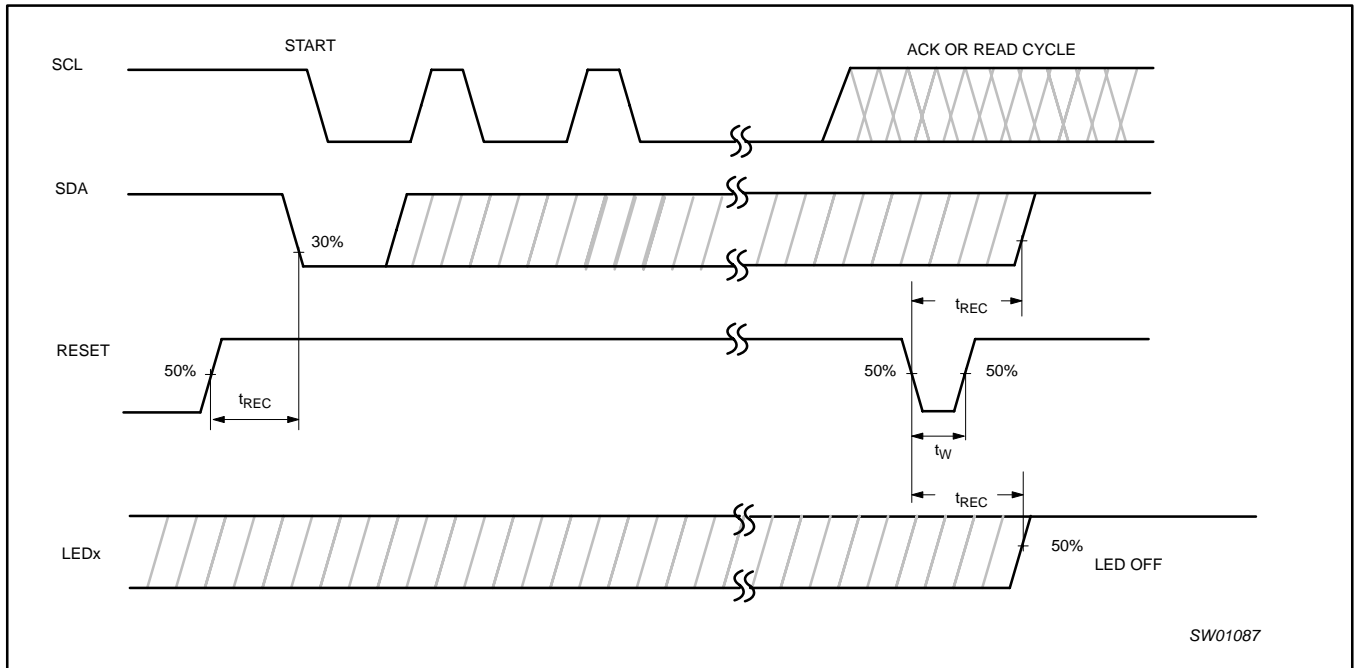


Figure 18. Definition of RESET timing

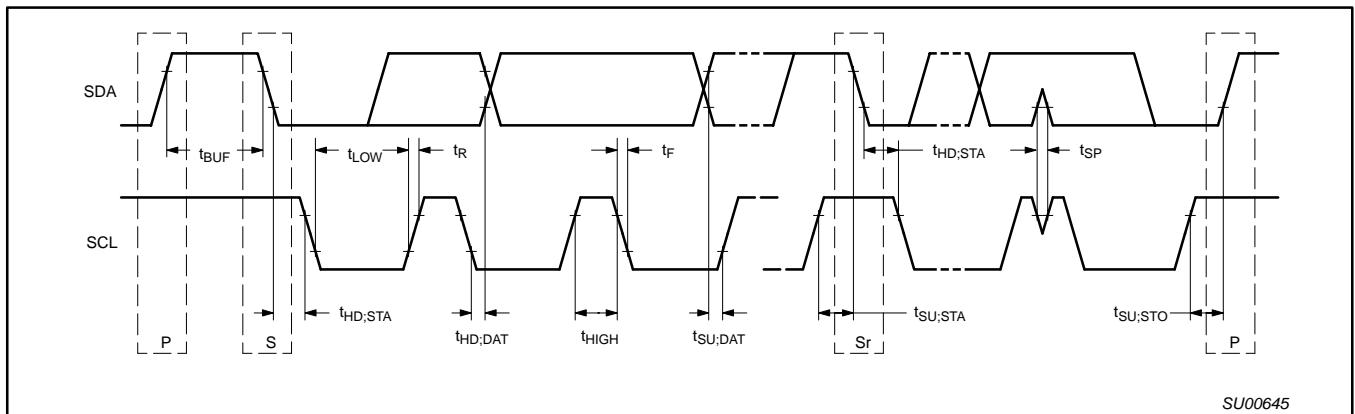


Figure 19. Definition of timing

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PCA9531

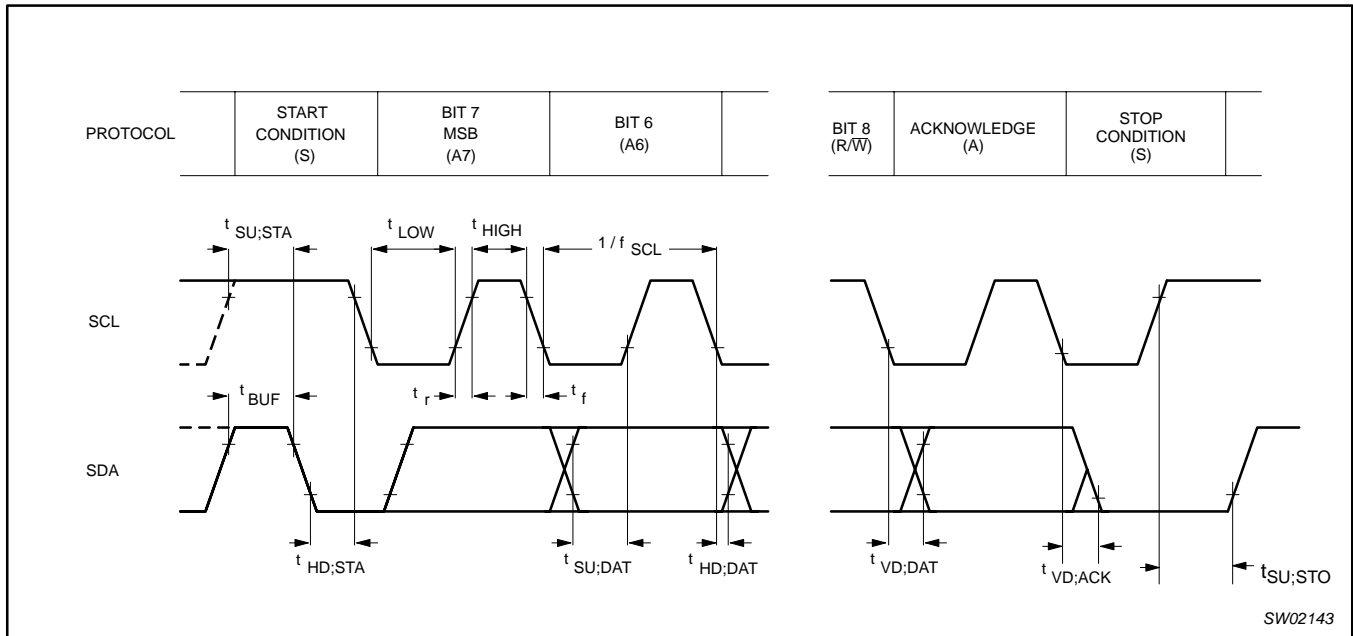


Figure 20. I²C-bus timing diagram; rise and fall times refer to V_{IL} and V_{IH}

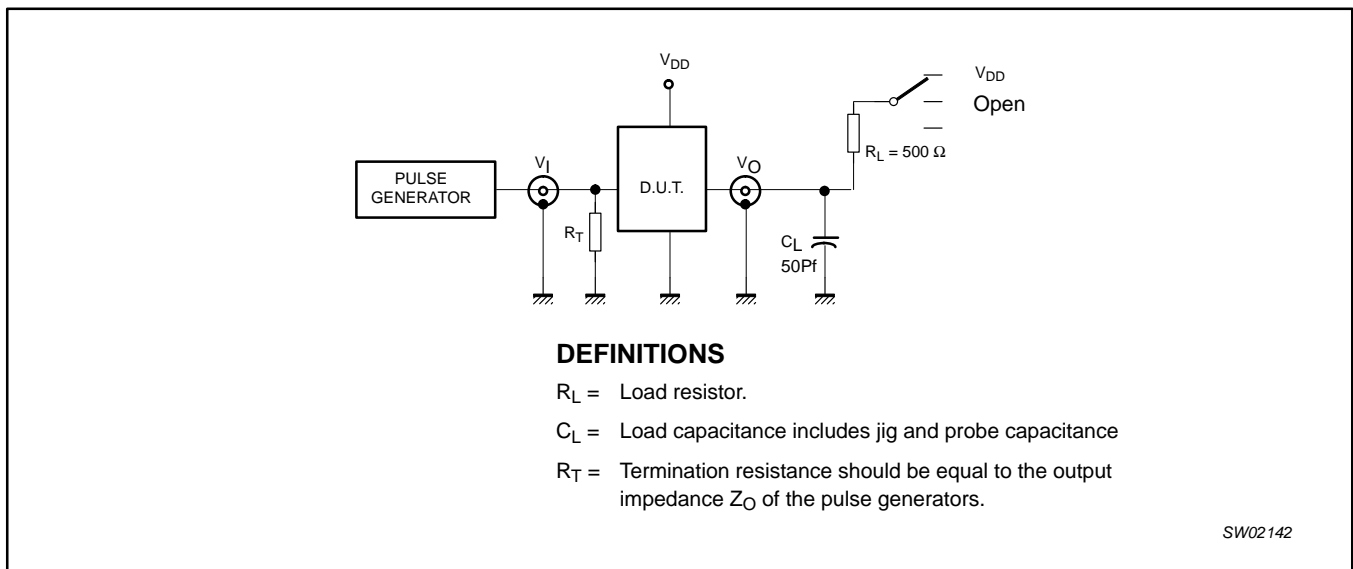


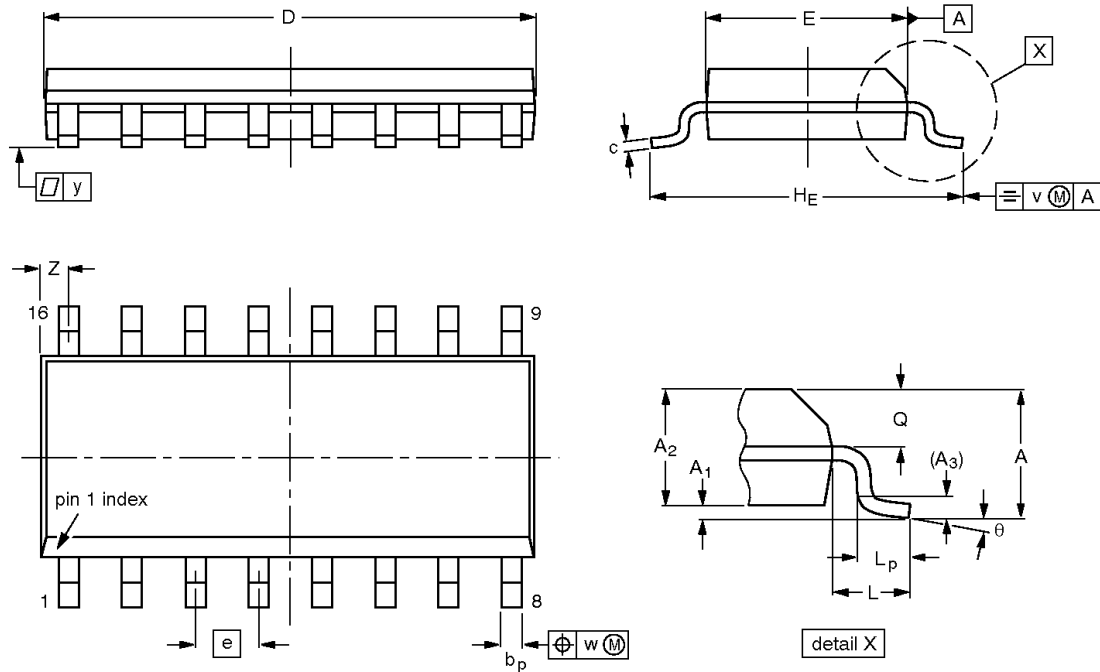
Figure 21. Test circuitry for switching times

8-bit I²C LED dimmer

PCA9531

SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

| UNIT | A max. | A ₁ | A ₂ | A ₃ | b _p | c | D ⁽¹⁾ | E ⁽¹⁾ | e | H _E | L | L _p | Q | v | w | y | Z ⁽¹⁾ | θ |
|--------|--------|----------------|----------------|----------------|----------------|------------------|------------------|------------------|------|----------------|-------|----------------|----------------|------|------|-------|------------------|----------|
| mm | 1.75 | 0.25 0.10 | 1.45 1.25 | 0.25 | 0.49 0.36 | 0.25 0.19 | 10.0 9.8 | 4.0 3.8 | 1.27 | 6.2 5.8 | 1.05 | 1.0 0.4 | 0.7 0.6 | 0.25 | 0.25 | 0.1 | 0.7 0.3 | 8° 0° |
| inches | 0.069 | 0.010 0.004 | 0.057 0.049 | 0.01 | 0.019 0.014 | 0.0100 0.0075 | 0.39 0.38 | 0.16 0.15 | 0.05 | 0.244 0.228 | 0.041 | 0.039 0.016 | 0.028 0.020 | 0.01 | 0.01 | 0.004 | 0.028 0.012 | |

Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

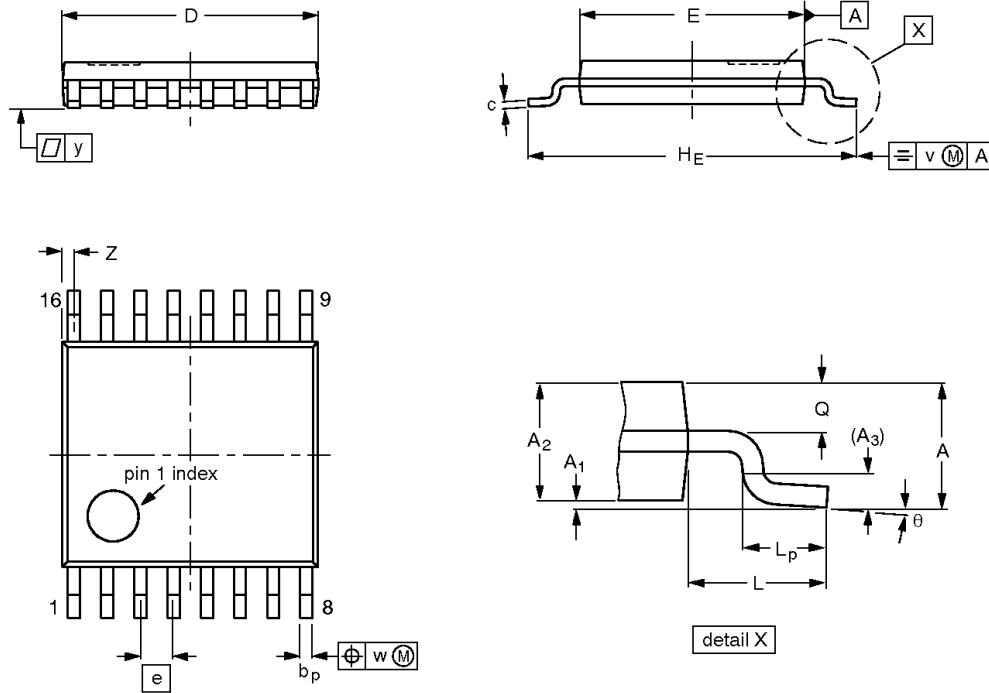
| OUTLINE VERSION | REFERENCES | | | EUROPEAN PROJECTION | ISSUE DATE |
|-----------------|------------|--------|-------|---------------------|----------------------|
| | IEC | JEDEC | JEITA | | |
| SOT109-1 | 076E07 | MS-012 | | | 99-12-27 03-02-19 |

8-bit I²C LED dimmer

PCA9531

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm

SOT403-1



DIMENSIONS (mm are the original dimensions)

| UNIT | A max. | A ₁ | A ₂ | A ₃ | b _p | c | D ⁽¹⁾ | E ⁽²⁾ | e | H _E | L | L _p | Q | v | w | y | Z ⁽¹⁾ | θ |
|------|--------|----------------|----------------|----------------|----------------|------------|------------------|------------------|------|----------------|---|----------------|------------|-----|------|-----|------------------|----------|
| mm | 1.1 | 0.15 0.05 | 0.95 0.80 | 0.25 | 0.30 0.19 | 0.2 0.1 | 5.1 4.9 | 4.5 4.3 | 0.65 | 6.6 6.2 | 1 | 0.75 0.50 | 0.4 0.3 | 0.2 | 0.13 | 0.1 | 0.40 0.06 | 8° 0° |

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

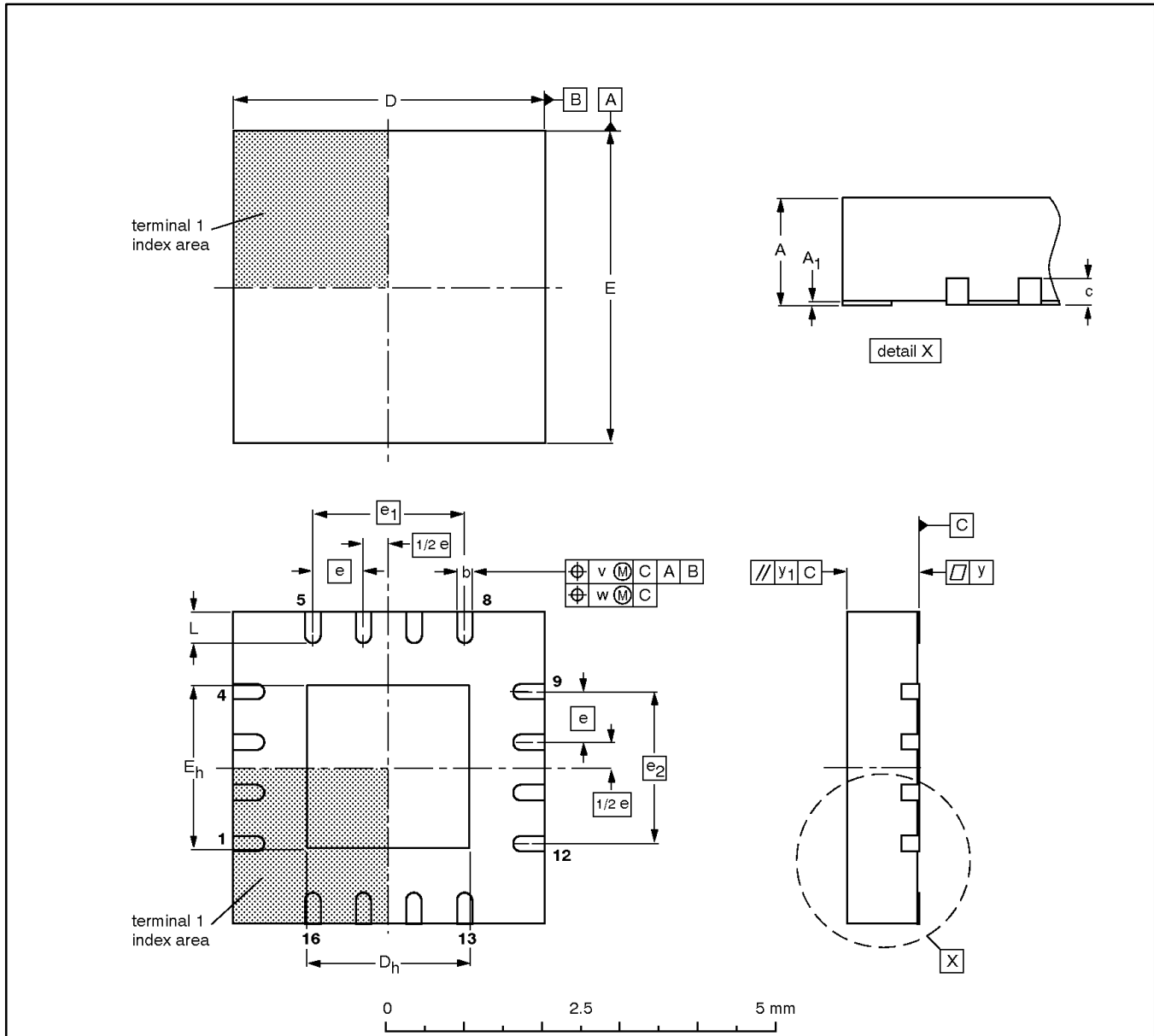
| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|-----------------|------------|--------|-------|--|---------------------|----------------------|
| | IEC | JEDEC | JEITA | | | |
| SOT403-1 | | MO-153 | | | | 99-12-27 03-02-18 |

8-bit I²C LED dimmer

PCA9531

HVQFN16: plastic thermal enhanced very thin quad flat package; no leads; 16 terminals; body 4 x 4 x 0.85 mm

SOT629-1



DIMENSIONS (mm are the original dimensions)

| UNIT | A ⁽¹⁾ max. | A ₁ | b | c | D ⁽¹⁾ | D _h | E ⁽¹⁾ | E _h | e | e ₁ | e ₂ | L | v | w | y | y ₁ |
|------|--------------------------|----------------|--------------|-----|------------------|----------------|------------------|----------------|------|----------------|----------------|--------------|-----|------|------|----------------|
| mm | 1 | 0.05 0.00 | 0.38 0.23 | 0.2 | 4.1 3.9 | 2.25 1.95 | 4.1 3.9 | 2.25 1.95 | 0.65 | 1.95 | 1.95 | 0.75 0.50 | 0.1 | 0.05 | 0.05 | 0.1 |

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|--------------------|------------|--------|-------|--|------------------------|-----------------------|
| | IEC | JEDEC | JEITA | | | |
| SOT629-1 | --- | MO-220 | --- | | | -01-08-08 02-10-22 |

8-bit I²C LED dimmer

PCA9531

REVISION HISTORY

| Rev | Date | Description |
|-----|----------|---|
| _1 | 20031110 | Product data (9397 750 12292); ECN 853-2407 30411 dated 06 September 2003. Initial version |

8-bit I²C LED dimmer

PCA9531



Purchase of Philips I²C components conveys a license under the Philips' I²C patent to use the components in the I²C system provided the system conforms to the I²C specifications defined by Philips. This specification can be ordered using the code 9398 393 40011.

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|-------|----------------------------------|-----------------------------------|--|
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For additional information please visit
<http://www.semiconductors.philips.com>. Fax: +31 40 27 24825

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For sales offices addresses send e-mail to:
sales.addresses@www.semiconductors.philips.com.

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