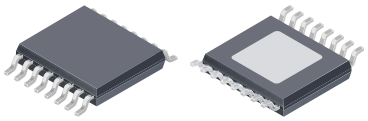
Wide Input Voltage Range, High Efficiency Fault Tolerant LED Driver

Features and Benefits

- AEC-Q100 Qualified
- Wide input voltage range of 4.5 to 40 V for start/stop, cold crank and load dump requirements
- Boost converter switching frequency up to 2 MHz, allowing operation above the AM band
- Excellent input voltage transient response
- Internal secondary OVP for redundant protection
- Fully integrated LED current sink and boost converter with 60 V DMOS FET
- Maximum LED current of 150 mA
- Drives up to 14 series LEDs
- Single EN/PWM pin interface for PWM Dimming and Enable function
- 5000:1 PWM dimming at 200 Hz

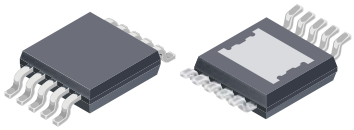
Continued on the next page…

Packages:



Not to scale

16-pin TSSOP with exposed thermal pad (LP package)



10-pin MSOP with exposed thermal pad (LY package)

Description

The A8513 is a single-output white LED (WLED) driver for LCD backlighting. It integrates a current-mode boost converter with an internal power switch and one current sink. The A8513 can operate from a single power supply from 4.5 to 40 V, to accommodate start/stop, cold crank, and load dump requirements. A 2 MHz boost converter switching frequency allows the A8513 to operate above the AM radio band.

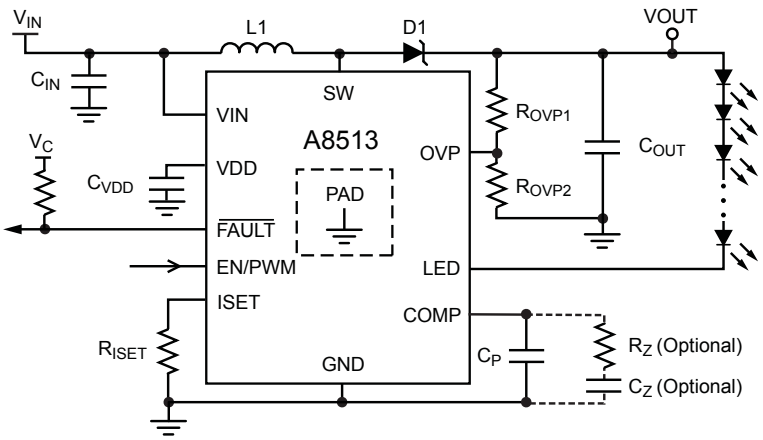
If required, the fault flag can be used as part of a circuit to drive an external P-FET to disconnect the input supply from the system in the event of a fault. The A8513 provides protection against output short and overvoltage, open or shorted diode, open or shorted LED pin, shorted boost switch or inductor, shorted I_{SET} resistor, and IC overtemperature. A dual level cycle-by-cycle current limit function provides soft start and protects the internal current switch against high current overloads.

The A8513 is provided in a 10-pin MSOP package (suffix LY) and a 16-pin TSSOP package (suffix LP). Both packages have an exposed thermal pad for enhanced thermal dissipation, and are lead (Pb) free, with 100% matte tin leadframe plating.

Applications:

- LCD backlighting for:
  - Automotive infotainment
  - Automotive cluster
  - Automotive center stack
  - Industrial LCD displays
  - Portable DVD players
- Flatbed Scanners
- LED Lighting

Typical Application Circuit



Boost f_{SW} (MHz)	V_{IN} (min) (V)	LEDs per String (max)
0.25/0.5/1	5	14
2	10	14
2	8	12
2	6	9
2	5	7

Features and Benefits (continued)

- Fault flag pin to alert the controller to a myriad of possible fault conditions
- Protection Features:
  - Shorted output
  - Open or shorted LED pin
  - Output undervoltage and overvoltage
  - Input undervoltage
  - Shorted boost switch or inductor
  - Shorted I_{SET} resistor
  - Open boost Schottky
  - Overtemperature

Selection Guide

Part Number	Oscillator Frequency, f_{SW} (MHz)	Packing*	Package
A8513KLYTR-T	2	4000 pieces per 13-in. reel	10-pin MSOP with exposed thermal pad
A8513KLYTR-1-T	1	Contact factory for availability	
A8513KLYTR-2-T	0.5		
A8513KLYTR-3-T	0.25		
A8513KLPTR-T	2	4000 pieces per 13-in. reel	16-pin TSSOP with exposed thermal pad
A8513KLPTR-1-T	1	Contact factory for availability	
A8513KLPTR-2-T	0.5		
A8513KLPTR-3-T	0.25		

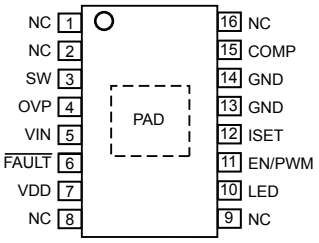
*Contact Allegro® for additional packing options

Absolute Maximum Ratings*

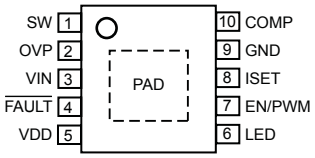
Characteristic	Symbol	Notes	Rating	Unit
LED Pin	V_{LED}		–0.3 to 55	V
OVP Pin	V_{OVP}		–0.3 to 60	V
VIN and $\overline{\text{FAULT}}$ Pins	V_{IN}, V_{FAULT}		-0.3 to 40	V
SW Pin	V_{SW}	Continuous	–0.6 to 60	V
		t < 50 ns	–1.0	V
ISET Pin	V_{ISET}		–0.3 to 5.5	V
All Other Pins			–0.3 to 7	V
Operating Ambient Temperature	T_A	Range K	–40 to 125	ºC
Maximum Junction Temperature	T_J(max)		150	ºC
Storage Temperature	T_{stg}		–55 to 150	ºC

*Stresses beyond those listed in this table may cause permanent damage to the device. The Absolute Maximum ratings are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the Electrical Characteristics table is not implied. Exposure to Absolute Maximum-rated conditions for extended periods may affect device reliability.

Pin-out Diagram



LP Package



LY Package

Terminal List Table

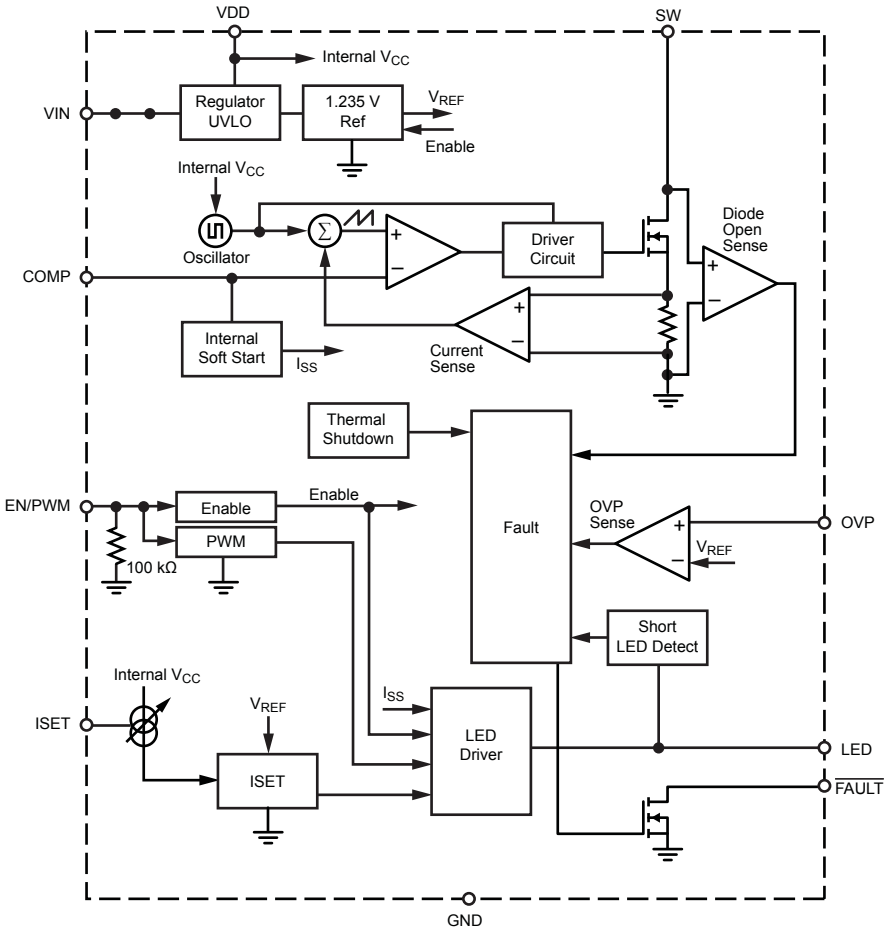
Name	Number		Function
	LP	LY	
COMP	15	10	Output of the error amplifier and compensation node. Connect compensation network from this pin to GND for control loop compensation.
$\overline{\text{FAULT}}$	6	4	This pin is used to indicate fault conditions. Logic low indicates that the A8513 has a fault present.
GND	13,14	9	Ground.
ISET	12	8	Connect the R_{ISET} resistor between this pin and GND to set the 100% LED current level.
LED	10	6	Connect the cathode of the LED string to this pin.
NC	1,2,8,9,16	–	No connection.
OVP	4	2	This pin is used to sense an overvoltage condition. Connect a resistive divider from the VOUT node to this pin to adjust the Overvoltage Protection (OVP).
PAD	–	–	Exposed pad of the package providing enhanced thermal dissipation. This pad must be connected to the ground plane(s) of the PCB with at least 8 thermal vias, directly in the pad.
EN/PWM	11	7	PWM dimming pin. Used to control LED intensity by using pulse width modulation.
SW	3	1	The drain of the internal NMOS switch of the boost converter.
VDD	7	5	Output of internal LDO. Connect a 0.1 µF decoupling capacitor between this pin and GND.
VIN	5	3	Input power to the A8513.

Thermal Characteristics* may require derating at maximum conditions, see application information

Characteristic	Symbol	Test Conditions*		Value	Unit
Package Thermal Resistance (Junction to Ambient)	$R_{\theta JA}$	LP package	On 4-layer PCB based on JEDEC standard	34	°C/W
			On 2-layer PCB with 3.8 in.^{2} of copper area each side	43	°C/W
		LY package	On 4-layer PCB based on JEDEC standard	48	°C/W
			On 2-layer PCB with 2.5 in.^{2} of copper area each side	48	°C/W
Package Thermal Resistance (Junction to Pad)	$R_{\theta JP}$			2	°C/W

*To be verified by characterization. Additional thermal information available on the Allegro® website.

Functional Block Diagram



ELECTRICAL CHARACTERISTICS[1] Valid at V_{IN} = 16 V, T_A = 25ºC, • indicates specifications guaranteed through the full operating temperature range with $T_A = T_J$ = –40ºC to125 ºC, typical specifications are at T_A = 25ºC; unless otherwise specified

Characteristics	Symbol	Test Conditions		Min.	Typ.	Max.	Unit
Input Voltage Specifications							
Operating Input Voltage Range	V_{IN}		•	4.5	–	40	V
VIN Pin UVLO Start Threshold	$V_{UVLOrise}$	V_{IN} rising	•	–	–	4.35	V
VIN Pin UVLO Stop Threshold	$V_{UVLOfall}$	V_{IN} falling	•	–	–	3.90	V
VIN Pin UVLO Hysteresis	$V_{UVLOhys}$			–	450	–	mV
Input Current							
Input Quiescent Current	I_Q	EN/PWM = V_{IH}, SW = 2 MHz, no load		–	5	–	mA
Input Sleep Supply Current	I_{QSLEEP}	VIN = 16 V, EN/PWM = 0 V	•	–	1	10	µA
Input Logic Levels (EN/PWM and $\overline{\text{FAULT}}$ [3])							
Input logic Level (Low)	V_{IL}	5 V < V_{IN} < 40 V	•	–	–	400	mV
Input logic Level (High)	V_{IH}	5 V < V_{IN} < 40 V	•	1.5	–	–	V
EN/PWM Pull-Down Resistor	$R_{EN/PWM}$	EN/PWM = 5 V		–	100	–	kΩ
$\overline{\text{FAULT}}$ Pin Pull-Down Voltage	V_{FAULT}	I_{FAULT} = 0.5 mA	•	–	–	0.4	V
$\overline{\text{FAULT}}$ Pin Leakage Current	$I_{FAULTlkg}$	V_{FAULT} = 5 V		–	–	1	µA
Error Amplifier							
Open Loop Voltage Gain	A_{VOL}			–	45	–	dB
Transconductance	g_m	ΔI_{COMP} = ±10 µA		–	990	–	µA/V
Source Current	$I_{EA(SRC)}$	V_{COMP} = 1.5 V		–	–360	–	µA
Sink Current	$I_{EA(SINK)}$	V_{COMP} = 1.5 V		–	360	–	µA
COMP Pin Pull-Down Resistance	R_{COMP}	$\overline{\text{FAULT}}$ asserted		–	2000	–	Ω
Output Overvoltage Protection							
Overvoltage Protection Threshold	$V_{OVPHI(th)}$	Measured at OVP Pin	•	1.168	1.218	1.268	V
OVP Pin Leakage Current	I_{OVPH}	Standard CMOS input, measured at V_{OVP} = 1.2 V	•	–	–	100	nA
OVP Pin Undervoltage Threshold	$V_{UVP(th)}$	Measured at OVP Pin	•	–	–	110	mV
Secondary Overvoltage Protection	$V_{OVP(sec)}$	Measured at SW Pin	•	53	55.5	58	V
BOOST Switch							
Switch On-Resistance	$R_{DS(on)SW}$	I_{SW} = 750 mA, V_{IN} = 16 V		–	450	800	mΩ
Switch Leakage Current	I_{SWlkg}	V_{SW} = 16 V, EN/PWM = V_{IL}, $T_A = T_J$ between –40ºC and 85ºC		–	0.1	1	uA
		V_{SW} = 16 V, EN/PWM = V_{IL}, $T_A = T_J$ = 125ºC		–	10	–	uA
Switch Current Limit	$I_{SW(LIM)}$		•	1.9	2.2	2.8	A
Secondary Switch Current Limit	$I_{SW(LIM2)}$	Higher than $I_{SW(LIM)}$(max) in all conditions, A8513 latches when detected	•	3	3.5	4.64	A
Minimum Switch On-Time	$t_{SW(ON)}$		•	–	75	100	ns
Minimum Switch Off-Time	$t_{SW(OFF)}$		•	–	55	85	ns

Continued on the next page…

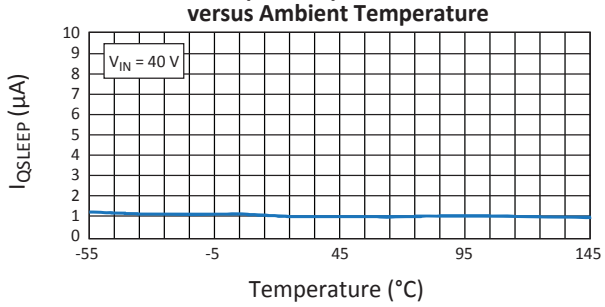
ELECTRICAL CHARACTERISTICS[1] (continued) Valid at V_{IN} = 16 V, T_A = 25ºC, • indicates specifications guaranteed through the full operating temperature range with $T_A = T_J$ = –40ºC to125 ºC, typical specifications are at T_A = 25ºC; unless otherwise specified

Characteristics	Symbol	Test Conditions		Min.	Typ.	Max.	Unit
Oscillator Frequency							
Oscillator Frequency	f_{SW}	A8513KLYTR-1-T, A8513KLPTR-1-T	•	1.8	2	2.2	MHz
		A8513KLYTR-2-T, A8513KLPTR-2-T	•	0.9	1	1.1	MHz
		A8513KLYTR-3-T, A8513KLPTR-3-T	•	450	500	550	kHz
		A8513KLYTR-4-T, A8513KLPTR-4-T	•	225	250	275	kHz
LED Current Sinks							
LED Accuracy	Err_{LED}	ISET = 150 µA	•	–	–	3	%
LED Regulation Voltage	V_{LED}	ISET = 150 µA		–	880	–	mV
I_{SET} to I_{LED} Current Gain	A_{ISET}	ISET = 150 µA	•	1014	1045	1076	A/A
ISET Pin Voltage	V_{ISET}			–	1.003	–	V
Allowable ISET Current	I_{SET}		•	40	–	160	µA
Soft Start LED Current Gain	A_{ILEDSS}	Current through enabled LED pin during soft start		–	48	–	A/A
Maximum PWM Dimming Off-Time	t_{PWML}	Measured while EN/PWM = low during dimming control, and internal references are powered-on (exceeding t_{PWML} results in shutdown)		–	16	–	ms
Minimum PWM On-Time	t_{PWMH}	First cycle when powering-up A8513	•	–	1.5	3	µs
EN/PWM High to LED-On Delay	$t_{dPWM(on)}$	Time between PWM enable and when LED current reaches 90% of maximum; V_{PWM} = 0 → 2 V	•	–	250	500	ns
EN/PWM Low to LED-Off Delay	$t_{dPWM(off)}$	Time between PWM enable going low and when LED current reaches 10% of maximum; V_{PWM} = 2 → 0 V	•	–	250	500	ns
Thermal Protection (TSD)							
Thermal Shutdown Threshold[2]	T_{TSD}	Temperature rising		–	165	–	ºC
Thermal Shutdown Hysteresis[2]	T_{TSDHYS}			–	20	–	ºC

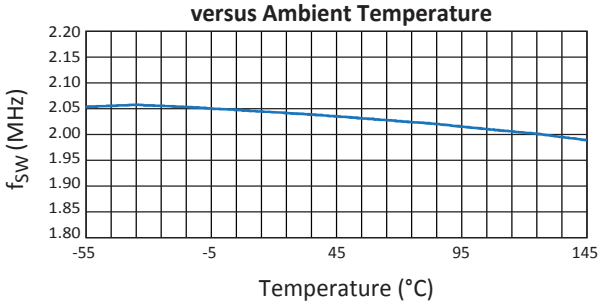
[1]For input and output current specifications, negative current is defined as coming out of the node or pin (sourcing), and positive current is defined as going into the node or pin (sinking).
[2]Ensured by design and characterization, not production tested.
[3] $\overline{FAULT}$ pin is high voltage tolerant

Characteristic Performance

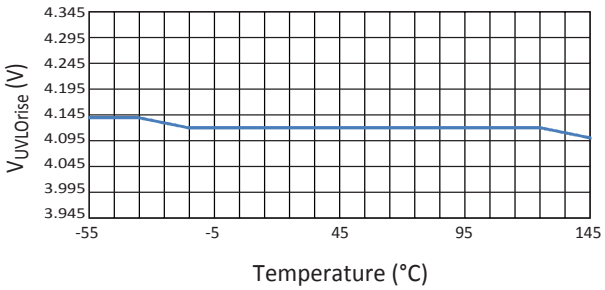
VIN Input Sleep Mode Current versus Ambient Temperature



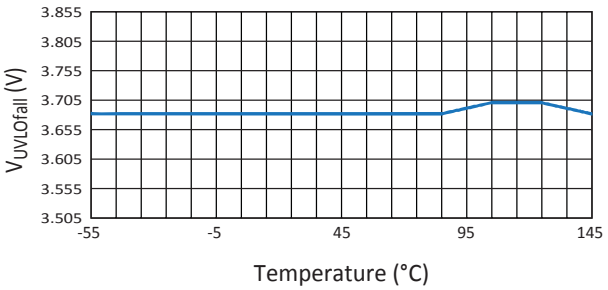
Switch Frequency versus Ambient Temperature



VIN UVLO Rising Threshold Voltage versus Ambient Temperature

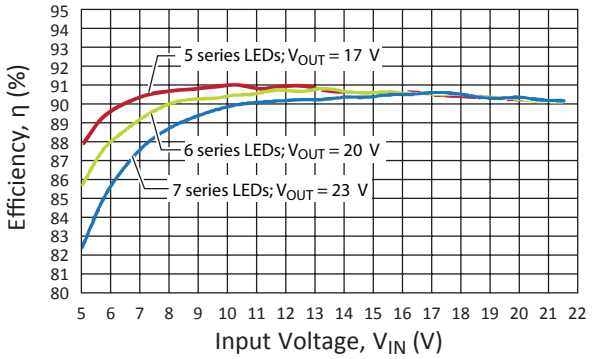


VIN UVLO Falling Threshold Voltage versus Ambient Temperature



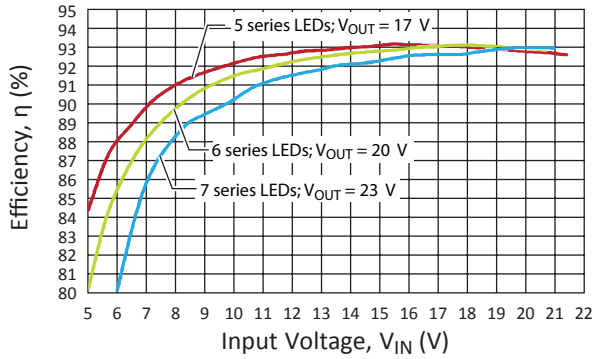
Efficiency Versus Input Voltage

I_{LED} = 90 mA, LED $V_f \approx 3.2$ V



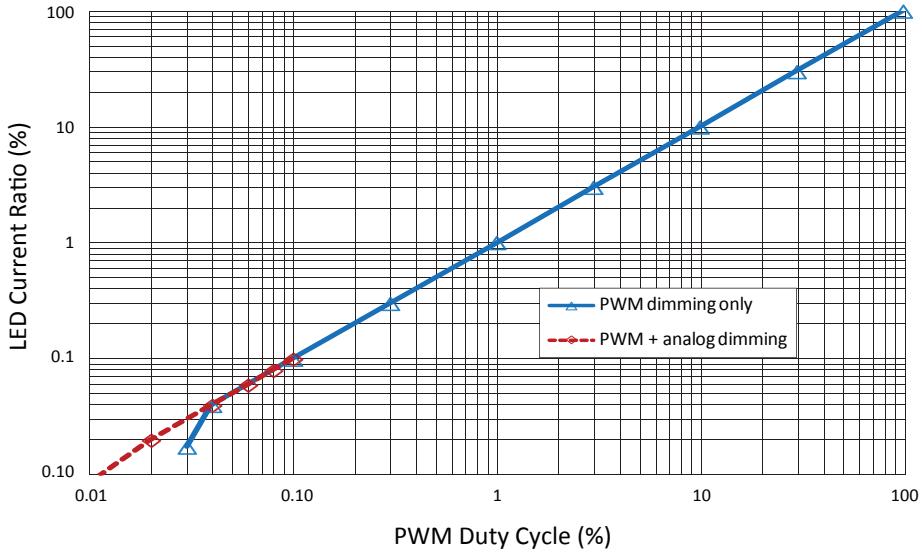
Efficiency Versus Input Voltage

I_{LED} = 150 mA, LED $V_f \approx 3.2$ V



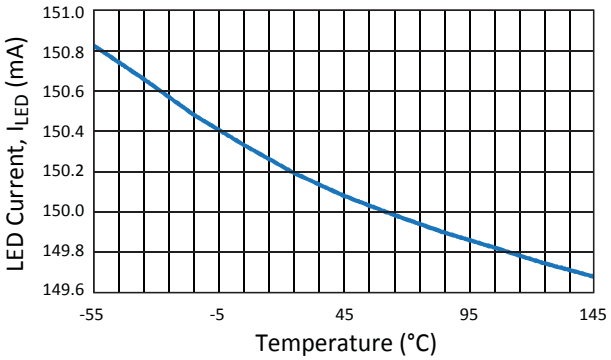
Normalized LED Current Ratio versus PWM Duty Cycle

f_{PWM} = 200 Hz, V_{IN} = 12 V, 6 series LEDs (≈ 21 V, 150 mA)

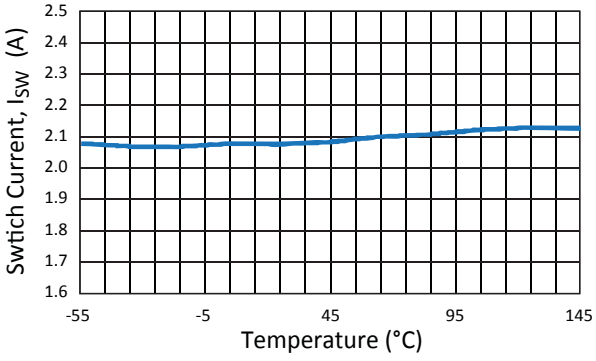


LED Current versus Ambient Temperature

I_{LED} = 150 µA



Switch Current Limit versus Ambient Temperature



Functional Description

The A8513 incorporates a current-mode boost controller with internal DMOS switch, and a single LED current sink. It can be used to drive an LED string of up to 14 white LEDs in series, with current up to 150 mA. For optimal efficiency, the output of the boost stage is adaptively adjusted to the minimum voltage required to power the LED string. This is expressed by the following equation:

$$V_{OUT} = V_{LED} + V_{REG} \quad (1)$$

where

V_{LED} is the voltage drop across the LED string, and

V_{REG} is the regulation voltage of the LED current sink (typically 0.88 V at the maximum LED current).

Enabling the IC

The IC turns on when a logic high signal is applied to the EN/PWM pin (figure 1), and turns off when this pin is pulled to a logic low. For the device to be enabled, the voltage on the VIN pin must be greater than $V_{UVLOrise}$ to clear the undervoltage lockout (UVLO) threshold (figure 2). Before startup, the A8513 goes through a system check to determine if there are any fault conditions that would prevent the system from functioning correctly.

Powering up: LED pin short to GND check

After the VIN pin goes above $V_{UVLOrise}$, the IC checks if the LED pin is shorted to GND by pre-charging the LED pin (figure 3). When the voltage on the LED pin exceeds 260 mV, the A8513 proceeds with soft start. If a short is present on the LED pin, the IC will not power up until the short is removed. At this time the output is also checked for a V_{OUT} short, using the OVP pin. If the OVP pin does not rise above $V_{OVPLO(th)}$ the IC will not power up.

Soft start function

During soft start, the COMP pin delivers a steady 80 uA current, the LED pin current gain is set to A_{ILEDSS}. The lower gain will help limit the inrush current generated by charging the output

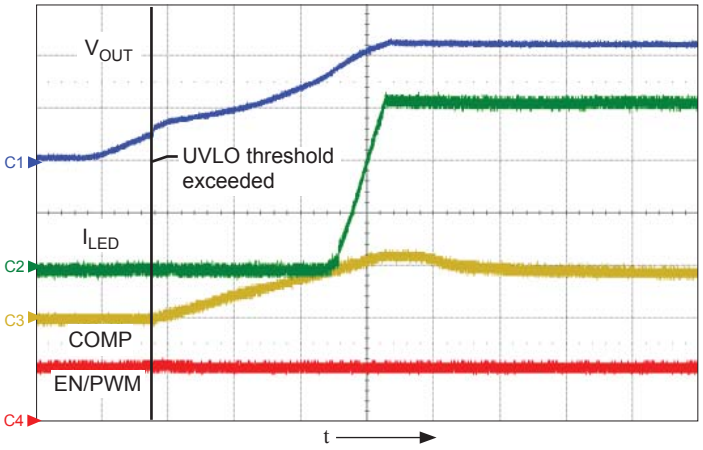


Figure 2. Start-up by slowly ramping up V_{IN} with EN/PWM at 2 V; shows V_{OUT} (ch1, 10 V/div.), I_{LED} (ch2, 50 mA/div.), COMP (ch3, 1 V/div.), and EN/PWM (ch4, 2 V/div.), time = 2 ms/div.

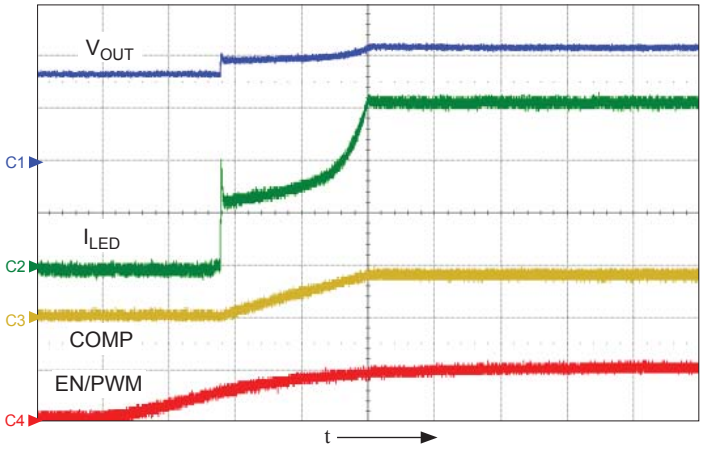


Figure 1. Start-up by slowly ramping up EN/PWM with V_{IN} at 16 V; shows V_{OUT} (ch1, 10 V/div.), I_{LED} (ch2, 50 mA/div.), COMP (ch3, 1 V/div.), and EN/PWM (ch4, 2 V/div.), time = 2 ms/div.

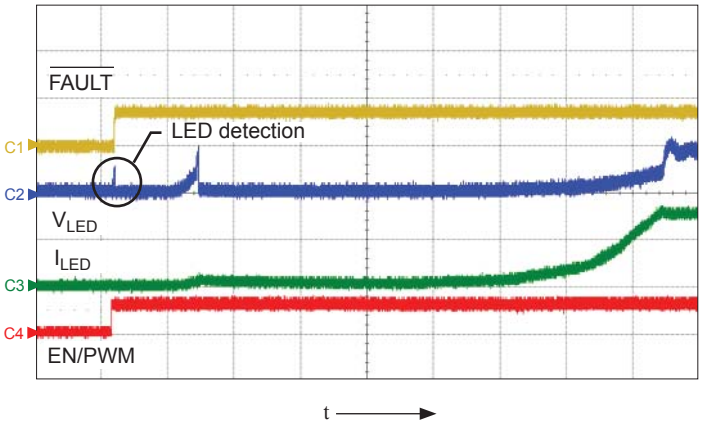


Figure 3. LED detection period; shows $\overline{FAULT}$ (ch1, 5 V/div.), V_{LED} (ch2, 1 V/div.), I_{LED} (ch3, 100 mA/div.), and EN/PWM (ch4, 5 V/div.), time = 500 µs/div.

capacitors. After the A8513 senses there is enough voltage on the LED pin, it increases the LED current to the preset regulation current. The COMP pin will continue to source 80 uA until the LEDs are able to run at the full preset current level.

Boost converter frequency

The switching frequency of the boost regulator is preset internally to one of four frequencies. The frequency options are:

Part Number	Switching Frequency (f_{SW}) (MHz)
A8513KLYTR-1-T	2
A8513KLYTR-2-T	1
A8513KLYTR-3-T	0.5
A8513KLYTR-4-T	0.25

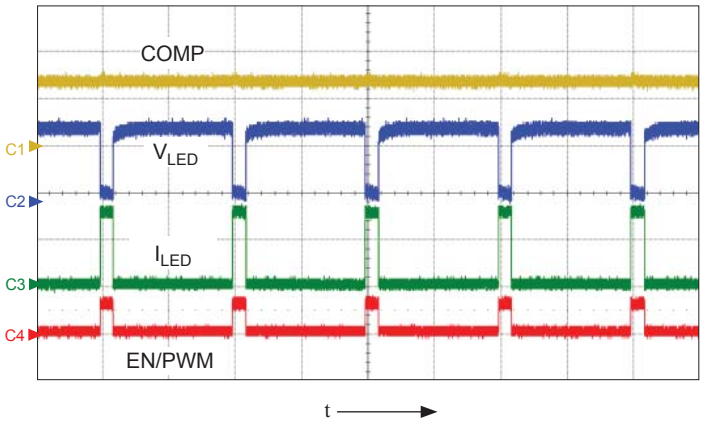


Figure 4. Typical PWM dimming sequence, with PWM dimming frequency of 1000 Hz and 10% duty cycle; shows COMP (ch1, 1 V/div.), V_{LED} (ch2, 10 V/div.), I_{LED} (ch3, 100 mA/div.), and EN/PWM (ch4, 5 V/div.), time = 500 µs/div.

LED current setting and LED dimming

The LED current, I_{LED}, is set using the ISET pin, and can range from 40 to 150 mA. Connect a resistor, R_{ISET}, between this pin and GND to set the I_{LED} current, according to the following formula :

$$I_{LED} = \frac{V_{ISET}}{R_{ISET}} \times A_{ISET} \quad (2)$$

$$= \frac{1.003\ V}{R_{ISET}} \times 1045$$

where I_{LED} is in A and R_{ISET} is in Ω.

This formula sets the maximum current through the LEDs, which is referred to as the *100% current*.

PWM dimming

The LED current can be reduced from the 100% current level by PWM dimming using the EN/PWM pin. When the EN/PWM pin is pulled high, the A8513 turns on and the LED pin sinks 100% current (figure 4). When EN/PWM is pulled low, the boost converter and LED sink are turned off. The compensation (COMP) pin is floated, and critical internal circuits are kept active.

The A8513 has very fast turn-on and turn-off times during PWM dimming to minimize low PWM duty cycle errors. The typical PWM signal delay $t_{dPWM(on)}$ is 250 ns (figure 5). The typical $t_{dPWM(off)}$ time, between the PWM signal and the LED current going low, is shown in figure 6.

Analog dimming

The A8513 can also be dimmed by using an external DAC or other voltage source applied either directly to the ground side of the R_{ISET} resistor or through an external resistive divider to the

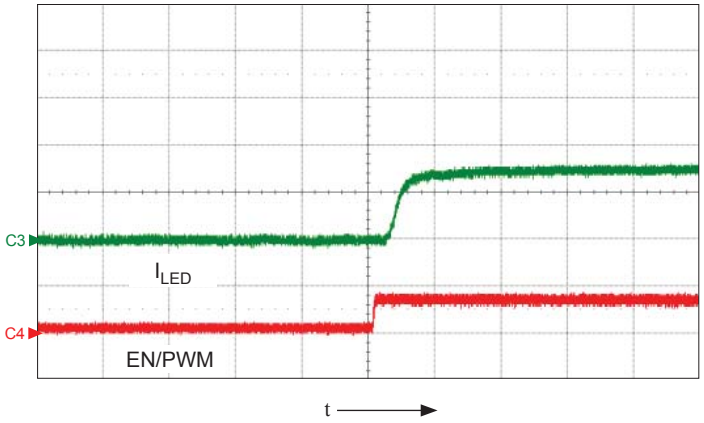


Figure 5. Typical EN/PWM signal (5 V/div.) to LED current (100 mA/div.) turn-on delay. The delay measured about 250 ns. V_{IN} is 12 V, V_{OUT} for 10 series LEDs is approximately 36 V, I_{LED} is 150 mA. (time = 500 ns/div.)

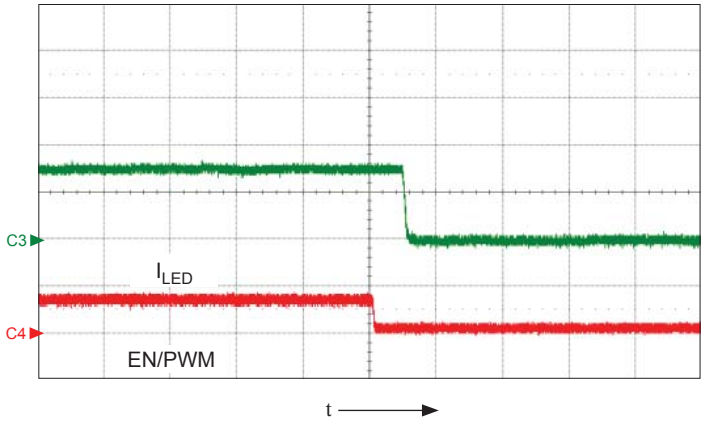


Figure 5. Typical EN/PWM signal (5 V/div.) to LED current (100 mA/div.) turn-off delay. The typical delay is about 250 ns. (time = 500 ns/div.)

ISET pin. The limitation of this form of dimming is that the internal I_{SET} error amplifier is designed to work from 40 to 160 µA, thus limiting the dimming ratios that can be achieved.

Figure 7, top panel is a typical application using a DAC to control the LED current using a single resistor connected to the ISET pin. The I_{SET} current is controlled by the following formula:

$$I_{SET} = \frac{V_{ISET} - V_{DAC}}{R_{ISET}} \quad (3)$$

Where V_{ISET} is the ISET pin voltage and V_{DAC} is the DAC output voltage.

When the DAC voltage is equal to V_{ISET}, the internal reference, there is no current through R_{ISET}. When the DAC voltage starts to decrease, the ISET current starts to increase, thus increasing the LED current. When the DAC voltage is 0 V, the LED current will be at its maximum.

• For a dual-resistor configuration (lower panel of figure 7), the ISET current is controlled by the following formula:

$$I_{SET} = \frac{V_{ISET}}{R_{ISET}} - \frac{V_{DAC} - V_{ISET}}{R_1} \quad (4)$$

The advantage of this circuit is that the DAC voltage can be higher or lower, thus adjusting the LED current to a higher or lower value of the preset LED current set by the R_{ISET} resistor:

- V_{DAC} = 1.003 V; the output is strictly controlled by R_{ISET}
- V_{DAC} > 1.003 V; the LED current is reduced
- V_{DAC} < 1.003 V; the LED current is increased

Output Overvoltage Protection (OVP) and Output Undervoltage Protection (UVP)

The A8513 has output overvoltage protection (OVP), output undervoltage protection and secondary overvoltage protection (open diode).

Overvoltage Protection The OVP pin has a threshold, $V_{OVPHI(th)}$, of 1.218 V. A resistive divider can be used to set the V_{OUT} overvoltage protection threshold up to 45 V (see figure 8). There is no restriction on the value of the resistor chosen, but it is recommended that the divider current be kept between 10 and 60 µA. This will minimize the effect of sense current on the accuracy of OVP, and minimize output voltage bleed-off during PWM dimming.

Formulas for calculating the OVP resistor voltage divider are shown below.

$$R_{OVP1} = (V_{OVP} - 1.218\ V) / I_{SET} \quad (5)$$

$$R_{OVP2} = 1.218\ V / I_{SET} \quad (6)$$

The OVP function is not inherently a latched fault. If the OVP condition occurs during a load dump, the IC will stop switching but not shut down.

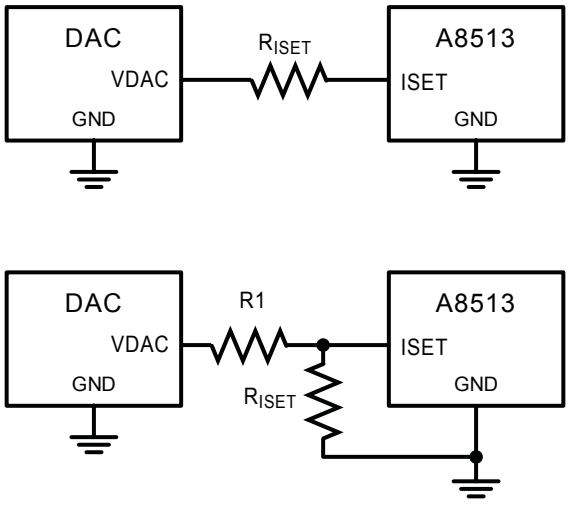


Figure 7. Simplified diagram of voltage LED current control (upper) single resistor, and (lower) dual resistors.

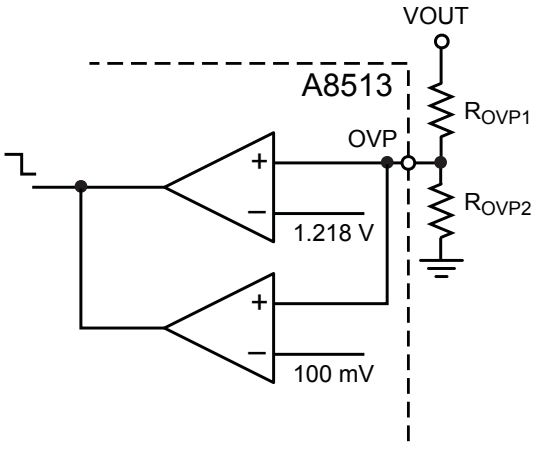


Figure 8. Simplified diagram of the OVP pin functions.

The OVP condition can become a latched fault if, during an OVP event, the LED current is not in regulation. This typically occurs during an open LED string situation. If both faults occur simultaneously the IC will shut down and the fault flag will be set (see figures 9, 10, and 11).

Undervoltage Protection The OVP pin is also used to detect output undervoltage protection (UVP) against V_{OUT} short to GND. When the UVP fault is tripped, the fault flag is set (figure 12). Using an external PMOSFET interfaced to the $\overline{FAULT}$ pin (figure 13), the user can disconnect the IC from VIN during a fault event.

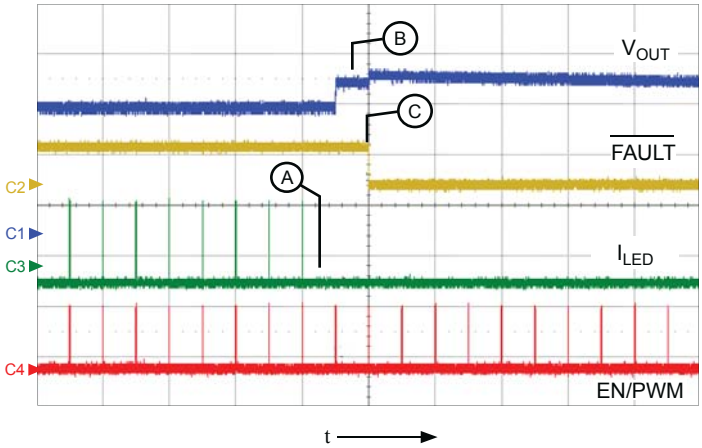


Figure 9. Open LED condition during PWM dimming. (A) The LED string (ch3, 100 mA/div.) is opened (no current flow through the LED pin) during an off-period for the PWM dimming signal (ch4, 5 V/div.). (B) At the next PWM cycle, the LED open condition is detected and the A8513 starts boosting the output voltage (ch1, 10 V/div.). (C) Upon reaching the OVP threshold and sensing no LED current flow, the A8513 shuts down and sets the fault flag (ch2, 5 V/div.). (time = 10 ms/div.)

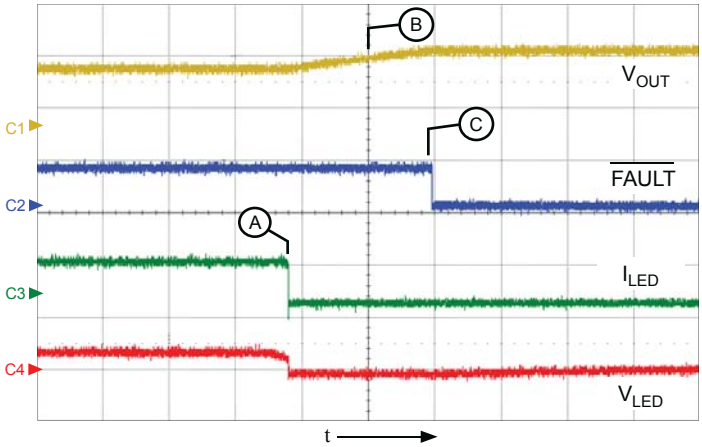


Figure 10. Open LED condition when PWM duty cycle is 100%. (A) The LED string (ch3, 200 mA/div.) is opened (no current flow through the LED pin). (B) The A8513 starts boosting the output voltage (ch1, 20 V/div.). (C) Upon reaching the OVP threshold there is still no current flow through the LED pin, and the A8513 shuts down and sets the fault flag (ch2, 5 V/div.). The LED pin voltage is ch4, 2 V/div. (time = 50 µs/div.)

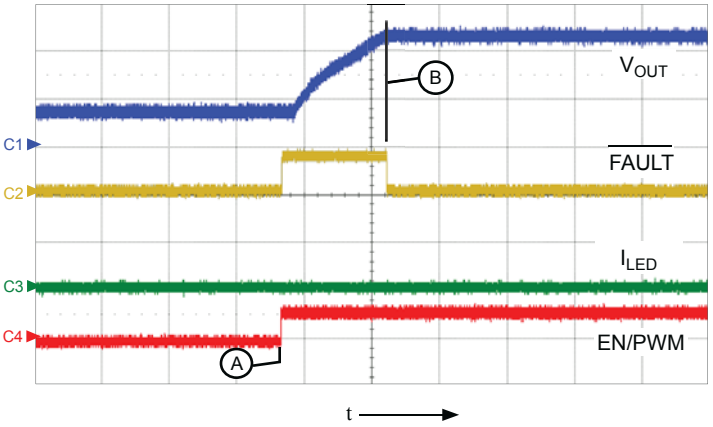


Figure 11. Power-up into an open LED situation. (A) A8513 enabled, (B) fault flag (ch2, 5 V/div.) is set when OVP threshold is reached. Shows V_{OUT} (ch1, 20 V/div.), I_{LED} (ch3, 100 mA/div.), and EN/PWM (ch4, 5 V/div.), time = 1 ms/div..

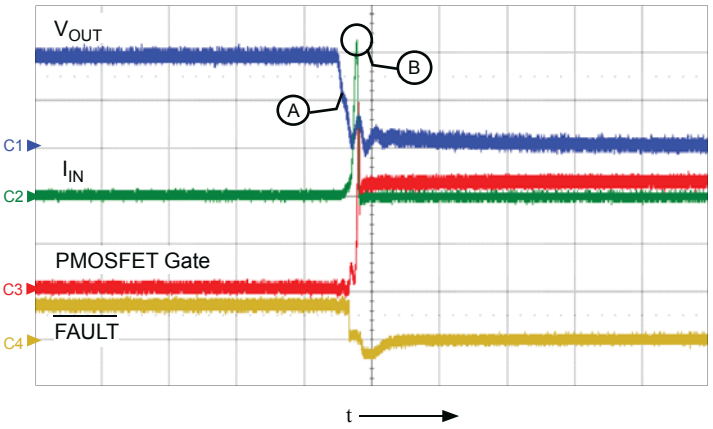


Figure 12. Input disconnect switch function during an output short. (A) V_{OUT} (ch1, 10 V/div.) falls during VOUT short to ground, (B) high peak current present due to short, before the PMOSFET (ch3, 5 V/div.) is disconnected. Shows input current (ch2, 10 A/div.) and fault flag (ch4, 5 V/div.), time = 50 µs/div.

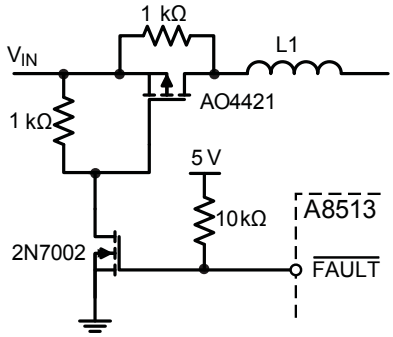


Figure 13. typical circuit for input disconnect switch.

Secondary Overvoltage Protection The A8513 has secondary overvoltage protection for the internal boost switch in the event of an open diode condition. If the voltage on the SW pin exceeds the device safe operating voltage rating, the A8513 is disabled and remains latched off (figure 14). The EN/PWM pin must be brought low longer than t_{PWML} to clear this fault.

Boost switch overcurrent protection

The boost switch is protected with cycle-by-cycle current limiting set to $I_{SW(LIM)}$ (figure 15). There is also a secondary current limit that is sensed on the boost switch. When this current limit is exceeded, the A8513 immediately shuts down (figure 16). The secondary current limit is above the cycle-by-cycle current limit and protects the switch from destructive currents if the boost inductor is shorted.

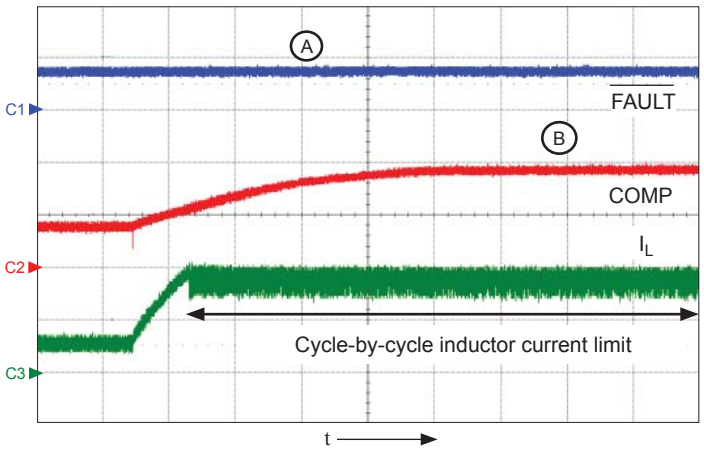


Figure 15. Cycle-by-cycle current limit, inductor current is C3 (1 A/div.). (A) Fault flag (ch1, 5 V/div.) is not set during cycle-by-cycle current limit, (B) COMP pin signal (C2, 2 V/div.) is close to 3.6 V. (time = 1 ms/div.)

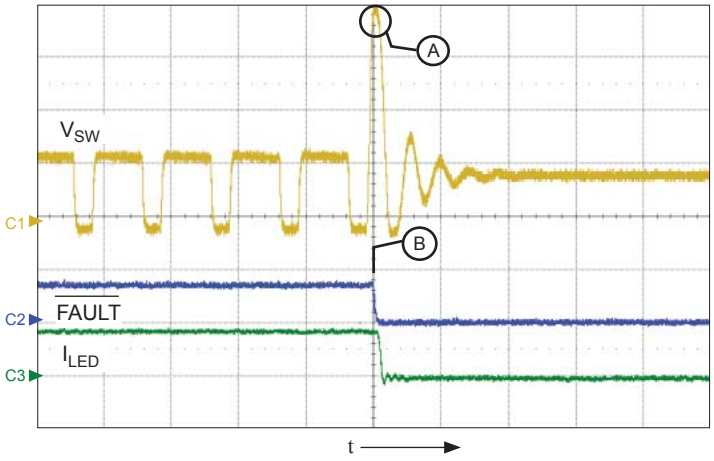


Figure 14. Secondary Overvoltage protection tripped when the switching diode is opened during operation. (A) High voltage is detected on SW node (ch1, 20 V/div.) and the A8513 is shut down. (B) Fault flag is set (ch2, 5 V/div.). Shows LED current (ch3, 100 mA/div.), time = 500 ns/div.

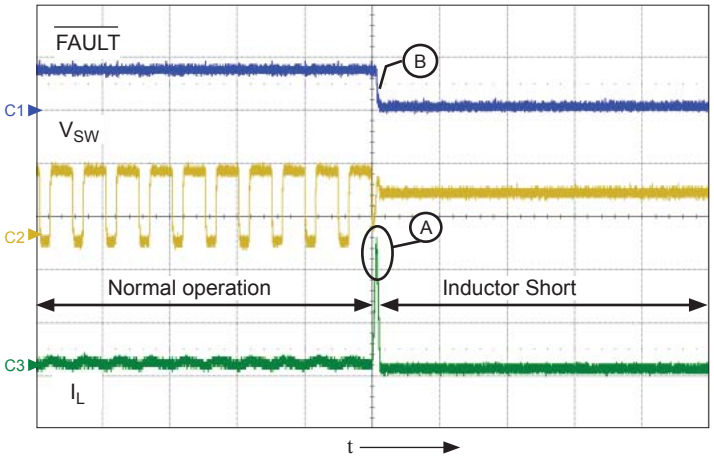


Figure 16. Secondary current limit during an inductor short condition. (A) limit is reached, (B) the IC shuts down and the fault flag is set. Shows fault flag (c1, 5 V/div.), switch node voltage (C2, 20 V/div.), and current through the inductor (C3, 2 A/div.); time = 1 µs/div.

Input UVLO

When V_{IN} rises above the UVLO threshold $V_{UVLOrise}$, the A8513 can be enabled by asserting EN/PWM. The A8513 is disabled when V_{IN} falls below $V_{UVLOfall} - V_{UVLOhys}$ for more than 1 µs (figure 17). This 1 µs lag prevents false shut downs during momentary glitches on the input power supply.

VDD

The VDD pin provides regulated bias supply for internal circuits. Connect a capacitor, C_{VDD}, with a value of 0.01 to 0.1 µF to this pin.

Shutdown

If the EN/PWM pin is pulled low for more than t_{PWML}, the device enters shutdown mode and clears all internal fault registers. In shutdown, the A8513 will disable all current sources and wait until EN/PWM goes high to re-enable the IC.

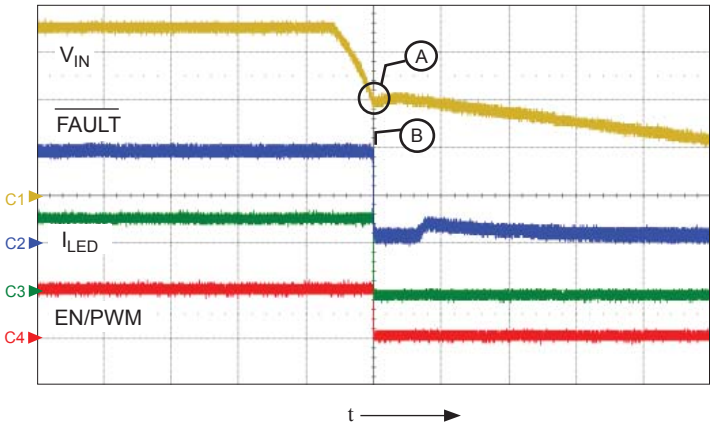


Figure 17. Input UVLO. (A) UVLO tripped (V_{IN}, ch1, 2 V/div.), (B) fault flag set (ch2, 2 V/ div.). Shows LED current (ch3, 100 mA/div.) and EN/PWM (ch4, 1 V/div.), time = 5 ms/div.

Fault protection during operation

The A8513 constantly monitors the state of the system to determine if any fault conditions occur. The response to a triggered fault condition is summarized in the table below.

Note: Some of the protection features might not be active during startup, to prevent false triggering of fault conditions.

The latching faults can be cleared in two ways:

- Keep the EN/PWM pin low for more than 16 ms.
- Cycle the power to create a UVLO condition.

Fault behavior diagrams are shown in figures 18, 19 and 20.

Fault Mode Table

Fault Name	Type	Active	Fault Flag Set	Description	Boost	Sink driver
Primary Switch Current Protection (cycle-by-cycle current limit)	Auto-restart	Always	No	This fault condition is triggered by the cycle-by-cycle current limit $I_{SW(LIM)}$. Prevents current in inductor from exceeding $I_{SW(LIM)}$.	Off for a single cycle	On
Secondary Switch Current Limit	Latched	Always	Yes	When the current through the boost switch exceeds the secondary current SW limit, $I_{SW(LIM2)}$, the A8513 immediately shuts down.	Off	Off
Secondary OVP	Latched	Always	Yes	Secondary overvoltage protection is used for open diode detection. When diode D1 opens, the switch pin voltage will increase until $V_{OVP(sec)}$ is reached.	Off	Off
LED Pin Short Protection	Auto-restart	Startup	Yes	This fault prevents the A8513 from starting-up if the LED pin is shorted to ground. After the short is removed, soft-start is allowed to begin.	Off	Off
ISET Short Protection	Auto-restart	Always	Yes	This fault occurs when the I_{SET} current goes above 150% of the maximum Allowable ISET Current, I_{SET}(max). The boost will stop switching and the IC will disable the LED sinks until the fault is removed. When the fault is removed, the IC tries to regulate to the preset LED current.	Off	Off
LED String Open Protection	Latched	Always	Yes	This fault occurs when the OVP pin exceeds the $V_{OVPHI(th)}$ threshold. The A8513 immediately stops switching. If at the same time, the LED voltage is below regulation, the IC will shut down.	Off	Off
Output Overvoltage Protection	Auto-restart	Always	No	This fault occurs when the OVP pin exceeds $V_{OVPHI(th)}$ threshold (for example, during a load dump). The A8513 immediately stops switching, but continues to sink current through the LED pin.	Off	On
Output Undervoltage Protection	Auto-restart	Always	Yes	This fault occurs when the OVP pin senses less than 110 mV on the pin.	Off	Off
Overtemperature Protection	Auto-restart	Always	Yes	This fault occurs when the die temperature exceeds T_{TSD}.	Off	Off
VIN UVLO	NA	Always	Yes until internal regulator shuts down	This fault occurs when V_{IN} drops below $V_{UVLOfall}$. This fault resets all latched faults.	Off	Off

ISET Short to Ground

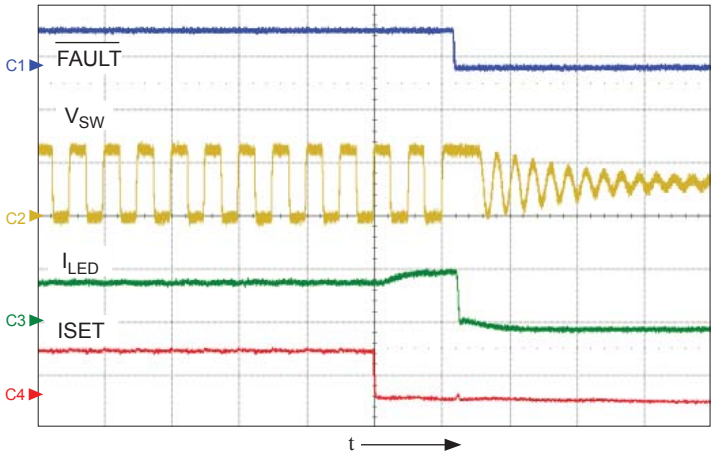


Figure 18. $\overline{\text{FAULT}}$ (ch1, 5 V/div.), V_{SW} (ch2, 20 V/div.), I_{LED} (ch3, 100 mA/div.), and ISET (ch4, 1 V/div.), time = 1 µs/div.

Recovery from ISET Short to Ground

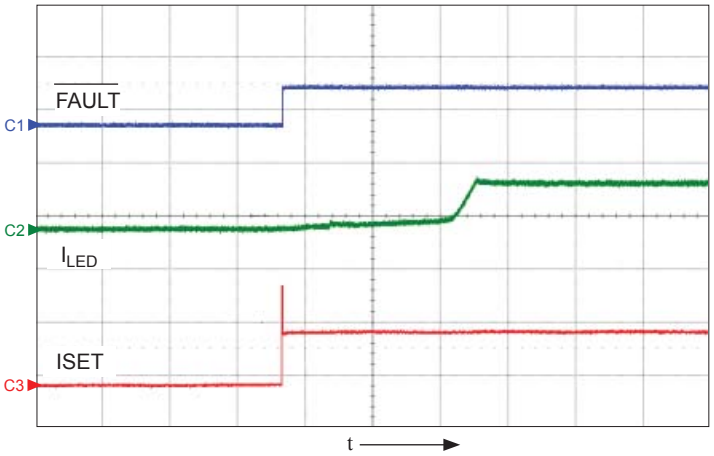


Figure 19. $\overline{\text{FAULT}}$ (ch1, 5 V/div.), I_{LED} (ch2, 100 mA/div.), and ISET (ch3, 1 V/div.), time = 2 ms/div.

OVP Tripped During Load Dump

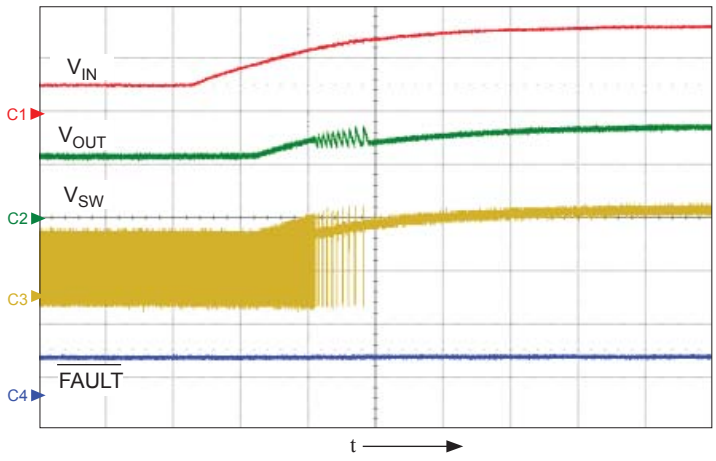


Figure 20. V_{IN} (ch1, 20 V/div.), V_{OUT} (ch2, 20 V/div.), and V_{SW} (ch3, 20 V/div.), $\overline{\text{FAULT}}$ (ch4, 5 V/div.), time = 2 ms/div.

Design Example

This section provides a method for selecting component values when designing an application using the A8513. A typical circuit using this design is shown in figure 21.

Assumptions: For the purposes of this example, the following are given as the application requirements:

- V_{IN}: 5 to 16 V
- Quantity of series LEDs, $\#_{SERIESLEDS}$: 6
- LED current, I_{LED}: 120 mA
- V_f at 120 mA: 3.2 V
- f_{SW}: 2 MHz
- T_A(max): 85°C
- PWM dimming frequency: 200 Hz with a minimum duty cycle of 1%.

Procedure: Select the appropriate configuration and the individual component values in an ordered sequence.

Step 1: Connect the series LED string from VOUT to the LED pin.

Step 2: Determine the value for the I_{LED} setting resistor, R_{ISET}:

$$R_{ISET} = V_{ISET} \times A_{ISET} / I_{LED} \quad (7)$$
$$= (1.003 \times 1045) / 120 \text{ mA} = 8.74 \text{ k}\Omega$$

Choose an 8.66 kΩ resistor.

Step 3: Determine the values of the OVP resistors. The OVP resistors are connected between the OVP pin and the output voltage (VOUT) and the OVP pin and ground.

Step 3a: The first step is to determine the maximum voltage based on the LED V_f requirements. To this value the regulation voltage should be added, as well as another 2 V to account for noise, output ripple, and resistor tolerances. The regulation voltage, V_{LED}, of the A8513 is 880 mV. Then:

$$V_{OUT(OVP)} = \#_{SERIESLEDS} \times V_f + V_{LED} + 2 \text{ V} \quad (8)$$
$$= 6 \times 3.2 \text{ V} + 0.880 \text{ V} + 2 \text{ V}$$
$$= 22.08 \text{ V}$$

To find the OVP resistor values, the user should choose a resistor divider that has very low current (I_{OVP}) and R_{OVP} should be approximately 1 MΩ. A good starting point is 50 µA as I_{OVP}. (The I_{OVP} current is used later in calculating the total leakage current.) Then:

$$R_{OVP1} = (V_{OUT(OVP)} - V_{OVPHI(th)}) / I_{OVP} \quad (9)$$
$$= (22.08 \text{ V} - 1.218 \text{ V}) / 50 \text{ µA} = 417.2 \text{ k}\Omega$$

and:

$$R_{OVP2} = V_{OVPHI(th)} / I_{OVP} \quad (10)$$
$$= 1.218 \text{ V} / 50 \text{ µA} = 24.36 \text{ k}\Omega$$

Choose a value of resistor that is higher value than the calculated R_{OVP}. In this case 422 kΩ was selected. Below is the actual value of the minimum OVP trip level with the selected resistor:

$$V_{OUT(OVP)} = R_{OVP} \times I_{OVP} \times V_{OVPHI(th)} \quad (11)$$
$$= 422 \text{ k}\Omega \times 50 \text{ µA} + 1.218 \text{ V} = 22.32 \text{ V}$$

STEP 3b: At this point a quick check should be done to determine if the conversion ratio is acceptable for the selected frequency:

$$D_{maxofboost} = 1 - t_{SW(OFF)} \times f_{SW} \quad (12)$$
$$= 1 - 85 \text{ ns} \times 2 \text{ MHz} = 83\%$$

where the Minimum Switch Off-Time, $t_{SW(OFF)}$, is found in the Electrical Characteristics table.

The Theoretical Maximum V_{OUT} is then calculated as:

$$V_{OUT}(\text{max}) = \frac{V_{IN}(\text{min})}{1 - D_{maxofboost}} - V_d \quad (13)$$

$$= \frac{5 \text{ V}}{1 - 0.83} - 0.4 \text{ V} = 29.01 \text{ V}$$

where V_d is the diode forward voltage.

The Theoretical Maximum V_{OUT} value must be greater than the value $V_{OUT(OVP)}$. If this is not the case, a lower frequency version of the A8513 should be chosen to meet the maximum duty cycle requirements.

Step 4: Inductor selection. The inductor should be chosen such that it can handle the necessary input current. In most applications, due to stringent EMI requirements, the system must operate in continuous conduction mode throughout the whole input voltage range.

Step 4a: Determine the Duty Cycle:

$$D(\max) = 1 - \frac{V_{IN}(\min)}{V_{OUT(OVP)} + V_d} \quad (14)$$

$$= 1 - \frac{5\ V}{22.32\ V + 0.4\ V} = 78\%$$

where V_d is the voltage drop of the boost diode.

Step 4b: Determine the maximum and minimum input current to the system. The minimum input current will dictate the inductor value. The maximum current rating will dictate the current rating of the inductor. Given $I_{OUT} = I_{LED} = 120$ mA:

$$I_{IN}(\max) = \frac{V_{OUT(OVP)} \times I_{OUT}}{V_{IN}(\min) \times \eta} \quad (15)$$

$$= \frac{22.32\ V \times 120\ mA}{5\ V \times 0.9} = 0.595\ A$$

where η is efficiency. Next, calculate minimum input current, as follows:

$$I_{IN}(\min) = \frac{V_{OUT(OVP)} \times I_{OUT}}{V_{IN}(\max) \times \eta} \quad (16)$$

$$= \frac{22.32\ V \times 120\ mA}{16\ V \times 0.9} = 0.19\ A$$

A good approximation of efficiency η can be taken from the efficiency curves located in the data sheet. A value of 90% is a good starting approximation.

STEP 4c: Determine the inductor value.

To assure that the inductor operates in continuous conduction mode the value of inductor should be set such that the ½ inductor ripple current is not greater than the average minimum input current. A good inductor choice for inductor ripple current is 30% of the maximum input current:

$$\Delta I_L = I_{IN}(\max) \times 0.3 \quad (17)$$

$$= 0.595\ A \times 0.3 = 0.18\ A$$

then:

$$L = \frac{V_{IN}(\min)}{\Delta I_L \times f_{SW}} \times D(\max) \quad (18)$$

$$= \frac{5\ V}{0.18\ A \times 2\ MHz} \times 0.78 = 10.83\ \mu H$$

Double-check to make sure the ½ current ripple is less than $I_{IN}(\min)$:

$$I_{IN}(\min) > {}^1/_2\ \Delta I_L \quad (19)$$

$$0.19\ A > 0.09\ A$$

A good inductor value to use would be 10 µH.

Step 4d: This step verifies that there is sufficient slope compensation for the inductor chosen. The required slope compensation value for different frequencies is listed below:

f_{SW} (MHz)	Slope Compensation (A/µs)
2	3.73
1	1.85
0.500	3.70
0.250	1.83

Next insert the inductor value used in the design:

$$\Delta I_{Lused} = \frac{V_{IN}(\min) \times D(\max)}{L_{used} \times f_{SW}} \quad (20)$$

$$= \frac{5\ V \times 0.78}{10\ \mu H \times 2.0\ MHz} = 0.20\ A$$

Calculate the minimum required slope:

$$\text{Required Slope (min)} = \frac{\Delta I_{Lused} \times 1 \times 10^{-6}}{\frac{1}{f_{SW}} \times (1 - D(\max))} \quad (21)$$

$$= \frac{0.20\ A \times 1 \times 10^{-6}}{\frac{1}{2.0\ MHz} \times (1 - 0.78)} = 1.8\ A/\mu s$$

For a stable system, the required minimum slope must be smaller than the IC slope compensation.

Note: The slope compensation value is in A/µs; the 1×10^{-6} is a constant multiplier.

STEP 4e: Determine the inductor current rating :

$$I_L \text{minimum rating} = I_{IN}(\max) + {}^1/_2\,\Delta I_{Lused} = 0.595\text{ A} + 0.20\text{ A} / 2 = 0.695\text{ A} \quad (22)$$

Step 5: Choose the proper switching diode. The switching diode should be chosen for three characteristics when it is used in LED lighting circuitry. The first and most obvious are the current rating of the diode and the reverse voltage rating. The reverse voltage rating should be such that during operation condition the voltage rating of the device is larger than the maximum output voltage; in this case it is $V_{OUT\,(OVP)}$. The peak current through the diode is:

$$I_{dp} = I_{IN}(\max) + {}^1/_2\,\Delta I_{Lused} = 0.595\text{ A} + 0.20\text{ A} / 2 = 0.695\text{ A} \quad (23)$$

The third major component in deciding the switching diode is the reverse current, I_R, characteristic of the diode. This characteristic is especially important when PWM dimming is implemented. During PWM off-time the boost converter is not switching. This results in a slow bleeding off of the output voltage, due to leakage currents. I_R can be a large contributor, especially at high temperatures. On the diode that was selected in this design, the current varies between 1 and 100 µA.

Step 6: Choose the output capacitors. The output capacitors should be chosen such that they provide filtering for both the boost converter and for the PWM dimming function. The biggest factors that contribute to the size of the output capacitor is PWM dimming frequency and the PWM duty cycle. Another major contributor is leakage current, I_{lkg}. This current is a combination of the OVP resistor divider, I_{OVP}, and the reverse leakage of the switching diode. In this design the PWM dimming frequency is 200 Hz and the minimum duty cycle is 1%. Typically the voltage variation on the output during PWM dimming must be less than 250 mV (V_{COUT}) so that no audible noise can be heard. The capacitance can be calculated as follows:

$$C_{OUT} = I_{lkg} \times \frac{1 - D_{dimming}(\min)}{f_{PWM(dimming)} \times V_{COUT}} = 120\ \mu\text{A} \times \frac{1 - 0.01}{200\text{ Hz} \times 0.250\text{ V}} = 2.38\ \mu\text{F} \quad (24)$$

A capacitor larger than 2.38 µF capacitor should be selected due to degradation of capacitance at high voltages on the capacitor. One ceramic 4.7 µF, 50 V capacitor is a good choice to fulfill this requirement. Corresponding capacitors include:

Vendor	Value	Part number
Murata	4.7 µF 50 V	GRM32ER71H475KA88L
Murata	2.2 µF 50 V	GRM31CR71H225KA88L

The rms current through the capacitor is given by:

$$I_{COUT}\text{rms} = I_{OUT} \sqrt{\frac{D(\max) + \frac{\Delta I_L}{I_{IN}(\max) \times 12}}{1 - D(\max)}} = 0.120\text{ A} \sqrt{\frac{0.78 + \frac{0.20\text{ A}}{0.595\text{ A} \times 12}}{1 - 0.78}} = 0.23\text{ A} \quad (25)$$

The output capacitor should have a current rating of at least 230 mA. The current rating of the 4.7 µF, 50V capacitor is 1.5 A.

STEP 7: Select the input capacitor. The input capacitor should be selected such that it provides good filtering of the input voltage waveform. A good rule of thumb is to set the input voltage ripple, ΔV_{IN} to be 1% of the minimum input voltage. The minimum input capacitor requirements are as follows:

$$C_{IN} = \frac{\Delta I_L}{8 \times f_{SW} \times \Delta V_{IN}} \quad (26)$$

$$= \frac{0.20\ \text{A}}{8 \times 2\ \text{MHz} \times 0.05\ \text{V}} = 0.25\ \mu\text{F}$$

The rms current through the capacitor is given by:

$$I_{IN}\text{rms} = \frac{I_{OUT} \times \frac{\Delta I_L}{I_{IN}(\text{max})}}{(1 - D(\text{max}))\sqrt{12}} \quad (27)$$

$$= \frac{0.120 \times \frac{0.20\ \text{A}}{0.595\ \text{A}}}{(1 - 0.78)\sqrt{12}} = 0.05\ \text{A}$$

A good ceramic input capacitor with ratings of 2.2 µF, 50V or 4.7 µF, 50 V will suffice for this application. Corresponding capacitors include:

Vendor	Value	Part number
Murata	4.7 µF 50 V	GRM32ER71H475KA88L
Murata	2.2 µF 50 V	GRM31CR71H225KA88L

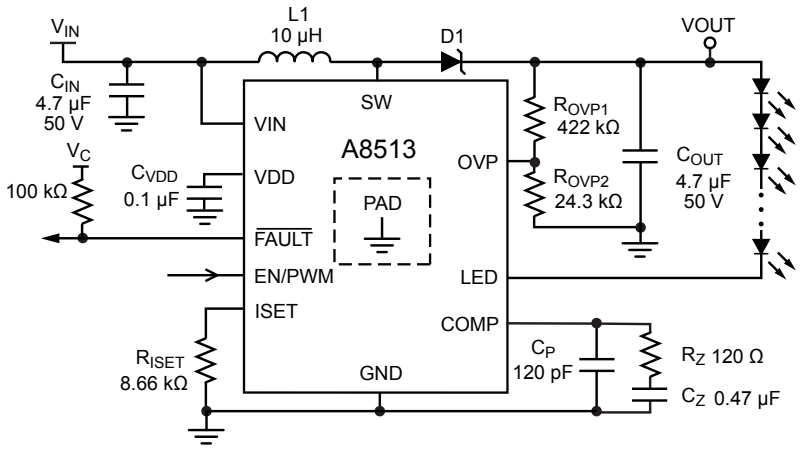
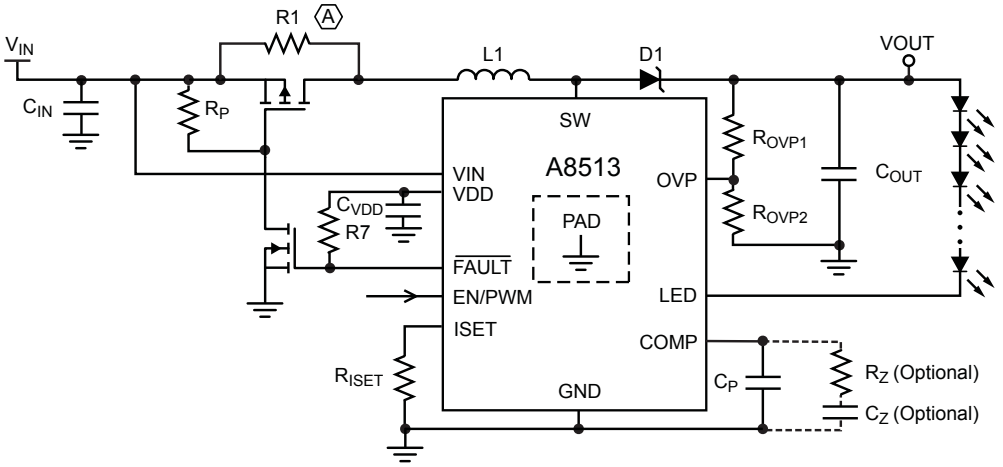


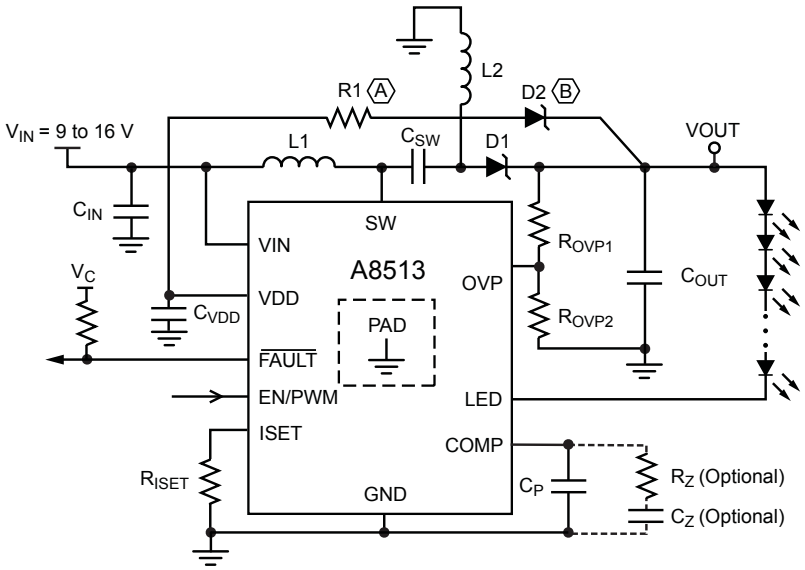
Figure 21. A typical circuit designed using the example above in this section.

Typical Application Drawings



A R1 is used to provide a leakage path such that the OVP pin is above 100 mV during startup. Otherwise the IC would assume the output is shorted to GND and would not proceed with soft start.

Figure 22. Typical application showing boost configuration and PMOS disconnect switch implementation

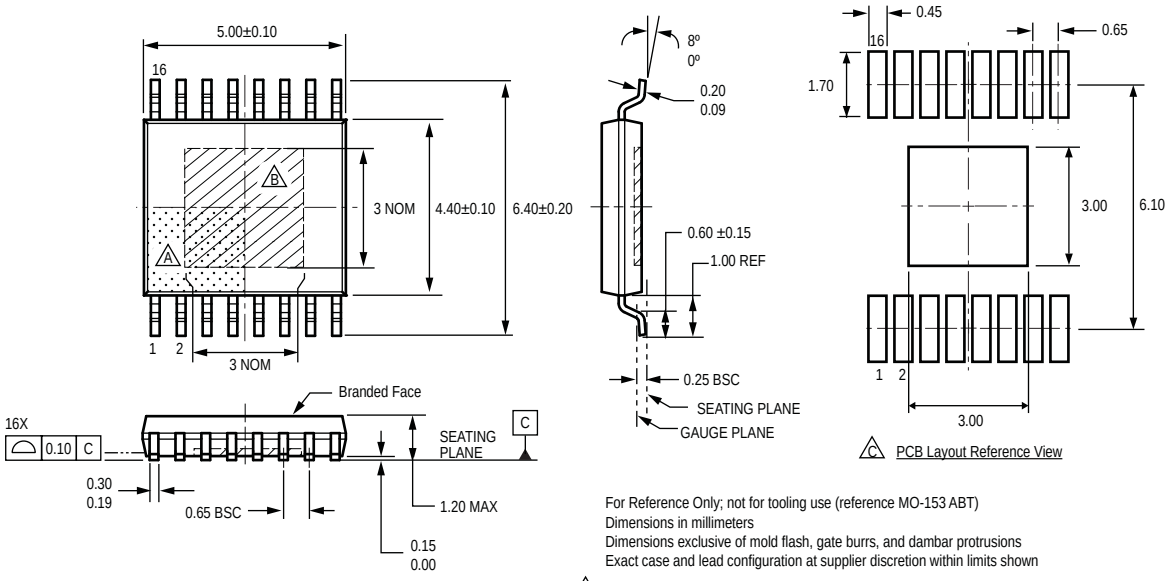


A R1 is used to provide a leakage path such that the OVP pin is above 100 mV during startup. Otherwise the IC would assume the output is shorted to GND and would not proceed with soft start.

B D2 is a blocking diode.

Figure 23. Typical application showing SEPIC configuration

Package LP, 16-Pin TSSOP with Exposed Thermal Pad



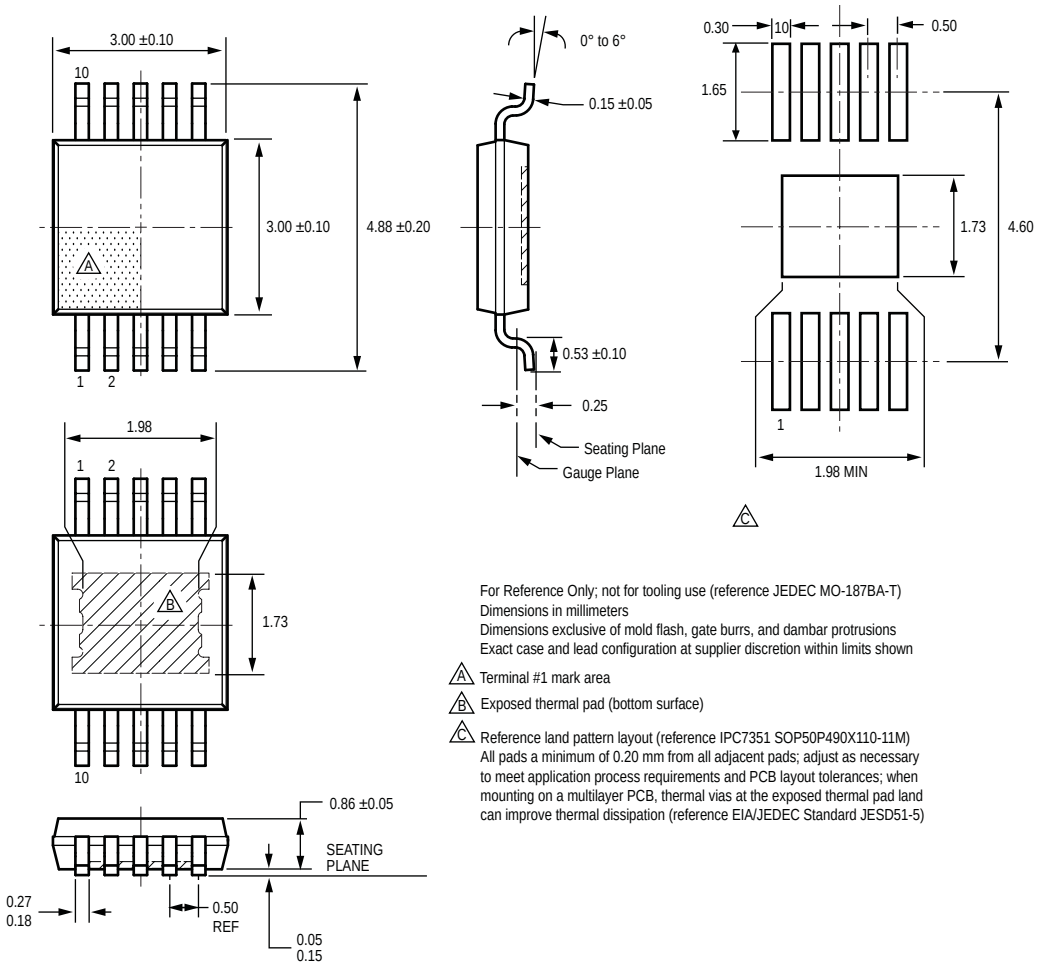
For Reference Only; not for tooling use (reference MO-153 ABT)
Dimensions in millimeters
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown

A Terminal #1 mark area

B Exposed thermal pad (bottom surface); dimensions may vary with device

C Reference land pattern layout (reference IPC7351 SOP65P640X110-17M);
All pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances; when mounting on a multilayer PCB, thermal vias at the exposed thermal pad land can improve thermal dissipation (reference EIA/JEDEC Standard JESD51-5)

Package LY, 10-Pin MSOP with Exposed Thermal Pad



For Reference Only; not for tooling use (reference JEDEC MO-187BA-T)
Dimensions in millimeters
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown

A Terminal #1 mark area

B Exposed thermal pad (bottom surface)

C Reference land pattern layout (reference IPC7351 SOP50P490X110-11M)
All pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances; when mounting on a multilayer PCB, thermal vias at the exposed thermal pad land can improve thermal dissipation (reference EIA/JEDEC Standard JESD51-5)

Revision History

Revision	Revision Date	Description of Revision
Rev. 2	January 18, 2012	Update Features List