CY24293

Two Outputs PCI-Express Clock Generator

Features

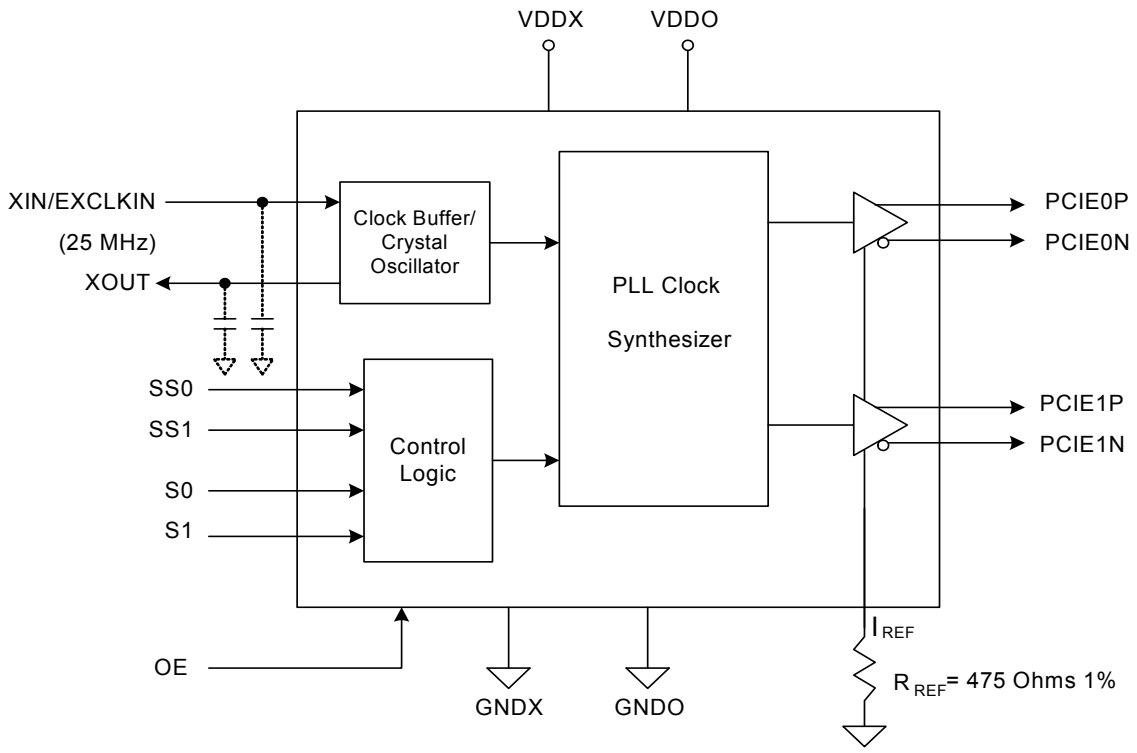
- 25 MHz Crystal or Clock Input
- Two sets of Differential PCI-Express Clocks
- Pin Selectable Output Frequencies
- Supports HCSL or LVDS Compatible Output Levels
- Spread Spectrum Capability on all Output Clocks with Pin Selectable Spread Range
- 16-pin TSSOP Package
- Operating Voltage 3.3V
- Commercial and Industrial Operating Temperature Range

Functional Description

CY24293 is a two output PCI-Express clock generator device intended for networking applications. The device takes 25 MHz crystal or clock input and provides two pairs of differential outputs at 25 MHz, 100 MHz, 125 MHz, or 200 MHz for HCSL, and 25 MHz or 100 MHz for the LVDS signaling standard.

The device incorporates Lexmark Spread Spectrum profile for maximum electromagnetic interference (EMI) reduction. The spread type and amount can be selected using select pins.

Logic Block Diagram



Pinouts

Figure 1. Pin Diagram - CY24293 16-Pin TSSOP

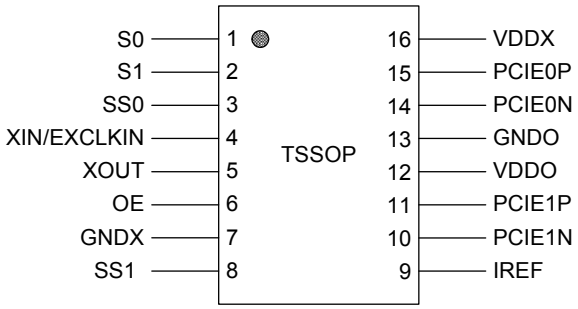


Table 1. Pin Definitions - CY24293 16-Pin TSSOP

Pin Number	Pin Name	Pin Type	Description
1	S0	Input	Frequency select pin. Has internal weak pull up. Refer to Table 2.
2	S1	Input	Frequency select pin. Has internal weak pull up. Refer to Table 2.
3	SS0	Input	Spread Spectrum Select pin 0. Has internal weak pull up. Refer to Table 3.
4	XIN/EXCLKIN	Input	Crystal or clock input. 25 MHz fundamental mode crystal or clock input.
5	XOUT	Output	Crystal output. 25 MHz fundamental mode crystal input. Float for clock input.
6	OE	Input	High true output enable pin. When set low, PCI-E outputs are tri-stated. Has internal weak pull up.
7	GNDX	Power	Ground
8	SS1	Input	Spread Spectrum Select pin 1. Has internal weak pull up. Refer to Table 3.
9	IREF	Output	Current set for all differential clock drivers. Connect 475Ω resistor to ground.
10	PCIE1N	Output	Differential PCI-Express complementary clock output. Tristated when disabled.
11	PCIE1P	Output	Differential PCI-Express true clock output. Tristated when disabled.
12	VDDO	Input	3.3V Power supply for output driver and analog circuits.
13	GNDO	Power	Ground
14	PCIE0N	Output	Differential PCI-Express complementary clock output. Tristated when disabled.
15	PCIE0P	Output	Differential PCI-Express true clock output. Tristated when disabled.
16	VDDX	Input	3.3V Power supply for oscillator and digital circuits.

Table 2. Output Selection Table

S1	S0	PCIE0[N,P], PCIE1[N,P]
0	0	25 MHz
0	1	100 MHz
1	0	125 MHz
1	1	200 MHz

Table 3. Spread Selection Table

SS1	SS0	Spread%
0	0	No Spread
0	1	-0.5%
1	0	-0.75%
1	1	No Spread

Application Information

Crystal Recommendations

CY24293 requires a parallel resonance crystal. Substituting a series resonance crystal causes the CY24293 to operate at the wrong frequency and violate the ppm specification. For most applications, there is a 300 ppm frequency shift between series and parallel crystals due to incorrect loading.

Table 4. Crystal Recommendations

Frequency	Cut	Load Cap	Eff Series Rest (max)	Drive (max)	Tolerance (max)	Stability (max)	Aging (max)
25.00 MHz	Parallel	16 pF	30 Ω	1.0 mW	30 ppm	10 ppm	5 ppm/yr.

Crystal Loading

Crystal loading plays a critical role in achieving low ppm performance. To realize low ppm performance, consider the total capacitance the crystal sees to calculate the appropriate capacitive loading (CL).

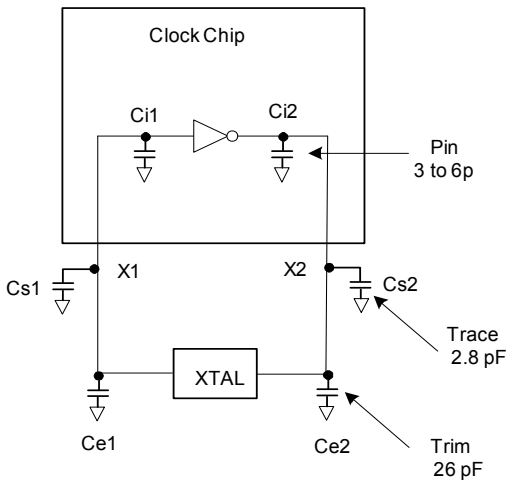
Figure 2 shows a typical crystal configuration using two trim capacitors. It is important to note that the trim capacitors in series with the crystal are not parallel. It is a common misconception that load capacitors are in parallel with the crystal and must be approximately equal to the load capacitance of the crystal. This is not true.

Calculating Load Capacitors

In addition to the standard external trim capacitors, trace capacitance and pin capacitance must also be considered to correctly calculate crystal loading.

As mentioned in the previous section, the capacitance on each side of the crystal is in series with the crystal. This means the total capacitance on each side of the crystal must be twice the specified crystal load capacitance (CL). While the capacitance on each side of the crystal is in series with the crystal, trim capacitors (Ce1, Ce2) must be calculated to provide equal capacitive loading on both sides.

Figure 2. Crystal Loading Example



Use the following formulas to calculate the trim capacitor values for Ce1 and Ce2:

Load capacitance (each side)

$$Ce = 2 * CL - (Cs + Ci)$$

Total capacitance (as seen by the crystal)

$$CLe = \frac{1}{\left(\frac{1}{Ce1 + Cs1 + Ci1} + \frac{1}{Ce2 + Cs2 + Ci2}\right)}$$

CL ..... Crystal load capacitance

CLe ..... Actual loading seen by crystal using standard value trim capacitors

Ce ..... External trim capacitors

Cs ..... Stray capacitance (terraced)

Ci ..... Internal capacitance

Current Source (Iref) Reference Resistor

If the board target trace impedance (Z) is 50Ω, then for R_{REF} = 475Ω (1%), provides IREF of 2.32 mA. The output current (I_{OH}) is equal to 6*IREF.

Output Termination

The PCI-Express differential clock outputs of the CY24293 are open source drivers and require an external series resistor and a resistor to ground. These resistor values and their allowable locations are explained in the section PCI-Express Layout Guidelines on page 4. The CY24293 can also be configured for LVDS compatible voltage levels. Refer to the section LVDS Compatible Layout Guidelines on page 5.

PCB Layout Recommendations

For optimum device performance and the lowest phase noise, the following guidelines must be observed:

1. Each 0.01 µF decoupling capacitor must be mounted on the component side of the board as close to the VDD pin as possible.
2. No vias must be used between the decoupling capacitor and the VDD pin.
3. The PCB trace to the VDD pin and the ground via must be kept as short as possible. Distance of the ferrite bead and bulk decoupling from the device is less critical.
4. An optimum layout is one with all components on the same side of the board, minimizing vias through other signal layers (any ferrite beads and bulk decoupling capacitors can be mounted on the back). Other signal traces must be routed away from the CY24293. This includes signal traces just underneath the device, or on layers adjacent to the ground plane layer used by the device.

Decoupling Capacitors

The decoupling capacitors of 0.01 µF must be connected between VDD and GND as close to the device as possible. Do not share ground vias between components. Route power from the power source through the capacitor pad and then into the CY24293 pin.

PCI-Express Layout Guidelines

HCSL Compatible Layout Guidelines

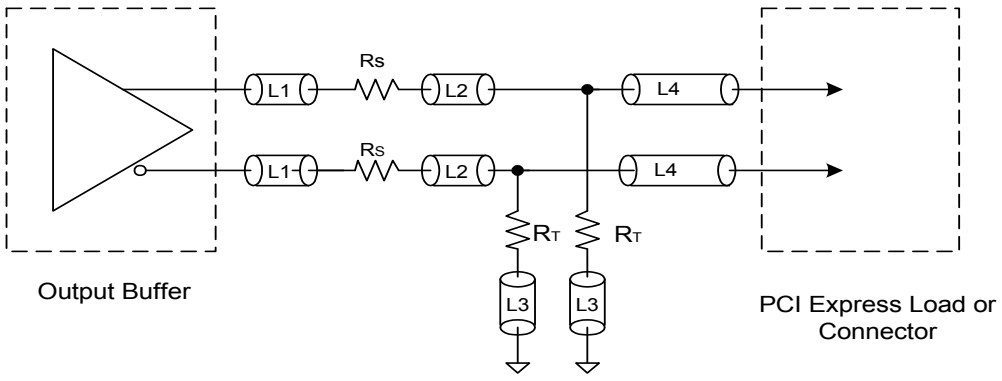
Table 5. Common Recommendations for Differential Routing

Differential Routing[1]	Dimension or Value	Unit
L1 length, route as non-coupled 50Ω trace	0.5 max	inch
L2 length, route as non-coupled 50Ω trace	0.2 max	inch
L3 length, route as non-coupled 50Ω trace	0.2 max	inch
R_S	33	Ω
R_T	49.9	Ω

Table 6. Differential Routing for PCI-Express Load or Connector

Differential Routing[1]	Dimension or Value	Unit
L4 length, route as coupled microstrip 100Ω differential trace	2 to 32	inch
L4 length, route as coupled stripline 100Ω differential trace	1.8 to 30	inch

Figure 3. PCI-Express Device Routing



Note
1. Refer to Figure 3.

LVDS Compatible Layout Guidelines

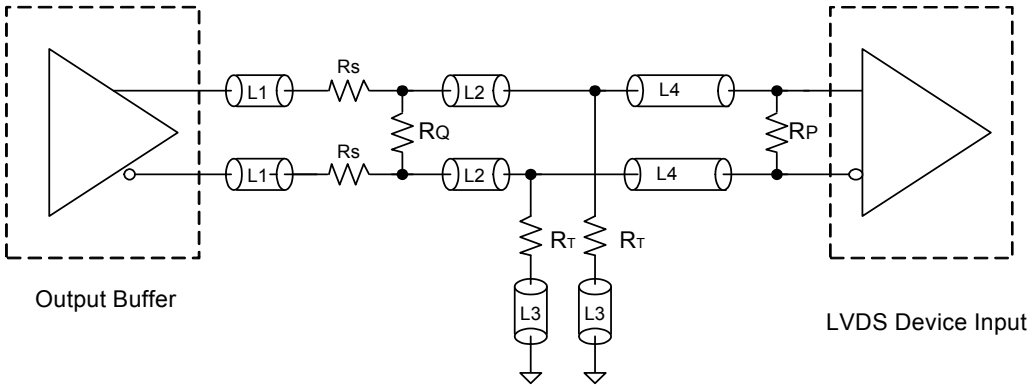
Table 7. Common Recommendations for Differential Routing

Differential Routing[2]	Dimension or Value	Unit
L1 length, route as noncoupled 50Ω trace	0.5 max	inch
L2 length, route as noncoupled 50Ω trace	0.2 max	inch
L3 length, route as noncoupled 50Ω trace	0.2 max	inch
R_P	100	Ω
R_Q	150	Ω
R_S	33	Ω
R_T	49.9	Ω

Table 8. LVDS Device Differential Routing

Differential Routing[2]	Dimension or Value	Unit
L4 length, route as coupled microstrip 100Ω differential trace	2 to 32	inch
L4 length, route as coupled stripline 100Ω differential trace	1.8 to 30	inch

Figure 4. LVDS Device Routing



Note
2. Refer to Figure 4.

Absolute Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Table 9. Absolute Maximum Ratings

Parameter	Description	Condition	Min	Max	Unit
V_{DD}	Supply voltage		–0.5	4.6	V
V_{IN}	Input voltage	Relative to V_{SS}	–0.5	V_{DD}+0.5	V
T_S	Temperature, Storage	Non Functional	–65	+150	°C
T_J	Temperature, Junction	Non Functional	–65	+150	°C
ESD_{HBM}	ESD Protection (Human Body Model)	JEDEC EIA/JESD22-A114-E	2000	–	V
UL-94	Flammability rating		V-0 at 1/8 in.		
MSL	Moisture sensitivity level		3		

Recommended Operation Conditions

Parameter	Description	Min	Typ	Max	Unit
V_{DD}	Supply voltage	3.0	–	3.6	V
T_{AC}	Commercial ambient temperature	0	–	+70	°C
T_{AI}	Industrial ambient temperature	–40	–	+85	°C
t_{PU}	Power up time for all V_{DD} to reach minimum specified voltage (power ramps must be monotonic)	0.05	–	500	ms

DC Electrical Characteristics

Unless otherwise stated, VDD = 3.3V ±0.3V, ambient temperature = -40°C to +85°C Industrial, 0°C to +70°C Commercial

Parameter[3]	Description	Condition	Min	Typ	Max	Unit
V_{IL}	Input low voltage		-0.3	–	0.8	V
V_{IH}	Input high voltage		2.0	–	V_{DD}+0.3	V
V_{OL}	Output low voltage of PCIE0[P/N], PCIE1[P/N]	HCSL termination (R_S = 33Ω, R_T = 49.9Ω)	-0.2	0	0.05	V
V_{OH}	Output high voltage of PCIE0[P/N], PCIE1[P/N]	HCSL termination (R_S = 33Ω, R_T = 49.9Ω)	0.65	0.71	0.85	V
I_{DD}	Operating supply current	No load, OE = 1	–	45	60	mA
I_{DDOD}	Output disabled current	OE = 0	–	–	50	mA
C_{IN}	Input capacitance	All input pins	–	5	–	pF
R_{PU}	Pull up resistance	S0, S1, SS0, SS1, OE	–	70k	–	Ω

Note
3. Parameters are guaranteed by design and characterization. Not 100% tested in production

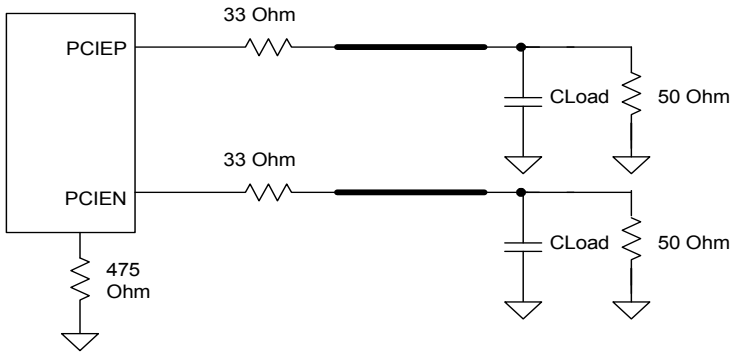
AC Electrical Characteristics

Unless otherwise stated: VDD = 3.3V ±0.3V, ambient temperature = -40°C to +85°C Industrial, 0°C to +70°C Commercial, Outputs HCSL terminated.

Parameter[3]	Description	Condition	Min	Typ	Max	Unit
F_{IN}	Input clock frequency (crystal or external clock)		–	25	–	MHz
F_{OUT}	Output frequency	HCSL Termination	–	–	200	MHz
		LVDS Termination	–	–	100	MHz
F_{ERR}	Frequency synthesis error		–	0	–	ppm
T_{CCJ}	Cycle-to-cycle jitter[4]		–	–	75	ps
SP_{MOD}	Spread modulation frequency		–	32	–	kHz
T_{DC}	Output clock duty cycle[4,6]		45	50	55	%
T_{OEH}	Output enable time	OE going high to differential outputs becoming valid	–	–	200	ns
T_{OEL}	Output disable time	OE going low to differential outputs becoming invalid	–	–	200	ns
T_{LOCK}	Clock stabilization from power up	Measured from 90% of the applied power supply level	–	1	2	ms
T_R	Output rise time[4,5]	Measured from 0.175V to 0.525V	130	–	700	ps
T_F	Output fall time[4,5]	Measured from 0.525V to 0.175V	130	–	700	ps
DT_R	Rise time variation[4,5]	For a given frequency, Max(T_R) - Min (T_R)	–	–	125	ps
DT_F	Fall time variation[4,5]	For a given frequency, Max(T_F) - Min (T_F)	–	–	125	ps
T_{OSKEW}	Output skew[6]	Measured at V_{CROSS} point	–	–	50	ps
V_{CROSS}	Absolute crossing point voltage[6,7]		0.25	0.35	0.55	V
V_{Xdelta}	Variation of V_{CROSS} over all clock edges[6,8]		–	–	140	mV

Test and Measurement Setup

Figure 5. Test Load Configuration for Differential Output Signals



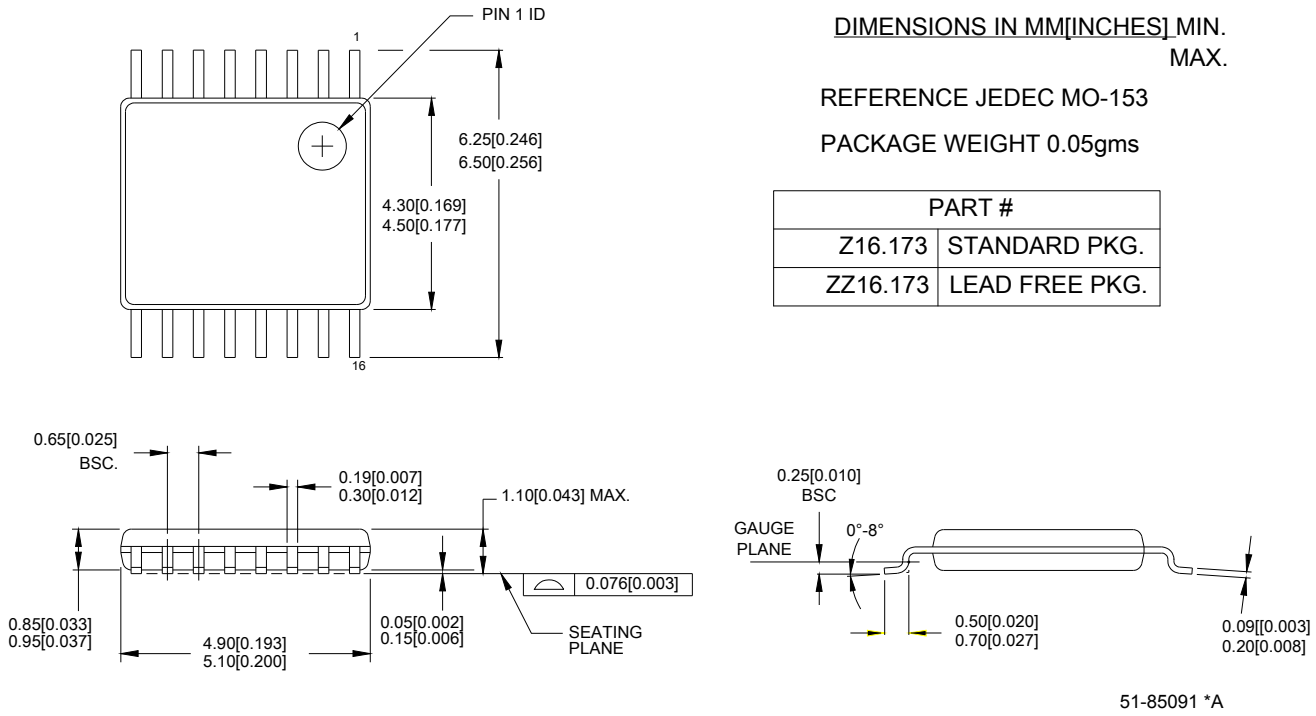
Notes
4. Measured with Cload = 4 pF max. (scope probe + trace load)
5. Measurement taken from a differential waveform.
6. Measured at crossing point where the instantaneous voltage value of the rising edge of PCIEP equals the falling edge of PCIEN.
7. Refers to the total variation from the lowest crossing point to the highest, regardless of which edge is crossing. Refers to all crossing points for this measurement.
8. Refers to the difference between the PCIEP rising edge V_{CROSS} average value and the PCIEN rising edge V_{CROSS} average value.

Ordering Information

Part Number	Type	Production Flow
Pb-free		
CY24293ZXC	16-pin TSSOP	Commercial, 0°C to 70°C
CY24293ZXCT	16-pin TSSOP tape & reel	Commercial, 0°C to 70°C
CY24293ZXI	16-pin TSSOP	Industrial, -40°C to 85°C
CY24293ZXIT	16-pin TSSOP tape & reel	Industrial, -40°C to 85°C

Package Dimensions

Figure 6. 16-Pin TSSOP 4.40 mm Body Package



Document History Page

Document Title: CY24293 Two Outputs PCI-Express Clock Generator Document Number: 001-46117				
REV.	**ECN NO.**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	2490167	PYG/DPF/AESA	See ECN	New Data Sheet
*A	2507681	DPF/AESA	05/23/2008	Added Note 1: Parameters are guaranteed by design and characterization. Not 100% tested in production. Added Note 2 for Duty cycle spec in the AC Elect. Characteristics. Added HCSL termination in Condition for V_{OL}, V_{OH} DC Elect. Char. Added V_{Xdelta} value of 140 mV in the Differential 100 MHz HCSL output. Changed Cload from 2 pF to 4 pF in Note 2. Added internal weak Pull ups for S0, S1, SS0, SS1 and OE pins. Updated T_{OEH} and T_{OEL} to 200 ns (max.). Updated data sheet template
*B	2621901	CXQ/AESA	12/19/2008	Updated I_{DD} spec in DC Electrical Characteristics. Added max spec for I_{DDOD} DC Electrical Characteristics. Added R_{PU} in DC Electrical Characteristics. Replaced T_{RFVAR} with DT_R and DT_F in AC Electrical Characteristics. Added definitions for rise and fall time variation, crossing point variation in AC Electrical Characteristics. Reduced cycle-to-cycle jitter spec to 75ps in AC Electrical Characteristics.
*C	2683343	CXQ/PYRS	04/03/2009	Removed “Preliminary” from datasheet title and headings Added “max” to crystal ESR spec. Changed “LVDS Down Device” to “LVDS Device” in Table 8 and Figure 4.

Sales, Solutions, and Legal Information

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