F85226AF

LPC to ISA Bridge

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F85226AF Datasheet Revision History

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V0.20P	2008/7/24	-	Release Version

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1. General Description

The F85226AF is a LPC to ISA Bridge IC for new generation chipset which is no support for ISA bus and slots. However the demand of ISA devices still exists. Therefore LPC to ISA Bridge IC is necessary to be used for new chipset system. The F85226AF is the best selection even though there is the PCI to ISA Bridge for supporting ISA device, because the issue of package size is critical for layout requirement. Follows the point at these issues, the F85226AF is optimal solution for the non-ISA chipset, the package of F85226AF will be the best chosen for economic solution and save the layout size of Motherboard.

The F85226AF absolutely meets LPC spec. 1.1 and supports fully ISA interface. Provides multi-ISA compatible slots without buffering and supports ISA parallel IRQ transfer to serial IRQ by IRQ Serialier. The F85226AF also provides programmable general purpose I/O pins for user. It is completely LPC to ISA bridge specialized chip.

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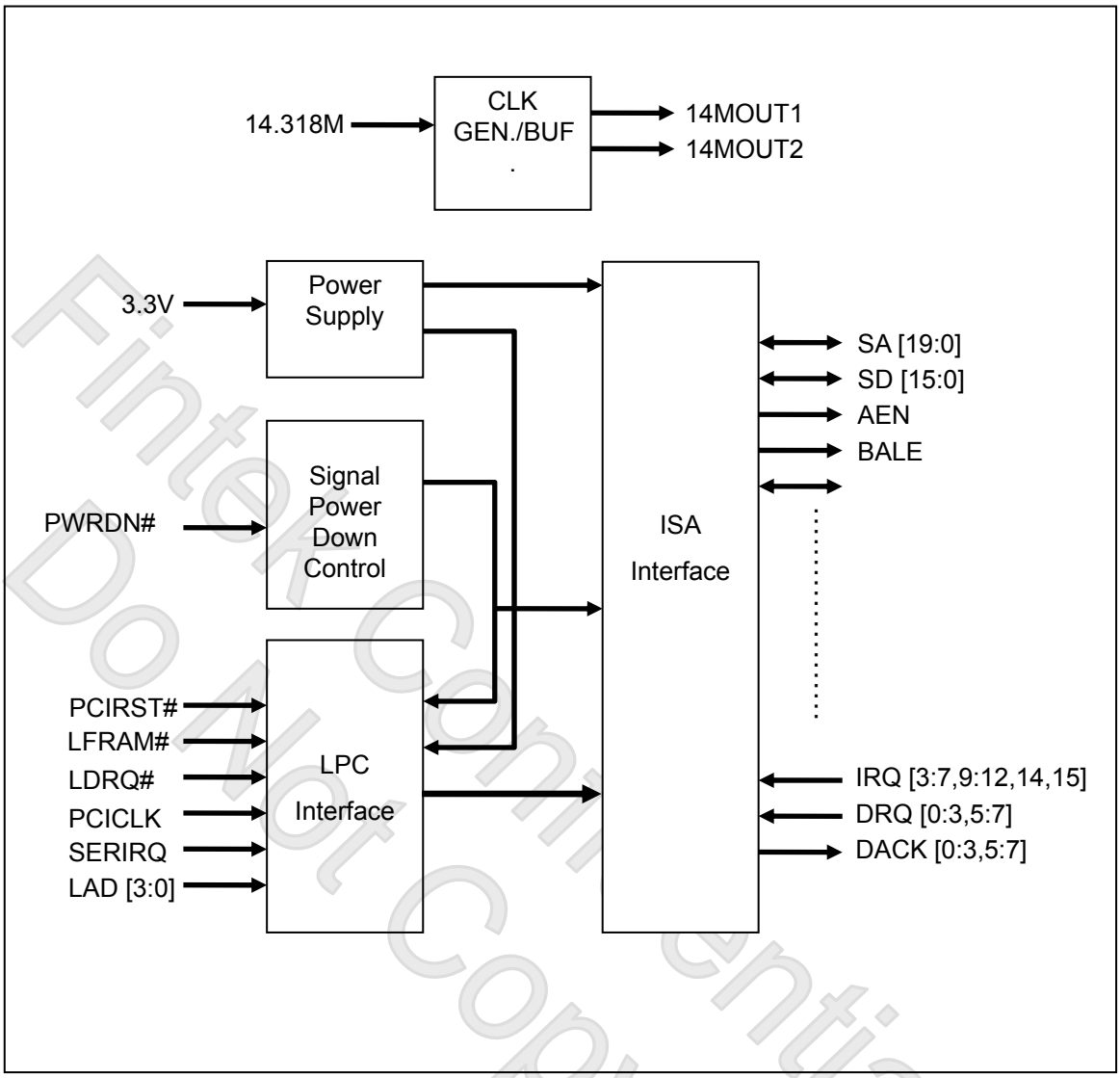
2. Features

- Meets LPC spec. 1.1
- Supports LDRQ#(LPC DMA), SERIRQ(Serial IRQ)
- Fully ISA bridge support except bus master(By conditions)
- Supports 8/16bit I/O and memory R/W
- All software transparent
- All ISA signals can be isolate
- ISA parallel IRQ transfer to serial IRQ by IRQ Serialier
- Supports multi-slots without buffering
- Supports the PCI clock to divide by 3 or 4 for ISA bus
- Supports to generate two 14.318MHz buffer out from one 14.318MHz in
- 4 sets of address decoder supported
- Supports programmable general purpose I/O pins
- Powered by 3Vcc (Signal 5V tolerance)
- 128pin PQFP package

3. Key Specifications

- Supply Voltage 3.0v to 3.6v
- Operating Supply current 4mA typ.

4. Block Diagram



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5. Pin Configuration

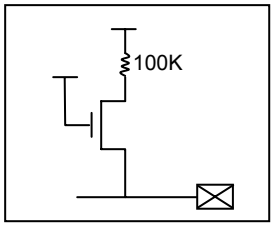
6. Pin Descriptions

I/O_{24ts} - TTL level bi-directional pin and Schmitt trigger with 24 mA source-sink capability.

I/OD_{24ts_u100k} - TTL level input pin and Schmitt trigger, Open-drain output with 24 mA sink capability, internal pull-up 100KΩ connected with 3.3V to protect electric leakage.

I/O_{24ts_u100k} - TTL level input pin and Schmitt trigger, Output pin with 24 mA sink capability, internal pull-up 100KΩ connected with 3.3V to protect electric leakage.

O_{24_u100k} - Output pin with 24 mA source-sink capability, internal pull-up 100KΩ connected with 3.3V to protect electric leakage.



O_{24} - Output pin with 24 mA source-sink capability.

O_{20} - Output pin with 20 mA source-sink capability.

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IN_t - TTL level input pin.

IN_{ts} - TTL level input pin and schmitt trigger.

P - Power.

6.1 Power Pin

Pin No.	Pin Name	Type	Description
5, 20, 25, 45, 55, 70, 85, 105, 120	VDD3V	P	Standard Power Supply Voltage Input with 3.3V.
15, 30, 50, 60, 80, 95, 110, 125	GND	P	Ground.

6.2 Power on strapping signal

Pin No	Pin Name	Type	PWR	Description
36	80PCS#/KBEN#	I/OD_{24ts_u100k} (5V-tolerance)	VDD3v	Power-on strapping with external pulled-down resistor 10k will enable K/B and mouse functions. When it is set, pin 38, 39 and 40 will execute IRQ1, KBCS# and MCCS# signals.
37	ROMCS#/ROM_EN	I/O_{24ts} (5V-tolerance)	VDD3v	Power-on strapping without internal resister, need external pulled-up resistor to enable CR03h (BIOS_ROM_EN bit) If there is a boot-ROM (BIOS). Else if without boot-ROM, please use external pulled-down 10K resister to disable this BIOS_ROM_EN.
126	DACK7#/RTCEN#	I/O_{24ts_u100k} (5V-tolerance)	VDD3v	Power-on strapping with external pulled-down 10k resistor will enable RTC functions. When it is set, pin 64 and 65 will do IRQ8 and RTCCS# signals.
128	DACK6#/HEFRAS	I/O_{24ts_u100k} (5V-tolerance)	VDD3v	Set this function will change the port that is used to access configuration registers. Default setting is 4Eh, but by power-on strapping with a external pulled-down 10k resister change to 2Eh.
2	DACK5#/EN_GP2X	I/O_{24ts_u100k} (5V-tolerance)	VDD3v	Power-on strapping with external pulled-down 10k resistor. Then it will disable LA [19:17] function and pin108~pin111, pin29 use as GPIO2X function.

6.3 LPC interface

Pin No.	Pin Name	Type	PWR	Description
16-19	LAD[3:0]	I/O_{24ts}	VDD3v	Multiplexed command, address bi-directional data and cycle status. Through the LPC bus between a host and a peripheral.
13	LFRAME#	IN_{ts}	VDD3v	Low pulse indicates start of a new cycle or termination of broken cycle.
21	PCICLK	IN_t	VDD3v	PCI clock used for the LPC bus. Same 33MHz clock as PCI clock on the host. Same clock phase with typical PCI skew.

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14	PCIRST#	IN_{ts}	VDD3v	PCI system reset used for the LPC bus. The Reset signal line can be connected to PCIRST# signal on the host.
23	SERIRQ	I/O_{24ts}	VDD3v	Serial IRQ Input/Output.
22	LDRQ#	O_{24}	VDD3v	Encoded DMA Request signal.
24	PWRDN#	IN_{ts}	VDD3v	Power Down. The signal is active low according to CR 44 Bit 7and wake-up enable by hardware setting. There are eight different power-down states (Power down Mode 3).

6.4 ISA interface

Pin No.	Pin Name	Type	PWR	Description
58-56	SA[19:17]	I/O_{24ts_u100k} (5V-tolerance)	VDD3v	System Address Bus. These are the upper addresses that define the ISA's byte address space (up to 1 M byte). The SA [19:17] are at tri-states during PCIRST#.
54-51 49-46 44-41 35-31	SA[16:0]	I/O_{24ts_u100k} (5V-tolerance)	VDD3v	System Address Bus. These define the ISA's byte address space (up to 128K byte). The SD [16:0] are at tri-states during PCIRST#.
122-121 119-114 75-71 69-67	SD[15:0]	I/O_{24ts_u100k} (5V-tolerance)	VDD3v	System Data Bus. These provide 16-bit data for devices to reside on the ISA Bus. The SD [15:0] are at tri-states during PCIRST#.
59	AEN	O_{24} (5V-tolerance)	VDD3v	Address Enable. AEN is asserted during DMA cycles, driven high during F85226AF initiated refresh cycles, driven low upon PCIRST#.
86	IOR#	I/O_{24ts_u100k} (5V-tolerance)	VDD3v	I/O Read. IOR# is asserted to request an ISA I/O slave to drive data onto the data bus.
84	IOW#	I/O_{24ts_u100k} (5V-tolerance)	VDD3v	I/O Write. IOW# is asserted to request an ISA I/O slave to accept data from the data bus.
61	IOCHRDY	I/O_{24ts} (5V-tolerance)	VDD3v	I/O Channel Ready. IOCHDRY asserted indicates that an ISA slave requires additional wait states. When the F85226AF is an ISA slave, IOCHRDY is an output indicating additional wait states are required.
92	SYSCLK	O_{24}	VDD3v	ISA System Clock. SYSCLK offers the reference clock to the ISA bus. The frequency is generated from dividing PCICLK by 3 or 4 (select by CR06 bit7).
77	RSTDRV	O_{24}	VDD3v	Reset Drive. RSTDRV asserted indicates to reset devices that reside on the ISA Bus while the PCIRST# has been asserted.

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11	IOCS16#	I/O_{24ts} (5V-tolerance)	VDD3v	16-bit I/O Chip Select. IOCS16# is asserted by 16-bit ISA I/O devices to indicate that they support 16-bit I/O bus cycles.
12	MEMCS16#	I/O_{24ts} (5V-tolerance)	VDD3v	Memory Chip Select 16. MEMCS16# is asserted by 16-bit ISA memory devices to indicate that the memory slave supports 16-bit accesses.
76	IOCHCK#	IN_{ts} (5V-tolerance)	VDD3v	I/O Channel Check. Asserted by an ISA device indicating an error condition.
81	OWS#	IN_{ts} (5V-tolerance)	VDD3v	Zero Wait States. An ISA slave asserts ZEROWS# after its address and command signals have been decoded to indicate that the current cycle can be executed as an ISA zero wait state cycle. ZEROWS# has no effect during 16-bit I/O cycles.
103-104 106-107	LA[23:20]	I/O_{24ts_u100k} (5V-tolerance)	VDD3v	Unlatched Address. The LA [23:20] address lines are bi-directional. These address lines allow accesses to physical memory on the ISA Bus up to 16 Mbytes. LA [23:20] are outputs when the F85226AF owns the ISA Bus.
108-109 111	LA[19:17]	I/O_{24ts_u100k} (5V-tolerance)	VDD3v	Unlatched Address. The LA [19:17] address lines are bi-directional. These address lines allow accesses to physical memory on the ISA Bus up to 16 Mbytes. LA [19:17] are outputs when the F85226AF owns the ISA Bus.
	GP23, GP22, GP21			General purpose I/O pin.
82	SMEMW#	O_{24} (5V-tolerance)	VDD3v	Standard (system) Memory Write. SMEMW# is asserted for memory write accesses below 1MB.
83	SMEMR#	O_{24} (5V-tolerance)	VDD3v	Standard (system) Memory Read. SMEMR# is asserted for memory read accesses below 1 MB.
91	REFRESH#	O_{24_u100k} (5V-tolerance)	VDD3v	Refresh Cycle indicator. REFRESH# asserted indicates that a refresh cycle is in progress, or ISA master requests F85226AF to generate a refresh cycle. The signal is at tri-stated upon PCIRST#.
101	BALE	I/O_{24ts_u100k} (5V-tolerance)	VDD3v	Bus Address Latch Enable. BALE asserted indicates when the address (SA[19:0], LA[23:17]) and SBHE# are valid. The LA [23:17] address lines are latched on the trailing edge of BALE. BALE is driven by low upon PCIRST#.
102	SBHE#	I/O_{24ts_u100k} (5V-tolerance)	VDD3v	System Byte High Enable. SBHE# asserted indicates that SD[15:8] will be used to transfer a byte. SBHE# is at an unknown state upon PCIRST#.
112	MEMR#	I/O_{24ts_u100k} (5V-tolerance)	VDD3v	Memory Read. MEMR# asserted indicates the current ISA bus cycle is a memory read.
113	MEMW#	I/O_{24ts_u100k} (5V-tolerance)	VDD3v	Memory Write. MEMW# asserted indicates the current ISA bus cycle is a memory write.

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123	MASTER#	IN_{ts} (5V-tolerance)	VDD3v	The MASTER# input asserted indicates an ISA bus master is driving the ISA bus. This signal is executed with DREQ line by an ISA master to gain control of the ISA Bus.
98	IRQ3	IN_{ts} (5V-tolerance)	VDD3v	Parallel Interrupt Requested Input 3.
97	IRQ4	IN_{ts} (5V-tolerance)	VDD3v	Parallel Interrupt Requested Input 4.
96	IRQ5	IN_{ts} (5V-tolerance)	VDD3v	Parallel Interrupt Requested Input 5.
94	IRQ6	IN_{ts} (5V-tolerance)	VDD3v	Parallel Interrupt Requested Input 6.
93	IRQ7	IN_{ts} (5V-tolerance)	VDD3v	Parallel Interrupt Requested Input 7.
78	IRQ9	IN_{ts} (5V-tolerance)	VDD3v	Parallel Interrupt Requested Input 9.
10	IRQ10	IN_{ts} (5V-tolerance)	VDD3v	Parallel Interrupt Requested Input 10.
9	IRQ11	IN_{ts} (5V-tolerance)	VDD3v	Parallel Interrupt Requested Input 11.
8	IRQ12	IN_{ts} (5V-tolerance)	VDD3v	Parallel Interrupt Requested Input 12.
6	IRQ14	IN_{ts} (5V-tolerance)	VDD3v	Parallel Interrupt Requested Input 14.
7	IRQ15	IN_{ts} (5V-tolerance)	VDD3v	Parallel Interrupt Requested Input 15.
3	DRQ0	IN_{ts} (5V-tolerance)	VDD3v	DMA Request input 0. The DREQ asserted indicates that either a slave DMA device is requesting DMA services or an ISA bus master is requesting to use the ISA bus.
90	DRQ1	IN_{ts} (5V-tolerance)	VDD3v	DMA Request input 1.
79	DRQ2	IN_{ts} (5V-tolerance)	VDD3v	DMA Request input 2.
88	DRQ3	IN_{ts} (5V-tolerance)	VDD3v	DMA Request input 3.
1	DRQ5	IN_{ts} (5V-tolerance)	VDD3v	DMA Request input 5.

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127	DRQ6	IN_{ts} (5V-tolerance)	VDD3v	DMA Request input 6.
124	DRQ7	IN_{ts} (5V-tolerance)	VDD3v	DMA Request input 7.
4	DACK0#	O_{24} (5V-tolerance)	VDD3v	DMA Acknowledge channel 0. The DACK# outputs asserted indicates that either a DMA channel or an ISA bus master has been granted the ISA bus.
89	DACK1#	O_{24} (5V-tolerance)	VDD3v	DMA Acknowledge channel 1.
99	DACK2#	O_{24} (5V-tolerance)	VDD3v	DMA Acknowledge channel 2.
87	DACK3#	O_{24} (5V-tolerance)	VDD3v	DMA Acknowledge channel 3.
2	DACK5# EN_GP2X	I/O_{24ts_u100k} (5V-tolerance)	VDD3v	DMA Acknowledge channel 5. During power-on strapping with external pulled-down 10k resistor. Then it will disable LA [19:17] function and pin108~pin111, pin29 use as GPIO2X function.
128	DACK6# HERFRA	I/O_{24ts_u100k} (5V-tolerance)	VDD3v	DMA Acknowledge channel 6. During power-on reset, this pin is pulled-up internally(Select 4Eh) ,and is defined as HEFRAS which provides the power-on value for CR3 bit4 .A 10k ohm is recommended if intends to pull down .(Select 2Eh)
126	DACK7# RTCEN#	I/O_{24ts_u100k} (5V-tolerance)	VDD3v	DMA Acknowledge channel 7. RTC Function Enable. The pin applies a pull-down resistor (4.7K ohm) to enable RTC functions (RTCCS#, and IRQ8)
100	TC	O_{24} (5V-tolerance)	VDD3v	Terminal Count. TC signals the final data transfer of a DMA transfer.
36	80PCS# KBEN#	I/OD_{24ts_u100k} (5V-tolerance)	VDD3v	80h PORT Chip Select.(Default) Only decode IO address port 80h and must apply with IOW#. K/B Functions Enable. During power-on reset this pin is weak pulled-up internally. The pin applied a pull-down resistor (10K ohm) to enable K/B functions. (IRQ1,KBCS#,and MCCS#)
37	ROMCS#	I/O_{24ts} (5V-tolerance)	VDD3v	ROMCS#, this pin enable positive decoder of BIOS address range.

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	ROM_EN			Power-on strapping with internal pulled-up resistor will enable CR03h (BIOS_ROM_EN, BIOS_WR_EN bit). If there is a boot-ROM (BIOS), else if without boot-ROM, please use external pulled-down 10K resister to disable this ROM_EN and WR_EN.
38	GPIO0 IRQ1	I/O_{24ts} (5V-tolerance)	VDD3v	General purpose I/O pin 0. Parallel Interrupt Requested Input 1. This pin is used for specific K/B functions.
39	GPIO1 KBCS#	I/O_{24t} (5V-tolerance)	VDD3v	General purpose I/O pin 1. Decode address 60h and 64h to generate chip selected signal. Enable by KBEN# power-on setting.
40	GPIO2 MCCS#	I/O_{24ts} (5V-tolerance)	VDD3v	General purpose I/O pin 2. Decode address 62h and 66h to generate chip selected signal. Enable by KBEN# power-on setting.
62	GPIO3 IRQIN	I/O_{24ts} (5V-tolerance)	VDD3v	General purpose I/O pin 3. It is programmable to transfer parallel IRQ input to serial IRQ, Enable by KBEN# power-on setting.
63	GPIO4 PLED	I/O_{24ts} (5V-tolerance)	VDD3v	General purpose I/O pin 4. Power LED output, the signal is at low state after system reset.
64	GPIO5 IRQ8	I/O_{24ts} (5V-tolerance)	VDD3v	General purpose I/O pin 5. Parallel Interrupt Requested Input 8. This interrupt request is used for specific RTC functions. Enable by RTCEN# power-on setting.
65	GPIO6 RTCCS#	I/O_{24ts} (5V-tolerance)	VDD3v	General purpose I/O pin 6. Decode address 70h and 71h to generate chip selected signal. Enable by RTCEN# power-on setting.
66	GPIO7 IOHCS#	I/O_{24ts} (5V-tolerance)	VDD3v	General purpose I/O pin 7. Decode SA [15-11] all are at “0” state initially and setting by CR04 Bit 7.
26	14.318M	IN_{ts} (5V-tolerance)	VDD3v	14.318 MHz Clock Input.
27	14MOUT 1	O_{20}	VDD3v	14.318 MHz Buffer Output 1.
28	14MOUT 2	O_{20}	VDD3v	14.318 MHz Buffer Output 2.
29	GP20 PLED	I/O_{24ts} (5V-tolerance)	VDD3v	General purpose I/O pin. Power LED output, the signal is at low state after system reset.

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7. Function Description

7.1 LPC interface:

The F85226AF implemented full functions that described in the LPC I/F 1.1 specification and transfers all subtractive cycles from LPC bus to ISA interface for more ISA compatibility. The F85226AF built in 16-bit IO/ Memory enhances transaction. Peripheral or Master devices can assert cycles that are not defined in positive decode ranges of LPC Interface. All LPC bus signals use PCI electrical characteristics. The following cycle types are supported by F85226AF.

- IO read write (8 / 16 bit)
- Memory read write (8 / 16 bit)
- DMA read write (8/ 16 / 32 bit)
- Firmware memory read write (only support size 8 or 16 bit).

eCycles:

S: Start Cycle

C: Command Type Cycle

Cycle Types	Encoding	Remark
IO Read	S: 0x0h; C: 0x0h	Size: 8 bit and 16 bit in Enhanced mode, for LPC peripheral.
IO Write	S: 0x0h; C: 0x2h	Size: 8 bit and 16 bit in Enhanced mode, for LPC peripheral.
Memory Read	S: 0x0h; C: 0x4h	Size: 8 bit and 16 bit in Enhanced mode, for LPC peripheral and host.
Memory Write	S: 0x0h; C: 0x6h	Size: 8 bit and 16 bit in Enhanced mode, for LPC peripheral and host.
DMA Read	S: 0x0h; C: 0x8h	Size: 8, 16 and 32 bit, for LPC peripheral.
DMA Write	S: 0x0h; C: 0xAh	Size: 8, 16 and 32 bit, for LPC peripheral.
Booting Memory Read	S: 0xDh;	Size: 8, 16, 32 and 1024 bit, for LPC peripheral.
Booting Memory Write	S: 0xEh;	Size: 8, 16, and 32 bit, for LPC peripheral.

Start:

The cycle indicates the beginning or abort of a transaction. When LFRAME# is asserted low and monitors LAD[3:0] that determine frame type to enter a valid Start.

Cycle Type and Direction:

LPC host will issue the transaction cycle and direction by LAD[3:1] and LAD0 is always ignored.

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Size:

LPC host on DMA or bus master on memory transaction issue data size that will be transferred by LAD[1:0] and LAD[3:2] must be driven 0x00b.

Turn-Around:

LPC host or peripheral will issue two clock wide cycles after turning control over to peripheral or turning back from peripheral to host. LAD[3:0] should be driven to high level on first cycle and release to tri-state on next one.

Address:

While doing IO transaction, this duration is four clock wide that indicates 16-bit address, on Memory cycles there are eight clocks that indicates 32-bit address will be asserted by LPC host or Master. The duration is not asserted on DMA transaction.

Channel and Terminal count:

Only on DMA transferring, LAD[2:0] signals indicate granted channel in one clock cycle. LAD[3] indicates Terminal count down.

Data:

Each frame can carry one byte (8 bit), first nibble is Data[7;4] and next is Data[3:0].

SYNC:

LPC host or peripheral can add wait state, response error and ready to accept a frame by LAD[3:0].

0x0h: Ready
0x5h: Short Wait, maximum number of SYNC is 8 clocks.
0x6h: Long Wait, no maximum number.
0x9h: Ready More on DMA transaction.
0xAh: Error, it relates to IOCHK# on ISA interface.
Others: Reserved.
STA : Start Cycle
CT : Cycle Type and Direction
H_TAR: Host Turn-Around
P_TAR: Peripheral Turn-Around

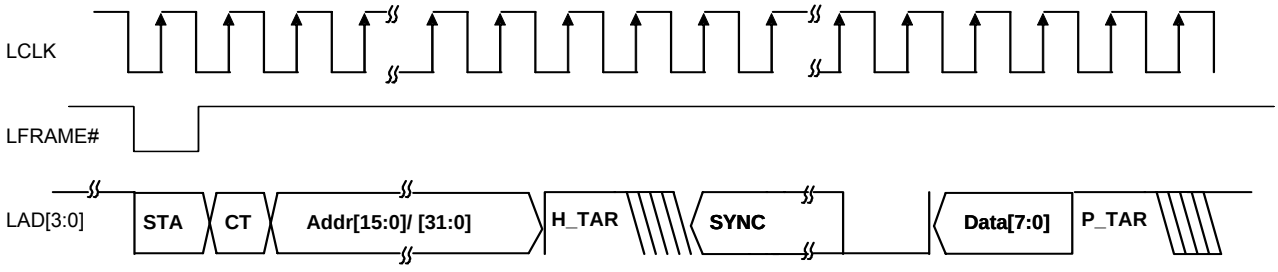

Figure: Read Cycles

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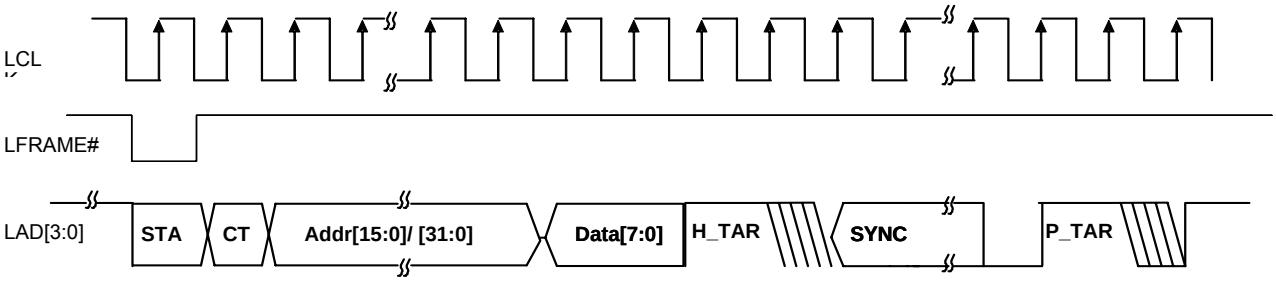

Figure: Write Cycles

7.1.1 IO/Memory Read and Write Cycles

When LPC interface Bridge issues IO cycles that meet subtractive decode, F85226AF will assert corresponded IOR#, IOW# , MEMR# ,SMEMR# , MEMW# and SMEMW# then respond by inserting wait cycles (long wait SYNC). After finishing ISA transaction and there isn't any valid ISA Wait state inserted, it responds Ready-state and terminates the cycles. If the host issues 16 bit transfer, F85226AF will active enhance 16-bit transferring function automatically.

7.1.2 DMA Read and Write Cycles

The read transactions transfer data from main memory to peripheral and write cycles transfer data from peripheral to main memory. DMA requests form ISA interface are delivered by LDRQ# to DMA controller (like 8237) and the acknowledge responds from LAD [3:0] encoding message. Terminal count is depended on the counter programmed in DMA controller, when reach the counter threshold, TC is related to LAD3 and asserted when DMA controller plan to terminal DMA transaction.

7.1.3 Booting Memory Read and Write Cycles

The ISA interface of F85226AF can communicate to ISA ROM (System BIOS) with ROMCS#, MEMER# and MEMW#, BIOS booting cycles of PC system may assert through different cycle type (like Memory Read and Firmware Memory Read) , F85226AF can perform a positive decoder on specified memory range included legacy BIOS , extended legacy BIOS and user defined High Memory address.

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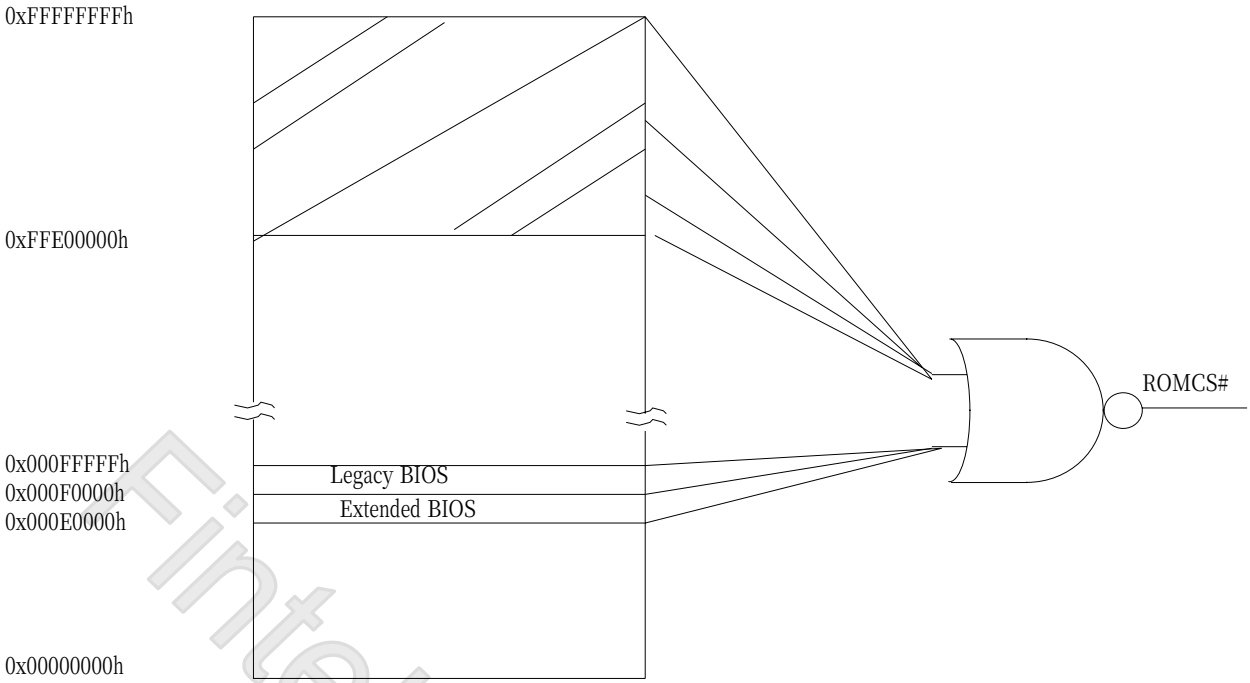


Figure: Chip Select of BIOS Memory

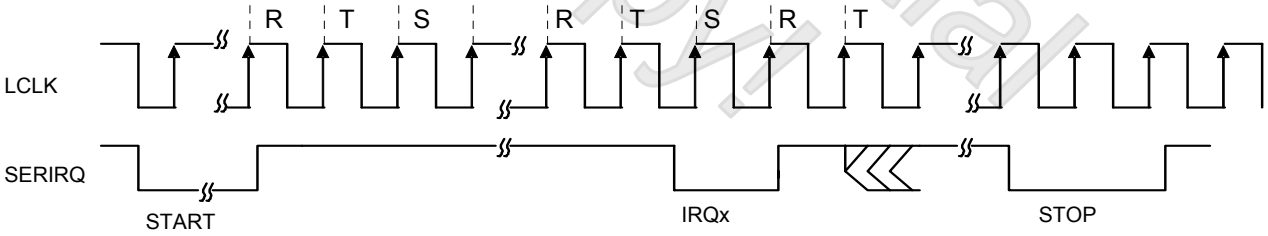
7.2 Serialized Interrupt

Serial Interrupt is a single bus that transmits parallel legacy interrupts and encodes suitable packet at corresponded moment. The signal refers to LCLK and it operates on an open-drain bus (multi-drop bus) that is shared with other devices. F85226AF supports two operation types included Continuous and Quiet mode. Eventually, it fully meets SERIRQ specification Version 6.0.

R: Recovery Phase, SERIRQ signal is driven to high level

T: Turn-Around Phase, Devices Tri-state SERIRQ,

S: Sampling Phase, SERIRQ signal is sink to low level



To identify parallel IRQ type on SERIRQ, following the table list supported source.

One SERIRQ Field contains three states included Recovery, Turn-Around and Sample.

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SERIRQ Field	Parallel IRQ	Number of clocks after Start finished (Rising Edge)
1	Reserved	2
2	Reserved	5
3	Reserved	8
4	IRQ3	11
5	IRQ4	14
6	IRQ5	17
7	IRQ6	20
8	IRQ7	23
9	Reserved	26
10	IRQ9	29
11	IRQ10	32
12	IRQ11	35
13	IRQ12	38
14	Reserved	41
15	IRQ14	44
16	IRQ15	47
17	IOCHK#	50
21:18	Reserved	53, 56, 59 , 62

Table: SERIRQ map

7.3 LPC DMA

LPC DMA supports Signal, Demand, Verify and Increment operations. The DMA channels are compatible with ISA interface. All channels can be encoded to LDRQ# in serial format even channel 4 that requests a bus master to LPC host. Channels 0-3 are for 8-bit transaction and channel 5-7 are for 16-bit transaction. F85226AF also supports 32-bit DMA if LPC host issues. LDRQ# also refers to LCLK and samples in negative edge by LPC host. ACT field indicates the DMA aborts or not.

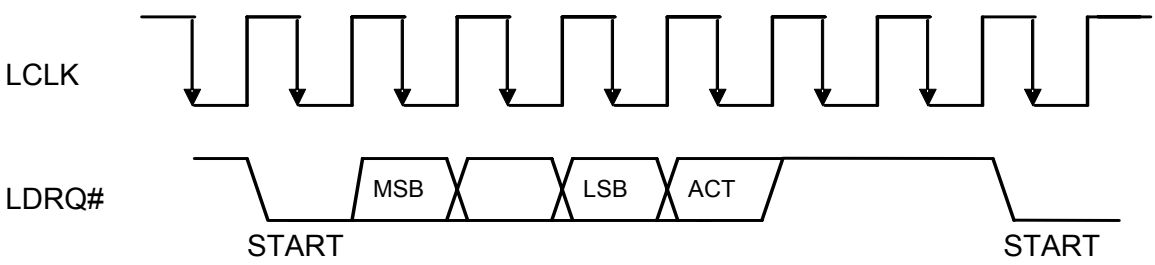

Figure: LCLK and LDRQ#

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8. Registers Description

8.1 Entry Key: Write 26h to the location 4Eh (Default) twice will enable the following configuration registers. Change the location to 2Eh by power-on strapping with an external pulled-down resister on pin 128.

8.2 Configuration and Control Register – Index 03h

Power-on default [7:0] =00_100_0_s_0b (s: mean default value effect by strapping)

Bit	Name	R/W	PWR	Description
7-6	ROM_SEL_TYPE	R/W	VDD3V	00: ROMCS# decoder address 0xF_xxxx, and 0xE_xxxx if BIOS_0E_EN set to 1 (REG03h bit0). 01: ROMCS# decoder address by define address 1 (REG2Ah, 2Bh) and define address 2 (REG 2Eh, 2Fh). 10: ROMCS# decoder address 0xF_xxxx, and 0xE_xxxx if BIOS_0E_EN set to 1 (REG03h bit0) or ROMCS# decoder address by define address 1 (REG2Ah, 2Bh) and define address 2 (REG 2Eh, 2Fh). 11: ROMCS# decoder address 0xF_xxxx, and 0xE_xxxx if BIOS_0E_EN set to 1 (REG03h bit0) or ROMCS# decoder address by define address 1 (REG2Ah, 2Bh) and define address 2 (REG 2Eh, 2Fh).
4-2	BIOS_ROM_SIZE	R/W	VDD3V	000: ROMCS# decodes range 1M. 001: ROMCS# decodes range 2M. 010: ROMCS# decodes range 4M. 011: ROMCS# decodes range 8M. 100: ROMCS# decodes range 16M. 101: ROMCS# decodes range 32M. 110: ROMCS# decodes range 64M. 111: ROMCS# decodes range 1M.
2	BIOS_0E_EN	R/W	VDD3V	Enable ROMCS# to decode the address 0xE_XXXX.
1	BIOS_ROM_EN	R/W	VDD3V	Enable ROMCS# to decode address.
0	BIOS_WR_EN	R/W	VDD3V	When BIOS_ROM_EN is enabled, sets this bit to protect BIOS write.

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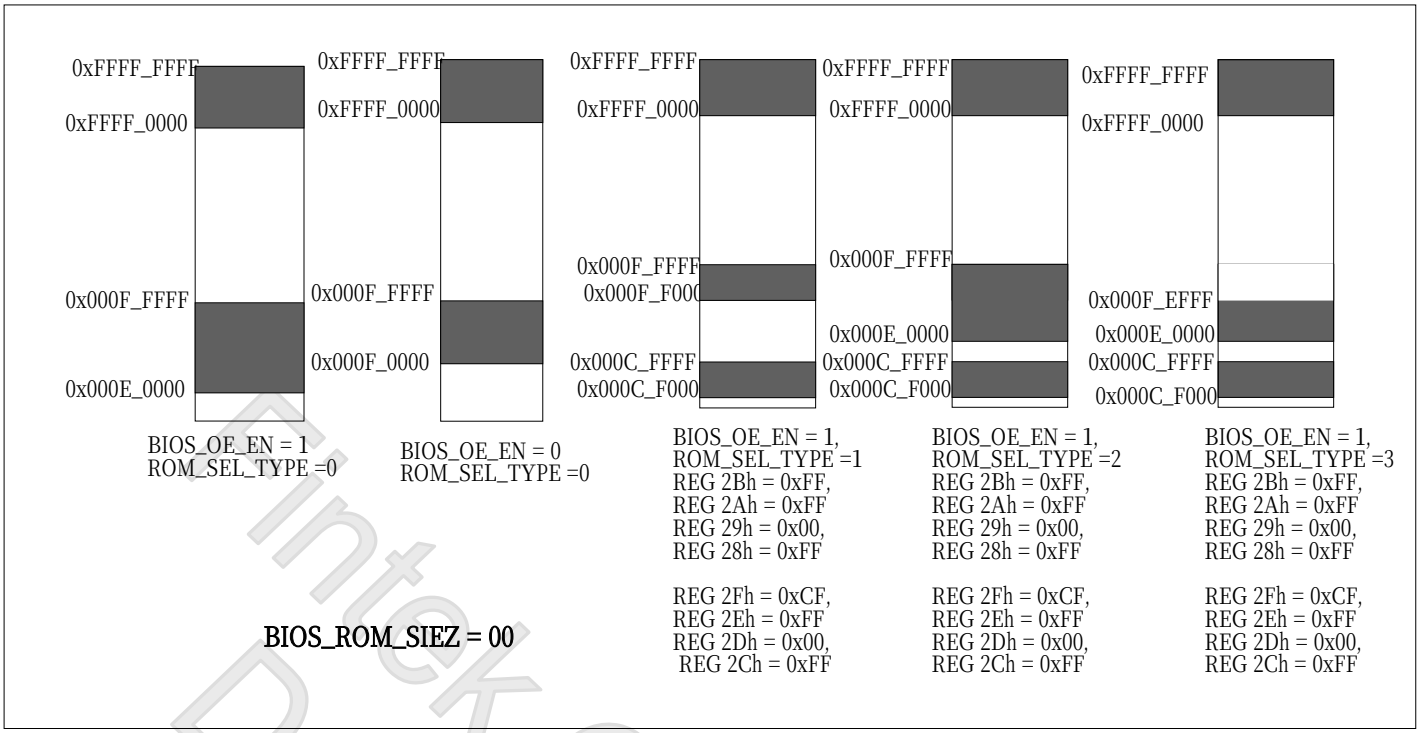

8.3 GPIO1 Function Select Register – Index 04h

Power-on default [7:0] =0ss0_ssssb

Bit	Name	R/W	PWR	Description
7	GP17_MODE	R/W	VDD3V	Set this bit to 0, the pin GP17/IOHCS# will be used as GP17 function. Set to 1, the pin GP17/IOHCS# used as IOHCS# function and decode range can program by (REG 0x3F~0x41).
6	GP16_MODE	R/W	VDD3V	Set this bit to 0, the pin GP16/RTCCS# will be used as GP16 function. Set to 1, the pin GP16/RTCCS# used as RTCCS# function and decode range can program by (REG 0x3C~0x3E). The default value is strapping by RTCEN.
5	GP15_MODE	R/W	VDD3V	Set this bit to 0, the pin GP15/IRQ8 will be used as GP15 function or GPCS#. Set to 1, the pin GP15/IRQ8 used as IRQ8. The default value is strapping by RTCEN.
4	GP14_MODE	R/W	VDD3V	Set this bit to 0, the pin GP14/PLED1 will be used as GP14 function. Set to 1, the pin GP12/PLED1 used as PLED1.
3	GP13_MODE	R/W	VDD3V	Set this bit to 0, the pin GP13/IRQIN will be used as GP13 function. Set to 1, the pin GP13/IRQIN used as IRQIN function. The default value is strapping by KBEN
2	GP12_MODE	R/W	VDD3V	Set this bit to 0, the pin GP12/MCCS# will be used as GP12 function. Set to 1, the pin GP12/MCCS# used as MCCS# function and decode range can program by (REG 0x39~0x3B). The default value is strapping by KBEN
1	GP11_MODE	R/W	VDD3V	Set this bit to 0, the pin GP11/KBCS# will be used as GP11 function. Set to 1, the pin GP11/KBCS# used as KBCS# function and decode range can program by (REG 0x36~0x38). The default value is strapping by KBEN
0	GP10_MODE	RO	VDD3V	Set this bit to 0, the pin GP10/IRQ1 will be used as GP10 function or GPCS#. Set to 1, the pin GP10/IRQ1 used as IRQ1. The default value is strapping by KBEN.

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8.4 GPIO2 Function Select Register – Index 05h

Power-on default [7:0] =0000_sss0b

Bit	Name	R/W	PWR	Description
7-5	Reserved	RO	VDD3V	
3	GP23_MODE	R/W	VDD3V	Set this bit to 0, the pin SA19/GP23 will be used as GP23 function or GPCS#. Set to 1, the pin SA19/GP23 used as SA19. The default value is strapping by DACK5#.
2	GP22_MODE	R/W	VDD3V	Set this bit to 0, the pin SA18/GP22 will be used as GP22 function or GPCS#. Set to 1, the pin SA18/GP22 use as SA18. The default value is strapping by DACK5#.
1	GP21_MODE	R/W	VDD3V	Set this bit to 0, the pin SA17/GP21 will be used as GP21 function or GPCS#. Set to 1, the pin SA17/GP21 used as SA17. The default value is strapping by DACK5#.
0	GP20_MODE	R/W	VDD3V	Set this bit to 0, the pin GP20/PLED0 will be used as GP20 function or GPCS#. Set to 1, this pin will be used as PLED0 output. (When use in LED mode, GP20 output control “CR18” must select to output mode, and user need to take care that decoder select ”CR13,14” can’t select to pin GP20).

8.5 System Clock Register – Index 06h

Power-on default [7:0] =0000_0000b

Bit	Name	R/W	PWR	Description
7	SYSCLK_SEL	R/W	VDD3V	Set to 1, ISA system clock period will be 3 PCI clock. Set to 0, system clock period will be 4 PCI clock.
6	EN_RECOVER8	R/W	VDD3V	Set to 1, enable bit [5:3] setting. Set to 0, disable bit [5:3] setting and uses 3.5 SYSCLKs for 8 bits I/O recovery time.
5-3	RECOVER_TIME8	R/W	VDD3V	When bit 6 was set to 1, these 3 bits field define the additional number of SYSCLKs added to standard 3.5 SYSCLKs recovery time for 8 bits I/O. = 000 --- 0 SYSCLK = 001 --- 1 SYSCLK = 010 --- 2 SYSCLKs = 011 --- 3 SYSCLKs = 100 --- 4 SYSCLKs = 101 --- 5 SYSCLKs = 110 --- 6 SYSCLKs = 111 --- 7 SYSCLKs
2	EN_RECOVER16	R/W	VDD3V	Set to 1, enable bit [1:0] setting. Set to 0, disable bit [1:0] setting and uses 3.5 SYSCLKs for 16 bits I/O recovery time.
1-0	RECOVER_TIME16	R/W	VDD3V	.When bit 2 was set to 1, these 3 bits field define the additional number of SYSCLKs added to standard 3.5 SYSCLKs recovery time for 16 bits I/O. = 01 --- 1 SYSCLK = 10 --- 2 SYSCLK s

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				= 11 --- 3 SYSCLK s = 00 --- 4 SYSCLK s

8.6 System Power down Register – Index 10h

Power-on default [7:0] =0011_0000b

Bit	Name	R/W	PWR	Description
7	Reserved	R/W	VDD3V	
6	SOFT_DOWN	R/W	VDD3V	Set this bit to isolate ISA bus.
5	EN_CLKOUT_PD	R/W	VDD3V	Enable CLKOUT1 and CLKOUT2 power down when isolate the ISA bus.
4	EN_SYSCLK_PD	R/W	VDD3V	Enable SYSCLK to power down when isolate the ISA bus.
3	EN_REFRESH	R/W	VDD3V	Enable refresh output.
2	DIS_CLKOUT2	R/W	VDD3V	If this bit set to 1, CLKOUT2 will power down.
1	DIS_CLKOUT1	R/W	VDD3V	If this bit set to 1, CLKOUT1 will power down.
0	EN_GPIO	R/W	VDD3V	Set this bit to enable write command to REG 0x11~0x1A.

8.7 GPIO Port Define Register (Low byte)– Index 11h

Power-on default [7:0] =0000_0000b

Bit	Name	R/W	PWR	Description

7-0	GP_ADDR[7:0]	R/W	VDD3V	User defines port address to control GPIO functions. To control GPIO state without entry configure mode. (If GPIO no enable “CR10 bit0”, This register will read only).
				For example: if define GP_ADDR 0x150 in CR11 and CR12t.
				If(GPIO output ctrl (REG 0x15, 0x18) set to output mode then:
				-o 150 aa (10101010b) to set GP17, GP15, GP13 and GP11 to High.
				-o 150 55 (01010101 b) to set GP16, GP14, GP12 and GP10 to High.
				-o 151 aa (10101010b) to set GP23 and GP21 to High.
				-o 151 55 (01010101 b) to set GP22 and GP20 to High.
				
				If(GPIO output ctrl (REG 0x15, 0x18) set to input mode then:
				- i 150 ------show pin states of GP1[7..0].
				- i 151------show pin states of GP2[3..0].

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8.8 GPIO Port Define Register (High byte)– Index 12h

Power-on default [7:0] =0000_0000b

Bit	Name	R/W	PWR	Description

7-0	GP_ADDR[15:8]	R/W	VDD3V	User defines port address to control GPIO functions. To control GPIO state without entry configure mode. (If GPIO no enable “CR10 bit0”, This register will read only).
				For example: if define GP_ADDR 0x150 in CR11 and CR12t.
				If(GPIO output ctrl (REG 0x15, 0x18) set to output mode then:
				-o 150 aa (10101010b) to set GP17, GP15, GP13 and GP11 to High.
				-o 150 55 (01010101 b) to set GP16, GP14, GP12 and GP10 to High.
				-o 151 aa (10101010b) to set GP23 and GP21 to High.
				-o 151 55 (01010101 b) to set GP22 and GP20 to High.
				
				If(GPIO output ctrl (REG 0x15, 0x18) set to input mode then:
				-i 150 ------ show pin states of GP1[7..0].
				-i 151 ------ show pin states of GP2[3..0].

8.9 Address Decoder Register (I) – Index 013h

Power-on default [7:0] =1111_1111b

Bit	Name	R/W	PWR	Description
7-4	DECODER_SEL2	R/W	VDD3V	Select GPIO pin to be GPCS2# that define decode address by CR21, 22. **(If GPIO no enable “CR10 bit0”, This register will read only).** 0000: if decode_sel2 set to 0x0h the GPCS2 will output from pin GP10. 0011: if decode_sel2 set to 0x3h the GPCS2 will output from pin GP13. 0100: if decode_sel2 set to 0x4h the GPCS2 will output from pin GP14. 0101: if decode_sel2 set to 0x5h the GPCS2 will output from pin GP15. 1000: if decode_sel2 set to 0x8h the GPCS2 will output from pin GP20. 1001: if decode_sel2 set to 0x9h the GPCS2 will output from pin GP21. 1010: if decode_sel2 set to 0xAh the GPCS2 will output from pin GP22. 1011: if decode_sel2 set to 0xBh the GPCS2 will output from pin GP23. Default : disable.
3-0	DECODER_SEL1	R/W	VDD3V	Select GPIO pin to be GPCS2# that define decode address by CR24, 25. **(If GPIO no enable “CR10 bit0”, This register will read only).** 0000: if decode_sel1 set to 0x0h the GPCS1 will output from pin GP10. 0011: if decode_sel1 set to 0x3h the GPCS1 will output from pin GP13. 0100: if decode_sel1 set to 0x4h the GPCS1 will output from pin GP14. 0101: if decode_sel1 set to 0x5h the GPCS1 will output from pin GP15. 1000: if decode_sel1 set to 0x8h the GPCS1 will output from pin GP20.

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				1001: if decode_sel1 set to 0x9h the GPCS1 will output from pin GP21. 1010: if decode_sel1 set to 0xAh the GPCS1 will output from pin GP22. 1011: if decode_sel1 set to 0xBh the GPCS1 will output from pin GP23. default: disable.

8.10 Address Decoder Register (II) – Index 014h

Power-on default [7:0] =1111_1111b

Bit	Name	R/W	PWR	Description
7-4	DECODER_SEL4	R/W	VDD3V	Select GPIO pin to be GPCS3# that define decode address by CR31, 32. **(If GPIO no enable "CR10 bit0", This register will read only).** 0000: if decode_sel4 set to 0x0h the GPCS4 will output from pin GP10. 0011: if decode_sel4 set to 0x3h the GPCS4 will output from pin GP13. 0100: if decode_sel4 set to 0x4h the GPCS4 will output from pin GP14. 0101: if decode_sel4 set to 0x5h the GPCS4 will output from pin GP15. 1000: if decode_sel4 set to 0x8h the GPCS4 will output from pin GP20. 1001: if decode_sel4 set to 0x9h the GPCS4 will output from pin GP21. 1010: if decode_sel4 set to 0xAh the GPCS4 will output from pin GP22. 1011: if decode_sel4 set to 0xBh the GPCS4 will output from pin GP23. default: disable.
3-0	DECODER_SEL3	R/W	VDD3V	Select GPIO pin to be GPCS3# that define decode address by CR34, 35. **(If GPIO no enable "CR10 bit0", This register will read only).** 0000: if decode_sel3 set to 0x0h the GPCS3 will output from pin GP10. 0011: if decode_sel3 set to 0x3h the GPCS3 will output from pin GP13. 0100: if decode_sel3 set to 0x4h the GPCS3 will output from pin GP14. 0101: if decode_sel3 set to 0x5h the GPCS3 will output from pin GP15. 1000: if decode_sel3 set to 0x8h the GPCS3 will output from pin GP20. 1001: if decode_sel3 set to 0x9h the GPCS3 will output from pin GP21. 1010: if decode_sel3 set to 0xAh the GPCS3 will output from pin GP22. 1011: if decode_sel3 set to 0xBh the GPCS3 will output from pin GP23. default: disable.

8.11 GPIO1x In/Out Control Register – Index 15h

Power-on default [7:0] =0000_0000b

Bit	Name	R/W	PWR	Description
7	GP17_OCTRL	R/W	VDD3V	GP17 in/out mode select: GP17 is input mode if set to 0. GP17 is output mode if set to 1. **(If GPIO no enable "CR10 bit0", This register will read only).**
6	GP16_OCTRL	R/W	VDD3V	GP16 in/out mode select: GP16 is input mode if set to 0. GP16 is output mode if set to 1. **(If GPIO no enable "CR10 bit0", This register will read only).**
5	GP15_OCTRL	R/W	VDD3V	GP15 in/out mode select: GP15 is input mode if set to 0. GP15 is output mode if set to 1. **(If GPIO no enable "CR10 bit0", This register will read only).**

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4	GP14_OCTRL	R/W	VDD3V	GP14 in/out mode select: GP14 is input mode if set to 0. GP14 is output mode if set to 1. **(If GPIO no enable "CR10 bit0", This register will read only).**
3	GP13_OCTRL	R/W	VDD3V	GP13 in/out mode select: GP13 is input mode if set to 0. GP13 is output mode if set to 1. **(If GPIO no enable "CR10 bit0", This register will read only).**
2	GP12_OCTRL	R/W	VDD3V	GP12 in/out mode select: GP12 is input mode if set to 0. GP12 is output mode if set to 1. **(If GPIO no enable "CR10 bit0", This register will read only).**
1	GP11_OCTRL	R/W	VDD3V	GP11 in/out mode select: GP11 is input mode if set to 0. GP11 is output mode if set to 1. **(If GPIO no enable "CR10 bit0", This register will read only).**
0	GP10_OCTRL	R/W	VDD3V	GP10 in/out mode select: GP10 is input mode if set to 0. GP10 is output mode if set to 1. **(If GPIO no enable "CR10 bit0", This register will read only).**

8.12 GPIO Output Data Register – Index 16h

Power-on default [7:0] =0000_0000b

Bit	Name	R/W	PWR	Description
7	GP17_DATA	R/W	VDD3V	When GP17 in out mode, set this bit to write data to pin GP17. **(If GPIO no enable "CR10 bit0", This register will read only).**
6	GP16_DATA	R/W	VDD3V	When GP16 in out mode, set this bit to write data to pin GP16. **(If GPIO no enable "CR10 bit0", This register will read only).**
5	GP15_DATA	R/W	VDD3V	When GP15 in out mode, set this bit to write data to pin GP15. **(If GPIO no enable "CR10 bit0", This register will read only).**
4	GP14_DATA	R/W	VDD3V	When GP14 in out mode, set this bit to write data to pin GP14. **(If GPIO no enable "CR10 bit0", This register will read only).**
3	GP13_DATA	R/W	VDD3V	When GP13 in out mode, set this bit to write data to pin GP13. **(If GPIO no enable "CR10 bit0", This register will read only).**
2	GP12_DATA	R/W	VDD3V	When GP12 in out mode, set this bit to write data to pin GP12. **(If GPIO no enable "CR10 bit0", This register will read only).**
1	GP11_DATA	R/W	VDD3V	When GP11 in out mode, set this bit to write data to pin GP11. **(If GPIO no enable "CR10 bit0", This register will read only).**
0	GP10_DATA	R/W	VDD3V	When GP10 in out mode, set this bit to write data to pin GP10. **(If GPIO no enable "CR10 bit0", This register will read only).**

8.13 GPIO1x Input Register – Index 17h

Power-on default [7:0] =pppp_ppppb (p: mean pin status)

Bit	Name	R/W	PWR	Description
7	GP17_ST	RO	VDD3V	This bit is read only, when read back is the status of the pin GP17.

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6	GP16_ST	RO	VDD3V	This bit is read only, when read back is the status of the pin GP16.
5	GP15_ST	RO	VDD3V	This bit is read only, when read back is the status of the pin GP15.
4	GP14_ST	RO	VDD3V	This bit is read only, when read back is the status of the pin GP14.
3	GP13_ST	RO	VDD3V	This bit is read only, when read back is the status of the pin GP13.
2	GP12_ST	RO	VDD3V	This bit is read only, when read back is the status of the pin GP12.
1	GP11_ST	RO	VDD3V	This bit is read only, when read back is the status of the pin GP11.
0	GP10_ST	RO	VDD3V	This bit is read only, when read back is the status of the pin GP10.

8.14 GPIO2x In/Out Control Register – Index 18h

Power-on default [7:0] =0000_0000b

Bit	Name	R/W	PWR	Description
7	Reserved	-	-	Reserved.
3	GP23_OCTRL	R/W	VDD3V	GP23 in/out mode select: GP23 is input mode if set to 0. GP23 is output mode if set to 1. **(If GPIO no enable "CR10 bit0", This register will read only).**
2	GP22_OCTRL	R/W	VDD3V	GP22 in/out mode select: GP22 is input mode if set to 0. GP22 is output mode if set to 1. **(If GPIO no enable "CR10 bit0", This register will read only).**
1	GP21_OCTRL	R/W	VDD3V	GP21 in/out mode select: GP21 is input mode if set to 0. GP21 is output mode if set to 1. **(If GPIO no enable "CR10 bit0", This register will read only).**
0	GP20_OCTRL	R/W	VDD3V	GP20 in/out mode select: GP20 is input mode if set to 0. GP20 is output mode if set to 1. **(If GPIO no enable "CR10 bit0", This register will read only).**

8.15 GPIO2 Output Data Register – Index 19h

Power-on default [7:0] =0000_0000b

Bit	Name	R/W	PWR	Description
7	Reserved	R/W	VDD3V	Reserved
3	GP23_DATA	R/W	VDD3V	When GP23 in out mode, set this bit to write data to pin GP23. **(If GPIO no enable "CR10 bit0", This register will read only).**
2	GP22_DATA	R/W	VDD3V	When GP22 in out mode, set this bit to write data to pin GP22. **(If GPIO no enable "CR10 bit0", This register will read only).**
1	GP21_DATA	R/W	VDD3V	When GP21 in out mode, set this bit to write data to pin GP21. **(If GPIO no enable "CR10 bit0", This register will read only).**
0	GP20_DATA	R/W	VDD3V	When GP20 in out mode, set this bit to write data to pin GP20. **(If GPIO no enable "CR10 bit0", This register will read only).**

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8.16 GPIO2x Input Register – Index 1Ah

Power-on default [7:0] =0000_ppppb (p: mean pin status)

Bit	Name	R/W	PWR	Description
7-4	Reserved	R/W	VDD3V	Reserved
3	GP23_ ST	R/W	VDD3V	This bit is read only, when read back is the status of the pin GP23.
2	GP22_ ST	R/W	VDD3V	This bit is read only, when read back is the status of the pin GP22.
1	GP21_ ST	R/W	VDD3V	This bit is read only, when read back is the status of the pin GP21.
0	GP20_ ST	R/W	VDD3V	This bit is read only, when read back is the status of the pin GP20.

8.17 LED & IRQIN Control Register – Index 1Bh

Power-on default [7:0] =0000_0000b

Bit	Name	R/W	PWR	Description
7	ADDR_DEC_TYPE[1]	R/W	VDD3V	If set to 1, the address decode 4 (CR34, CR35) will decode the memory cycle, else it will decode io cycle.
6	ADDR_DEC_TYPE[0]	R/W	VDD3V	If set to 1, the address decode 3 (CR31, CR32) will decode the memory cycle, else it will decode io cycle.
5-4	LED_FREQ	R/W	VDD3V	When pin GP14 or GP20 be selected to LED mode, user can use these two bits to define LED frequency: 00: Power LED pin is tri-stated. 01: Power LED pin is driven low. 10: Power LED pin is a 1Hz toggle pulse with 50 duty cycle. 11: Power LED pin is a 1/2 Hz toggle pulse with 50 duty cycle.
3-0	IRQIN_SEL	R/W	VDD3V	These bits select IRQ resource for IRQIN. Four bits transfer the decimal value to octal system. For example: Bit [3..0] = 1001b = 0x9h means IRQ 9 be selected. Bit [3..0] = 1100b = 0xCh means IRQ12 be selected.

8.18 LPC Timout Setting Register – Index 1Dh

Power-on default [7:0] =0110_0011b

Bit	Name	R/W	PWR	Description
7	EN_TIMEOUT	R/W	VDD3V	Enable this bit to timeout LPC long wait when ISA bus had pull IOCHRDY to low.
6-0	TIMEOUT_VALUE	R/W	VDD3V	Define the timeout value, the unit is ISA system clock. So if ISA pull IOCHRDY to

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				low more then this time, the device will end of the LPC long wait. (default are 100 ISA Clock)

8.19 Refresh Address Register (Low Byte) – Index 1Eh

Power-on default [7:0] =1111_1111b

Bit	Name	R/W	PWR	Description
7-0	REFRESH_ADDR	R/W	VDD3V	CR 1E, 1F are used to define the refresh counter repeat value: For example, if set REFRESH_ADDR to 0x01FF, the address in refresh will increase until reach 0x01FF and then refresh address return to 0x0000.

8.20 Refresh Address Register (High Byte) – Index 1Fh

Power-on default [7:0] =0000_0000b

Bit	Name	R/W	PWR	Description
7-0	REFRESH_ADDR	R/W	VDD3V	CR 1E, 1F are used to define the refresh counter repeat value: For example, if set REFRESH_ADDR to 0x01FF, the address in refresh will increase until reach 0x01FF and then refresh address return to 0x0000.

8.21 Address1 Decode Mask Register – Index 20h

Power-on default [7:0] =0000_0000b

Bit	Name	R/W	PWR	Description
7-0	ADDR_MASK1	R/W	VDD3V	This register is used to mask address bits (A7~A0) for specify address decoder, if the corresponding bit of this register is set to a 1, the corresponding address bit(A7~A0) is ignored by the specify address decoder. For example: If the decoding range is 0x3F8 ~ 0x3FF, you can set 0x03F8 to CR21, 22 and 07h to CR20.

8.22 Address1 Decode Register (Low Byte) – Index 21h

Power-on default [7:0] =0000_0000b

Bit	Name	R/W	PWR	Description
7-0	ADDR_DEC1	R/W	VDD3V	This register contains the address for specify decoder. CR21 Bit [7..0] are used to define low byte of specify address. CR22 Bit [7..0] are used to define high byte of specify address. For example: Decoding address was set to be 0x3F5h when wrote F5h to CR21 and 03h to CR22.

8.23 Address1 Decode Register (High Byte) – Index 22h

Power-on default [7:0] =0000_0000b

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Bit	Name	R/W	PWR	Description
7-0	ADDR_DEC1	R/W	VDD3V	This register contains the address for specify decoder. CR21 Bit [7..0] are used to define low byte of specify address. CR22 Bit [7..0] are used to define high byte of specify address. For example: Decoding address was set to be 0x3F5h when wrote F5h to CR21 and 03h to CR22.

8.24 Address2 Decode Mask Register – Index 23h

Power-on default [7:0] =0000_0000b

Bit	Name	R/W	PWR	Description
7-0	ADDR_MASK2	R/W	VDD3V	This register is used to mask address bits (A7~A0) for specify address decoder, if the corresponding bit of this register is set to a 1, the corresponding address bit(A7~A0) is ignored by the specify address decoder. For example: If the decoding range is 0x3F8 ~ 0x3FF, you can set 0x03F8 to CR24, 25 and 07h to CR23.

8.25 Address2 Decode Register (Low Byte) – Index 24h

Power-on default [7:0] =0000_0000b

Bit	Name	R/W	PWR	Description
7-0	ADDR_DEC2	R/W	VDD3V	This register contains the address for specify decoder. CR24 Bit [7:0] are used to define low byte of specify address. CR25 Bit [7:0] are used to define high byte of specify address. For example: Decoding address was set to be 0x3F5h when wrote F5h to CR24 and 03h to CR25.

8.26 Address2 Decode Register (High Byte) – Index 25h

Power-on default [7:0] =0000_0000b

Bit	Name	R/W	PWR	Description
7-0	ADDR_DEC2	R/W	VDD3V	This register contains the address for specify decoder. CR24 Bit [7..0] are used to define low byte of specify address. CR25 Bit [7..0] are used to define high byte of specify address. For example: Decoding address was set to be 0x3F5h when wrote F5h to CR24 and 03h to CR25 .

8.27 ROM1 Decoder Mask Low Byte Register – Index 0x28

Power-on default [7:0] =0000_0000b

Bit	Name	R/W	PWR	Description

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7-0	ROM_MASK1	R/W	VDD3V	The register CR28, 29 are used to mask address bits (A19~A4) for specify address decoder, if the corresponding bit of this register is set to a 1, the corresponding address bit(A19~A4) is ignored by the specify address decoder. For example: If the decoding range is 0xF_FFFX ~ 0xF_E00X, you can set 0xF_FFFF to CR2A, 2B and ffh to CR28, 01h to CR29.

8.28 ROM Decoder Mask (High Byte) Register – Index 0x29

Power-on default [7:0] =0000_0000b

Bit	Name	R/W	PWR	Description
7-0	ROM_ MASK1	R/W	VDD3V	The register CR28, 29 are used to mask address bits (A19~A4) for specify address decoder, if the corresponding bit of this register is set to a 1, the corresponding address bit(A19~A4) is ignored by the specify address decoder. For example: If the decoding range is 0xF_FFFX ~ 0xF_E00X, you can set 0xF_FFFF to CR2A, 2B and ffh to CR28, 01h to CR29.

8.29 ROM Decoder Address (Low Byte) Register – Index 0x2A

Power-on default [7:0] =0000_0000b

Bit	Name	R/W	PWR	Description
7-0	ROM_DEC1	R/W	VDD3V	This register contains the address for specify decoder. CR2A Bit [7..0] are used to define low address[11:4]. CR2B Bit [7..0] are used to define high address[19:12]. For example: Decoding address was set to be 0xF_FEEXh when wrote EEh to CR2A and FFh to CR2B.

8.30 ROM Decoder Address (High Byte) Register – Index 0x2B

Power-on default [7:0] =0000_0000b

Bit	Name	R/W	PWR	Description
7-0	ROM_DEC1	R/W	VDD3V	This register contains the address for specify decoder. CR2A Bit [7..0] are used to define low address[11:4]. CR2B Bit [7..0] are used to define high address[19:12]. For example: Decoding address was set to be 0xF_FEEXh when wrote EEh to CR2A and FFh to CR2B.

8.31 ROM2 Decoder Mask Low Byte Register – Index 0x2C

Power-on default [7:0] =0000_0000b

Bit	Name	R/W	PWR	Description
7-0	ROM_MASK2	R/W	VDD3V	The register CR2C, 2D are used to mask address bits (A19~A4) for specify address decoder, if the corresponding bit of this register is set to a 1, the corresponding

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				address bit(A19~A4) is ignored by the specify address decoder. For example: If the decoding range is 0xF_FFFX ~ 0xF_E00X, you can set 0xF_FFFF to CR2E, 2F and ffh to CR2C, 01h to CR2D.

8.32 ROM2 Decoder Mask (High Byte) Register – Index 0x2D

Power-on default [7:0] =0000_0000b

Bit	Name	R/W	PWR	Description
7-0	ROM_ MASK2	R/W	VDD3V	The register CR2C, 2D are used to mask address bits (A19~A4) for specify address decoder, if the corresponding bit of this register is set to a 1, the corresponding address bit(A19~A4) is ignored by the specify address decoder. For example: If the decoding range is 0xF_FFFX ~ 0xF_E00X, you can set 0xF_FFFF to CR2E, 2F and ffh to CR2C, 01h to CR2D.

8.33 ROM2 Decoder Address (Low Byte) Register – Index 0x2E

Power-on default [7:0] =0000_0000b

Bit	Name	R/W	PWR	Description
7-0	ROM_DEC2	R/W	VDD3V	This register contains the address for specify decoder. CR2E Bit [7..0] are used to define low address[11:4]. CR2F Bit [7..0] are used to define high address[19:12]. For example: Decoding address was set to be 0x5_5AAXh when wrote AAh to CR2E and 55h to CR2F.

8.34 ROM2 Decoder Address (High Byte) Register – Index 0x2F

Power-on default [7:0] =0000_0000b

Bit	Name	R/W	PWR	Description
7-0	ROM_DEC2	R/W	VDD3V	This register contains the address for specify decoder. CR2E Bit [7..0] are used to define low address[11:4]. CR2F Bit [7..0] are used to define high address[19:12]. For example: Decoding address was set to be 0x5_5AAXh when wrote AAh to CR2E and 55h to CR2F.

8.35 ADDR3 Decoder Mask High Byte Register – Index 0x30

Power-on default [7:0] =0000_0000b

Bit	Name	R/W	PWR	Description
7-0	ADDR3_DEC_MASK	R/W	VDD3V	This register is used to mask io address bits A7~A0 or memory addrss bits A23~A16 for specify address decoder, if the corresponding bit of this register is set to a 1, the corresponding address bits will ignored by the specify address decoder. For example: If the decoding range is 0x3F8 ~ 0x3FF, you can set 0x03F8 to CR31,

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				32 and 07h to CR30.

8.36 ADDR3 Decoder Address Low Byte Register – Index 0x31

Power-on default [7:0] =0000_0000b

Bit	Name	R/W	PWR	Description
7-0	ADDR3_DEC	R/W	VDD3V	This register contains the address for specify decoder. CR31 Bit [7..0] are used to define low byte of specify address. CR32 Bit [7..0] are used to define high byte of specify address. For example: Decoding address was set to be 0x3F5h when wrote F5h to CR31 and 03h to CR32. (The address decoder will decode the match "IO" address that define in CR31 and CR32 register, but when set CR1B bit6 to 1, The address decoder will decode the match "memory" address[31:16] that define in CR31 and CR32 registers).

8.37 ADDR3 Decoder Address High Byte Register – Index 0x32

Power-on default [7:0] =0000_0000b

Bit	Name	R/W	PWR	Description
7-0	ADDR3_DEC	R/W	VDD3V	This register contains the address for specify decoder. CR31 Bit [7..0] are used to define low byte of specify address. CR32 Bit [7..0] are used to define high byte of specify address. For example: Decoding address was set to be 0x3F5h when wrote F5h to CR31 and 03h to CR32. (The address decoder will decode the match "IO" address that define in CR31 and CR32 register, but when set CR1B bit6 to 1, The address decoder will decode the match "memory" address[31:16] that define in CR31 and CR32 registers).

8.38 ADDR4 Decoder Mask High Byte Register – Index 0x33

Power-on default [7:0] =0000_0000b

Bit	Name	R/W	PWR	Description
7-0	ADDR4_DEC_MASK	R/W	VDD3V	This register is used to mask io address bits A7~A0 or memory addrss bits A23~A16 for specify address decoder, if the corresponding bit of this register is set to a 1, the corresponding address bits will ignored by the specify address decoder. For example: If the decoding range is 0x3F8 ~ 0x3FF, you can set 0x03F8 to CR34, 35 and 07h to CR33.

8.39 ADDR4 Decoder Address Low Byte Register – Index 0x34

Power-on default [7:0] =0000_0000b

Bit	Name	R/W	PWR	Description

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7-0	ADDR4_DEC	R/W	VDD3V	This register contains the address for specify decoder. CR34 Bit [7..0] are used to define low byte of specify address. CR35 Bit [7..0] are used to define high byte of specify address. For example: Decoding address was set to be 0x3F5h when wrote F5h to CR34 and 03h to CR35. (The address decoder will decode the match "IO" address that define in CR34 and CR35 register, but when set CR1B bit7 to 1, The address decoder will decode the match "memory" address[31:16] that define in CR34 and CR35 registers).

8.40 ADDR4 Decoder Address High Byte Register – Index 0x35

Power-on default [7:0] =0000_0000b

Bit	Name	R/W	PWR	Description
7-0	ADDR4_DEC	R/W	VDD3V	This register contains the address for specify decoder. CR34 Bit [7..0] are used to define low byte of specify address. CR35 Bit [7..0] are used to define high byte of specify address. For example: Decoding address was set to be 0x3F5h when wrote F5h to CR34 and 03h to CR35. (The address decoder will decode the match "IO" address that define in CR34 and CR35 register, but when set CR1B bit7 to 1, The address decoder will decode the match "memory" address[31:16] that define in CR34 and CR35 registers).

8.41 KBC Decoder Mask Register – Index 0x36

Power-on default [7:0] =0000_0100b

Bit	Name	R/W	PWR	Description
7-0	KBC _MASK	R/W	VDD3V	This register is used to mask address bits (A7~A0) for specify address decoder, if the corresponding bit of this register is set to a 1, the corresponding address bit(A7~A0) is ignored by the specify address decoder. For example: If the decoding range is 0x060 & 0x064, you can set 0x060 to CR37, 38 and 04h to CR36.

8.42 KBC Decoder Address Low Byte Register – Index 0x37

Power-on default [7:0] =0110_0000b

Bit	Name	R/W	PWR	Description
7-0	KBC_DEC	R/W	VDD3V	This register contains the address for KBC decoder. CR37 Bit [7..0] are used to define low byte of specify address. CR38 Bit [7..0] are used to define high byte of specify address. For example: Decoding address was set to be 0x060h when wrote 60h to CR37 and 00h to CR38.

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8.43 KBC Decoder Address High Byte Register – Index 0x38

Power-on default [7:0] =0000_0000b

Bit	Name	R/W	PWR	Description
7-0	KBC_DEC	R/W	VDD3V	This register contains the address for KBC decoder. CR37 Bit [7..0] are used to define low byte of specify address. CR38 Bit [7..0] are used to define high byte of specify address. For example: Decoding address was set to be 0x060h when wrote 60h to CR37 and 00h to CR38.

8.44 MC Decoder Mask Register – Index 0x39

Power-on default [7:0] =0000_0100b

Bit	Name	R/W	PWR	Description
7-0	MC _MASK	R/W	VDD3V	This register is used to mask address bits (A7~A0) for specify address decoder, if the corresponding bit of this register is set to a 1, the corresponding address bit(A7~A0) is ignored by the specify address decoder. For example: If the decoding range is 0x062 & 0x066, you can set 0x062 to CR3A, 3B and 04h to CR39.

8.45 MC Decoder Address Low Byte Register – Index 0x3A

Power-on default [7:0] =0110_0010b

Bit	Name	R/W	PWR	Description
7-0	MC_DEC	R/W	VDD3V	This register contains the address for KBC decoder. CR3A Bit [7..0] are used to define low byte of specify address. CR3B Bit [7..0] are used to define high byte of specify address. For example: Decoding address was set to be 0x062h when wrote 60h to CR3A and 00h to CR3B.

8.46 MC Decoder Address High Byte Register – Index 0x3B

Power-on default [7:0] =0000_0000b

Bit	Name	R/W	PWR	Description
7-0	MC_DEC	R/W	VDD3V	This register contains the address for KBC decoder. CR3A Bit [7..0] are used to define low byte of specify address. CR3B Bit [7..0] are used to define high byte of specify address. For example: Decoding address was set to be 0x062h when wrote 60h to CR3A and 00h to CR3B.

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8.47 RTC Decoder Mask Register – Index 0x3C

Power-on default [7:0] =0000_0001b

Bit	Name	R/W	PWR	Description
7-0	RTC_ MASK	R/W	VDD3V	This register is used to mask address bits (A7~A0) for specify address decoder, if the corresponding bit of this register is set to a 1, the corresponding address bit(A7~A0) is ignored by the specify address decoder. For example: If the decoding range is 0x070 & 0x071, you can set 0x070 to CR3D, 3E and 01h to CR3C.

8.48 RTC Decoder Address Low Byte Register – Index 0x3D

Power-on default [7:0] =0111_0000b

Bit	Name	R/W	PWR	Description
7-0	RTC_DEC	R/W	VDD3V	This register contains the address for KBC decoder. CR3D Bit [7..0] are used to define low byte of specify address. CR3E Bit [7..0] are used to define high byte of specify address. For example: Decoding address was set to be 0x060h when wrote 70h to CR3D and 00h to CR3E.

8.49 RTC Decoder Address High Byte Register – Index 0x3E

Power-on default [7:0] =0000_0000b

Bit	Name	R/W	PWR	Description
7-0	RTC_DEC	R/W	VDD3V	This register contains the address for KBC decoder. CR3D Bit [7..0] are used to define low byte of specify address. CR3E Bit [7..0] are used to define high byte of specify address. For example: Decoding address was set to be 0x060h when wrote 70h to CR3D and 00h to CR3E.

8.50 IOH Decoder Mask Register – Index 0x3F

Power-on default [7:0] =1111_1111b

Bit	Name	R/W	PWR	Description
7-0	IOH_ MASK	R/W	VDD3V	This register is used to mask address bits (A7~A0) for specify address decoder, if the corresponding bit of this register is set to a 1, the corresponding address bit(A7~A0) is ignored by the specify address decoder. For example: If the decoding range is 0x0000 ~ 0x00FF, you can set 0x00 to

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				CR40, 41 and FFh to CR3F.

8.51 IOH Decoder Address Low Byte Register – Index 0x40

Power-on default [7:0] =0000_0000b

Bit	Name	R/W	PWR	Description
7-0	IOH_DEC	R/W	VDD3V	This register contains the address for IOH decoder. CR40 Bit [7..0] are used to define low byte of specify address. CR41 Bit [7..0] are used to define high byte of specify address. For example: Decoding address was set to be 0x0080h when wrote 80h to CR40 and 00h to CR41.

8.52 IOH Decoder Address High Byte Register – Index 0x41

Power-on default [7:0] =0000_0000b

Bit	Name	R/W	PWR	Description
7-0	IOH_DEC	R/W	VDD3V	This register contains the address for IOH decoder. CR40 Bit [7..0] are used to define low byte of specify address. CR41 Bit [7..0] are used to define high byte of specify address. For example: Decoding address was set to be 0x0080h when wrote 80h to CR40 and 00h to CR41.

8.53 Edge Detector Status Register – Index 0x50

Power-on default [7:0] =0000_0000b

Bit	Name	R/W	PWR	Description
7-3	Reserved	RO	VDD3V	Reserved
2	EN_IOCHK_IRQ	R/W	VDD3V	Write 1 to enable IOCHK# signal to trigger SERIRQ channel 17.
1	INV_IOCHK	R/W	VDD3V	When CR50 bit2 enable and this bit set to 1, the IOCHK# input signal will be inverted and trigger SERIRQ channel 17
0	CLK_PD	RW	VDD3V	Set to 1 to disable SYSCLK output.

8.54 IRQ Wakeup Register (I) – Index 0x51

Power-on default [7:0] =0000_0000b

Bit	Name	R/W	PWR	Description
7	EN_IRQ7_W	RW	VDD3V	Set to 1 to enable IRQ7 to wakeup the system.
6	EN_IRQ6_W	R/W	VDD3V	Set to 1 to enable IRQ6 to wakeup the system.

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5	EN_IRQ5_W	R/W	VDD3V	Set to 1 to enable IRQ5 to wakeup the system.
4	EN_IRQ4_W	R/W	VDD3V	Set to 1 to enable IRQ4 to wakeup the system.
3	EN_IRQ3_W	R/W	VDD3V	Set to 1 to enable IRQ3 to wakeup the system.
2	Reserved	R/W	VDD3V	Reserved
1	EN_IRQ1_W	R/W	VDD3V	Set to 1 to enable IRQ1 to wakeup the system.
0	EN_PWRDN_W	RW	VDD3V	Set to 1 to enable PWRDN pin to power down or wakeup the system.

8.55 IRQ Wakeup Register (II) – Index 0x52

Power-on default [7:0] =0000_0000b

Bit	Name	R/W	PWR	Description
7	Reserved	RW	VDD3V	Reserved
6	EN_IRQ15_W	R/W	VDD3V	Set to 1 to enable IRQ15 to wakeup the system.
5	EN_IRQ14_W	R/W	VDD3V	Set to 1 to enable IRQ14 to wakeup the system.
4	EN_IRQ12_W	R/W	VDD3V	Set to 1 to enable IRQ12 to wakeup the system.
3	EN_IRQ11_W	R/W	VDD3V	Set to 1 to enable IRQ11 to wakeup the system.
2	EN_IRQ10_W	R/W	VDD3V	Set to 1 to enable IRQ10 to wakeup the system.
1	EN_IRQ9_W	R/W	VDD3V	Set to 1 to enable IRQ9 to wakeup the system.
0	EN_IRQ8_W	RW	VDD3V	Set to 1 to enable IRQ8 to wakeup the system.

8.56 Frame waiting control Register — Index 0x53

Bit	Name	R/W	Default	Description
7-0	FRAME_WAIT_TIME	R/W	0x0A	When F85226AF return SYNC to LPC host, F85226AF internal timer will start to count, and after timer count more then value that define in this register. It will abort ISA 16 bits read write.

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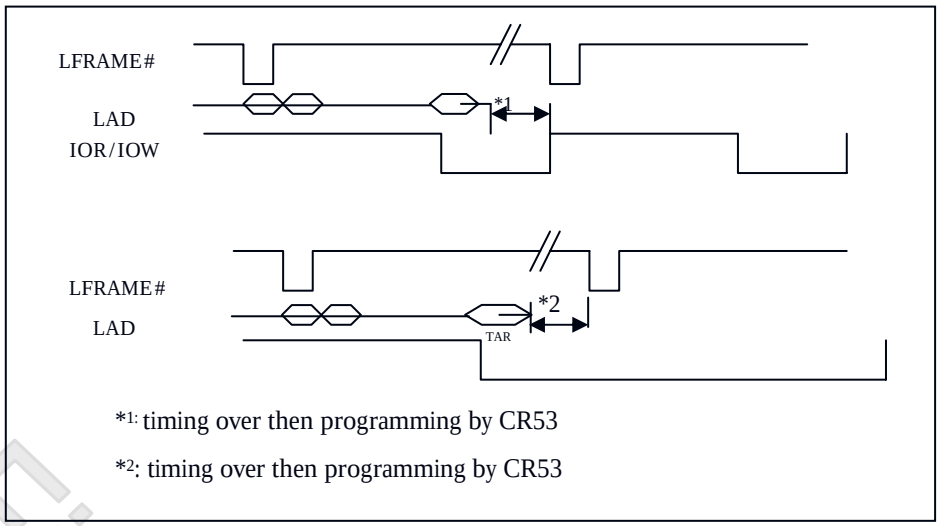

*1: timing over then programming by CR53

*2: timing over then programming by CR53

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8.57 VDD0 voltage value Register — Index 0x54

Bit	Name	R/W	Default	Description
7	IRQ7_MASK	R/W	0	Set 1 to disable IRQ7
6	IRQ6_MASK	R/W	0	Set 1 to disable IRQ6
5	IRQ5_MASK	R/W	0	Set 1 to disable IRQ5
4	IRQ4_MASK	R/W	0	Set 1 to disable IRQ4
3	IRQ3_MASK	R/W	0	Set 1 to disable IRQ3
2	IRQ_IOCHK_MASK	R/W	0	Set 1 to disable IRQ_IOCHK
1	IRQ1_MASK	R/W	0	Set 1 to disable IRQ1
0	IRQ_IN_MASK	R/W	0	Set 1 to disable IRQ_IN

8.58 VDD0 voltage value Register — Index 0x55

Bit	Name	R/W	Default	Description
7	IRQ15_MASK	R/W	0	Set 1 to disable IRQ15
6	IRQ14_MASK	R/W	0	Set 1 to disable IRQ14
5	Reserved	R/W	0	Reserved
4	IRQ12_MASK	R/W	0	Set 1 to disable IRQ12
3	IRQ11_MASK	R/W	0	Set 1 to disable IRQ11
2	IRQ10_MASK	R/W	0	Set 1 to disable IRQ10
1	IRQ9_MASK	R/W	0	Set 1 to disable IRQ9
0	IRQ8_MASK	R/W	0	Set 1 to disable IRQ8

8.59 CHIPID (1) Register – Index 0x5A

Power-on default [7:0] =0000_0011b

Bit	Name	R/W	PWR	Description
7-0	CHIPID	RO	VDD3V	Chip ID, High byte (8'h03).

8.60 CHIPID (2) Register – Index 0x5B

Power-on default [7:0] =0000_0101b

Bit	Name	R/W	PWR	Description
7-0	CHIPID	RO	VDD3V	Chip ID, Low byte (8'h05).

8.61 VENDOR ID (1) Register – Index 0x5D

Power-on default [7:0] =0001_1001b

Bit	Name	R/W	PWR	Description
7-0	VENDOR1	RO	VDD3V	Vendor ID, 8'h19.

8.62 VENDOR ID (2) Register – Index 0x5E

Power-on default [7:0] =0011_0100b

Bit	Name	R/W	PWR	Description
7-0	VENDOR2	RO	VDD3V	Vendor ID, 8h34.

8.63 SBHE control Register – Index 0xF1

Power-on default [7:0] =0000_0001b

Bit	Name	R/W	PWR	Description
7	Reserved	RO	VDD3V	Always return 0
6	ISA_SBHE_EN	R/W	VDD3V	When set to 1, and ISA transmit in 8 bit mode, SBHE# will active with an odd address and during a 16 bit transfer mode, SBHE# will be asserted at an even address.
5-0	Reserved	R/W	VDD3V	Fintek test mode

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9. Ordering Information

Part Number	Package Type	Production Flow
F85226AF	128 pin PQFP (Green Package)	Commercial, 0°C to +70°C

10. Electrical characteristic

10.1 Absolute Maximum Ratings

PARAMETER	RATING	UNIT
Power Supply Voltage	-0.5 to 5.5	V
Input Voltage	-0.5 to VDD+0.5	V
Operating Temperature	0 to +70	° C
Storage Temperature	-55 to 150	° C

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device

10.2 DC Characteristics

(Ta = 70° C, VDD = 3.3V, VSS = 0V)

PARAMETER	SYM.	MIN.	TYP.	MAX.	UNIT	CONDITIONS
I/OD_{24ts} - TTL level bi-directional pin, with Schmitt trigger, can select to OD by register, with 24 mA source-sink capability						
Input Low Threshold Voltage	Vt-			0.8	V	VDD = 3.3 V
Input High Threshold Voltage	Vt+	2.0			V	VDD = 3.3 V
Output Low Current	IOL	24			mA	VOL = 0.4 V
Input High Leakage	ILIH			1	μA	VIN = VDD
Input Low Leakage	ILIL	-1			μA	VIN = 0V
$I/O24_{ts}$ - TTL level bi-directional pin, with Schmitt trigger and 24 mA source-sink capability						
Input Low Threshold Voltage	Vt-			0.8	V	VDD = 3.3 V
Input High Threshold Voltage	Vt+	2.0			V	VDD = 3.3 V
Output High Current	IOH			-24	mA	VOL = 2.4 V
Output Low Current	IOL	24			mA	VOL = 0.4 V
Input High Leakage	ILIH			1	μA	VIN = VDD

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Input Low Leakage	ILIL	-1			μA	VIN = 0V
O_{20} - Output pin with 20 mA source-sink capability						
Output High Current	IOH			-20	mA	VOL = 2.4 V
Output Low Current	IOL	20			mA	VOL = 0.4 V
O_{24} - Output pin with 24 mA source-sink capability						
Output High Current	IOH			-24	mA	VOL = 2.4 V
Output Low Current	IOL	24			mA	VOL = 0.4 V
IN_t - TTL level input pin						
Input Low Threshold Voltage	Vt-			0.8	V	VDD = 3.3 V
Input High Threshold Voltage	Vt+	2.0			V	VDD = 3.3 V
Input High Leakage	ILIH			1	μA	VIN = VDD
Input Low Leakage	ILIL	-1			μA	VIN = 0V
IN_{ts} - TTL level input pin with schmitt trigger						
Input Low Threshold Voltage	Vt-			0.8	V	VDD = 3.3 V
Input High Threshold Voltage	Vt+	2.0			V	VDD = 3.3 V
Input High Leakage	ILIH			1	μA	VIN = VDD
Input Low Leakage	ILIL	-1			μA	VIN = 0V

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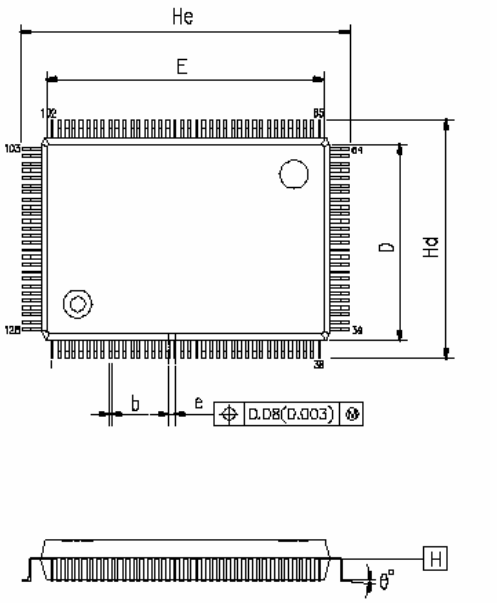
11. Package specification

128 PQFP



SYMBOLS	MIN.	NOM.	MAX.
A1	0.25	0.35	0.45
A2	2.57	2.72	2.87
b	0.10	0.20	0.30
C	0.10	0.15	0.20
D	13.90	14.00	14.10
E	19.90	20.00	20.10
e	–	0.50	–
Hd	17.00	17.20	17.40
He	23.00	23.20	23.40
L	0.65	0.80	0.95
L1	–	1.60	–
Y	–	–	0.08
θ°	0	–	12

UNIT : mm

NOTES:

1.JEDEC OUTLINE:N/A

2.DATUM PLANE [H] IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.

3.DIMENSIONS E AND D DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 mm PER SIDE. DIMENSIONS E AND E DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE [H].

4.DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION .

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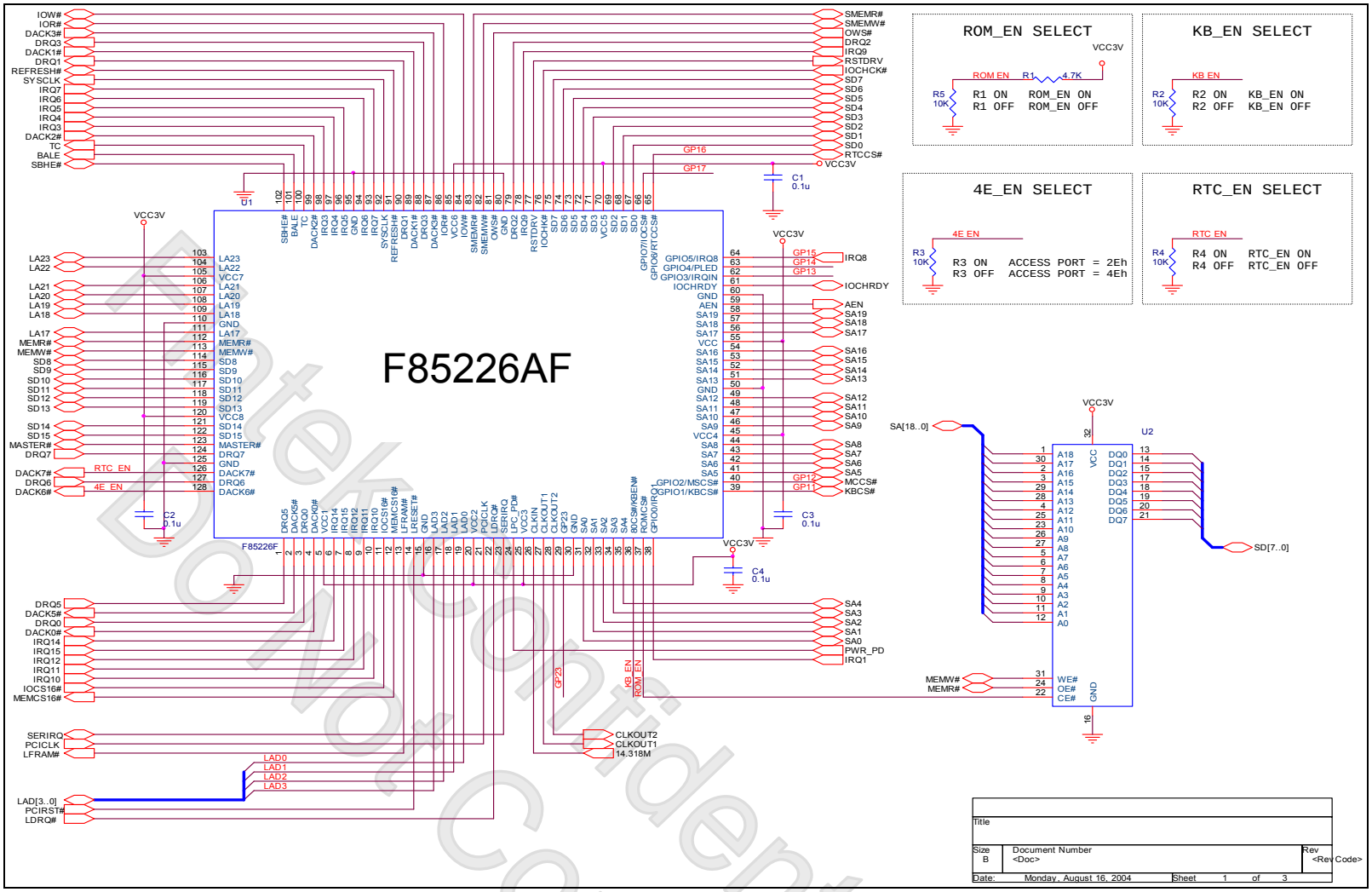
12. Application Circuit



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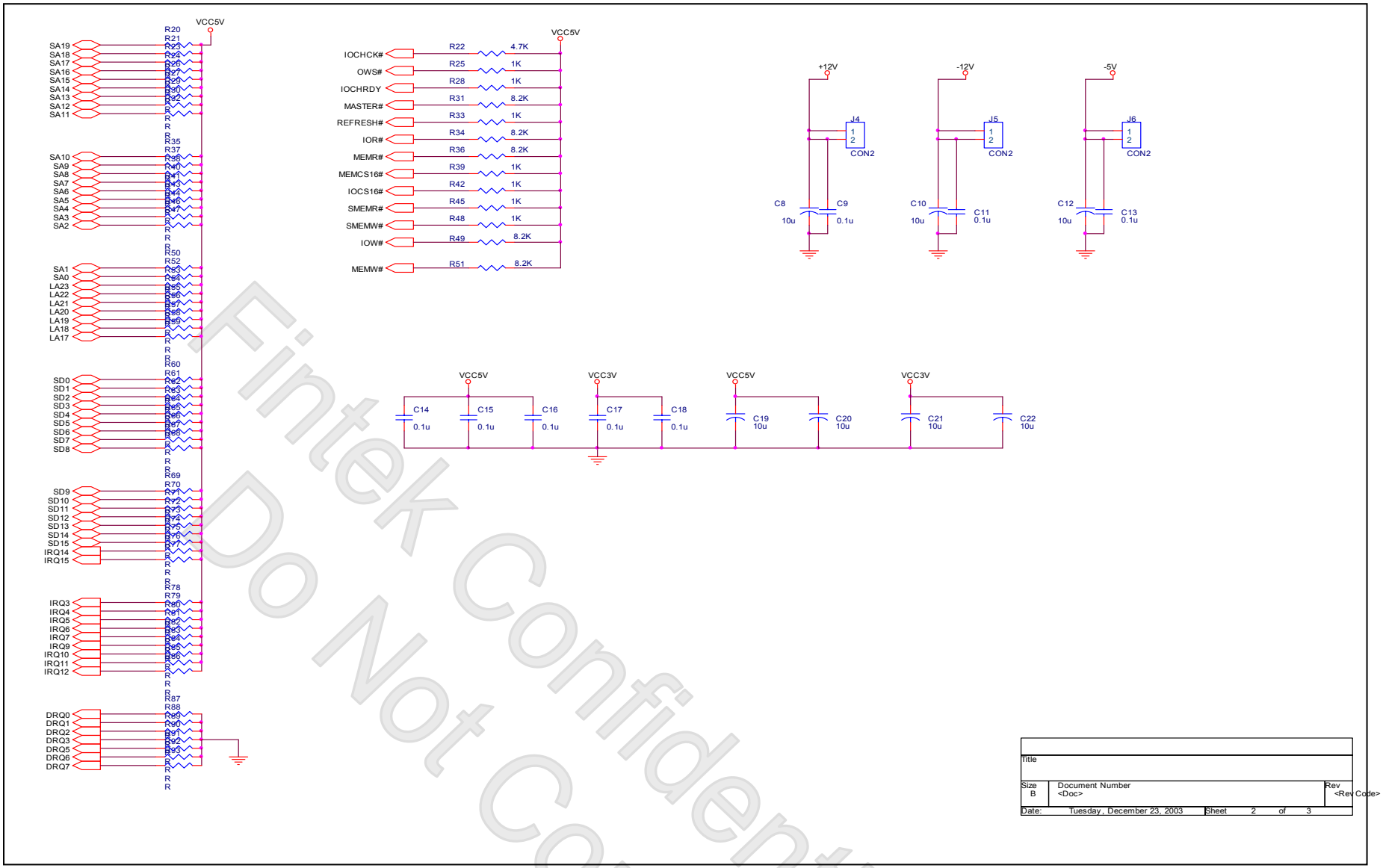

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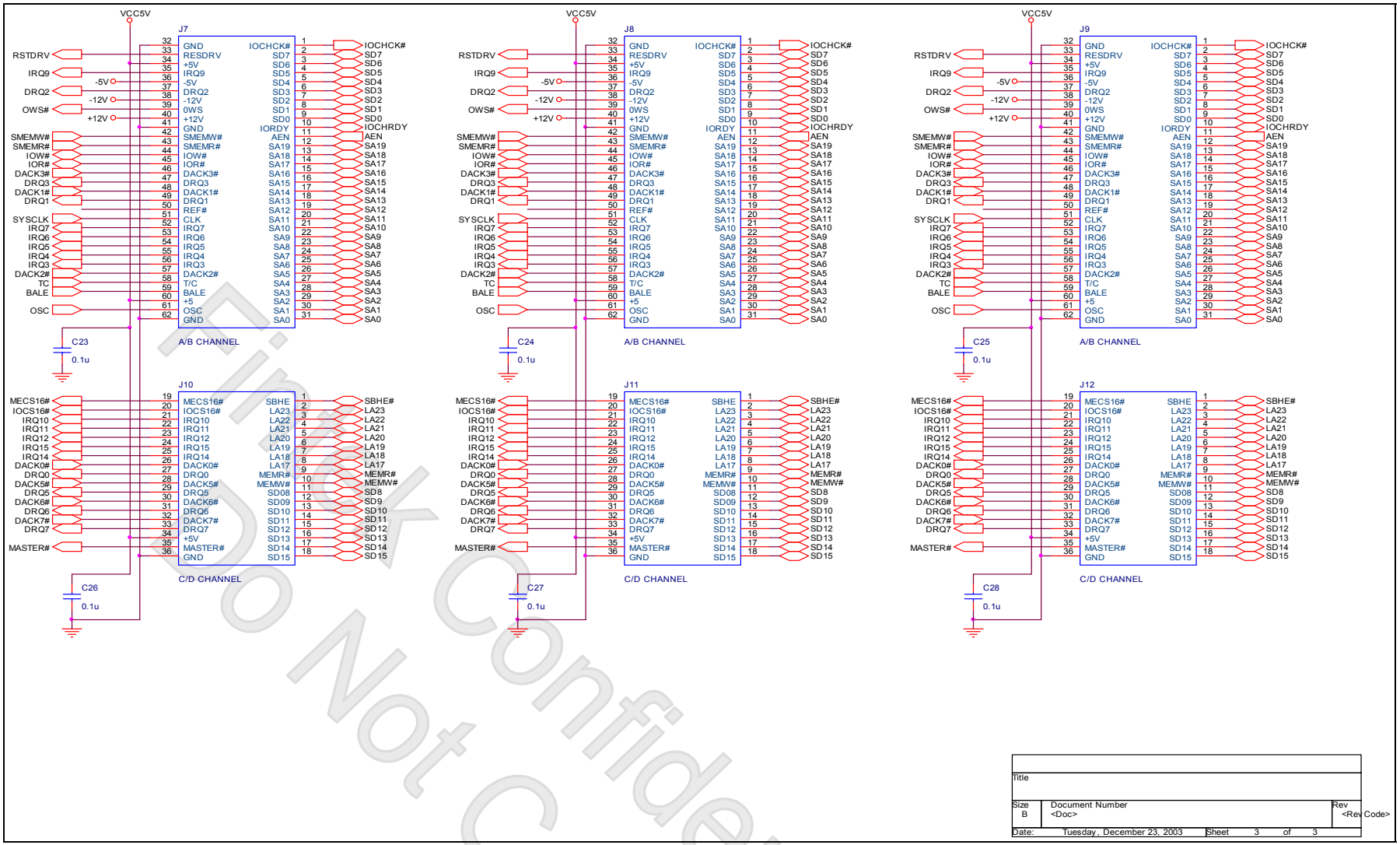

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