



### Driver Characteristics

Parameter	Rating	Units
$V_{\text{OFFSET}}$	600	V
$I_{\text{O } \pm}$ (Source/Sink)	250/500	mA
$V_{\text{CStH}}$	250	mV
$t_{\text{ON}} / t_{\text{OFF}}$ (Typical)	100	ns

### Features

- Floating Channel Designed for Bootstrap Operation up to 600V
- Tolerant to Negative Transient Voltages; dV/dt Immune
- Undervoltage Lockout
- 3.3V, 5V, and 12V Input Logic Compatible
- Open-Drain FAULT Indicator Pin Shows Over-Current Shutdown
- Output in Phase with the Input

### Applications

- High-Speed Gate Driver
- Motor Drive Inverter

### Description

The IX2127 is a high-voltage, high-speed power MOSFET and IGBT driver. High-voltage level-shift circuitry enables this device to operate up to 600V. Clare's proprietary common-mode design techniques provide stable operation in high dV/dt noise environments.

An on-board comparator can be used to detect an over-current condition in the driven MOSFET or IGBT device, and then shut down drive to that device. An open-drain output,  $\overline{\text{FAULT}}$ , indicates that an over-current shutdown has occurred.

The gate driver output typically can source 250mA and sink 500mA, which is suitable for fluorescent lamp ballast, motor control, SMPS, and other converter drive topologies.

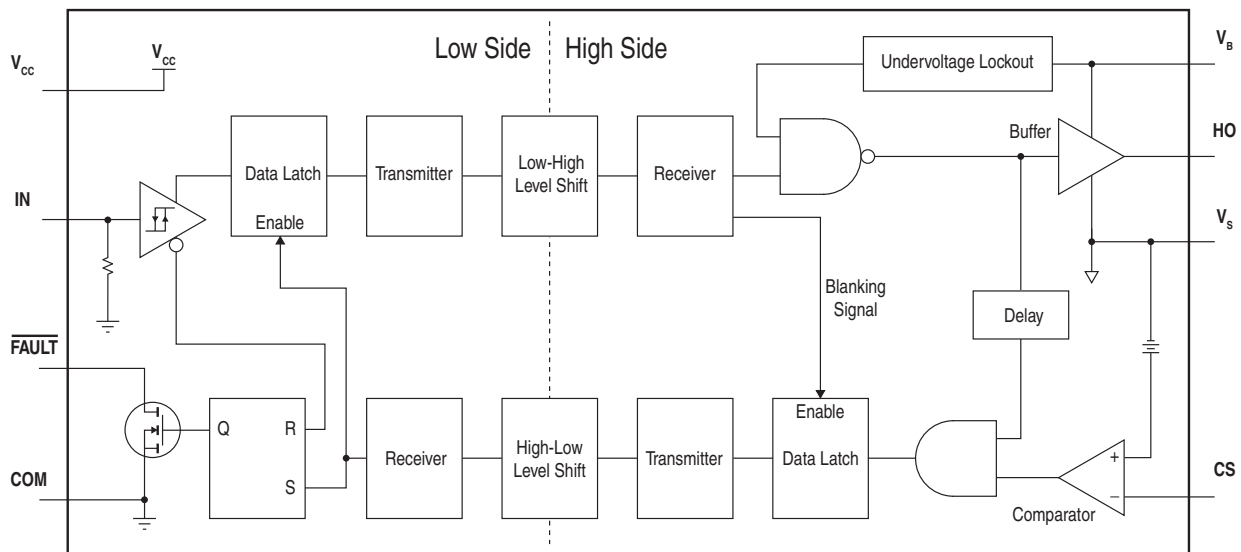
The IX2127 is provided in 8-pin DIP and 8-pin SOIC packages, and is available in Tape & Reel versions. See ordering information below.

### Ordering Information

Part	Description
IX2127G	8-Pin DIP (50/Tube)
IX2127N	8-Pin SOIC (100/Tube)
IX2127NTR	8-Pin SOIC (2000/Reel)



### IX2127 Block Diagram

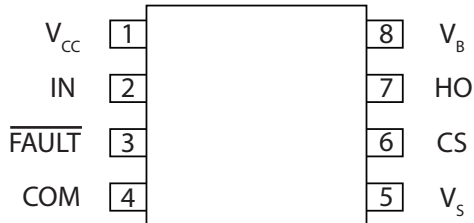


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## 1 Specifications

### 1.1 Package Pinout



### 1.2 Pin Description

Pin#	Name	Description
1	V <sub>CC</sub>	Logic Supply Voltage
2	IN	Logic Input
3	$\overline{\text{FAULT}}$	Fault Indicator Output
4	COM	Logic Ground
5	V <sub>S</sub>	High Side Return
6	CS	Comparator Input, Over-Current Detect
7	HO	High Side Gate Drive Output
8	V <sub>B</sub>	High Side Supply Voltage

### 1.3 Absolute Maximum Ratings

Unless otherwise specified, ratings are provided at T<sub>A</sub>=25°C and all bias levels are with respect to COM.

Parameter	Symbol	Minimum	Maximum	Units
Logic Supply Voltage	V <sub>CC</sub>	-0.3	15	V
High Side Floating Supply Voltage	V <sub>B</sub>	-0.3	625	
High Side Floating Offset Voltage	V <sub>S</sub>	V <sub>B</sub> -12	V <sub>B</sub> +0.3	
Logic Input Voltage	V <sub>IN</sub>	-0.3	V <sub>CC</sub> +0.3	
High Side Floating Output Voltage	V <sub>HO</sub>	V <sub>S</sub> -0.3	V <sub>B</sub> +0.3	
Current Sense Voltage	V <sub>CS</sub>	V <sub>S</sub> -0.3	V <sub>B</sub> +0.3	
$\overline{\text{FAULT}}$ Output Voltage	V <sub>FLT</sub>	-0.3	V <sub>CC</sub> +0.3	
Allowable Offset Supply Voltage Transient	dV <sub>S</sub> /dt	-	50	V/ns
Package Power Dissipation	P <sub>D</sub>	-	1	W
8-Lead DIP			0.625	
8-Lead SOIC				
Junction Temperature	T <sub>J</sub>	-	150	°C
Storage Temperature	T <sub>S</sub>	-55	150	

Absolute maximum electrical ratings are at 25°C

*Absolute maximum ratings are stress ratings. Stresses in excess of these ratings can cause permanent damage to the device. Functional operation of the device at conditions beyond those indicated in the operational sections of this data sheet is not implied.*

### 1.4 Recommended Operating Conditions

Parameter	Symbol	Minimum	Maximum	Units
Logic Supply	$V_{CC}$	9	12	V
High Side Floating Supply	$V_B$	$V_S+9$	$V_S+12$	
High Side Offset Voltage	$V_S$	-5	600	
Logic Input Voltage	$V_{IN}$	0	$V_{CC}$	
High Side Floating Output	$V_{HO}$	$V_S$	$V_B$	
Current Sense Signal Voltage	$V_{CS}$	$V_S$	$V_S+5$	
$\overline{FAULT}$ Output Voltage	$V_{FLT}$	0	$V_{CC}$	
Ambient Temperature	$T_A$	-40	+125	°C

### 1.5 General Conditions

Typical values are characteristic of the device at 25°C and are the result of engineering evaluations. They are provided for information purposes only and are not part of the manufacturing testing requirements.

Unless otherwise noted, all electrical specifications are listed for  $T_A=25^\circ\text{C}$ .

### 1.6 Electrical Characteristics

Unless otherwise specified, the test conditions are:  $V_{CC}=V_{BS}=12\text{V}$ ;  $V_{CC}$ , IN,  $\overline{FAULT}$ , and Leakage voltages and currents are referenced to COM;  $V_B$ , HO, and CS voltages and currents are referenced to  $V_S$ .

#### 1.6.1 Power Supply Specifications

Parameter	Conditions	Symbol	Minimum	Typical	Maximum	Units
Quiescent $V_{CC}$ Supply Current	$V_{IN}=0\text{V}$	$I_{QCC}$	-	280	400	$\mu\text{A}$
Quiescent $V_{BS}$ Supply Current	$V_{IN}=0\text{V}$	$I_{QBS}$	-	500	1000	
$V_{BS}$ UVLO Positive-Going Threshold	-	$V_{BS\_UV+}$	6.8	7.7	8.6	V
$V_{BS}$ UVLO Negative-Going Threshold	-	$V_{BS\_UV-}$	6.3	7.2	8.1	
Offset Supply Leakage Current	$V_B=V_S=600\text{V}$	$I_{LKG}$	-	-	2	$\mu\text{A}$

#### 1.6.2 Gate Drive and Shutdown Specifications

Parameter	Conditions	Symbol	Minimum	Typical	Maximum	Units
High Level Output Voltage, $V_B-V_{HO}$	$I_{HO}=0\text{A}$	$V_{OH}$	-	-	100	mV
Low Level Output Voltage, $V_{HO}$	$I_{HO}=0\text{A}$	$V_{OL}$	-	-	100	
Output Short Circuit Pulsed Current	$V_{HO}=0\text{V}$ , $V_{IN}=5\text{V}$ , $PW \leq 10\mu\text{s}$ , $R_{GATE}=20\Omega^*$ (see Figure 1)	$I_{HO+}$	-200	-250	-	mA
	$V_{HO}=12\text{V}$ , $V_{IN}=0\text{V}$ , $PW \leq 10\mu\text{s}$ , $R_{GATE}=20\Omega^*$ (see Figure 1)	$I_{HO-}$	420	500	-	
CS Input, Positive-Going Threshold	$V_{CC}=9\text{V}$ to $12\text{V}$	$V_{CS\_TH+}$	180	260	320	mV
"High" CS Bias Current	$V_{CS}=3\text{V}$	$I_{CS+}$	-	-	1	$\mu\text{A}$
	$V_{CS}=0\text{V}$	$I_{CS-}$	-	-	-1	

\*  $R_{GATE}$  value must be  $20\Omega$  or greater.

1.6.3 Logic I/O Specifications

Parameter	Conditions	Symbol	Minimum	Typical	Maximum	Units
Logic "1" Input Voltage	$V_{CC}=9V$ to $12V$	$V_{IH}$	3.0	-	-	V
Logic "0" Input Voltage	$V_{CC}=9V$ to $12V$	$V_{IL}$	-	-	0.8	V
Logic "1" Input Bias Current	$V_{IN}=5V$	$I_{IN+}$	-	2.6	15	$\mu A$
Logic "0" Input Bias Current	$V_{IN}=0V$	$I_{IN-}$	-	-	-1	$\mu A$
FAULT On-Resistance	-	FLT, $R_{ON}$	-	72	-	$\Omega$

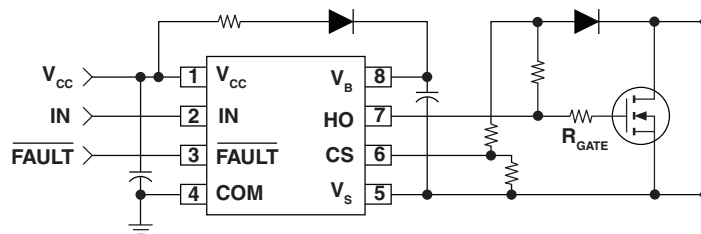
1.6.4 Thermal Specifications

Parameter	Conditions	Symbol	Minimum	Typical	Maximum	Units
Thermal Resistance, Junction to Ambient: 8-Lead DIP 8-Lead SOIC	-	$R_{\theta JA}$	-	-	125 200	$^{\circ}C/W$

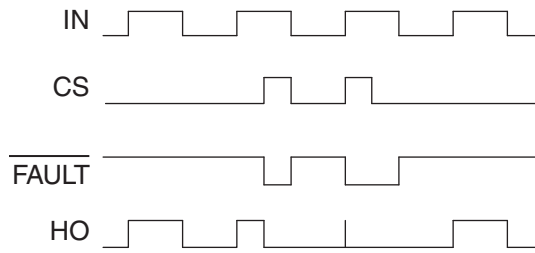
1.7 Timing Characteristics

Parameter	Conditions	Symbol	Minimum	Typical	Maximum	Units
Turn-On Propagation Delay	$V_{CC}=V_{BS}=12V$ , $C_L=1nF$ , $T_A=25^{\circ}C$	$t_{on}$	-	100	200	ns
Turn-Off Propagation Delay		$t_{off}$	-	73	200	
Turn-On Rise Time		$t_r$	-	23	130	
Turn-Off Fall Time		$t_f$	-	20	65	
Start-Up Blanking Delay		$t_{blk}$	550	766	950	
CS Shutdown Propagation Delay		$t_{CS}$	-	220	360	
CS to FLT Propagation Delay		$t_{FLT}$	-	236	510	

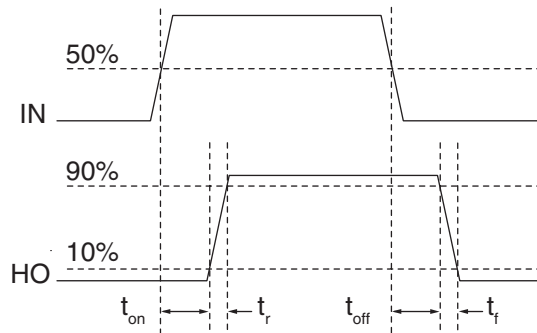
Figure 1. Typical Connection Diagram



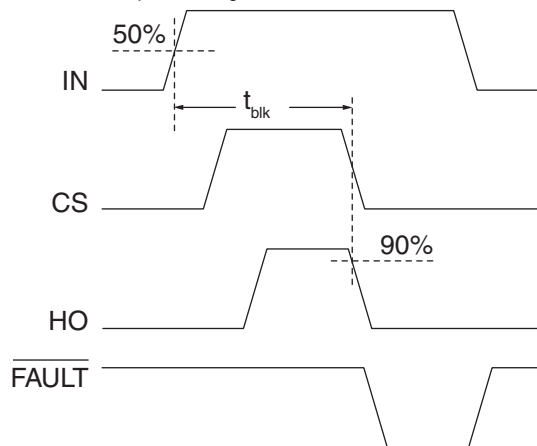
1.7.1 I/O Timing Diagram



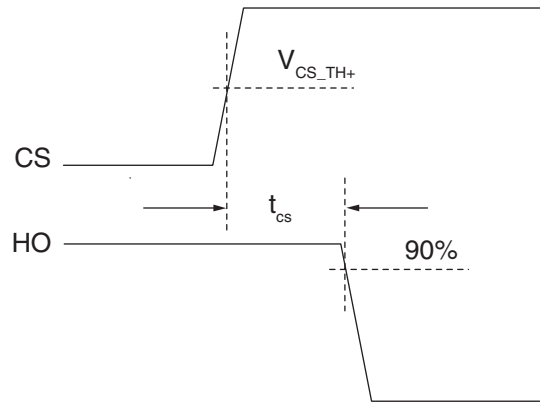
1.7.2 Switching Time Waveforms



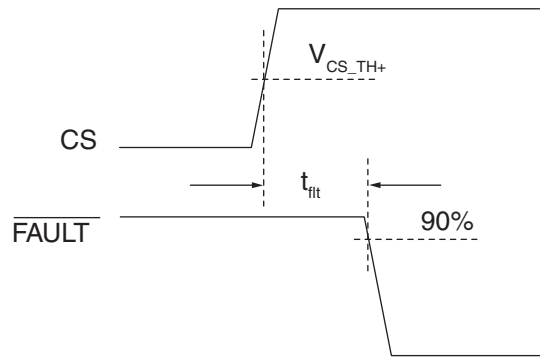
1.7.3 Startup Blanking Time Waveforms



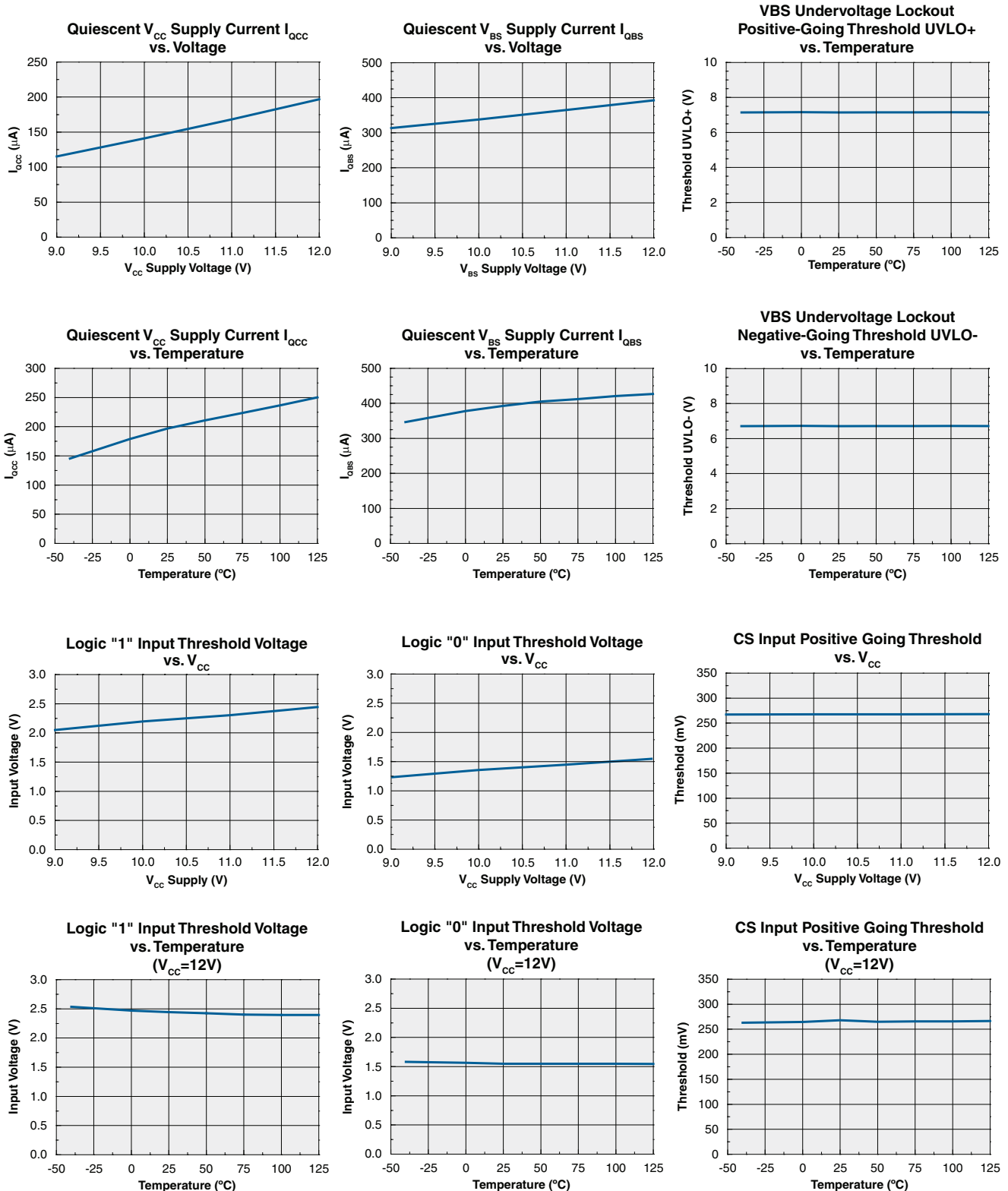
1.7.4 CS Shutdown Waveforms

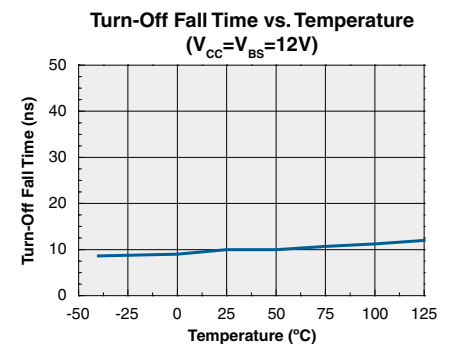
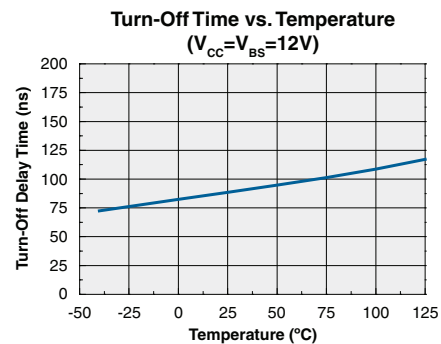
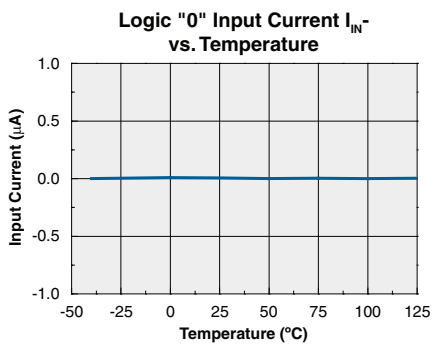
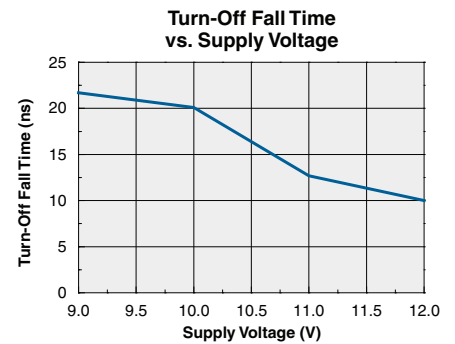
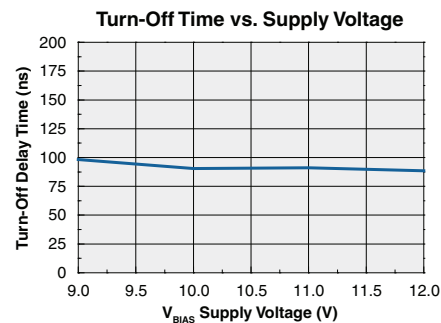
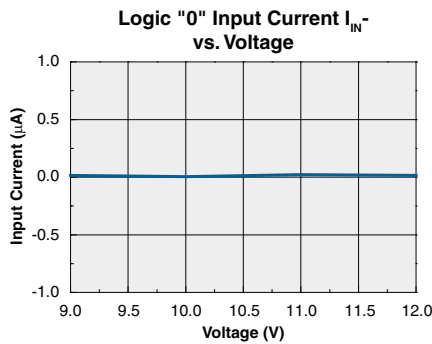
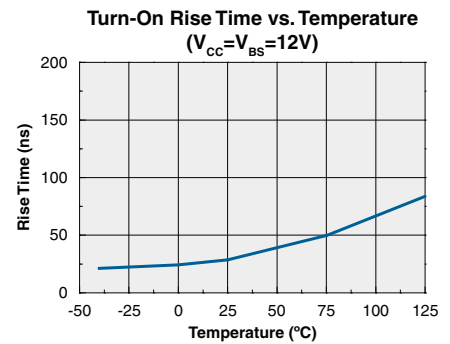
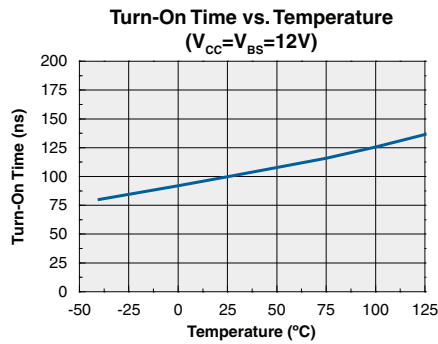
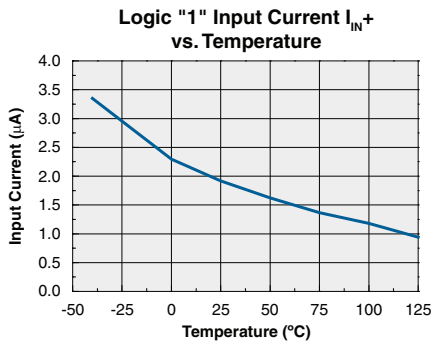
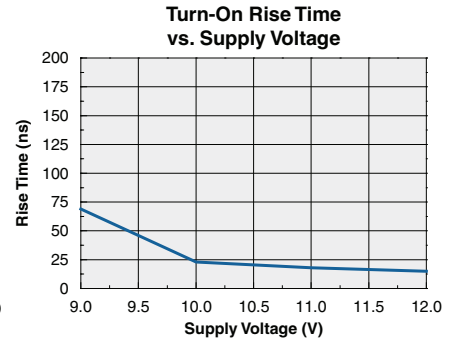
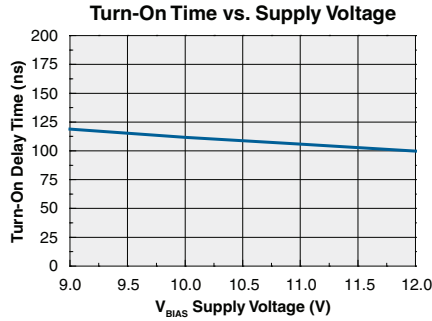
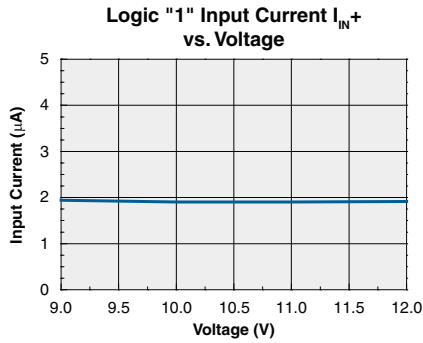


1.7.5 CS to FLT Waveforms

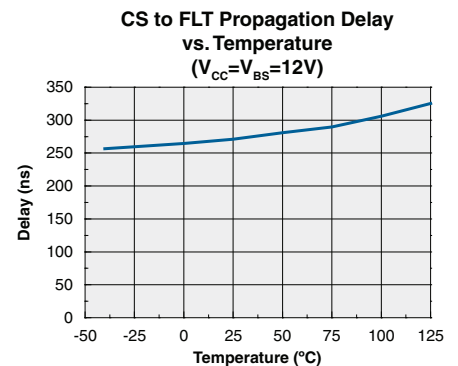
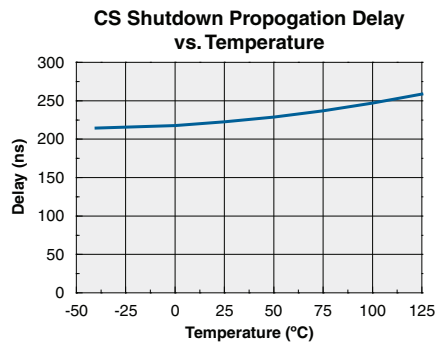
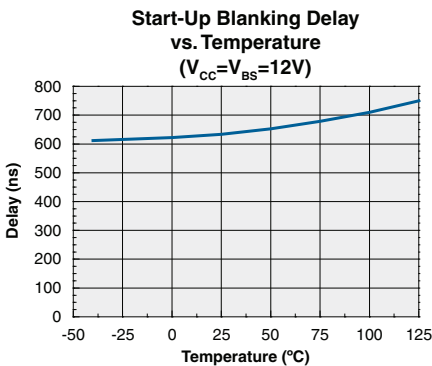
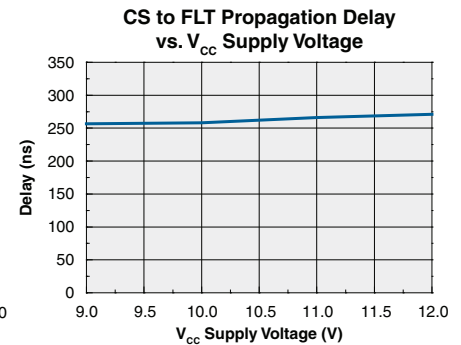
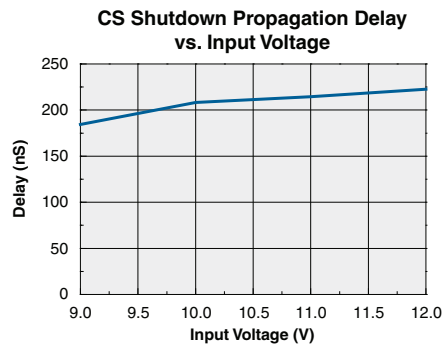
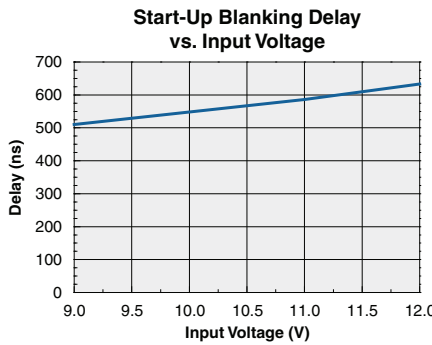
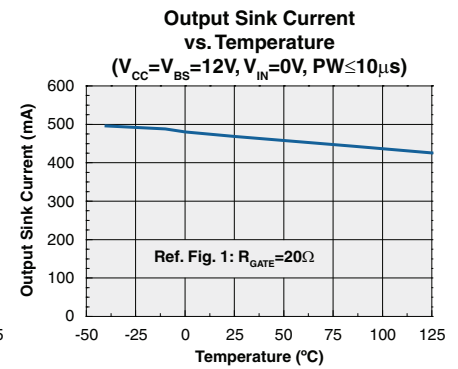
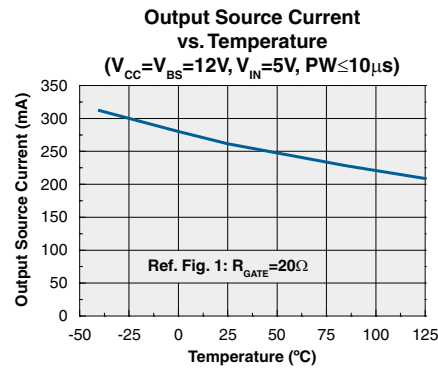
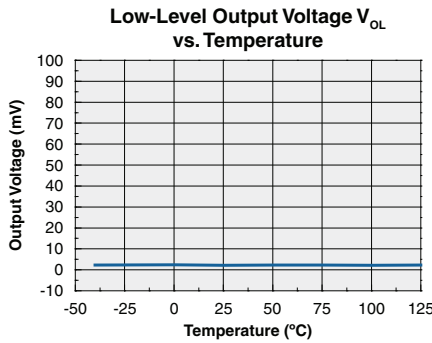
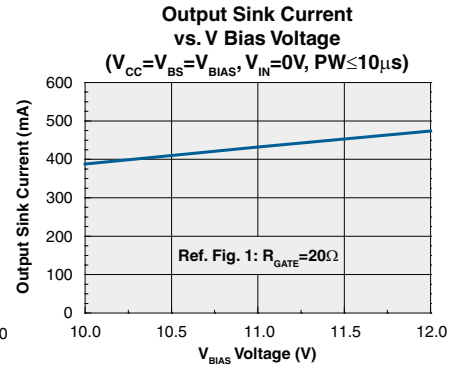
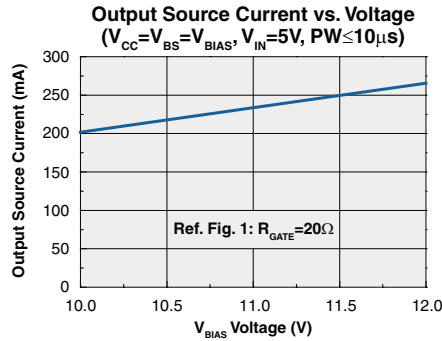
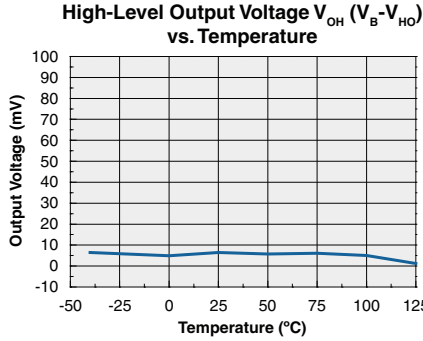


2 Performance Data









### 3 Manufacturing Information

#### 3.1 Moisture Sensitivity



All plastic encapsulated semiconductor packages are susceptible to moisture ingress. Clare classified all of its plastic encapsulated devices for moisture sensitivity according to the latest version of the joint industry standard, **IPC/JEDEC J-STD-020**, in force at the time of product evaluation. We test all of our products to the maximum conditions set forth in the standard, and guarantee proper operation of our devices when handled according to the limitations and information in that standard as well as to any limitations set forth in the information or standards referenced below.

Failure to adhere to the warnings or limitations as established by the listed specifications could result in reduced product performance, reduction of operable life, and/or reduction of overall reliability.

This product carries a **Moisture Sensitivity Level (MSL) rating** as shown below, and should be handled according to the requirements of the latest version of the joint industry standard **IPC/JEDEC J-STD-033**.

Device	Moisture Sensitivity Level (MSL) Rating
IX2127G / IX2127N	MSL 1

#### 3.2 ESD Sensitivity



This product is **ESD Sensitive**, and should be handled according to the industry standard **JESD-625**.

#### 3.3 Reflow Profile

This product has a maximum body temperature and time rating as shown below. All other guidelines of **J-STD-020** must be observed.

Device	Maximum Temperature x Time
IX2127G	250°C for 30 seconds
IX2127N	260°C for 30 seconds

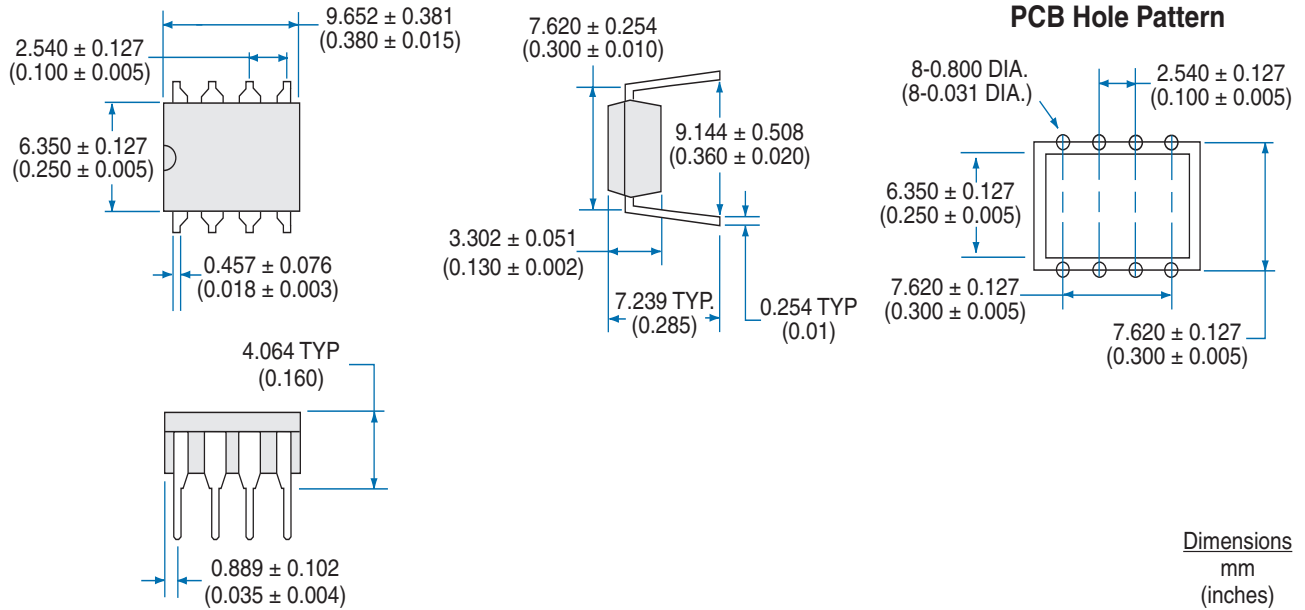
#### 3.4 Board Wash

Clare recommends the use of no-clean flux formulations. However, board washing to remove flux residue is acceptable, and the use of a short drying bake may be necessary. Chlorine-based or Fluorine-based solvents or fluxes should not be used. Cleaning methods that employ ultrasonic energy should not be used.

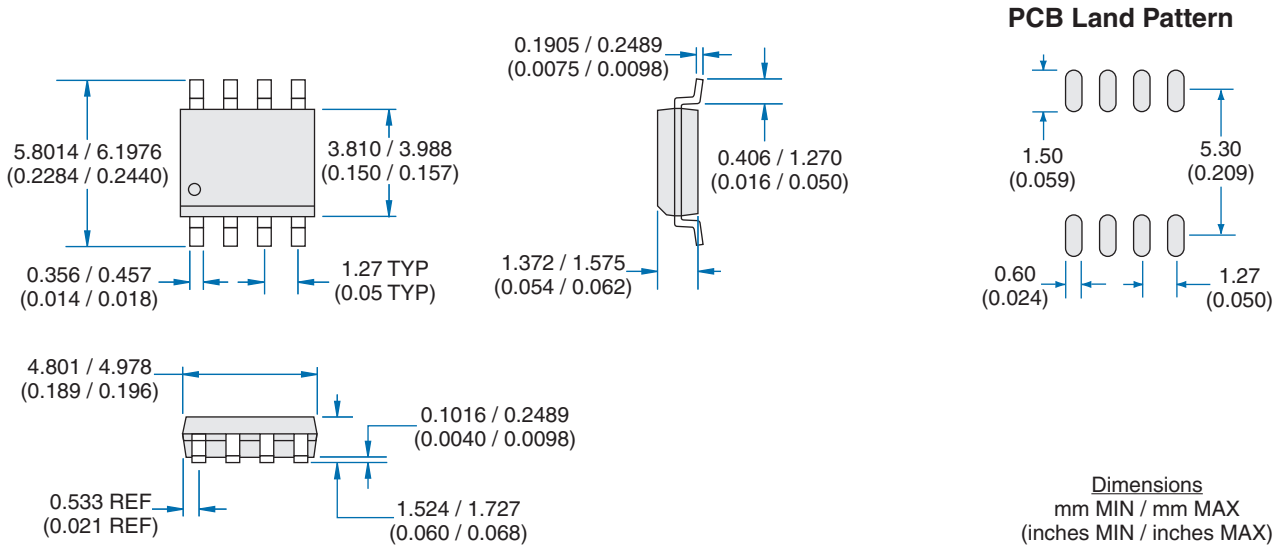


### 3.5 Mechanical Dimensions

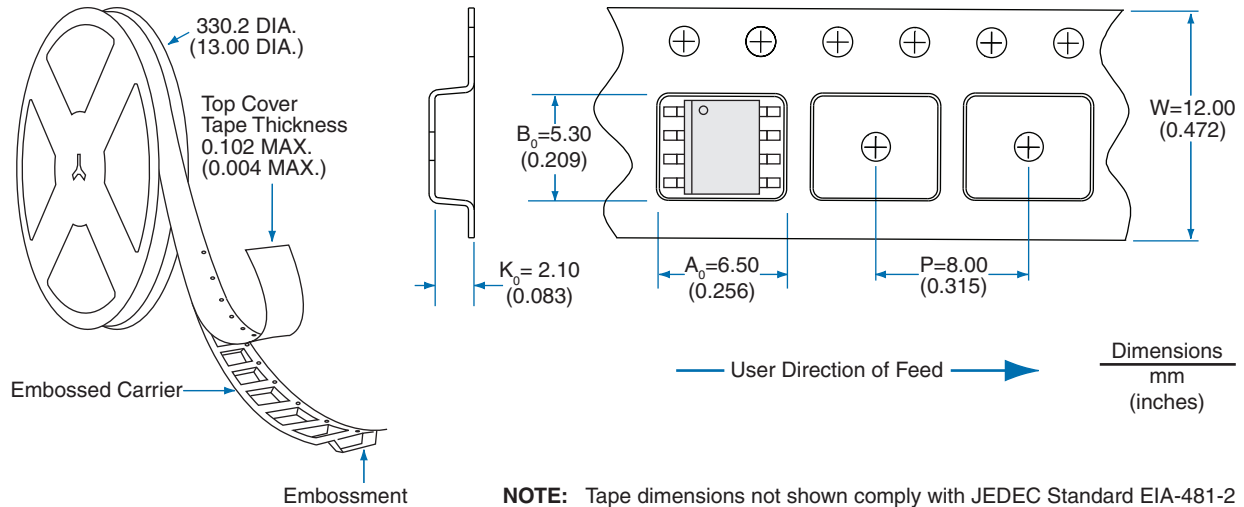
#### 3.5.1 8-Pin DIP Through-Hole Package



#### 3.5.2 8-Pin SOIC Package



3.5.3 Tape & Reel Packaging for 8-Pin SOIC Package



For additional information please visit our website at: [www.clare.com](http://www.clare.com)

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