1.5A DDR Termination Regulator

FEATURES

- Source and sink current capability of 1.5A
- Low output voltage offset, ±20mV
- High accuracy output voltage at full-load
- V_{OUT} adjustable by external resistors
- Low external component count
- Current limit protection
- Thermal protection
- SO-8 package

APPLICATIONS

- Mother Board
- Graphic Cards
- DDR Termination Voltage Supply - supports DDR1 (1.25V_{TT}), DDR2 (0.9V_{TT}), and meets JEDEC SSTL-2 and SSTL-3 term. specifications

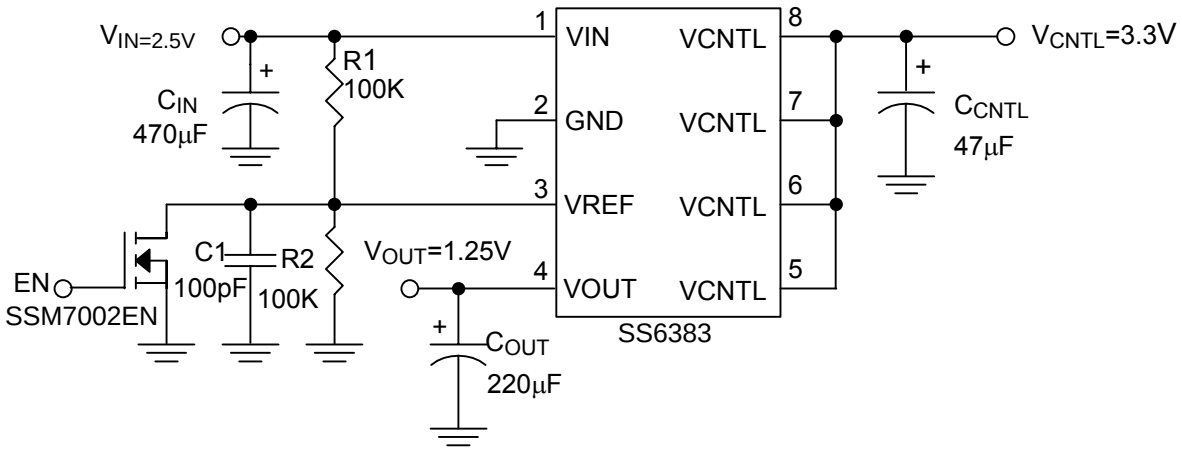
DESCRIPTION

The SS6383 linear regulator is designed to provide 1.5A source and sink current while regulating an output voltage to within 25mV.

The SS6383 converts voltage supplies ranging from 1.6V to 6V into an output voltage that is set by two external voltage-divider resistors. It provides an excellent voltage source for active termination schemes for high-speed transmission lines such as those seen in high-speed memory buses.

The built-in current-limiting in source and sink mode, together with thermal shutdown, provides maximum protection to the SS6383 against fault conditions.

TYPICAL APPLICATION CIRCUIT



This device is available with Pb-free lead finish (second-level interconnect) as SS6383GS

ORDERING INFORMATION

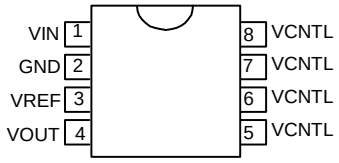
SS6383XX XX

- Packing
  - TR: Tape and reel
- Package type
  - CS: SO-8, Commercial
  - GS: SO-8, Commercial with Pb-free lead finish

Example: SS6383GSTR
→ in SO-8 package with Pb-free lead finish
shipped on tape and reel

PIN CONFIGURATION

SO-8
TOP VIEW



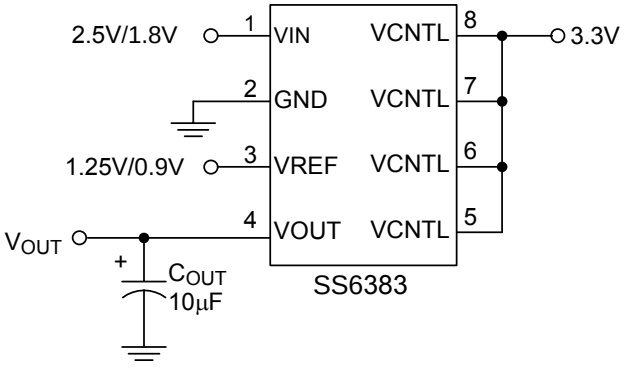
ABSOLUTE MAXIMUM RATINGS

Supply Voltage		-0.4V to 7V
Operating Temperature Range		-40°C~85°C
Junction Temperature Range		125°C
Lead Temperature (Solder, 10sec)		260°C
Storage Temperature Range		-65°C ~150°C
Thermal Resistance .JC	SO-8	40°C /W
Thermal Resistance θ_{JA}	SO-8	160°C /W

(Assumes no ambient airflow, no heatsink)

Note1: Any stress beyond these Absolute Maximum Ratings may cause permanent damage to the device.

TEST CIRCUIT



ELECTRICAL CHARACTERISTICS

(V_{CNTL}=3.3V, V_{IN}=2.5V, V_{REF}=0.5V_{IN}, C_{OUT}=10µF, T_A=25°C, unless otherwise specified) (Note 1)

PARAMETER	TEST CONDITIONS	SYMBOL	MIN.	TYP.	MAX.	UNIT
Input Voltage (DDR1/2)	Keep $V_{CNTL} \geq V_{IN}$ during power on and off sequences	V_{IN}	1.6	2.5/1.8		V
		V_{CNTL}	3.0	3.3	6	
Output Voltage	I_{OUT} = 0mA	V_{OUT}		V_{REF}		V
Output Voltage Offset	I_{OUT} = 0mA **(Note 2)**	V_{OS}	-20		20	mV
Load Regulation (DDR1/2) **(Note 3)**	I_{OUT} =0.1mA ~ +1.5A	ΔV_{LOR}		10	25	mV
	I_{OUT} = 0.1mA ~ -1.5A			10	25	
Quiescent Current	V_{REF}<0.2V, V_{OUT} = OFF	I_Q		8	30	µA
Operating Current of V_{CNTL}	No load	I_{CNTL}		3	10	mA
V_{REF} Bias Current	V_{REF}=1.25V				1	µA
Current Limit **(Note 4)**		I_{IL}	2.1	3	4.5	A
THERMAL PROTECTION						
Thermal Shutdown Temperature	3.3V≤V_{CNTL}≤5V	T_{SD}	125	150		°C
Thermal Shutdown Hysteresis	Guaranteed by design			30		°C
SHUTDOWN SPECIFICATIONS						
Shutdown Threshold	Output ON (V_{REF}=0V→1.25V)		0.8			V
	Output OFF (V_{REF}=1.25V→0V)				0.2	

Note 1: Specifications are production-tested at T_A=25°C. Specifications over the -40°C to 85°C operating temperature range are assured by design, characterization and correlation with Statistical Quality Controls (SQC).

Note 2: V_{OS} is the difference between V_{OUT} and V_{REF}.

Note 3: Load regulation is measured at constant junction temperature, using pulse testing with a low duty cycle.

Note 4: Current limit is measured using a low duty cycle.

Note 5: To operate safely, V_{CNTL} must always be greater than V_{IN}.

TYPICAL PERFORMANCE CHARACTERISTICS

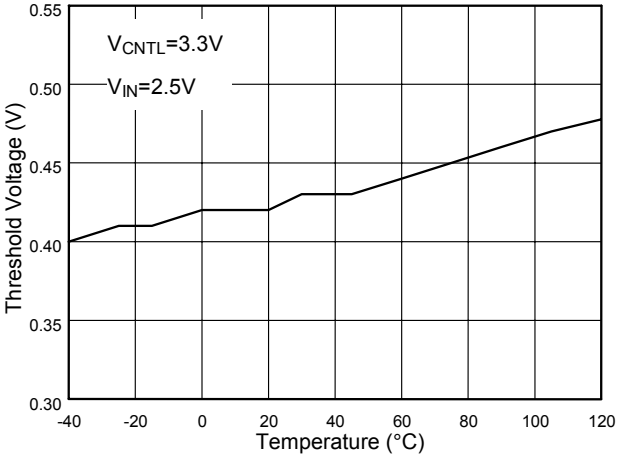


Fig. 1 Turn-On Threshold vs. Temp.

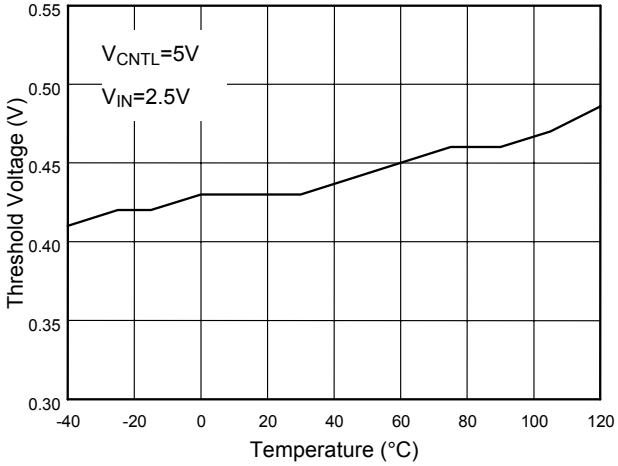


Fig. 2 Turn-On Threshold vs. Temp

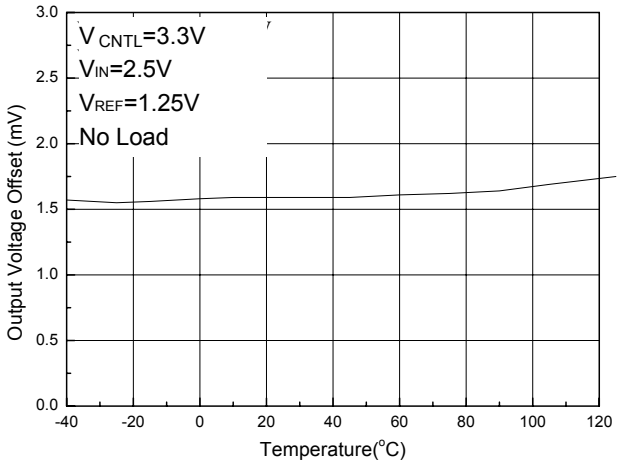


Fig. 3 Output Voltage Offset vs. Temperature

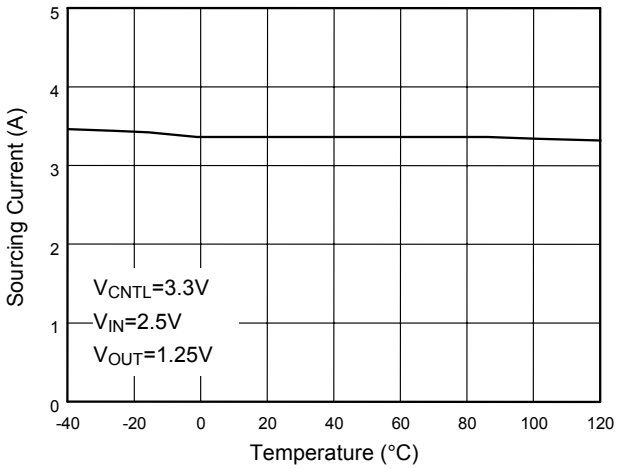


Fig. 4 Current-Limit (Sourcing) vs. Temperature

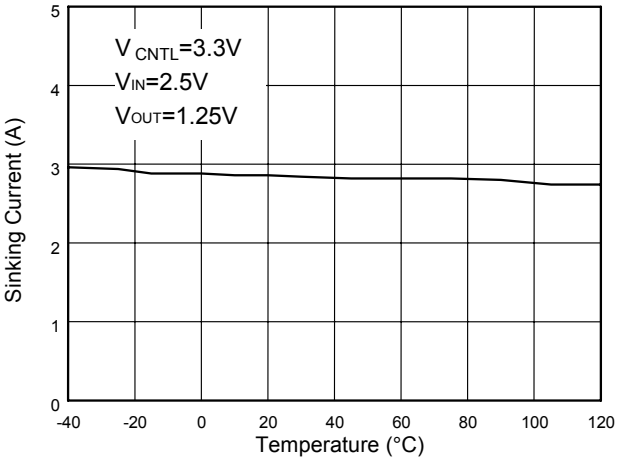


Fig. 5 Current-Limit (Sinking) vs. Temperature

TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

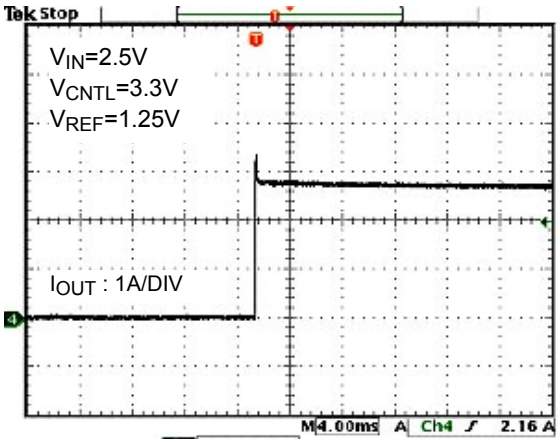


Fig. 6 Output Short-Circuit (Sinking)

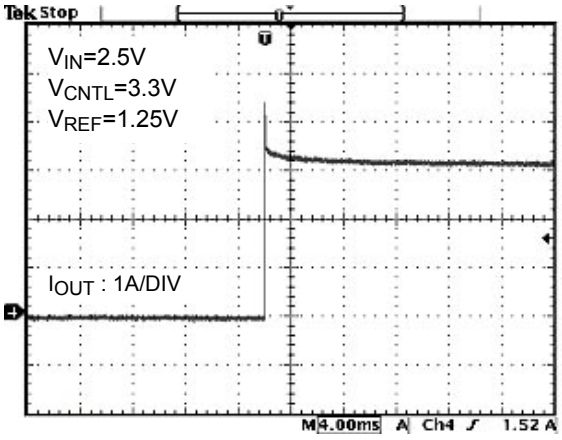


Fig. 7 Output Short-Circuit Protection (Sourcing)

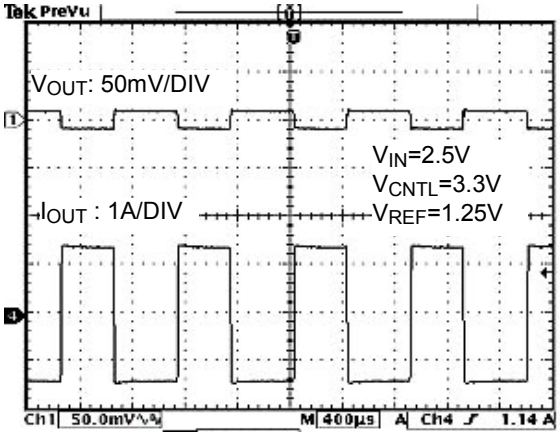


Fig. 8 Transient Response at $1.25V_{TT}$/1.5A

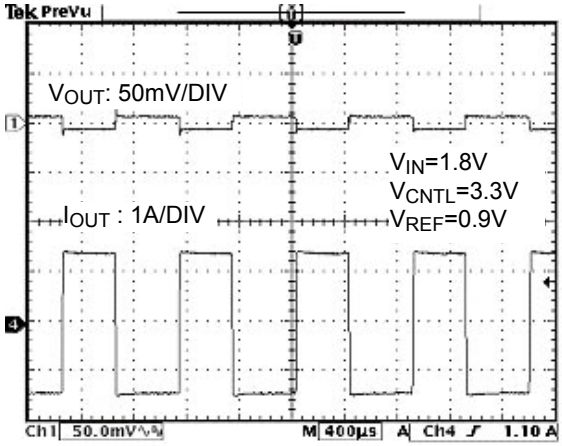
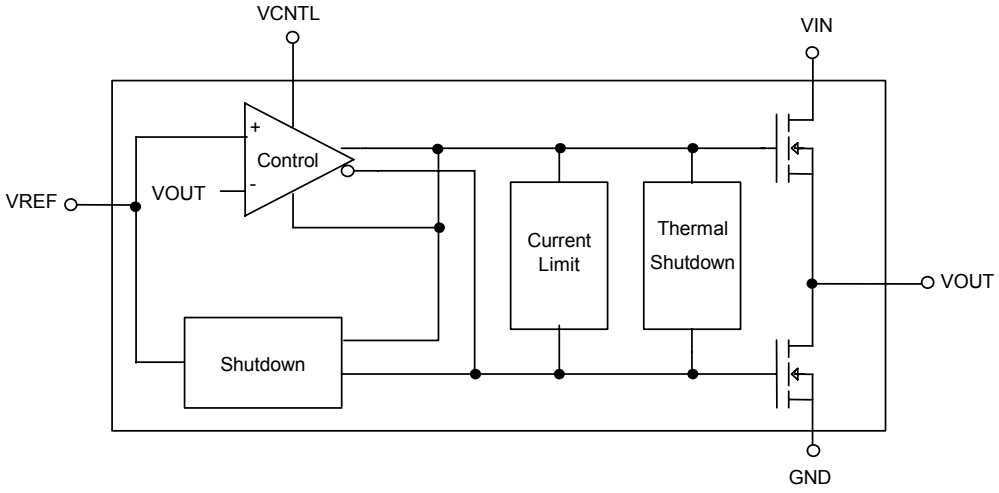


Fig. 9 Transient Response at $0.9V_{TT}$/1.5A

BLOCK DIAGRAM



PIN DESCRIPTIONS

PIN 1: VIN - Input supply pin - provides power to create the external reference voltage using a resistor divider for regulating V_{REF} and V_{OUT}.

PIN 2: GND - Ground pin.

PIN 3: VREF - Reference voltage input. Pull this pin low to shut the device down.

PIN 4: VOUT - Output pin.

PIN 5~8: VCNTL - Input supply pin - supplies all the internal control circuitry.

APPLICATION INFORMATION

Layout Consideration

The SS6383 is in an SO-8 package and is unable to dissipate heat easily when operating with high currents. In order to avoid exceeding the maximum junction temperature, an appropriate area of copper must be used.

The large copper area around the V_{CNTL} pins can be used to assist the heat dissipation. Vias to lead heat into the bottom layer are also recommended.

All capacitors should be placed as close to the relative IC pin as possible.

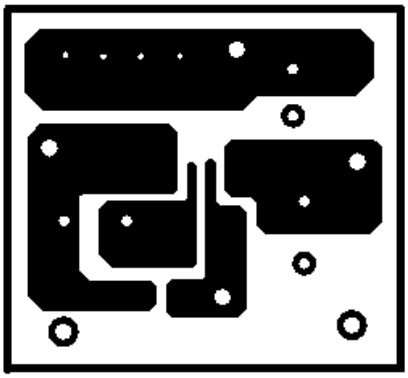


Fig. 10. Top layer

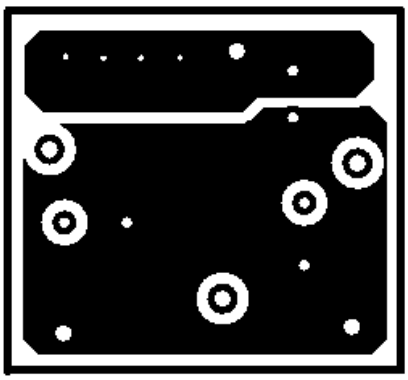


Fig. 11. Bottom layer

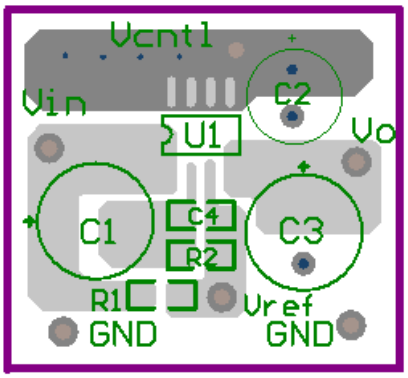
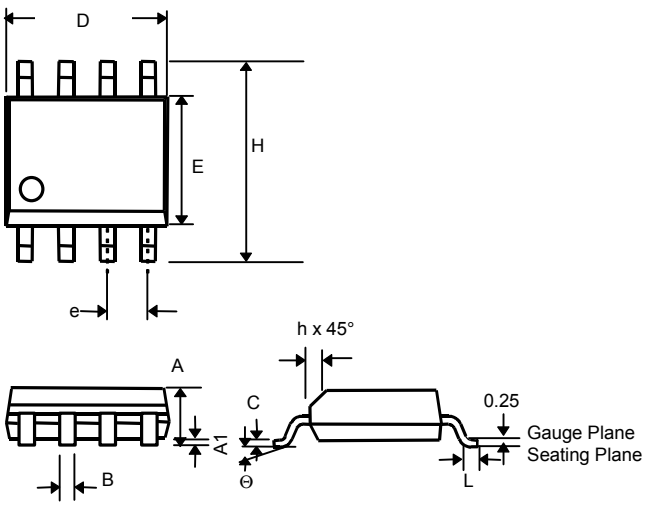


Fig. 12. Placement

PHYSICAL DIMENSIONS (unit: mm)

SO-8



SYMBOL	MIN	MAX
A	1.35	1.75
A1	0.10	0.25
B	0.33	0.51
C	0.19	0.25
D	4.80	5.00
E	3.80	4.00
e	1.27BSC	
H	5.80	6.20
h	0.25	0.50
L	0.40	1.27
Θ	0°	8°