



ST8024T

COM/SEG LCD Driver

Datasheet

Version 0.12

2008/01/24

P r e l i m i n a r y

Note: Sitronix Technology Corp. reserves the right to change the contents in this document without prior notice. This is not a final specification. Some parameters are subject to change.

1. FEATURES

- Number of LCD drive outputs: 240
- Supply voltage for LCD drive: +15.0 to +30.0 V
- Supply voltage for the logic system: +2.5 to +5.5 V
- Low power consumption
- Low output impedance

(Segment mode)

- Shift clock frequency
 - 15MHz(MAX.): $V_{DD} = +5.0 \pm 0.5V$
 - 12MHz(MAX.): $V_{DD} = +3.0$ to $+ 4.5V$
 - 8MHz(MAX.): $V_{DD} = +2.5$ to $+ 3.0V$
- Adopts a data bus system
- 4-bit/8-bit parallel input modes are selectable with a mode (MD) pin
- Automatic transfer function of an enable signal
- Automatic counting function which, in the chip selection mode, causes the internal clock to be stopped by automatically counting 240 bits of input data
- Line latch circuits are reset when /DISPOFF active

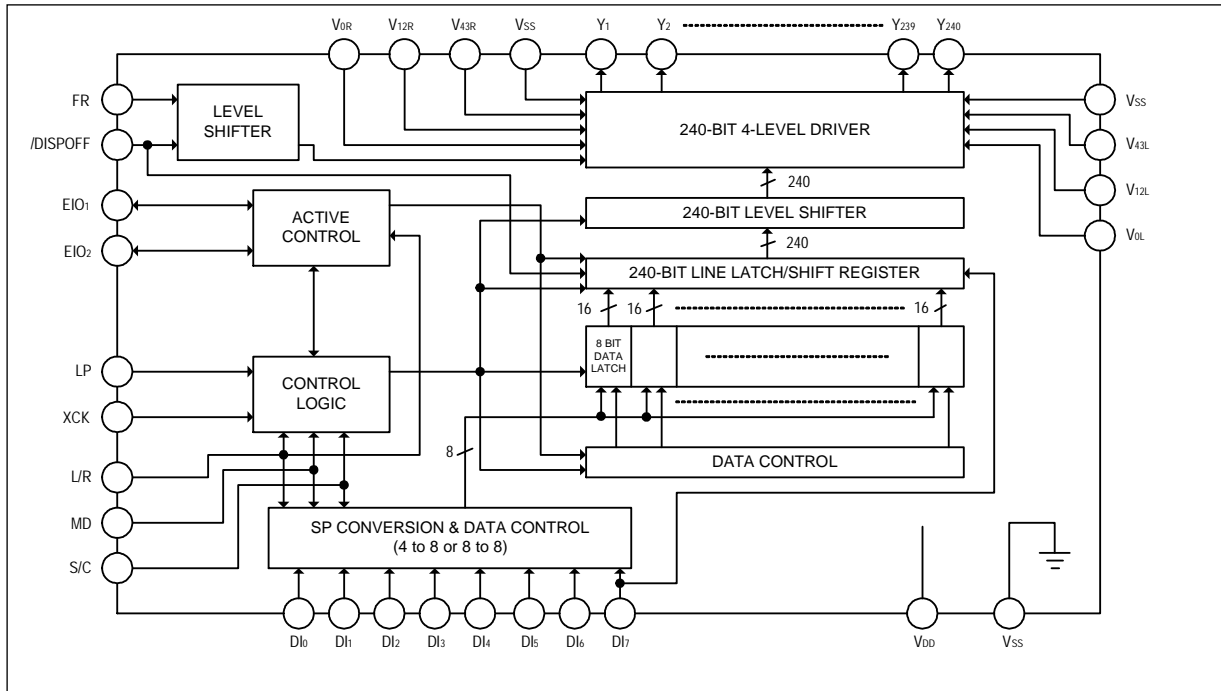
(Common mode)

- Shift clock frequency: 4 MHz (MAX.)
 - Built-in 240-bit bi-directional shift register (divisible into 120 bits x 2)
 - Available in a single mode (240-bit shift register) or in a dual mode (120-bit shift register x 2)
 - Y1->Y240 Single mode
 - Y240->Y1 Single mode
 - Y1->Y120, Y121->Y240 Dual mode
 - Y240->Y121, Y120->Y1 Dual mode
- The above 4 shift directions are pin-selectable
- Shift register circuits are reset when /DISPOFF active

2. DESCRIPTION

The ST8024T is a 240-output segment/common driver IC suitable for driving large/medium scale dot matrix LCD panels, and is used in personal computers/work stations. The ST8024T is good both as a segment driver and a common driver, and it can create a low power consuming, high-resolution LCD.

3. BLOCK DIAGRAM



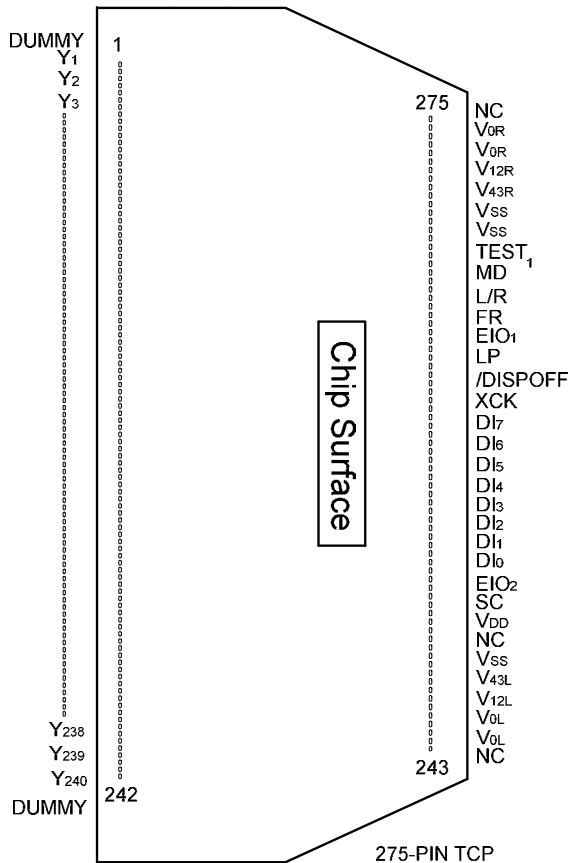
4. FUNCTIONAL OPERATIONS OF EACH BLOCK

BLOCK	FUNCTION
Active Control	In case of segment mode, controls the selection or non-selection of the chip. Following an LP signal input, and after the chip selection signal is input, a selection signal is generated internally until 240 bits of data have been read in. Once data input has been completed, a selection signal for cascade connection is output, and the chip is non-selected. In case of common mode, controls the input/output data of bi-directional pins.
SP Conversion & Data Control	In case of segment mode, keeps input data which are 2 clocks of XCK at 4-bit parallel input mode in latch circuit, or keeps input data which are 1 clock of XCK at 8-bit parallel input mode in latch circuit; after that they are put on the internal data bus 8 bits at a time.
Data Latch Control	In case of segment mode, selects the state of the data latch which reads in the data bus signals. The shift direction is controlled by the control logic. For every 16 bits of data read in, the selection signal shifts one bit based on the state of the control circuit.
Data Latch	In case of segment mode, latches the data on the data bus. The latch state of each LCD drive output pin is controlled by the control logic and the data latch control; 240 bits of data are read in 30 sets of 8 bits.
Line Latch/Shift Register	In case of segment mode, all 240 bits which have been read into the data latch are simultaneously latched at the falling edge of the LP signal, and are output to the level shifter block. In case of common mode, shifts data from the data input pin at the falling edge of the LP signal.
Level Shifter	The logic voltage signal is level-shifted to the LCD drive voltage level, and is output to the driver block.
4-Level Driver	Drives the LCD drive output pins from the line latch/shift register data, and selects one of 4 levels (V0, V12, V43 or VSS) based on the S/C, FR and /DISPOFF signals.
Control Logic	Controls the operation of each block. In case of segment mode, when an LP signal has been input, all blocks are reset and the control logic waits for the selection signal output from the active control block. Once the selection signal has been output, operation of the data latch and data transmission is controlled, 240 bits of data are read in, and the chip is non-selected. In case of common mode, controls the direction of data shift.

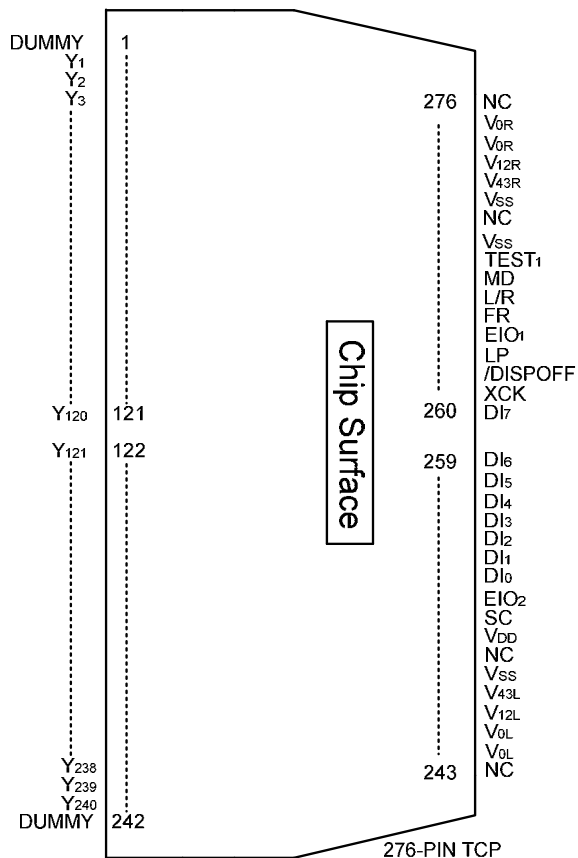
5. PIN DESCRIPTION (TCP TYPE)

SYMBOL	I/O	DESCRIPTION
Y ₁ -Y ₂₄₀	O	LCD drive output
V _{0L} , V _{0R}	P	Power supply for LCD drive
V _{12L} , V _{12R}	P	Power supply for LCD drive
V _{43L} , V _{43R}	P	Power supply for LCD drive
L/R	I	Display data shift direction selection
V _{DD}	P	Power supply for logic system (+2.5 to +5.5 V)
S/C	I	Segment mode/common mode selection
EIO ₂ , EIO ₁	I/O	Input/output for chip selection at segment mode Shift data input/output for shift register at common mode
DI ₀ -DI ₆	I	Display data input at segment mode
DI ₇	I	Display data input at segment mode/Dual mode data input at common mode
XCK	I	Clock input for taking display data at segment mode
/DISPOFF	I	Control input for output of non-select level
LP	I	Latch pulse input for display data at segment mode/ Shift clock input for shift register at common mode
FR	I	AC-converting signal input for LCD drive waveform
MD	I	4 or 8 bits mode selection input
V _{SS}	P	Ground (0 V)
TEST1, TEST2	I	Connect to GND or floating

PS : Detail size see TCP drawing data



ST8024 F14 TCP



ST8024 F4 TCP

6. INPUT/OUTPUT CIRCUITS

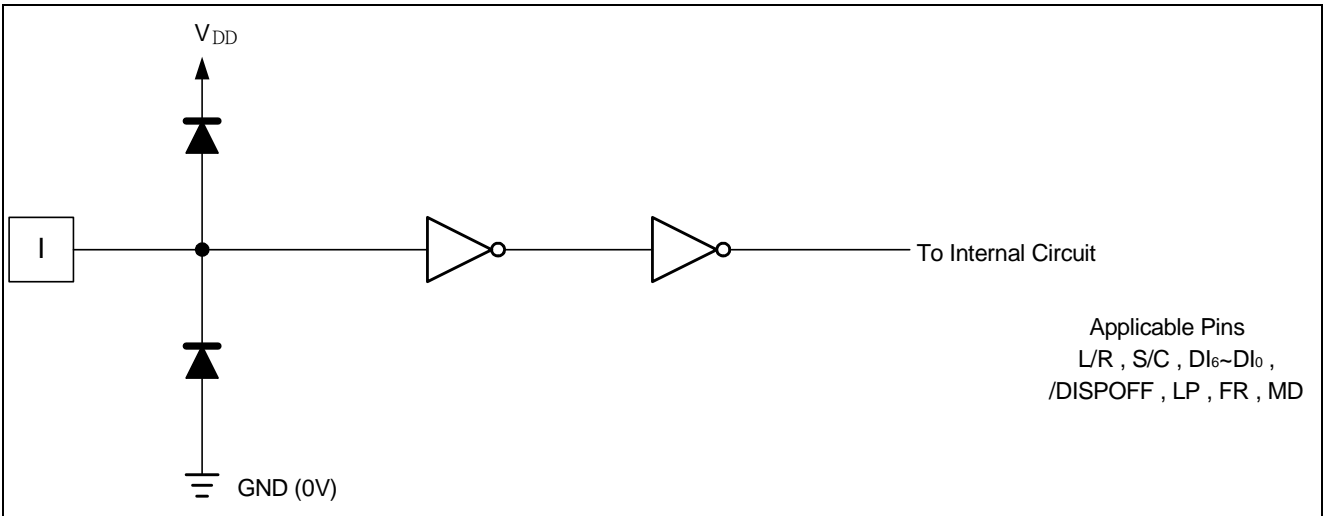


Figure 1 Input Circuit (1)

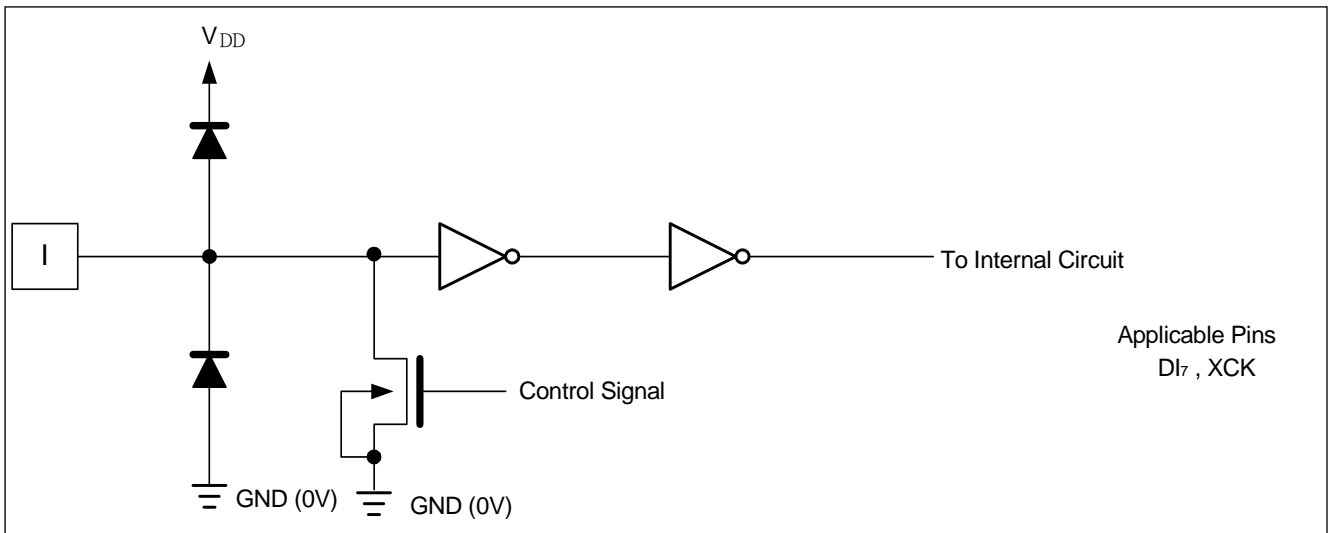


Figure 2 Input Circuit (2)

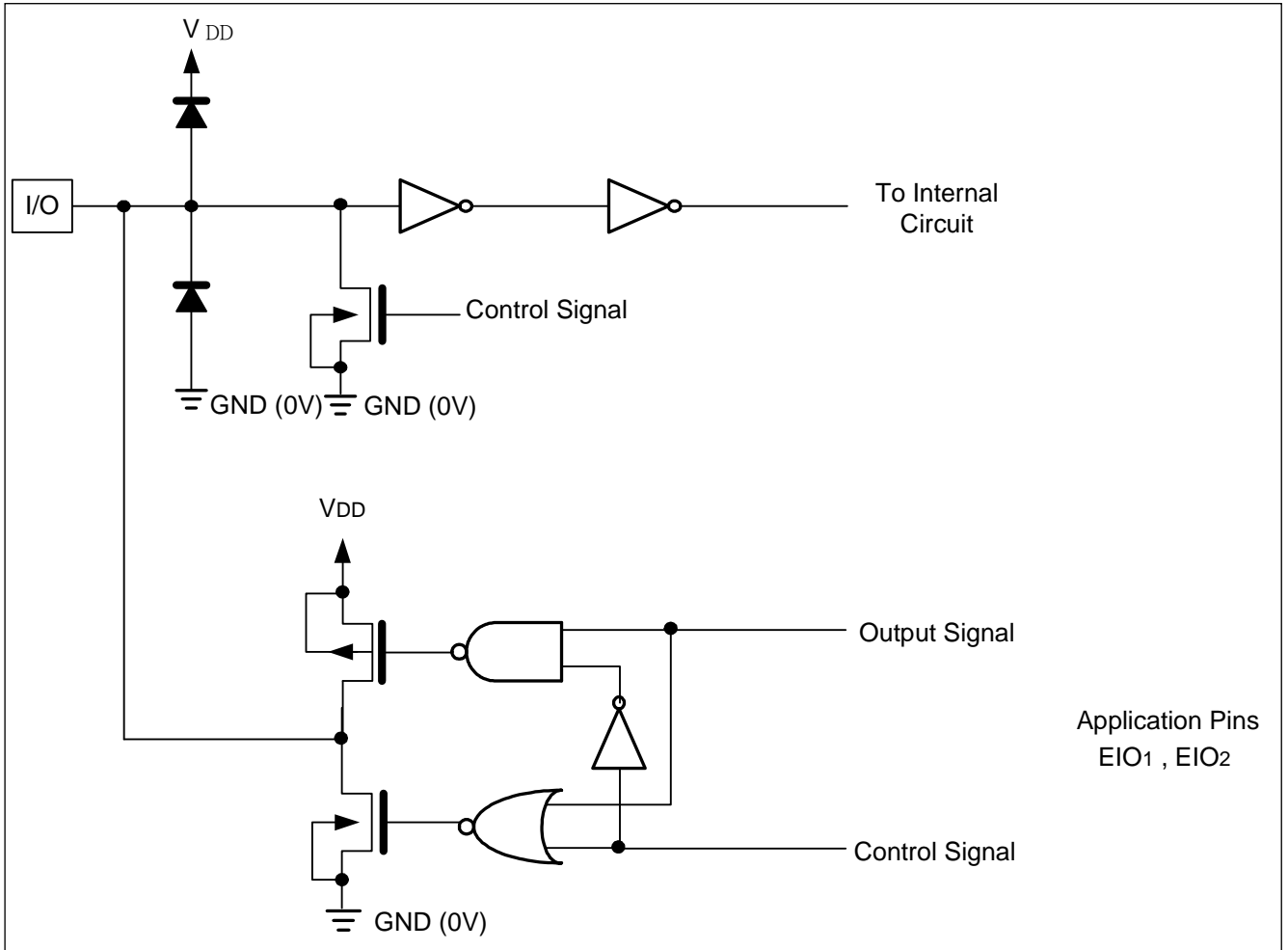


Figure 3 Input/Output Circuit

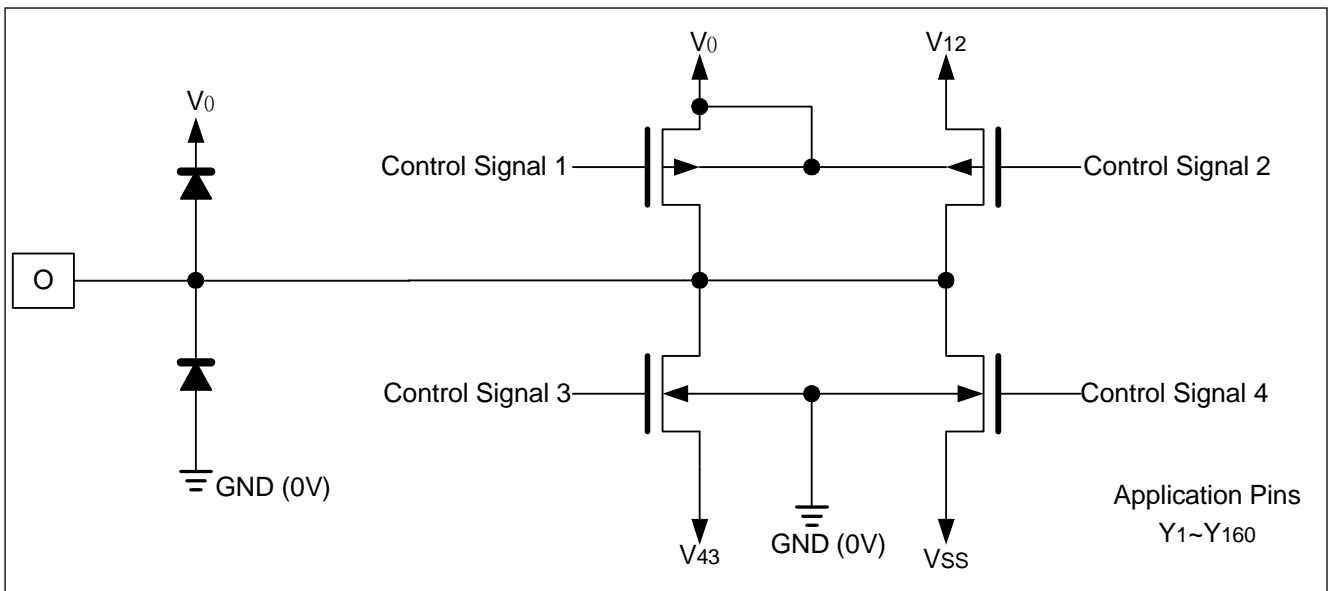


Figure 4 LCD Drive Output Circuit

7. FUNCTIONAL DESCRIPTION

7.1 Pin Functions

(Segment mode)

SYMBOL	FUNCTION
V _{DD}	Logic system power supply pin, • Connected to +2.5 to +5.5 V.
GND	Ground pin
LGND	Logic ground pin • Do not short LGND with GND and V _{SS} by ITO on LCD panel • Connect it to GND on PCB or FPC.
V _{SS}	Connect to GND by ITO on LCD panel.
V _{0L} , V _{0R} V _{12L} , V _{12R} V _{43L} , V _{43R}	Bias power supply pins for LCD drive voltage • Normally use the bias voltages set by a resistor divider • Ensure that voltages are set such that V _{SS} < V ₄₃ < V ₁₂ < V ₀ . • V _{iL} and V _{iR} (i = 0, 12, 43) must connect to an external power supply, and supply regular voltage which is assigned by specification for each power pin
DI7-DI0	Input pins for display data • In 4-bit parallel mode, DI3-DI0 are the display data input pins, and DI7-DI4 must be connected to LGND or V _{DD} . • In 8-bit parallel mode, All DI7-DI0 pins are the display data input pins. • Refer to section 7.2.2.
XCK	Clock input pin for taking display data • Data is read at the falling edge of the clock pulse.
LP	Latch pulse input pin for display data • Data is latched at the falling edge of the clock pulse.
L/R	Input pin for selecting the reading direction of display data • When set to LGND level "L", data is read sequentially from Y ₂₄₀ to Y ₁ . • When set to V _{DD} level "H", data is read sequentially from Y ₁ to Y ₂₄₀ . Refer to section 7.2.2.
/DISPOFF	Control input pin for output of non-select level • The input signal is level-shifted from logic voltage level to LCD drive voltage level, and controls the LCD drive circuit. • When set to LGND level "L", the LCD drive output pins (Y ₁ -Y ₂₄₀) are set to level V _{SS} . • When set to "L", the contents of the line latch are reset, but the display data are read in the data latch regardless of the condition of /DISPOFF. When the /DISPOFF function is canceled, the driver outputs non-select level (V ₁₂ or V ₄₃), then outputs the contents of the data latch at the next falling edge of the LP. At that time, if /DISPOFF removal time does not correspond to what is shown in AC characteristics, it can not output the reading data correctly. • Table of truth values is shown in "TRUTH TABLE" in Functional Operations.
FR	AC signal input pin for LCD drive waveform • The input signal is level-shifted from logic voltage level to LCD drive voltage level, and controls the LCD drive circuit. • Normally it inputs a frame inversion signal. • The LCD drive output pins' output voltage levels can be set using the line latch output signal and the FR signal. • Table of truth values is shown in "TRUTH TABLE" in Functional Operations.
MD	Mode selection pin • When set to LGND level "L", 8-bit parallel input mode is set. • When set to V _{DD} level "H", 4-bit parallel input mode is set. • Refer to section 7.2.2.
S/C	Segment mode/common mode selection pin • When set to V _{DD} level "H", segment mode is set.
EIO ₁ , EIO ₂	Input/output pins for chip selection • When L/R input is at LGND level "L", EIO ₁ is set for output, and EIO ₂ is set for input. • When L/R input is at V _{DD} level "H", EIO ₁ is set for input, and EIO ₂ is set for output.

	<ul style="list-style-type: none"> • During output, set to "H" while LP • XCK is "H" and after 240 bits of data have been read, set to "L" for one cycle (from falling edge to failing edge of XCK), after which it returns to "H". • During input, the chip is selected while EI is set to "L" after the LP signal is input. The chip is non-selected after 240 bits of data have been read.
Y ₁ -Y ₂₄₀	<p>LCD drive output pins</p> <ul style="list-style-type: none"> • Corresponding directly to each bit of the data latch, one level (V₀, V₁₂, V₄₃, or V_{SS}) is selected and output. • Table of truth values is shown in "TRUTH TABLE" in Functional Operations.

(Common mode)

SYMBOL	FUNCTION
V _{DD}	Logic system power supply pin, connected to +2.5 to +5.5 V.
GND	Ground pin
LGND	<p>Logic ground pin</p> <ul style="list-style-type: none"> • Do not short LGND with GND and V_{SS} by ITO on LCD panel • Connect it to GND on PCB or FPC.
V _{SS}	Connect to GND by ITO on LCD panel.
V _{0L} , V _{0R} V _{12L} , V _{12R} V _{43L} , V _{43R}	<p>Bias power supply pins for LCD drive voltage</p> <ul style="list-style-type: none"> • Normally use the bias voltages set by a resistor divider. • Ensure that voltages are set such that V_{SS} < V₄₃ < V₁₂ < V₀. • V_{iL} and V_{iR} (i = 0, 12, 43) must connect to an external power supply, and supply regular voltage which is assigned by specification for each power pin.
EIO ₁	<p>Shift data input/output pin for bi-directional shift register</p> <ul style="list-style-type: none"> • Output pin when L/R is at LGND level "L", input pin when L/R is at V_{DD} level "H". • When L/R = H, EIO₁ is used as input pin, it will be pulled down. • When L/R = L, EIO₁ is used as output pin, it won't be pulled down. • Refer to section 7.2.2.
EIO ₂	<p>Shift data input/output pin for bi-directional shift register</p> <ul style="list-style-type: none"> • Input pin when L/R is at LGND level "L", output pin when L/R is at V_{DD} level "H". • When L/R = L, EIO₂ is used as input pin, it will be pulled down. • When L/R = H, EIO₂ is used as output pin, it won't be pulled down. • Refer to section 7.2.2.
LP	<p>Shift clock pulse input pin for bi-directional shift register</p> <ul style="list-style-type: none"> • Data is shifted at the falling edge of the clock pulse.
L/R	<p>Input pin for selecting the shift direction of bi-directional shift register</p> <ul style="list-style-type: none"> • Data is shifted from Y₂₄₀ to Y₁ when set to LGND level "L", and data is shifted from Y₁ to Y₂₄₀ when set to V_{DD} level "H". • Refer to section 7.2.2.
/DISPOFF	<p>Control input pin for output of non-select level</p> <ul style="list-style-type: none"> • The input signal is level-shifted from logic voltage level to LCD drive voltage level, and controls the LCD drive circuit. • When set to LGND level "L", the LCD drive output pins (Y₁-Y₂₄₀) are set to level LGND. • When set to "L", the contents of the shift register are reset to not reading data. When the /DISPOFF function is canceled, the driver outputs non-select level (V₁₂ or V₄₃), and the shift data is read at the next falling edge of the LP. At that time, if /DISPOFF removal time does not correspond to what is shown in AC characteristics, the shift data is not read correctly. • Table of truth values is shown in "TRUTH TABLE" in Functional Operations.
FR	<p>AC signal input pin for LCD drive waveform</p> <ul style="list-style-type: none"> • The input signal is level-shifted from logic voltage level to LCD drive voltage level, and controls the LCD drive circuit. • Normally it inputs a frame inversion signal. • The LCD drive output pins' output voltage levels can be set using the shift register output signal and the FR signal. • Table of truth values is shown in "TRUTH TABLE" in Functional Operations.
MD	<p>Mode selection pin</p> <ul style="list-style-type: none"> • When set to LGND level "L", single mode operation is selected; when set to V_{DD} level

	"H" dual mode operation is selected. • Refer to section 7.2.2.
DI ₇	Dual mode data input pin • According to the data shift direction of the data shift register, data can be input starting from the 121st bit. When the chip is used in dual mode, DI ₇ will be pulled down. When the chip is used in single mode, DI ₇ won't be pulled down. • Refer to section 7.2.2.
S/C	Segment mode/common mode selection pin • When set to LGND level "L", common mode is set.
DI ₆ -DI ₀	Not used • Connect DI ₆ -DI ₀ to LGND or V _{DD} , avoiding floating.
XCK	Not used • XCK is pulled down in common mode, so connect to LGND or open.
Y ₁ -Y ₂₄₀	LCD drive output pins • Corresponding directly to each bit of the shift register, one level (V ₀ , V ₁₂ , V ₄₃ , or V _{SS}) is selected and output. • Table of truth values is shown in "TRUTH TABLE" in Functional Operations.

7.2 Functional Operations

7.2.1 Truth table

(Segment Mode)

FR	LATCH DATA	/DISPOFF	LCD DRIVE OUTPUT VOLTAGE LEVEL (Y1-Y240)
L	L	H	V ₄₃
L	H	H	V _{SS}
H	L	H	V ₁₂
H	H	H	V ₀
X	X	L	V _{SS}

(Common Mode)

FR	LATCH DATA	/DISPOFF	LCD DRIVE OUTPUT VOLTAGE LEVEL (Y1-Y240)
L	L	H	V ₄₃
L	H	H	V ₀
H	L	H	V ₁₂
H	H	H	V _{SS}
X	X	L	V _{SS}

NOTES:

- $V_{SS} < V_{43} < V_{12} < V_0$
 - L: LGND (0 V), H: V_{DD} (+2.5 to +5.5 V), X: Don't care
 - "Don't care" should be fixed to "H" or "L", avoiding floating.
- There are two kinds of power supply (logic level voltage and LCD drive voltage) for the LCD driver. Supply regular voltage which is assigned by specification for each power pin.

7.2.2 Relationship between the display data and LCD drive output Pins

(Segment Mode)

(a) 4-bit Parallel Input Mode

MD	L/R	EIO ₁	EIO ₂	DATA INPUT	NUMBER OF CLOCKS						
					60 CLOCK	59 CLOCK	58 CLOCK	...	3 CLOCK	2 CLOCK	1 CLOCK
H	L	Output	Input	DI0	Y1	Y5	Y9	...	Y229	Y233	Y237
				DI1	Y2	Y6	Y10	...	Y230	Y234	Y238
				DI2	Y3	Y7	Y11	...	Y231	Y235	Y239
				DI3	Y4	Y8	Y12	...	Y232	Y236	Y240
H	H	Input	Output	DI0	Y240	Y236	Y232	...	Y12	Y8	Y4
				DI1	Y239	Y235	Y231	...	Y11	Y7	Y3
				DI2	Y238	Y234	Y230	...	Y10	Y6	Y2
				DI3	Y237	Y233	Y229	...	Y9	Y5	Y1

(b) 8-bit Parallel Input Mode

MD	L/R	EIO ₁	EIO ₂	DATA INPUT	NUMBER OF CLOCKS						
					30 CLOCK	29 CLOCK	28 CLOCK	...	3 CLOCK	2 CLOCK	1 CLOCK
L	L	Output	Input	DI0	Y1	Y9	Y17	...	Y217	Y225	Y233
				DI1	Y2	Y10	Y18	...	Y218	Y226	Y234
				DI2	Y3	Y11	Y19	...	Y219	Y227	Y235
				DI3	Y4	Y12	Y20	...	Y220	Y228	Y236
				DI4	Y5	Y13	Y21	...	Y221	Y229	Y237
				DI5	Y6	Y14	Y22	...	Y222	Y230	Y238
				DI6	Y7	Y15	Y23	...	Y223	Y231	Y239
				DI7	Y8	Y16	Y24	...	Y224	Y232	Y240
L	H	Input	Output	DI0	Y240	Y232	Y224	...	Y24	Y16	Y8
				DI1	Y239	Y231	Y223	...	Y23	Y15	Y7
				DI2	Y238	Y230	Y222	...	Y22	Y14	Y6
				DI3	Y237	Y229	Y221	...	Y21	Y13	Y5
				DI4	Y236	Y228	Y220	...	Y20	Y12	Y4
				DI5	Y235	Y227	Y219	...	Y19	Y11	Y3
				DI6	Y234	Y226	Y218	...	Y18	Y10	Y2
				DI7	Y233	Y225	Y217	...	Y17	Y9	Y1

(Common Mode)

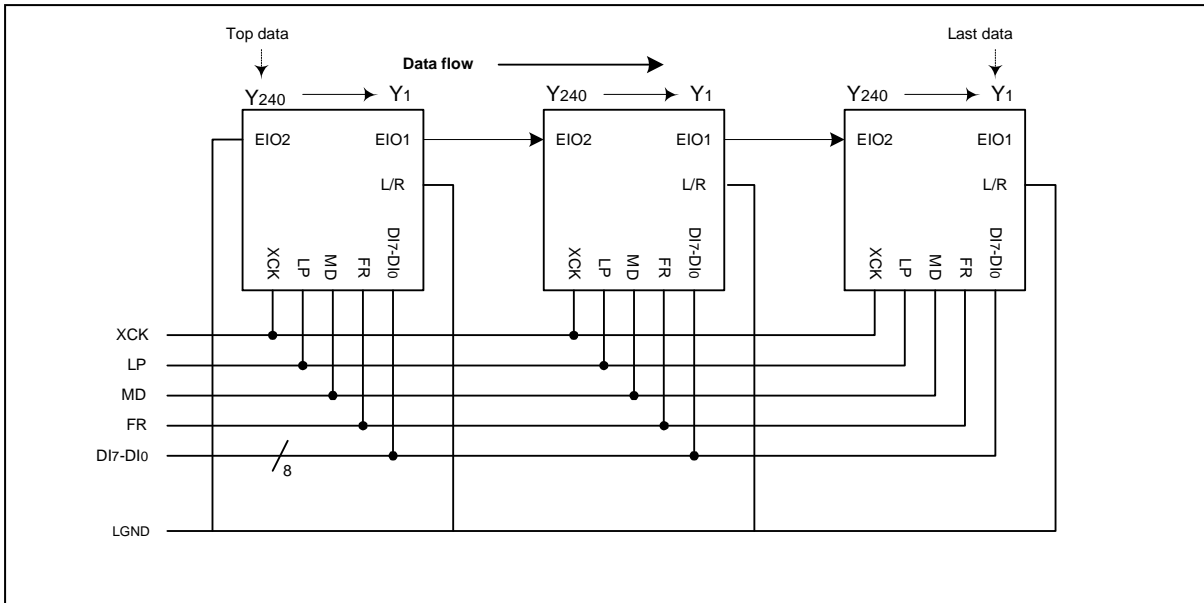
MD	L/R	DATA TRANSFER DIRECTION	EIO ₁	EIO ₂	DI ₇
L (Single)	L	Y240 → Y1	Output	Input	X
	H	Y1 → Y240	Input	Output	X
H (Dual)	L	Y240 → Y121 Y120 → Y1	Output	Input	Input
	H	Y1 → Y120 Y121 → Y240	Input	Output	Input

NOTES:

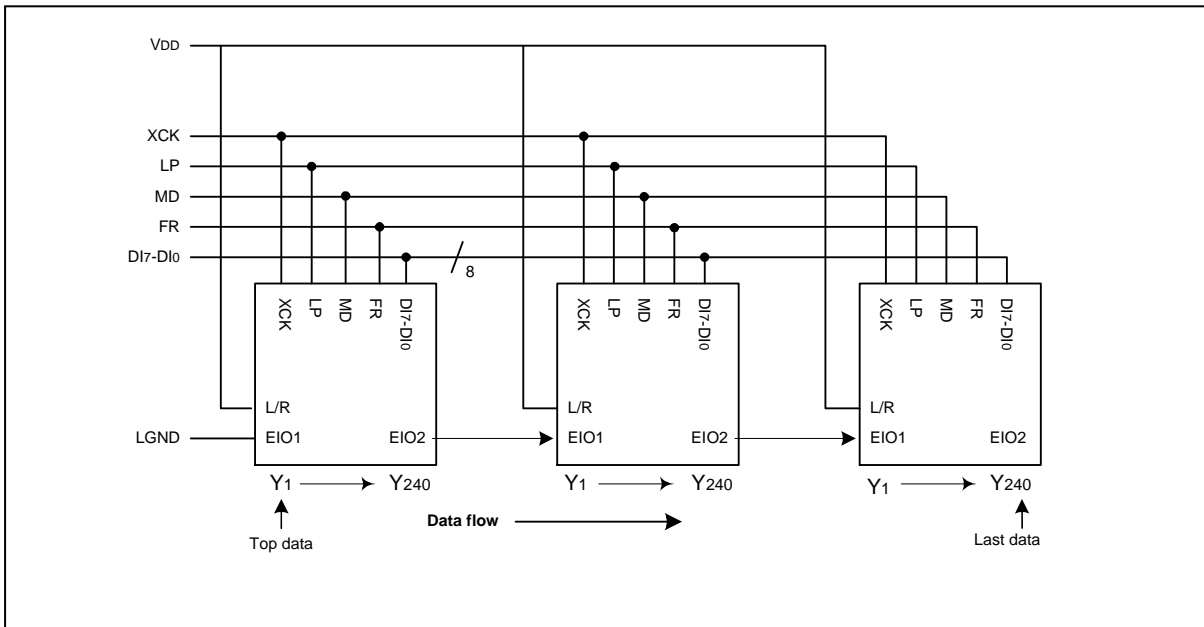
- L: LGND (0 V), H: V_{DD} (+2.5 to +5.5 V), X: Don't care
- "Don't care" should be fixed to "H" or "L", avoiding floating.

7.2.3 Connection examples of plural segment drivers

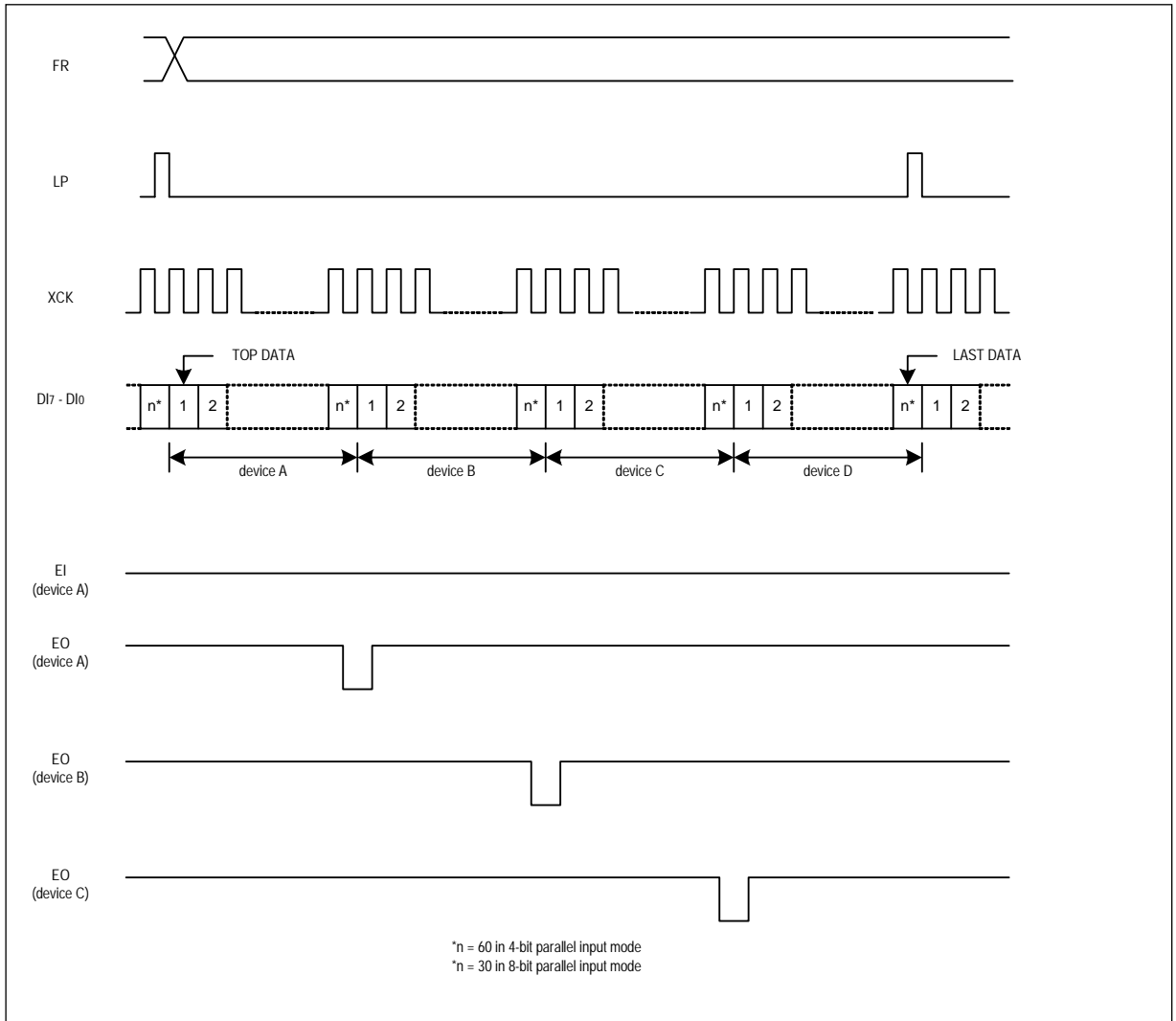
(a) When L/R = "L"



(b) When L/R = "H"

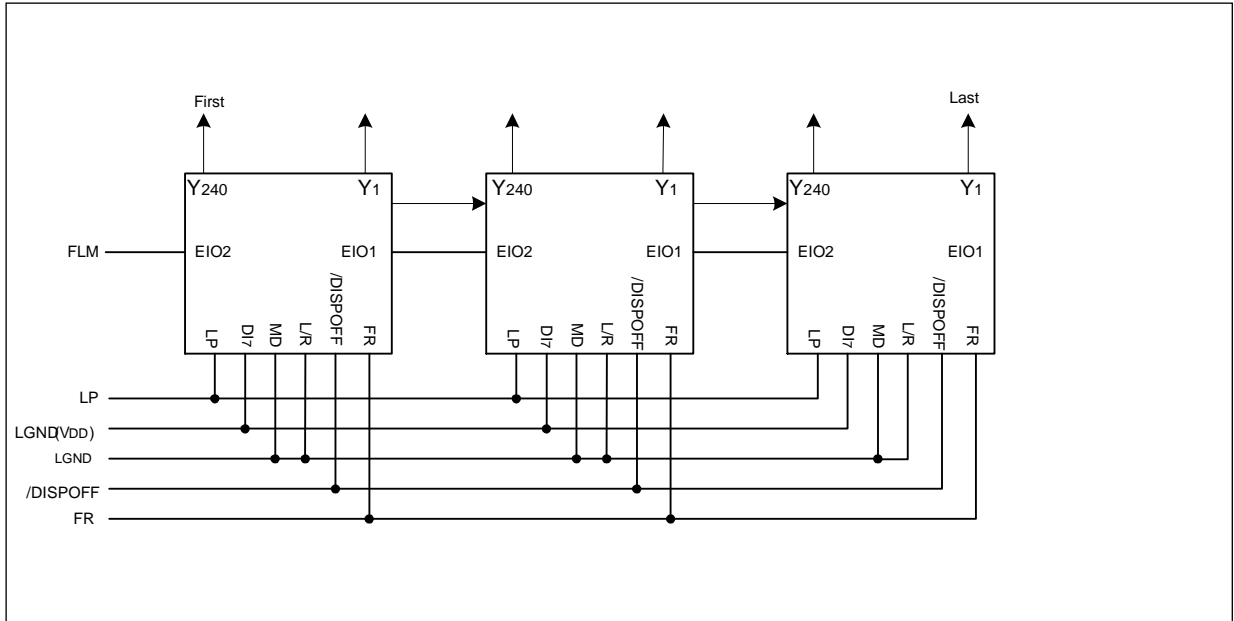


7.2.4 Timing chart of 4-device cascade connection of segment drivers

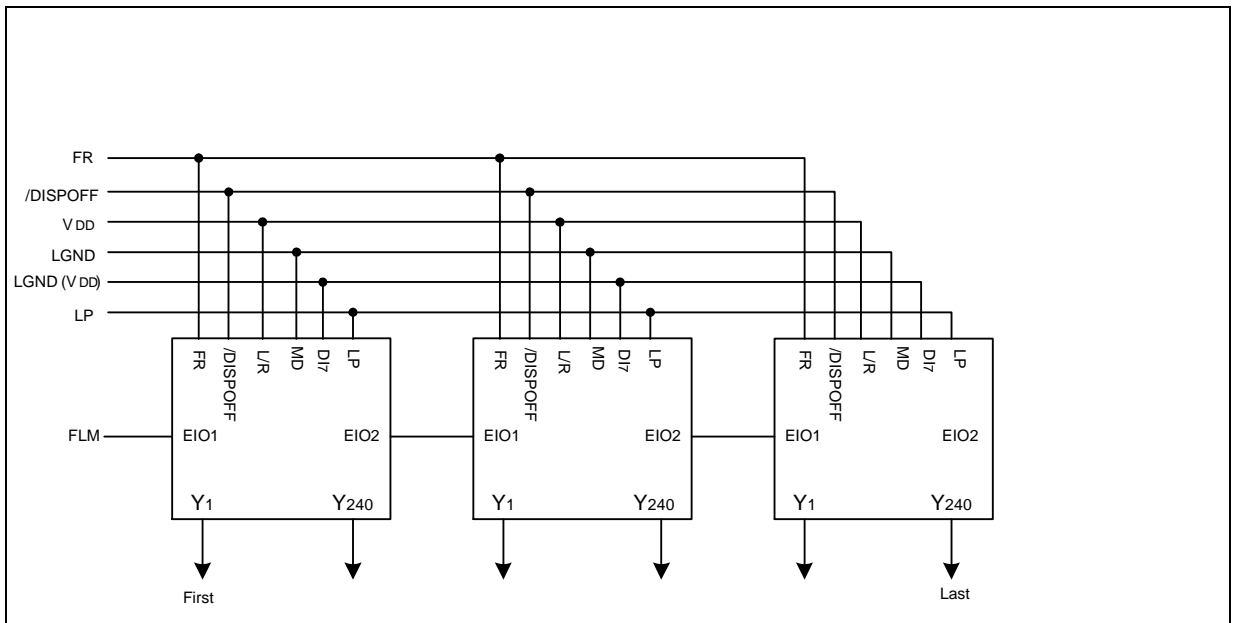


7.2.5 Connection examples for plural common drivers

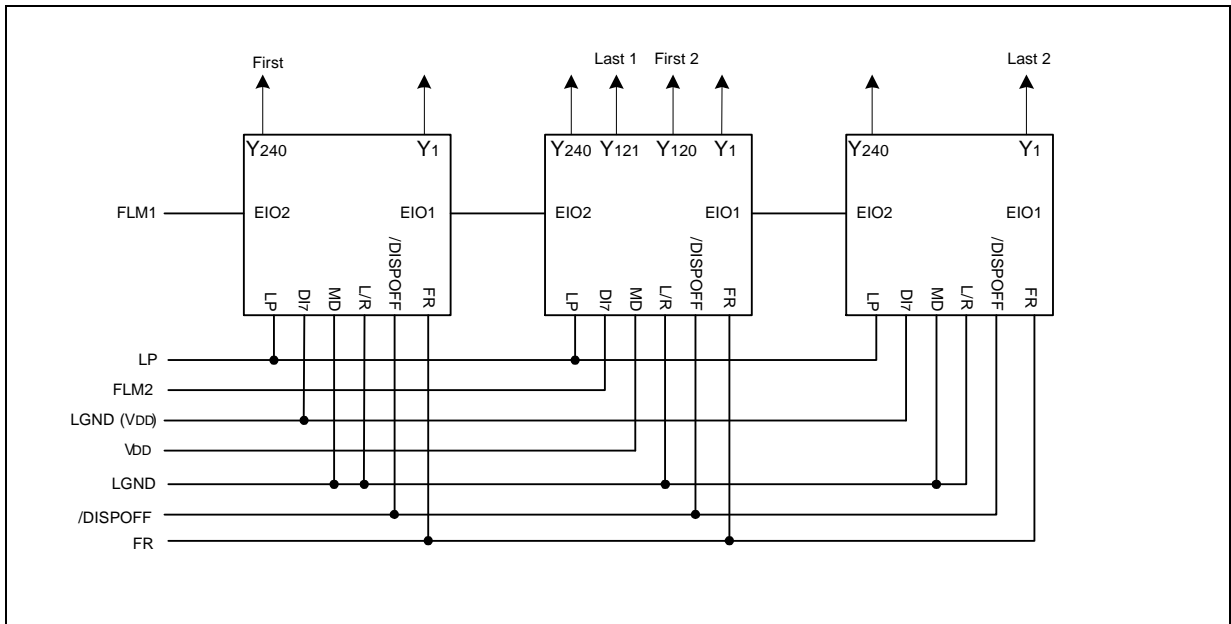
(a) Single Mode (L/R = "L")



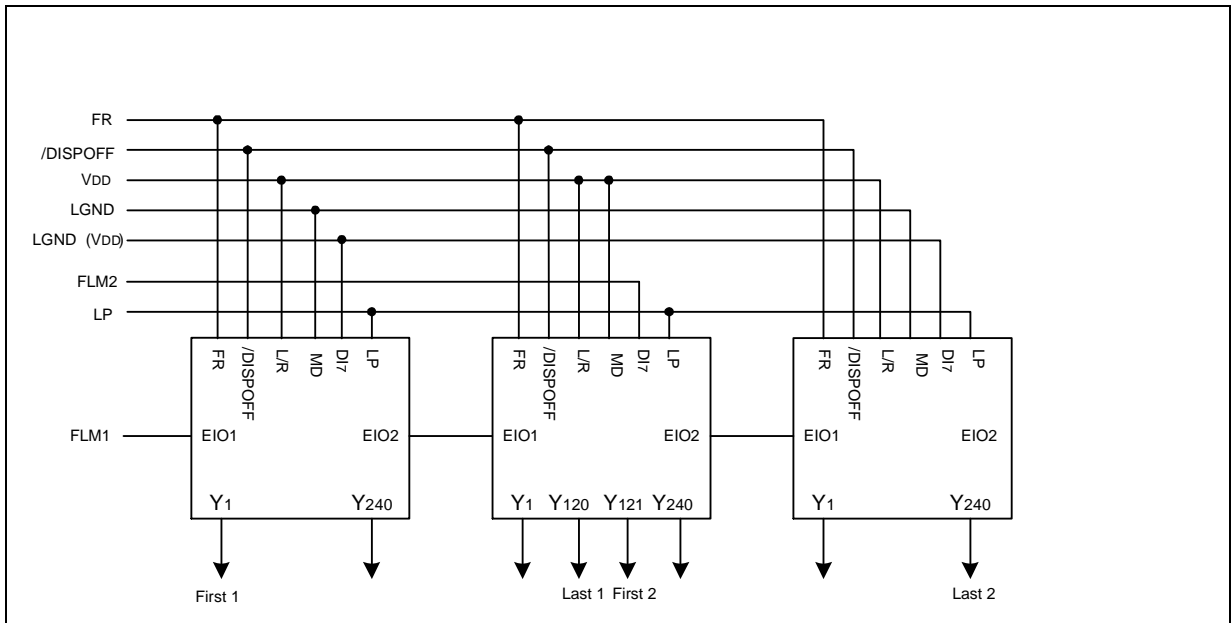
(b) Single Mode (L/R = "H")



(c) Dual Mode (L/R = "L")



(d) Dual mode (L/R = "H")



8. PRECAUTIONS

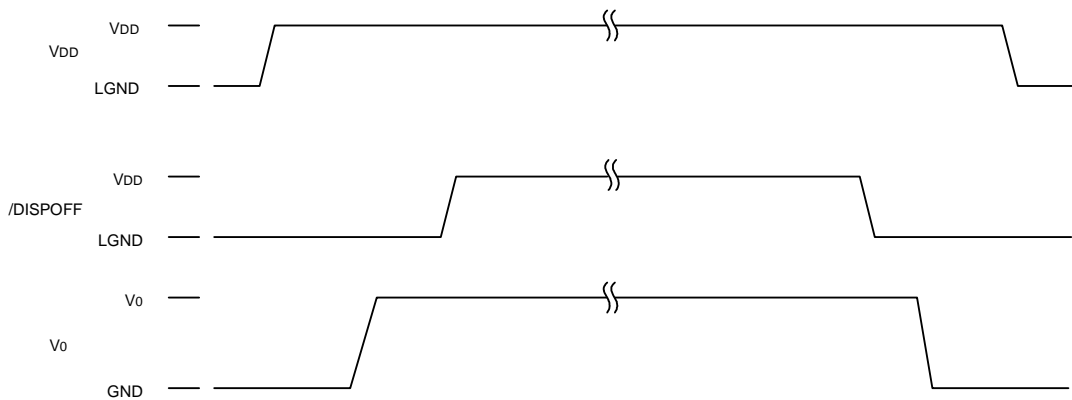
Precautions when connecting or disconnecting the power supply

This IC has a high-voltage LCD driver, so it may be permanently damaged by a high current which may flow if voltage is supplied to the LCD drive power supply while the logic system power supply is floating. The details are as follows,

- When connecting the power supply, connect the LCD drive power after connecting the logic system power. Furthermore, when disconnecting the power, disconnect the logic system power after disconnecting the LCD drive power
- It is advisable to connect the serial resistor (50 to 100 Ω) or fuse to the LCD drive power V_0 of the system as a current limiter. Set up a suitable value of the resistor in consideration of the display grade.

And when connecting the logic power supply, the logic condition of this IC inside is insecure. Therefore connect the LCD drive power supply after resetting logic condition of this IC inside on /DISPOFF function. After that, cancel the /DISPOFF function after the LCD drive power supply has become stable. Furthermore, when disconnecting the power, set the LCD drive output pins to level LGND on /DISPOFF function. Then disconnect the logic system power after disconnecting the LCD drive power.

When connecting the power supply, follow the recommended sequence shown here



9. ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	APPLICABLE PINS	RATING	UNIT	NOTE
Supply voltage (1)	V_{DD}	V_{DD}	-0.3 to +7.0	V	1,2
Supply voltage (2)	V_0	V_{0L}, V_{0R}	-0.3 to +33.0	V	
	V_{12}	V_{12L}, V_{12R}	-0.3 to $V_0 + 0.3$	V	
	V_{43}	V_{43L}, V_{43R}	-0.3 to $V_0 + 0.3$	V	
	V_{SS}	V_{SS}	-0.3 to $V_0 + 0.3$	V	
Input voltage	V_I	DI7-DI0, XCK, LP, L/R, FR, MD, S/C, EIO1, EIO2, /DISPOFF	-0.3 to $V_{DD} + 0.3$	V	
Storage temperature	T_{STG}		-45 to +125	°C	

NOTES:

1. $T_A = +25\text{ °C}$
2. The applicable voltage on logic pins with respect to LGND, high voltage pins with V_{SS} (0 V).

10. RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	APPLICABLE PINS	MIN.	TYP.	MAX.	UNIT	NOTE
Supply voltage (1)	V_{DD}	V_{DD}	+2.5		+5.5	V	1, 2
Supply voltage (2)	V_0	V_{0L}, V_{0R}	+15.0		+30.0	V	
Operating temperature	T_{OPR}		-25		+70	°C	

NOTES:

1. The applicable voltage on logic pins with respect to LGND, high voltage pins with V_{SS} (0 V).
2. Ensure that voltages are set such that $V_{SS} < V_{43} < V_{12} < V_0$.

11. ELECTRICAL CHARACTERISTICS

11.1 DC Characteristics

(Segment Mode) (LGND=V_{SS}=GND=0V, V_{DD}=+2.5~+5.5V, V₀=+15.0~+30.0V, T_{OPR}=-25 to +70°C)

PARAMETER	SYMBOL	CONDITIONS	APPLICABLE PINS	MIN.	TYP.	MAX.	UNIT	NOTE
Input "Low" voltage	V _{IL}		DI7-DI0, XCK, LP, L/R, FR, MD, S/C, EIO1, EIO2, /DISPOFF			0.2V _{DD}	V	
Input "High" voltage	V _{IH}			0.8V _{DD}			V	
Output "Low" voltage	V _{OL}	I _{OL} = +0.4 mA	EIO1, EIO2			+0.4	V	
Output "High" voltage	V _{OH}	I _{OH} = -0.4 mA		V _{DD} -0.4				V
Input leakage current	I _{LIL}	V _I = LGND	DI7-DI0, XCK, LP, L/R, FR, MD, S/C, EIO1, EIO2, /DISPOFF			-10.0	μA	
	I _{LIH}	V _I = V _{DD}				+10.0	μA	
Output resistance	R _{ON}	ΔV _{ON} = 0.5V	Y1-Y240		1.5	2.0	kΩ	
					2.0	2.5		
Standby current	I _{STB}		LGND+GND+V _{SS}			75.0	μA	1
Supply current (1) (Non-selection)	I _{DD1}		V _{DD}			2.0	mA	2
Supply current (2) (Selection)	I _{DD2}		V _{DD}			12.0	mA	3
Supply current (3)	I ₀		V _{OL} , V _{OR}			1.5	mA	4

NOTES:

- V_{DD} = +5.0 V, V₀ = +30.0 V, V_I = LGND.
- V_{DD} = +5.0 V, V₀ = +30.0 V, f_{XCK} = 15 MHz, no-load, E_I = V_{DD}. The input data is turned over by data taking clock (4-bit parallel input mode).
- V_{DD} = +5.0 V, V₀ = +30.0 V, f_{XCK} = 15 MHz, no-load, E_I = LGND. The input data is turned over by data taking clock (4-bit parallel input mode).
- V_{DD} = +5.0 V, V₀ = +30.0 V, f_{XCK} = 15MHz, f_{LP} = 20.8 kHz, f_{FR} = 80 Hz, no-load. The input data is turned over by data taking clock (4-bit parallel input mode).

(Common Mode) (LGND=V_{SS}=GND=0V, V_{DD}=+2.5~+5.5V, V₀=+15.0~+30.0V, T_{OPR}=-25 to +70 °C)

PARAMETER	SYMBOL	CONDITIONS	APPLICABLE PINS	MIN.	TYP.	MAX.	UNIT	NOTE
Input "Low" voltage	V _{IL}		DI7-DI0, XCK, LP, L/R			0.2V _{DD}	V	
Input "High" voltage	V _{IH}		FR, MD, S/C, EIO1, EIO2, /DISPOFF	0.8V _{DD}			V	
Output "Low" voltage	V _{OL}	I _{OL} = +0.4 mA	EIO1, EIO2			+0.4	V	
Output "High" voltage	V _{OH}	I _{OH} = -0.4 mA		V _{DD} -0.4				V
Input leakage current	I _{LIL}	V _I = LGND	DI7-DI0, XCK, LP, L/R, FR, MD, S/C, EIO1, EIO2, /DISPOFF			-10.0	μA	
	I _{LIH}	V _I = V _{DD}		DI6-DI0, LP, L/R, FR, MD, S/C, /DISPOFF			+10.0	μA
Input pull-down current	I _{PD}	V _I = V _{DD}	DI7, XCK, EIO1, EIO2			100.0	μA	
Output resistance	R _{ON}	ΔV _{ON} = 0.5V	Y1-Y240		1.5	2.0	kΩ	
					2.0	2.5		
Standby current	I _{SPD}		LGND+GND+V _{SS}			75.0	μA	1
Supply current (1)	I _{DD}		V _{DD}			120.0	μA	2
Supply current (2)	I ₀		V _{OL} , V _{OR}			240.0	μA	2

NOTES:

- V_{DD} = +5.0 V, V₀ = +30.0 V, V_I = LGND
- V_{DD} = +5.0 V, V₀ = +30.0 V, f_{LP} = 20.8 kHz, f_{FR} = 80 Hz, 1/480 duty operation, no-load.

11.2 AC Characteristics

(Segment Mode 1) (LGND=V_{SS} = GND = 0 V, V_{DD} = +5.0±0.5 V, V₀ = + 15.0 ~ +30.0V, T_{OPR} = -25 to +70 °C)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP.	MAX.	UNIT	NOTE
Shift clock period	t _{WCK}	t _r , t _f ≤ 10ns	66			ns	1
Shift clock "H" pulse width	t _{WCKH}		23			ns	
Shift clock "L" pulse width	t _{WCKL}		23			ns	
Data setup time	t _{DS}		15			ns	
Data hold time	t _{DH}		23			ns	
Latch pulse "H" pulse width	t _{WLPH}		30			ns	
Shift clock rise to latch pulse rise time	t _{LD}		0			ns	
Shift clock fall to latch pulse fall time	t _{SL}		50			ns	
Latch pulse rise to shift clock rise time	t _{LS}		30			ns	
Latch pulse fall to shift clock fall time	t _{LH}		30			ns	
Enable setup time	t _S		15			ns	
Input signal rise time	t _R				50	ns	2
Input signal fall time	t _F				50	ns	2
/DISPOFF removal time	t _{SD}		100			ns	
/DISPOFF "L" pulse width	t _{WDL}		1.2			μs	
Output delay time (1)	t _D	CL = 15 pF			41	ns	
Output delay time (2)	t _{PD1} , t _{PD2}	CL = 15 pF			1.2	μs	
Output delay time (3)	t _{PD3}	CL = 15 pF			1.2	μs	

NOTES:

1. Takes the cascade connection into consideration.
2. (t_{WCK} - t_{WCKH} - t_{WCKL})/2 is maximum in the case of high speed operation.

(Segment Mode 2) (LGND=V_{SS} =GND = 0V, V_{DD} = +3.0 ~ +4.5V, V₀ = + 15.0 ~ +30.0V, T_{OPR} = -25 to +70 °C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Shift clock period	t _{WCK}	t _r , t _f ≤ 10ns	82			ns	1
Shift clock "H" pulse width	t _{WCKH}		28			ns	
Shift clock "L" pulse width	t _{WCKL}		28			ns	
Data setup time	t _{DS}		20			ns	
Data hold time	t _{DH}		23			ns	
Latch pulse "H" pulse width	t _{WLPH}		30			ns	
Shift clock rise to latch pulse rise time	t _{LD}		0			ns	
Shift clock fall to latch pulse fall time	t _{SL}		65			ns	
Latch pulse rise to shift clock rise time	t _{LS}		30			ns	
Latch pulse fall to shift clock fall time	t _{LH}		30			ns	
Enable setup time	t _S		15			ns	
Input signal rise time	t _R				50	ns	2
Input signal fall time	t _F				50	ns	2
/DISPOFF removal time	t _{SD}		100			ns	
/DISPOFF "L" pulse width	t _{WDL}		1.2			μs	
Output delay time (1)	t _D	CL = 15 pF			57	ns	
Output delay time (2)	t _{PD1} , t _{PD2}	CL = 15 pF			1.2	μs	
Output delay time (3)	t _{PD3}	CL = 15 pF			1.2	μs	

NOTES:

1. Takes the cascade connection into consideration.
2. (t_{WCK} - t_{WCKH} - t_{WCKL})/2 is maximum in the case of high speed operation.

(Segment Mode 3) (LGND=V_{SS}=GND=0V, V_{DD}=+2.5~+3.0V, V₀=+15.0~+30.0V, T_{OPR}=-25 to+70 °C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Shift clock period	t _{WCK}	t _r , t _f ≤ 10ns	130			ns	1
Shift clock "H" pulse width	t _{WCKH}		35			ns	
Shift clock "L" pulse width	t _{WCKL}		35			ns	
Data setup time	t _{DS}		25			ns	
Data hold time	t _{DH}		23			ns	
Latch pulse "H" pulse width	t _{WLPH}		30			ns	
Shift clock rise to latch pulse rise time	t _{LD}		0			ns	
Shift clock fall to latch pulse fall time	t _{SL}		80			ns	
Latch pulse rise to shift clock rise time	t _{LS}		30			ns	
Latch pulse fall to shift clock fall time	t _{LH}		30			ns	
Enable setup time	t _S		15			ns	
Input signal rise time	t _R				50	ns	2
Input signal fall time	t _F				50	ns	2
/DISPOFF removal time	t _{SD}		100			ns	
/DISPOFF "L" pulse width	t _{WDL}		1.2			μs	
Output delay time (1)	t _D	CL = 15 pF			80	ns	
Output delay time (2)	t _{PD1} , t _{PD2}	CL = 15 pF			1.2	μs	
Output delay time (3)	t _{PD3}	CL = 15 pF			1.2	μs	

NOTES:

1. Takes the cascade connection into consideration.
2. (t_{WCK} - t_{WCKH} - t_{WCKL})/2 is maximum in the case of high speed operation.

(Common Mode) (LGND=V_{SS}=0 V, V_{DD}=+2.5~+5.5V, V₀=+15.0~+30.0V, T_{OPR}=-25 to +70° C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Shift clock period	t _{WLP}	t _r , t _f ≤ 20ns	250			ns
Shift clock "H" pulse width	t _{WLPH}	V _{DD} = +5.0± 0.5V	15			ns
		V _{DD} = +2.5+ 4.5V	30			ns
Data setup time	t _{SU}		30			ns
Data hold time	t _H		50			ns
Input signal rise time	t _R				50	ns
Input signal fall time	t _F				50	ns
/DISPOFF removal time	t _{SD}		100			ns
/DISPOFF "L" pulse width	t _{WDL}		1.2			μs
Output delay time (1)	t _{DL}	CL = 15 pF			200	ns
Output delay time (2)	t _{PD1} , t _{PD2}	CL = 15 pF			1.2	μs
Output delay time (3)	t _{PD3}	CL = 15 pF			1.2	μs

11.3 Timing Chart of Segment Mode

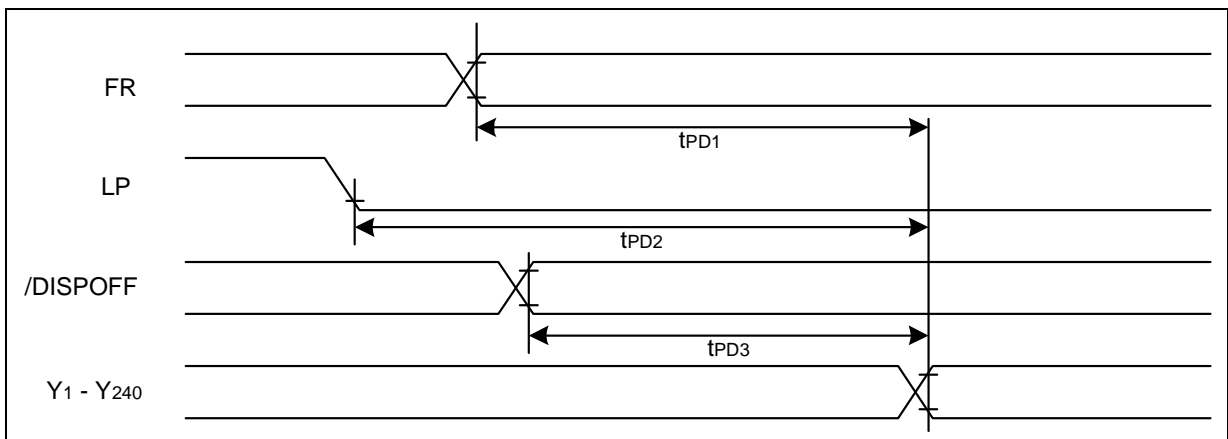
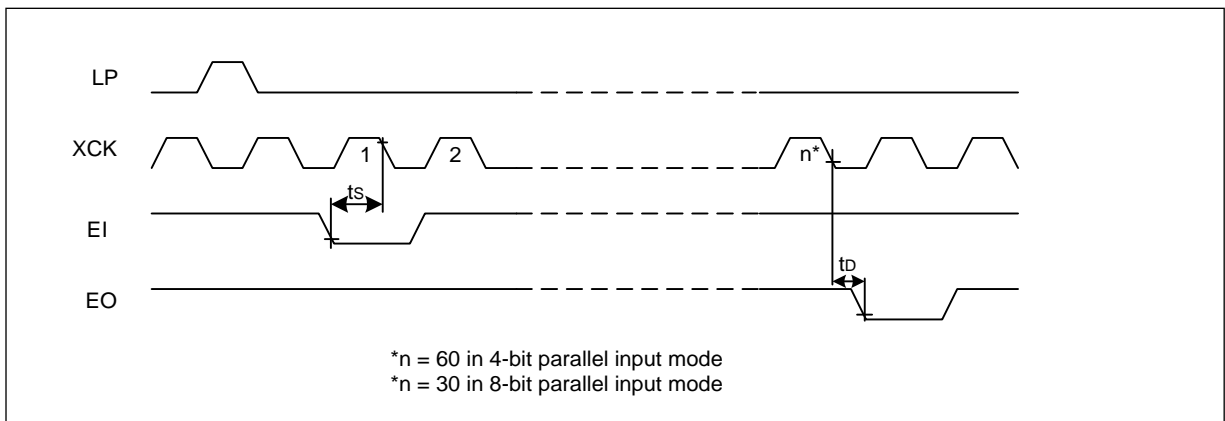
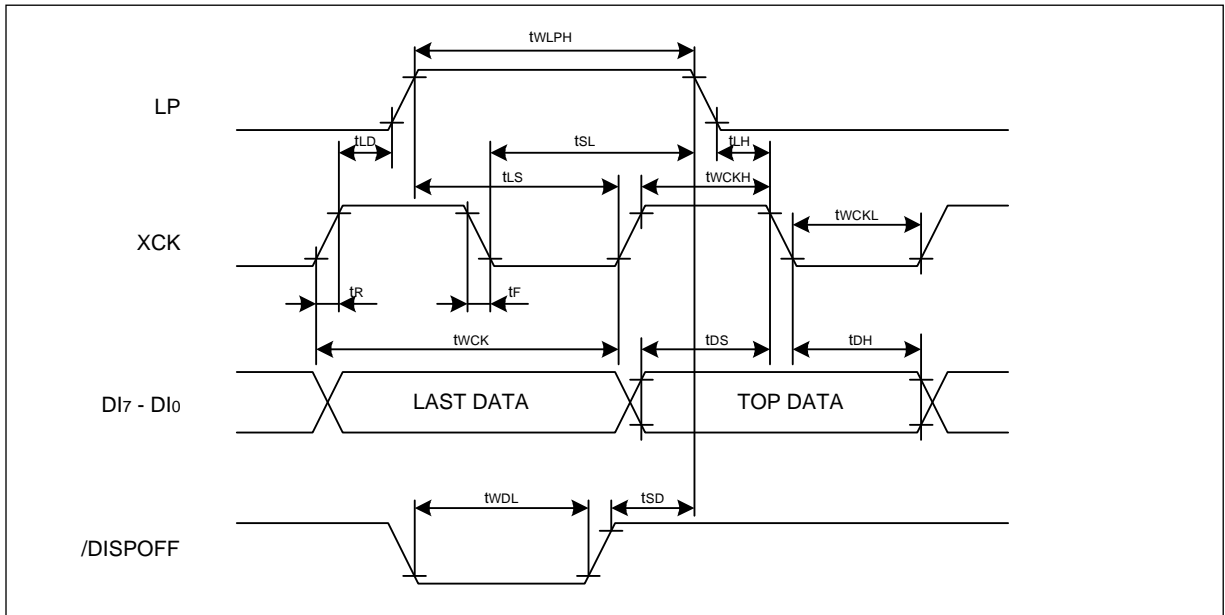
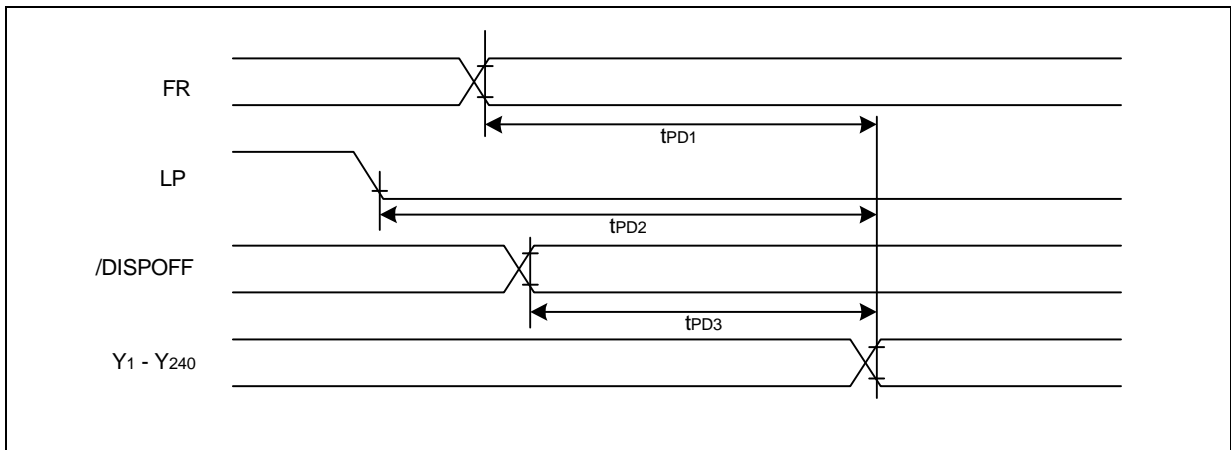
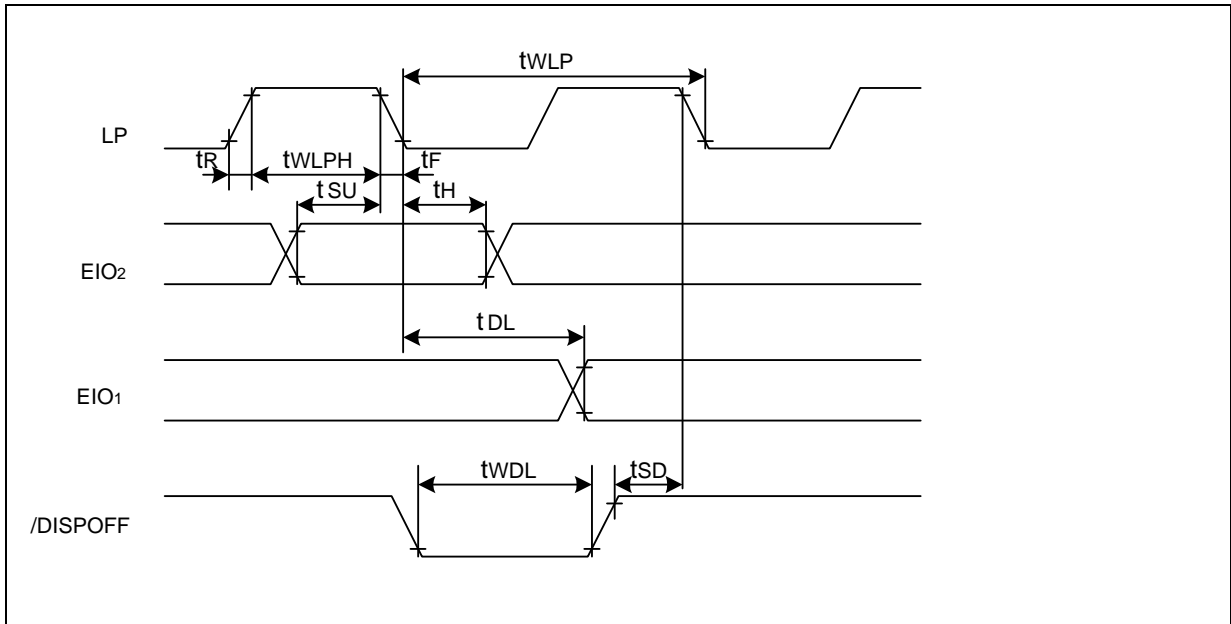
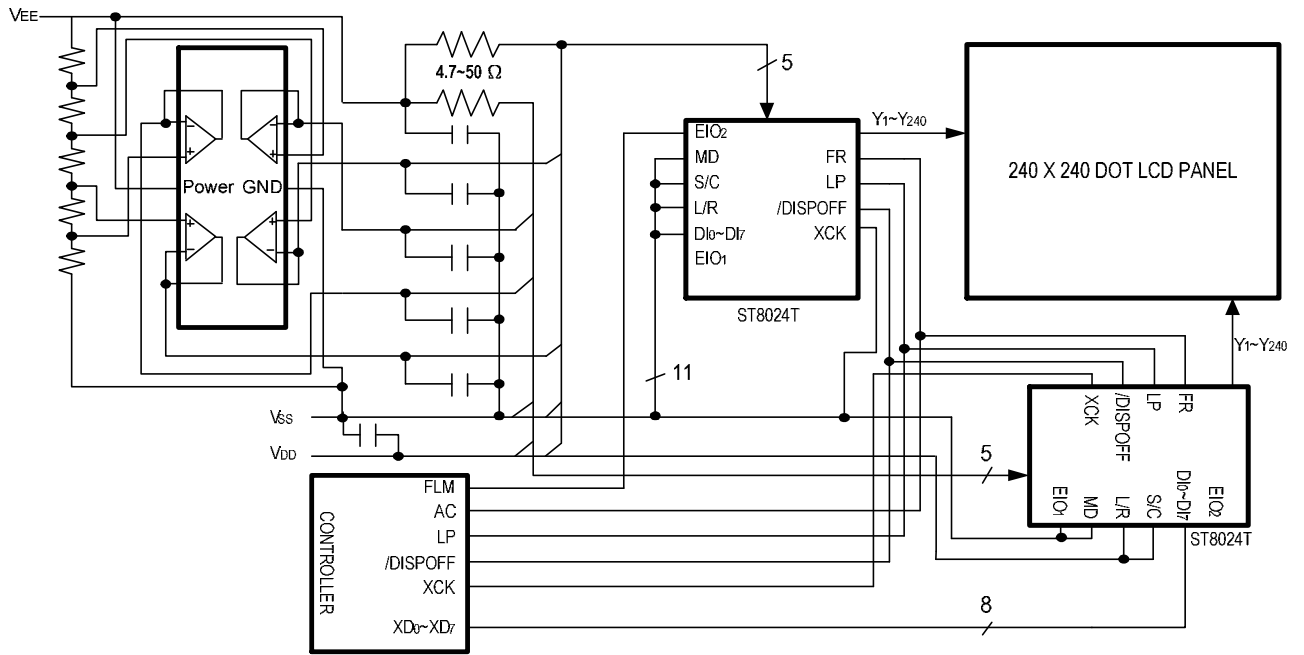


Fig. 8 Timing Characteristics (3)

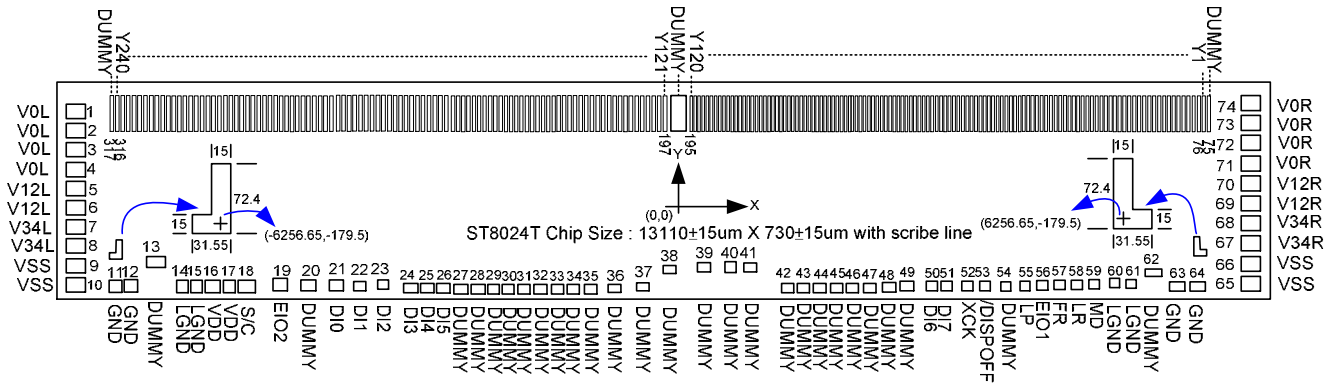
11.4 Timing Chart of Common Mode



12. APPLICATION CIRCUIT
 12.1 Application Circuit for Module



13. PAD DIAGRAM



Unit : um

Pad#	Name	X	Y	Pad#	Name	X	Y	Pad#	Name	X	Y
1	V0L	-6437.25	266.85	33	DUMMY	-1525.35	-263.10	65	VSS	6437.25	-266.85
2	V0L	-6437.25	207.55	34	DUMMY	-1360.40	-263.10	66	VSS	6437.25	-207.55
3	V0L	-6437.25	148.25	35	DUMMY	-1195.45	-263.10	67	V34R	6437.25	-148.25
4	V0L	-6437.25	88.95	36	DUMMY	-874.05	-263.10	68	V34R	6437.25	-88.95
5	V12L	-6437.25	29.65	37	DUMMY	-527.80	-224.40	69	V12R	6437.25	-29.65
6	V12L	-6437.25	-29.65	38	DUMMY	-161.08	-227.68	70	V12R	6437.25	29.65
7	V34L	-6437.25	-88.95	39	DUMMY	228.83	-217.73	71	V0R	6437.25	88.95
8	V34L	-6437.25	-148.25	40	DUMMY	614.43	-217.73	72	V0R	6437.25	148.25
9	VSS	-6437.25	-207.55	41	DUMMY	878.05	-220.48	73	V0R	6437.25	207.55
10	VSS	-6437.25	-266.85	42	DUMMY	1297.05	-263.10	74	V0R	6437.25	266.85
11	GND	-6268.15	-263.15	43	DUMMY	1474.50	-263.10	75	DUMMY	6317.00	250.10
12	GND	-6136.55	-263.15	44	DUMMY	1651.95	-263.10	76	Y1	6267.00	250.10
13	DUMMY	-5978.15	-209.05	45	DUMMY	1829.40	-263.10	77	Y2	6215.00	250.10
14	LGND	-5680.50	-263.15	46	DUMMY	2006.85	-263.10	78	Y3	6163.00	250.10
15	LGND	-5573.05	-263.15	47	DUMMY	2184.30	-263.10	79	Y4	6111.00	250.10
16	VDD	-5452.80	-263.15	48	DUMMY	2361.75	-263.10	80	Y5	6059.00	250.10
17	VDD	-5345.35	-263.15	49	DUMMY	2539.20	-263.10	81	Y6	6007.00	250.10
18	S/C	-5208.40	-263.10	50	DI6	2731.90	-263.10	82	Y7	5955.00	250.10
19	EIO2	-4786.70	-263.10	51	DI7	2893.20	-263.10	83	Y8	5903.00	250.10
20	DUMMY	-4412.48	-263.10	52	XCK	3214.45	-263.10	84	Y9	5851.00	250.10
21	DI0	-4005.45	-263.10	53	/DISPOFF	3505.05	-263.10	85	Y10	5799.00	250.10
22	DI1	-3621.55	-263.10	54	DUMMY	3709.58	-263.10	86	Y11	5747.00	250.10
23	DI2	-3317.00	-263.10	55	LP	4122.15	-263.10	87	Y12	5695.00	250.10
24	DI3	-3005.05	-263.10	56	EIO1	4450.75	-263.10	88	Y13	5643.00	250.10
25	DI4	-2840.45	-263.10	57	FR	4806.65	-263.10	89	Y14	5591.00	250.10
26	DI5	-2679.15	-263.10	58	L/R	5094.20	-263.10	90	Y15	5539.00	250.10
27	DUMMY	-2515.05	-263.10	59	MD	5349.25	-263.10	91	Y16	5487.00	250.10
28	DUMMY	-2350.10	-263.10	60	LGND	5573.05	-263.15	92	Y17	5435.00	250.10
29	DUMMY	-2185.15	-263.10	61	LGND	5680.50	-263.15	93	Y18	5383.00	250.10
30	DUMMY	-2020.20	-263.10	62	DUMMY	5978.15	-209.05	94	Y19	5331.00	250.10
31	DUMMY	-1855.25	-263.10	63	GND	6136.55	-263.15	95	Y20	5279.00	250.10
32	DUMMY	-1690.30	-263.10	64	GND	6268.15	-263.15	96	Y21	5227.00	250.10

97	Y22	5175.00	250.10	148	Y73	2523.00	250.10	199	Y123	-183.00	250.10
98	Y23	5123.00	250.10	149	Y74	2471.00	250.10	200	Y124	-235.00	250.10
99	Y24	5071.00	250.10	150	Y75	2419.00	250.10	201	Y125	-287.00	250.10
100	Y25	5019.00	250.10	151	Y76	2367.00	250.10	202	Y126	-339.00	250.10
101	Y26	4967.00	250.10	152	Y77	2315.00	250.10	203	Y127	-391.00	250.10
102	Y27	4915.00	250.10	153	Y78	2263.00	250.10	204	Y128	-443.00	250.10
103	Y28	4863.00	250.10	154	Y79	2211.00	250.10	205	Y129	-495.00	250.10
104	Y29	4811.00	250.10	155	Y80	2159.00	250.10	206	Y130	-547.00	250.10
105	Y30	4759.00	250.10	156	Y81	2107.00	250.10	207	Y131	-599.00	250.10
106	Y31	4707.00	250.10	157	Y82	2055.00	250.10	208	Y132	-651.00	250.10
107	Y32	4655.00	250.10	158	Y83	2003.00	250.10	209	Y133	-703.00	250.10
108	Y33	4603.00	250.10	159	Y84	1951.00	250.10	210	Y134	-755.00	250.10
109	Y34	4551.00	250.10	160	Y85	1899.00	250.10	211	Y135	-807.00	250.10
110	Y35	4499.00	250.10	161	Y86	1847.00	250.10	212	Y136	-859.00	250.10
111	Y36	4447.00	250.10	162	Y87	1795.00	250.10	213	Y137	-911.00	250.10
112	Y37	4395.00	250.10	163	Y88	1743.00	250.10	214	Y138	-963.00	250.10
113	Y38	4343.00	250.10	164	Y89	1691.00	250.10	215	Y139	-1015.00	250.10
114	Y39	4291.00	250.10	165	Y90	1639.00	250.10	216	Y140	-1067.00	250.10
115	Y40	4239.00	250.10	166	Y91	1587.00	250.10	217	Y141	-1119.00	250.10
116	Y41	4187.00	250.10	167	Y92	1535.00	250.10	218	Y142	-1171.00	250.10
117	Y42	4135.00	250.10	168	Y93	1483.00	250.10	219	Y143	-1223.00	250.10
118	Y43	4083.00	250.10	169	Y94	1431.00	250.10	220	Y144	-1275.00	250.10
119	Y44	4031.00	250.10	170	Y95	1379.00	250.10	221	Y145	-1327.00	250.10
120	Y45	3979.00	250.10	171	Y96	1327.00	250.10	222	Y146	-1379.00	250.10
121	Y46	3927.00	250.10	172	Y97	1275.00	250.10	223	Y147	-1431.00	250.10
122	Y47	3875.00	250.10	173	Y98	1223.00	250.10	224	Y148	-1483.00	250.10
123	Y48	3823.00	250.10	174	Y99	1171.00	250.10	225	Y149	-1535.00	250.10
124	Y49	3771.00	250.10	175	Y100	1119.00	250.10	226	Y150	-1587.00	250.10
125	Y50	3719.00	250.10	176	Y101	1067.00	250.10	227	Y151	-1639.00	250.10
126	Y51	3667.00	250.10	177	Y102	1015.00	250.10	228	Y152	-1691.00	250.10
127	Y52	3615.00	250.10	178	Y103	963.00	250.10	229	Y153	-1743.00	250.10
128	Y53	3563.00	250.10	179	Y104	911.00	250.10	230	Y154	-1795.00	250.10
129	Y54	3511.00	250.10	180	Y105	859.00	250.10	231	Y155	-1847.00	250.10
130	Y55	3459.00	250.10	181	Y106	807.00	250.10	232	Y156	-1899.00	250.10
131	Y56	3407.00	250.10	182	Y107	755.00	250.10	233	Y157	-1951.00	250.10
132	Y57	3355.00	250.10	183	Y108	703.00	250.10	234	Y158	-2003.00	250.10
133	Y58	3303.00	250.10	184	Y109	651.00	250.10	235	Y159	-2055.00	250.10
134	Y59	3251.00	250.10	185	Y110	599.00	250.10	236	Y160	-2107.00	250.10
135	Y60	3199.00	250.10	186	Y111	547.00	250.10	237	Y161	-2159.00	250.10
136	Y61	3147.00	250.10	187	Y112	495.00	250.10	238	Y162	-2211.00	250.10
137	Y62	3095.00	250.10	188	Y113	443.00	250.10	239	Y163	-2263.00	250.10
138	Y63	3043.00	250.10	189	Y114	391.00	250.10	240	Y164	-2315.00	250.10
139	Y64	2991.00	250.10	190	Y115	339.00	250.10	241	Y165	-2367.00	250.10
140	Y65	2939.00	250.10	191	Y116	287.00	250.10	242	Y166	-2419.00	250.10
141	Y66	2887.00	250.10	192	Y117	235.00	250.10	243	Y167	-2471.00	250.10
142	Y67	2835.00	250.10	193	Y118	183.00	250.10	244	Y168	-2523.00	250.10
143	Y68	2783.00	250.10	194	Y119	131.00	250.10	245	Y169	-2575.00	250.10
144	Y69	2731.00	250.10	195	Y120	79.00	250.10	246	Y170	-2627.00	250.10
145	Y70	2679.00	250.10	196	DUMMY	0.00	250.10	247	Y171	-2679.00	250.10
146	Y71	2627.00	250.10	197	Y121	-79.00	250.10	248	Y172	-2731.00	250.10
147	Y72	2575.00	250.10	198	Y122	-131.00	250.10	249	Y173	-2783.00	250.10
250	Y174	-2835.00	250.10	273	Y197	-4031.00	250.10	296	Y220	-5227.00	250.10

251	Y175	-2887.00	250.10	274	Y198	-4083.00	250.10	297	Y221	-5279.00	250.10
252	Y176	-2939.00	250.10	275	Y199	-4135.00	250.10	298	Y222	-5331.00	250.10
253	Y177	-2991.00	250.10	276	Y200	-4187.00	250.10	299	Y223	-5383.00	250.10
254	Y178	-3043.00	250.10	277	Y201	-4239.00	250.10	300	Y224	-5435.00	250.10
255	Y179	-3095.00	250.10	278	Y202	-4291.00	250.10	301	Y225	-5487.00	250.10
256	Y180	-3147.00	250.10	279	Y203	-4343.00	250.10	302	Y226	-5539.00	250.10
257	Y181	-3199.00	250.10	280	Y204	-4395.00	250.10	303	Y227	-5591.00	250.10
258	Y182	-3251.00	250.10	281	Y205	-4447.00	250.10	304	Y228	-5643.00	250.10
259	Y183	-3303.00	250.10	282	Y206	-4499.00	250.10	305	Y229	-5695.00	250.10
260	Y184	-3355.00	250.10	283	Y207	-4551.00	250.10	306	Y230	-5747.00	250.10
261	Y185	-3407.00	250.10	284	Y208	-4603.00	250.10	307	Y231	-5799.00	250.10
262	Y186	-3459.00	250.10	285	Y209	-4655.00	250.10	308	Y232	-5851.00	250.10
263	Y187	-3511.00	250.10	286	Y210	-4707.00	250.10	309	Y233	-5903.00	250.10
264	Y188	-3563.00	250.10	287	Y211	-4759.00	250.10	310	Y234	-5955.00	250.10
265	Y189	-3615.00	250.10	288	Y212	-4811.00	250.10	311	Y235	-6007.00	250.10
266	Y190	-3667.00	250.10	289	Y213	-4863.00	250.10	312	Y236	-6059.00	250.10
267	Y191	-3719.00	250.10	290	Y214	-4915.00	250.10	313	Y237	-6111.00	250.10
268	Y192	-3771.00	250.10	291	Y215	-4967.00	250.10	314	Y238	-6163.00	250.10
269	Y193	-3823.00	250.10	292	Y216	-5019.00	250.10	315	Y239	-6215.00	250.10
270	Y194	-3875.00	250.10	293	Y217	-5071.00	250.10	316	Y240	-6267.00	250.10
271	Y195	-3927.00	250.10	294	Y218	-5123.00	250.10	317	DUMMY	-6317.00	250.10
272	Y196	-3979.00	250.10	295	Y219	-5175.00	250.10				

13.1 Gold Bump Size

Pad No.	X	Y	Area (um ²)
1~10, 65~74	87.50	44.30	3876.2500
11, 12, 63, 64	116.60	42.30	4932.1800
13, 62	160.20	33.30	5334.6600
14~17, 60, 61	92.50	42.30	3912.7500
18, 19, 21~26, 50~53, 55~59	131.30	42.40	5567.1200
20, 54	152.35	42.40	6459.6400
27~36	134.30	42.40	5694.3200
37	94.30	44.40	4186.9200
38	103.85	37.85	3930.7225
39, 40	85.65	57.75	4946.2875
41	117.20	52.25	6123.7000
42~49	140.80	42.40	5969.9200
196	91.00	81.00	7371.0000
75, 317	33.00	81.00	2673.0000
76~195, 197~316	37.00	81.00	2997.0000

Wafer thickness = 480±20um, Bump pad height = 15um, strength=30g

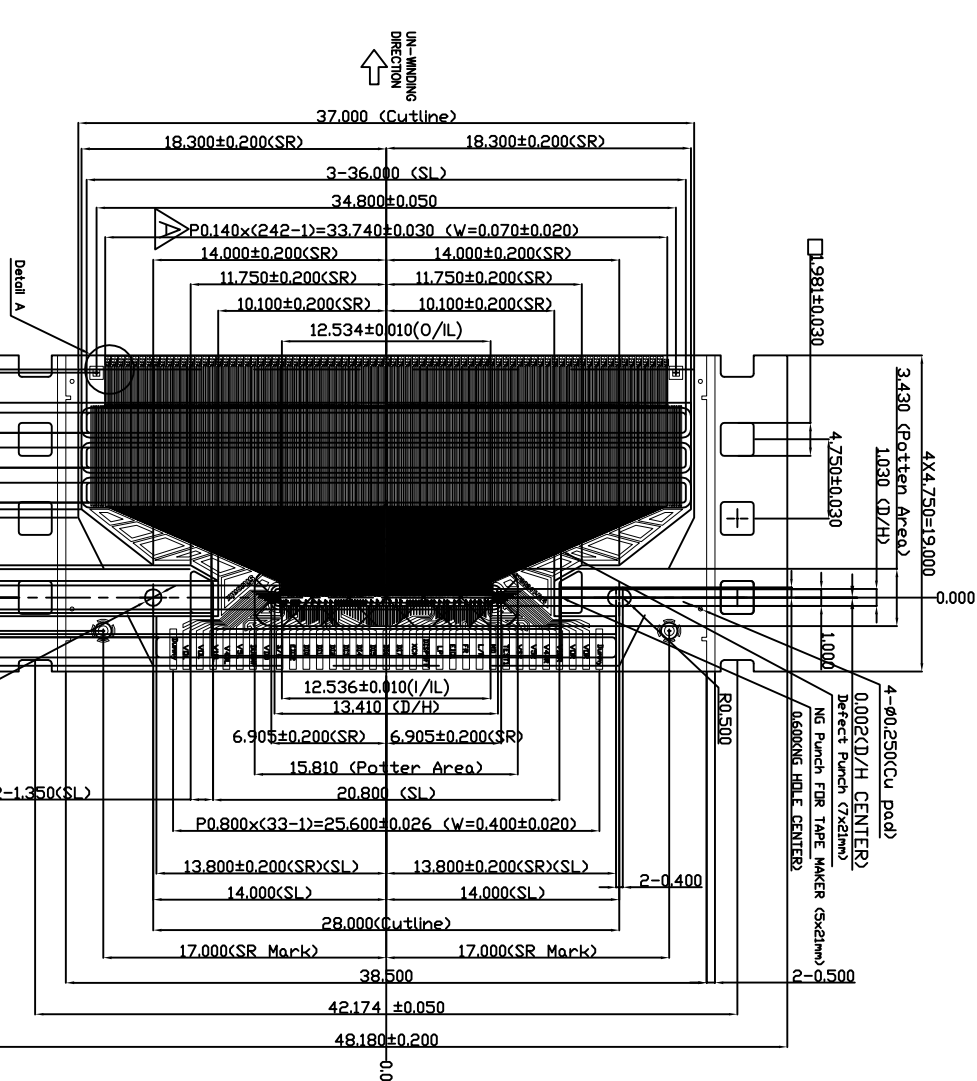
14. REVISION

REVISION	DESCRIPTION	PAGE	DATE
0.10	First release	1-26	2006/12/11
0.11	Change Max. operating voltage to +30V Change Standby Current Application Pin to LGND+GND+VSS	1-26	2007/04/20
0.12	Change operating temperature to 70 °C	16-19	2008/01/24

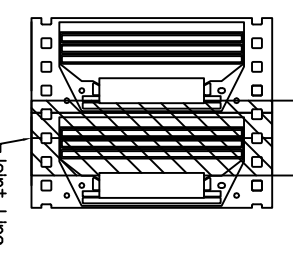
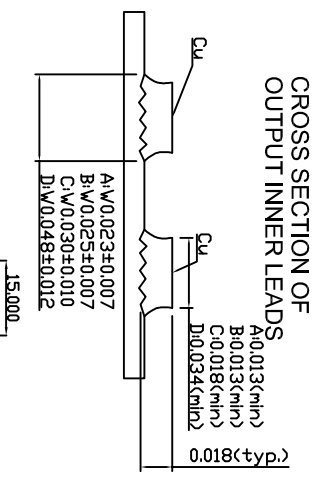
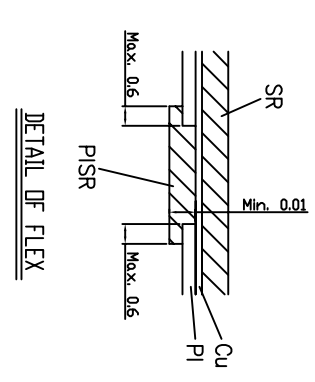
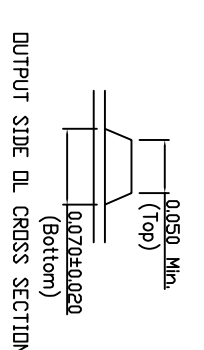
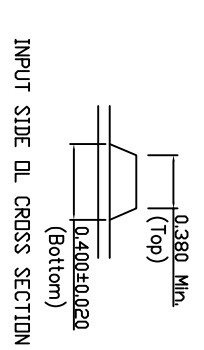
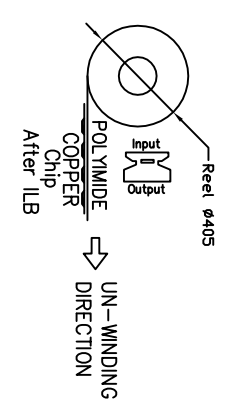
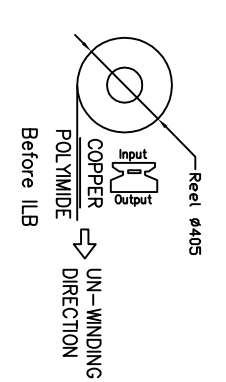
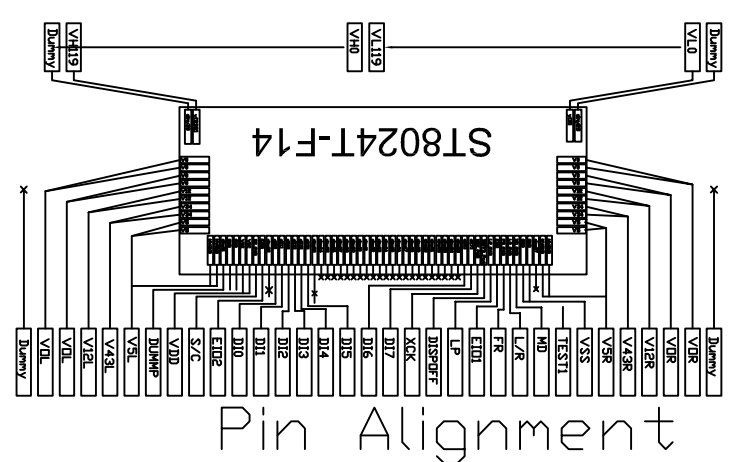
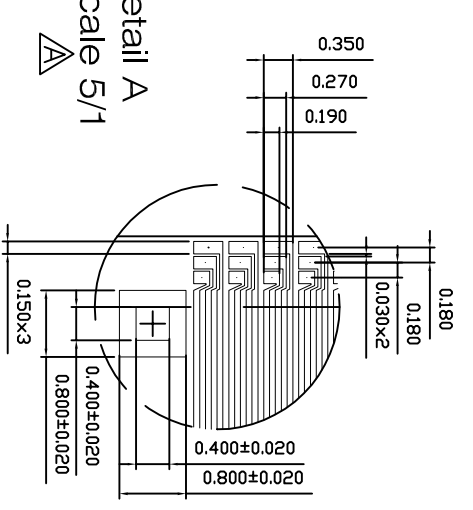
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RevNo.	Revision note.	Date

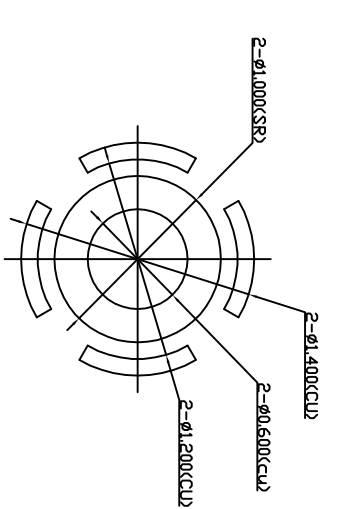
COPPER VIEW



Detail A
Scale 5/1



SR Mark
Scale 10/1



1. Space Tape Material
Leader Tape Material
PKG Reel Size
Polyimide
Adhesive
Copper
Plating
Solder Resist Tolerance:±0.200mm
Flex Coat
Fix Coat
2. ALL CHAMFER IS R0.200mm.
3. SPRING HOLE DIA. FOR 1 TAPE SITE
4. Etching factor = 2.5 for output outer lead.
5. Min. Pitch = 0.25mm
6. Inner Lead Width Measure Location: Bump Center.
7. General Tolerance: ±0.05mm
- Material Description
- Polyester(PET)
Polyetherimide(PEI)
405mm
UP/LEX-S
#7100
RQ-WP
Sn
AE-70-M11
FS-100L
- ATCCT
Daiichi
UBE
Toray
Mitsui
Alphamato
- 75±6 μm
12±3 μm
18±5 μm
0.21±0.05 μm
28 ±14 μm

L1_Copper	L2_SOLDER RESIST	L3_PUNCH	L31_SECOND PUNCH	OTHER:FOLLOW CUSTOMER LAYER	Change	Date
DWG NO:	C/P/N:	ST8024T-F14C	SIMPAL DWG NO:	ST044A-02		96.04.30
Designed by-date:	Checked by-date:	Approved by date:	TOLERANCE:	x ± x.x x.xxx±		

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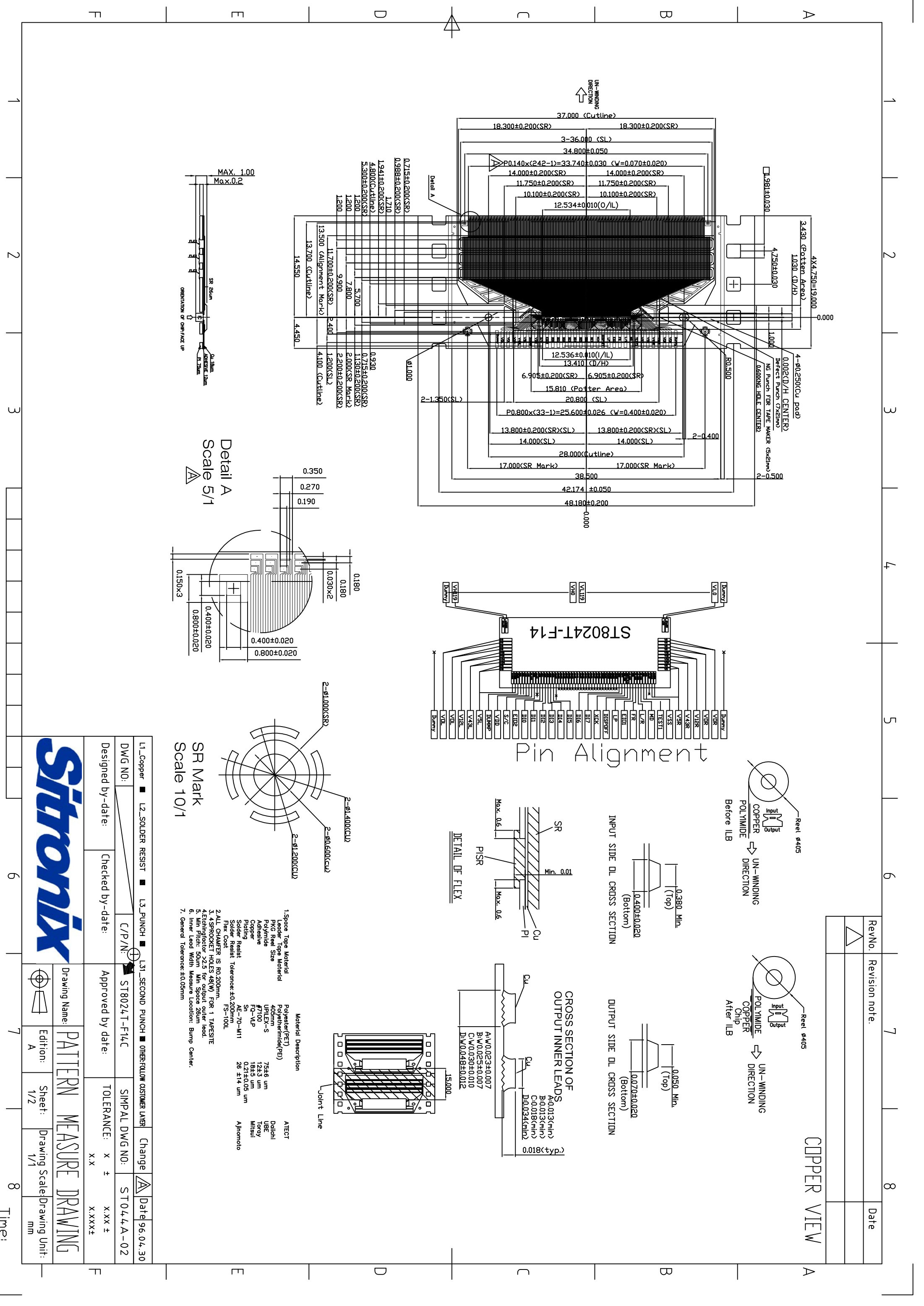
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Edition: A

Sheet: 1/2

Drawing Scale: 1/1

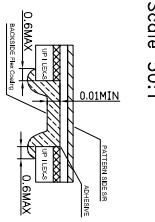
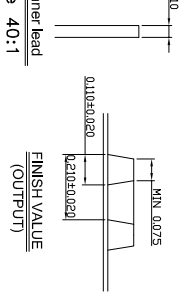
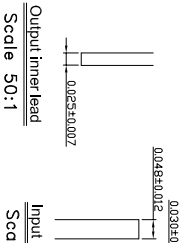
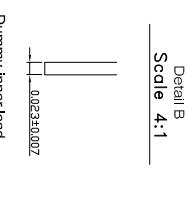
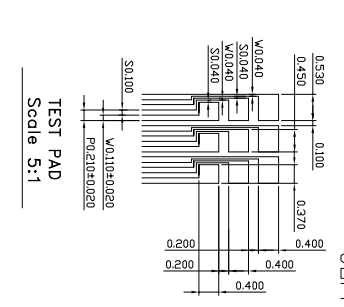
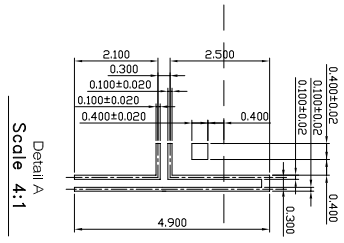
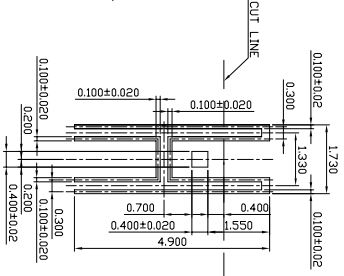
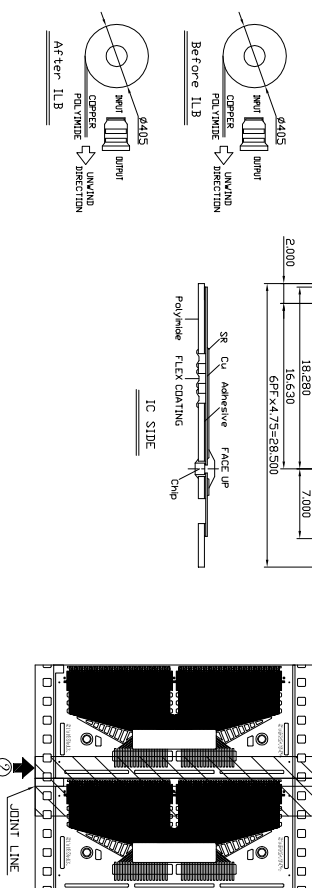
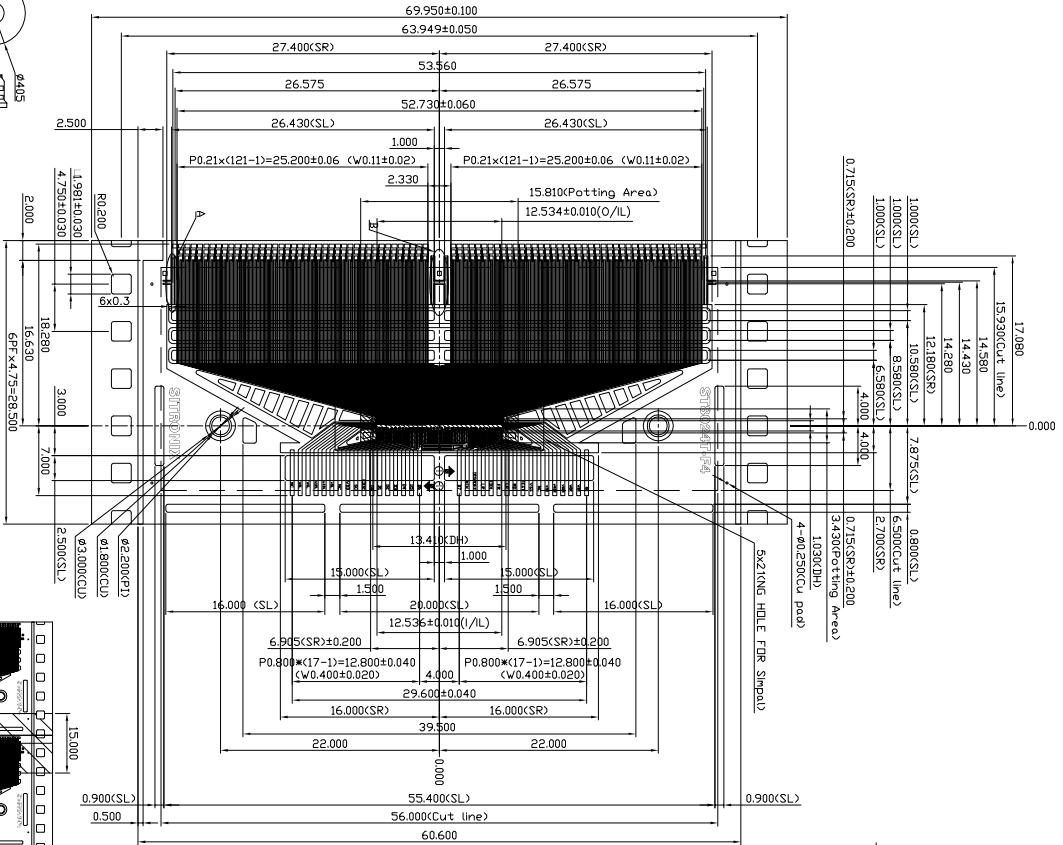
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Time:

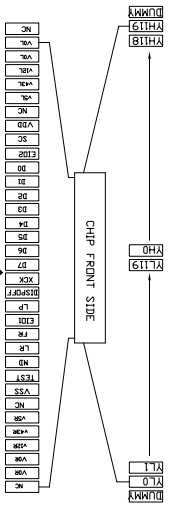
Rev/No.	Revision note.	Date

COPPER VIEW



Pin Wiring Diagram

- Notes:
1. All Chomter is R0.200mm
 2. Spoce Tape Material PET
 3. Leoding Tape Material PI
 4. PKG Reel Size : 405mm
 5. IL width on device hole : Min 10um(Top)
 6. Troce lead width on PI : Min 10um(Top)
 7. All SR Tolerance is ±0.2mm
 8. All Slot Tolerance is ±0.05mm
 9. Modify input outer lead (Test1), <customer request>
 10. Modify input inner lead (Test1), <customer request>
 11. Min. pitch : 50um ; Min. space : 27um



TAPE SPEC	TO W
PRODUCT PITCH	6 PERFORATIONS (28.5mm)
POLYIMIDE	UPLEX-S 75±5um
CU FOIL	FO-VLP 18um±5um
ADHESIVE	TOBAY #7100 12±5um
SOLDER RESIST	AC-70-W11 28±1um
PIER (FLEX)	FS-100L Min10um
PLATING	Sn 0.21±0.05um

Stronix Technology Corp.

Designed by:-date: 95.09.26

Checked by:-date:

Approved by date:

TOLERANCE: x ± xxx±
 x x xxxx±

DWG NO: L1-Copper ■ L2-SOLDER RESIST ■ L3-PUNCH ■ L31-SECOND PUNCH ■ OTHER-FOLLOW CUSTOMER LABEL

C/P/N: ST8024-T-F4, REV. SIMPAL DWG NO. ST012B-01

Drawing Name: PATTERN MEASURE DRAWING

Edition: B

Sheet: 1/1

Drawing Scale: Drawing Unit: mm

Time: