Silicon PNP Power Transistors 2SB1393 2SB1393A

DESCRIPTION

·With TO-220Fa package
·Satisfactory linearity of h_{FE}
·Low collector to emitter saturation voltage
·Complement to type 2SD1985/1985A

APPLICATIONS

·For power amplification

PINNING

PIN	DESCRIPTION
1	Base
2	Collector
3	Emitter

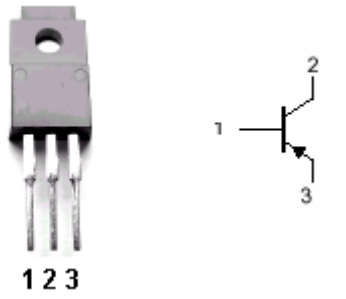

Fig.1 simplified outline (TO-220Fa) and symbol

Absolute maximum ratings(Ta=25□)

SYMBOL	PARAMETER		CONDITIONS	VALUE	UNIT
V_{CBO}	Collector-base voltage	2SB1393	Open emitter	-60	V
		2SB1393A		-80	
V_{CEO}	Collector-emitter voltage	2SB1393	Open base	-60	V
		2SB1393A		-80	
V_{EBO}	Emitter-base voltage		Open collector	-5	V
I_C	Collector current (DC)			-3	A
I_{CM}	Collector current-Peak			-5	A
P_C	Collector power dissipation		T_C=25□	25	W
			T_a=25□	2	
T_j	Junction temperature			150	□
T_{stg}	Storage temperature			-55~150	□

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CHARACTERISTICS

Tj=25□ unless otherwise specified

SYMBOL	PARAMETER		CONDITIONS	MIN	TYP.	MAX	UNIT
$V_{(BR)CEO}$	Collector-emitter breakdown voltage	2SB1393	I_C=-30mA , I_B=0	-60			V
		2SB1393A		-80			
V_{CEsat}	Collector-emitter saturation voltage		I_C=-3A; I_B=-0.375A			-1.2	V
V_{BE}	Base-emitter voltage		V_{CE}=-4V; I_C=-3A			-1.8	V
I_{CES}	Collector cut-off current	2SB1393	V_{CE}=-60V ;V_{BE}=0			-200	μA
		2SB1393A	V_{CE}=-80V; V_{BE}=0				
I_{CEO}	Collector cut-off current	2SB1393	V_{CE}=-30V; I_B=0			-300	μA
		2SB1393A	V_{CE}=-60V; I_B=0				
I_{EBO}	Emitter cut-off current		V_{EB}=-5V; I_C=0			-1.0	mA
h_{FE-1}	DC current gain		I_C=-1A ; V_{CE}=-4V	70		250	
h_{FE-2}	DC current gain		I_C=-3A ; V_{CE}=-4V	10			
f_T	Transition frequency		I_C=-0.1A; V_{CE}=-5V;f=1MHz		20		MHz
Switching times							
t_{on}	Turn-on time		I_C=-1A ;I_{B1}=-0.1A I_{B2}=0.1A;V_{CC}=-50V		0.5		μs
t_s	Storage time				1.2		μs
t_f	Fall time				0.3		μs

◆ **h_{FE-1} Classifications**

Q	P
70-150	120-250

PACKAGE OUTLINE

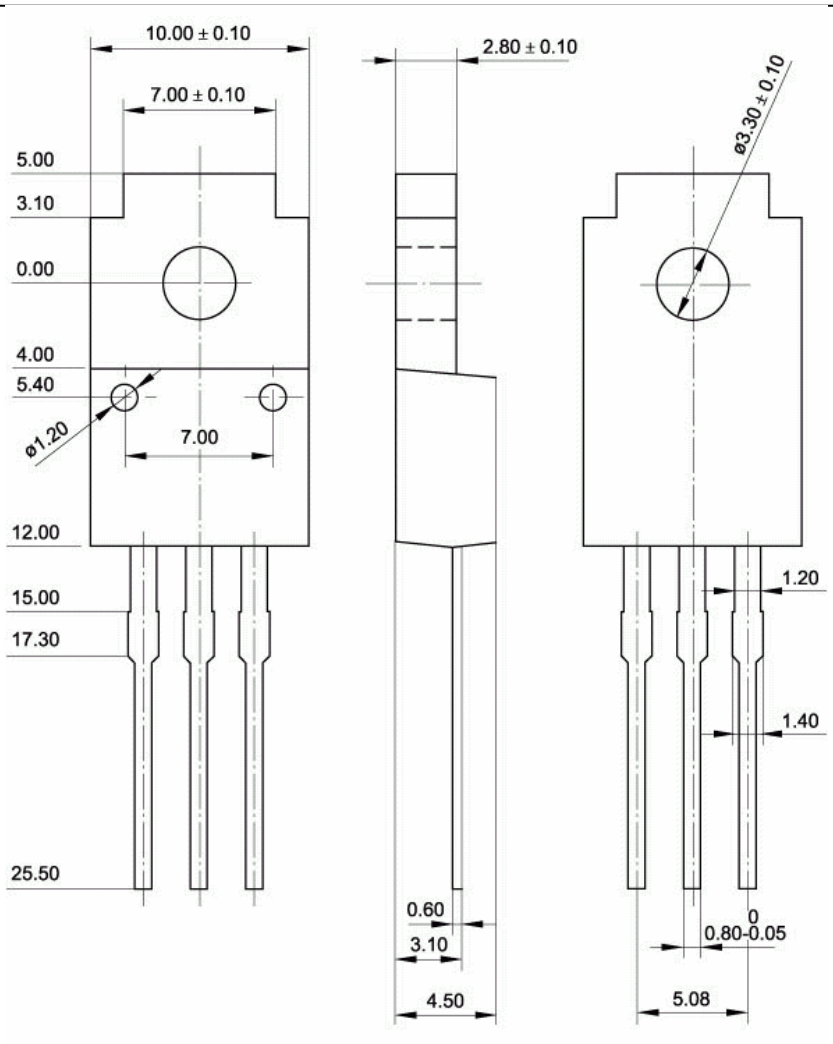

Fig.2 Outline dimensions (unindicated tolerance:±0.15 mm)

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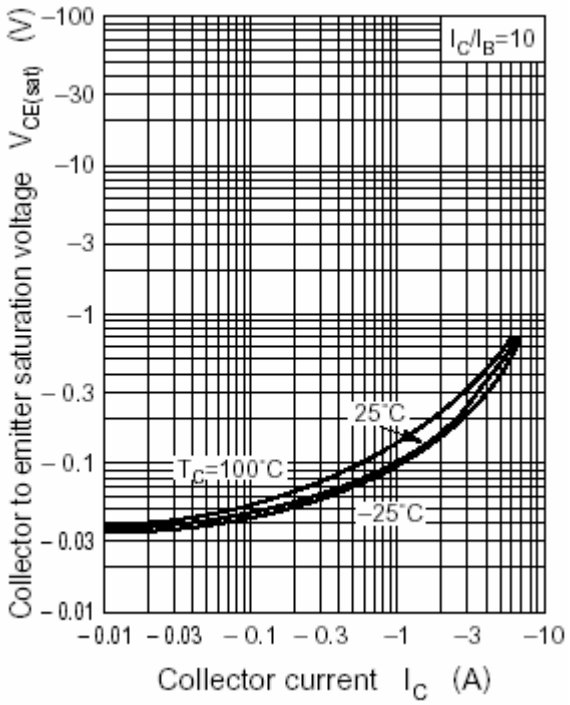

Fig.3 Collector-Emitter Saturation Voltage

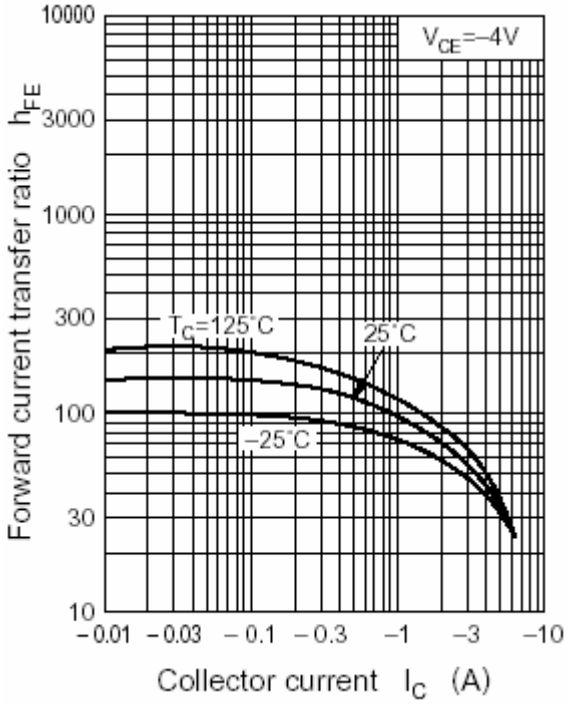

Fig.4 DC current Gain

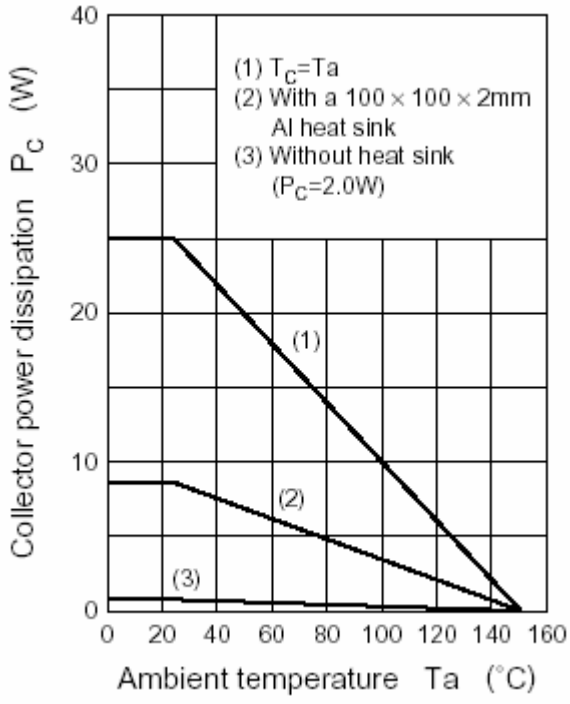

Fig.5 Pc−Ta Derating

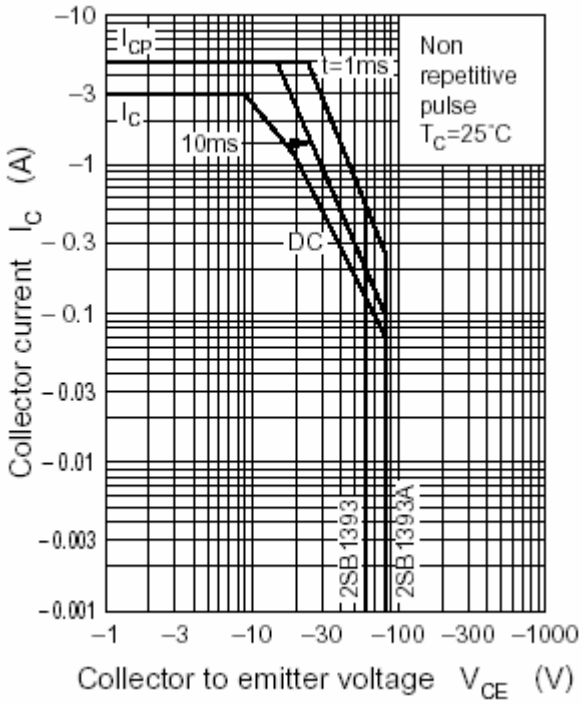

Fig.6 Safe Operating Area