

4V Drive Pch + Pch MOSFET

QS8J4

● Structure

Silicon P-channel MOSFET

● Features

- 1) Low on-resistance.
- 2) High power package(TSMT8).
- 3) Low voltage drive(4V drive).

● Application

Switching

● Packaging specifications

Type	Package	Taping
	Code	TR
	Basic ordering unit (pieces)	3000
QS8J4		○

● Absolute maximum ratings (Ta = 25°C)

Parameter	Symbol	Limits	Unit	
Drain-source voltage	V_{DSS}	-30	V	
Gate-source voltage	V_{GSS}	±20	V	
Drain current	Continuous	I_D	±4	A
	Pulsed	I_{DP} *1	±16	A
Source current (Body Diode)	Continuous	I_s	-1	A
	Pulsed	I_{sp} *1	-16	A
Power dissipation	P_D *2	1.5	W / TOTAL	
		1.25	W / ELEMENT	
Channel temperature	T_{ch}	150	°C	
Range of storage temperature	T_{stg}	-55 to +150	°C	

*1 $P_w \leq 10\mu s$, Duty cycle $\leq 1\%$

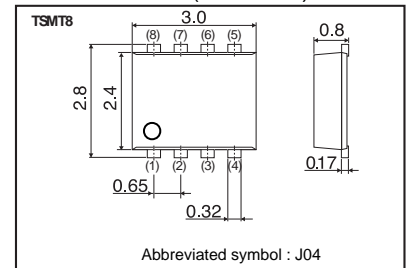
*2 Each terminal mounted on a ceramic board.

● Thermal resistance

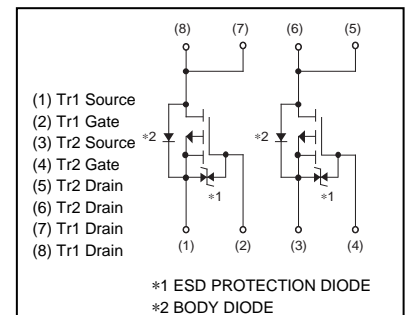
Parameter	Symbol	Limits	Unit
Channel to Ambient	$R_{th}(ch-a)$ *	83.3	°C / W / TOTAL
		100	°C / W / ELEMENT

* Each terminal mounted on a ceramic board.

● Dimensions (Unit : mm)



● Inner circuit



● **Electrical characteristics** (Ta = 25°C)

<It is the same ratings for Tr1 and Tr2.>

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Gate-source leakage	I_{GSS}	-	-	±10	μA	$V_{GS}=\pm 20V, V_{DS}=0V$
Drain-source breakdown voltage	$V_{(BR)DSS}$	-30	-	-	V	$I_D=-1mA, V_{GS}=0V$
Zero gate voltage drain current	I_{DSS}	-	-	-1	μA	$V_{DS}=-30V, V_{GS}=0V$
Gate threshold voltage	$V_{GS(th)}$	-1.0	-	-2.5	V	$V_{DS}=-10V, I_D=-1mA$
Static drain-source on-state resistance	$R_{DS(on)}^*$	-	40	56	mΩ	$I_D=-4A, V_{GS}=-10V$
		-	55	77		$I_D=-2A, V_{GS}=-4.5V$
		-	60	84		$I_D=-2A, V_{GS}=-4V$
Forward transfer admittance	$ Y_{fs} ^*$	3	-	-	S	$I_D=-4A, V_{DS}=-10V$
Input capacitance	C_{iss}	-	800	-	pF	$V_{DS}=-10V$
Output capacitance	C_{oss}	-	120	-	pF	$V_{GS}=0V$
Reverse transfer capacitance	C_{rss}	-	110	-	pF	$f=1MHz$
Turn-on delay time	$t_{d(on)}^*$	-	8	-	ns	$I_D=-2A, V_{DSt}=-15V$
Rise time	t_r^*	-	20	-	ns	$V_{GS}=-10V$
Turn-off delay time	$t_{d(off)}^*$	-	80	-	ns	$R_L=7.5\Omega$
Fall time	t_f^*	-	50	-	ns	$R_G=10\Omega$
Total gate charge	Q_g^*	-	8.4	-	nC	$I_D=-4A, V_{DSt}=-15V$
Gate-source charge	Q_{gs}^*	-	3.0	-	nC	$V_{GS}=-5V$
Gate-drain charge	Q_{gd}^*	-	3.5	-	nC	$R_L=3.8\Omega, R_G=10\Omega$

*Pulsed

● **Body diode characteristics** (Source-Drain) (Ta = 25°C)

<It is the same ratings for Tr1 and Tr2.>

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Forward Voltage	V_{SD}^*	-	-	-1.2	V	$I_s=-4A, V_{GS}=0V$

*Pulsed

● Electrical characteristic curves

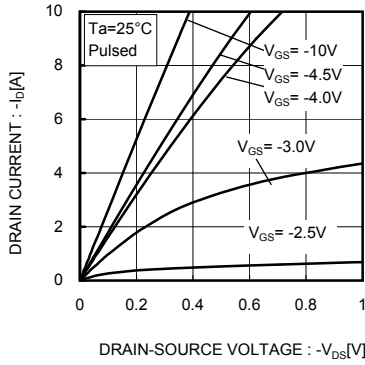


Fig.1 Typical Output Characteristics(I)

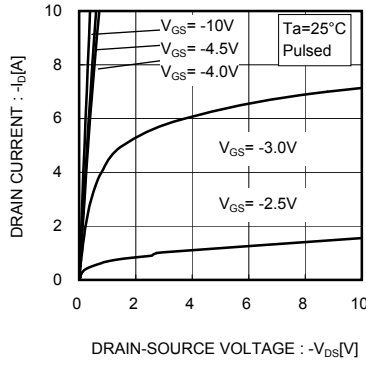


Fig.2 Typical Output Characteristics(II)

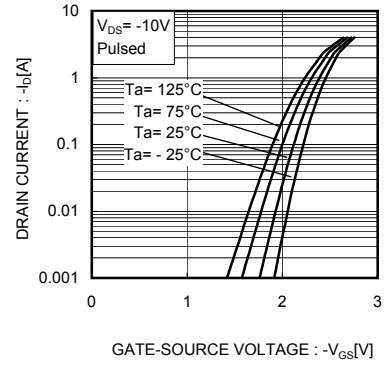


Fig.3 Typical Transfer Characteristics

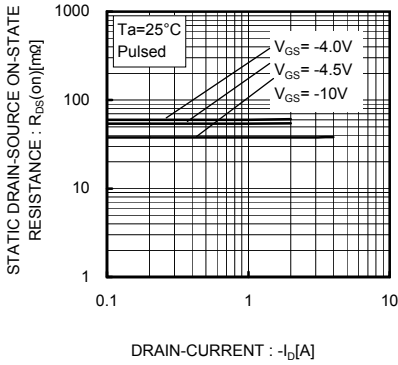


Fig.4 Static Drain-Source On-State Resistance vs. Drain Current(I)

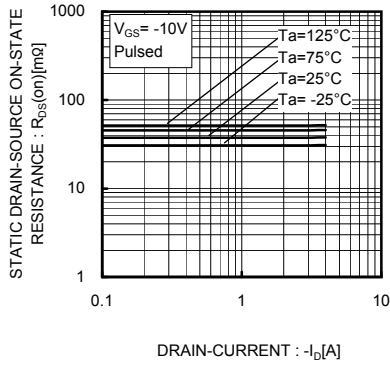


Fig.5 Static Drain-Source On-State Resistance vs. Drain Current(II)

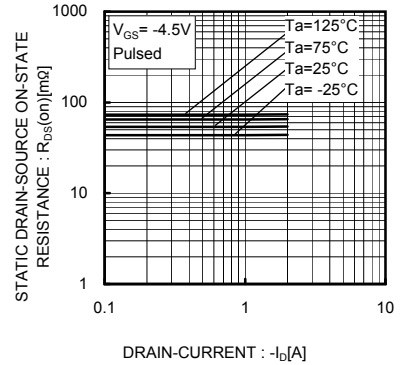


Fig.6 Static Drain-Source On-State Resistance vs. Drain Current(III)

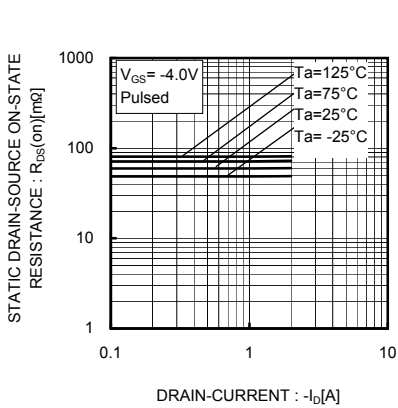


Fig.7 Static Drain-Source On-State Resistance vs. Drain Current(IV)

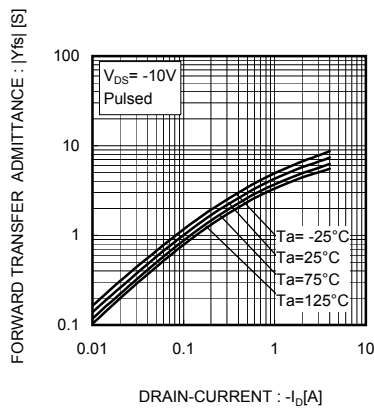


Fig.8 Forward Transfer Admittance vs. Drain Current

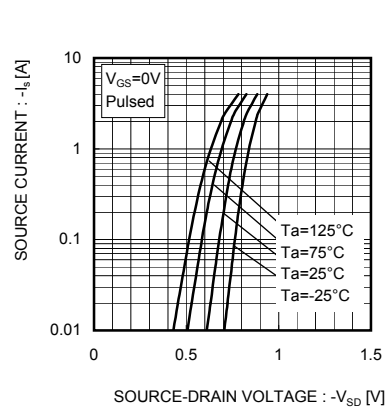


Fig.9 Reverse Drain Current vs. Source-Drain Voltage

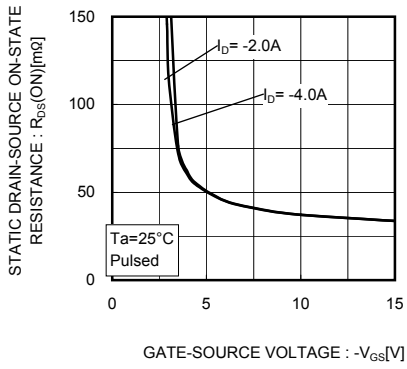


Fig.10 Static Drain-Source On-State Resistance vs. Gate Source Voltage

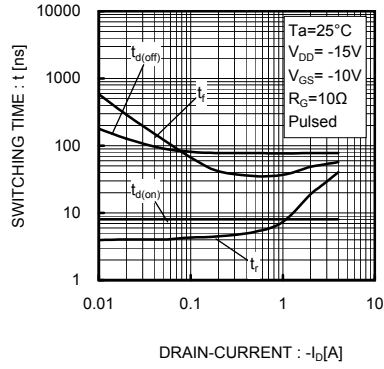


Fig.11 Switching Characteristics

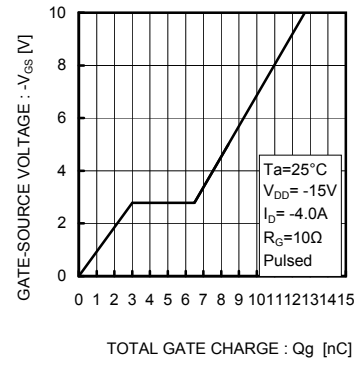


Fig.12 Dynamic Input Characteristics

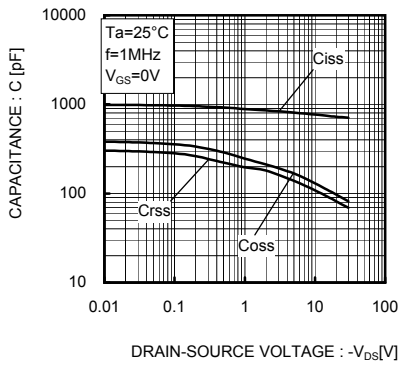


Fig.13 Typical Capacitance vs. Drain-Source Voltage

● Measurement circuits

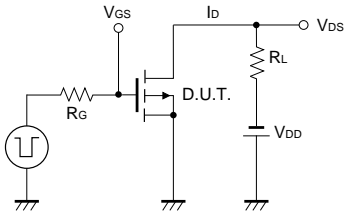


Fig.1-1 Switching Time Measurement Circuit

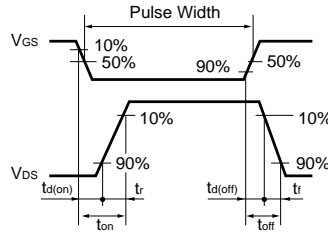


Fig.1-2 Switching Waveforms

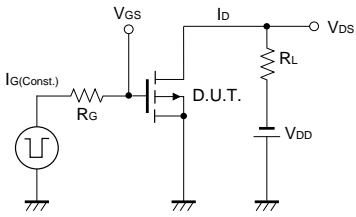


Fig.2-1 Gate Charge Measurement Circuit

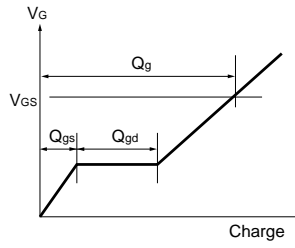


Fig.2-2 Gate Charge Waveform

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