PROCESS CP705

Small Signal Transistor

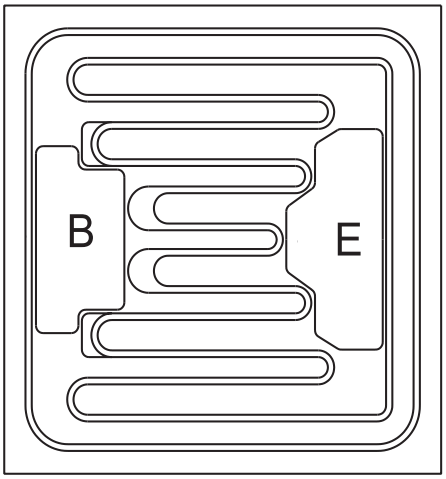
PNP - High Current Transistor Chip

Central™
Semiconductor Corp.

PROCESS DETAILS

Process	EPITAXIAL PLANAR
Die Size	31 x 31 MILS
Die Thickness	9.0 MILS
Base Bonding Pad Area	5.9 x 11.8 MILS
Emitter Bonding Pad Area	6.5 x 13.8 MILS
Top Side Metalization	Al - 30,000Å
Back Side Metalization	Au - 18,000Å

GEOMETRY



BACKSIDE COLLECTOR R1

GROSS DIE PER 4 INCH WAFER

11,300

PRINCIPAL DEVICE TYPES

2N4033
CMPT4033
CXT4033
CZT4033

145 Adams Avenue
Hauppauge, NY 11788 USA
Tel: (631) 435-1110
Fax: (631) 435-1824
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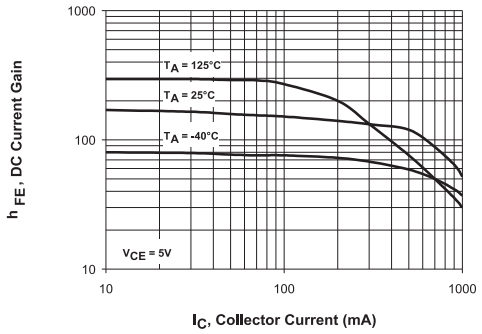
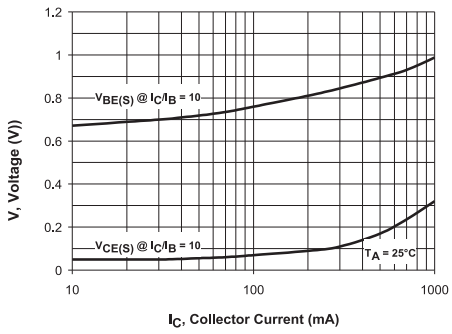
R2 (1-August 2002)

Typical Electrical Characteristics

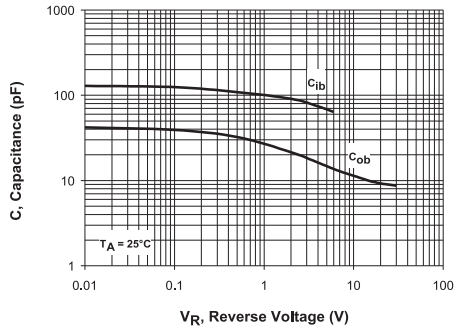
DC Current Gain



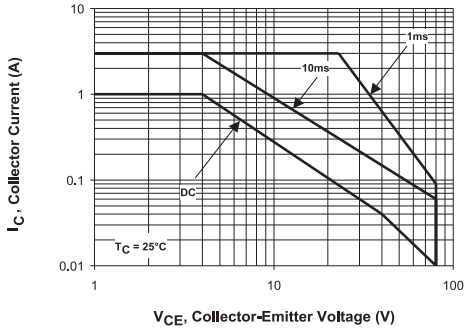
"ON" Voltage



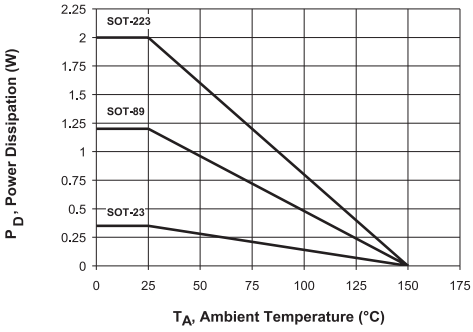
Capacitance



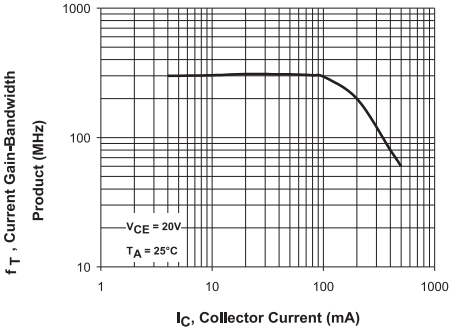
Safe Operating Area



Power Derating



Current Gain-Bandwidth Product



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