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DATA SHEET

ARM POWERED®

LC823410-10R

CMOS IC
Ultra-Low Power Consumption 7.0mW Large-Scale System LSI, GokLow, for IC Recorders

Overview
The LC823410-10R is a system IC that uses ultra-low power consumption technology to realize long-time playback and recording, and has various IC recorder functions. The IC is optimal for use in IC recorder applications.

Features
• ARM7TDMI-S^{TM} [1], AMBA® (AHB/APB) system
  -On-chip SRAM (160kbytes)
  -On-chip ROM (256kbytes)
  -DMA controller (2 channels)
  -Interrupt controller (external 6 channels)
  -SIO (2 channels), UART (3 channels, of which 2 channels run on the 12MHz oscillator XT1.)

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-I^{2}C (1 channel, single master, full speed mode/standard mode support)

-GPIO (multiplexed port I/O pin, 32 channels)

-Plain timer, multiple timer (2 channels, runs on the 12MHz oscillator XT1)

-10-bit A/D converter (4 channels)

-NAND flash memory I/F (multi-level cell NAND)

 4-bit correctable ECC, automatic correction of error bits

-SD card I/F (CPRM not supported) [optional]

 SD card clock can be generated through AHB clock.

-Memory stick I/F [optional]

-USB2.0 device I/F with PHY

 Communication operation possible even when the AHB runs at a low clock rate. Insertion/extraction detection possible even when the PHY clock is stopped.

-RTC (realtime clock)

 Operation at a voltage independent from the internal core operating voltage, and RTC only power on operation possible.

-JTAG ICE

• MP3[*2] hard-wired encoder/decoder

-MPEG1, MPEG2, MPEG2.5

 (Fs=8kHz to 48kHz, 8kbps to 320kbps)

• High quality sound technologies & functions (underlined functions support 96kHz sampling)

-SANYO "AViSS" surround circuit

-YY filter high frequency compensation circuit (2 modes, LP2: High bit rate and LP4: Low bit rate)

-Sampling rate converter. Convertible up to 96kHz (max.) within the range of 0.5 to 64 times

-6-band equalizer. Equalizer characteristics can be adjusted by setting the coefficient.

-Digital volume and mute functions (except the recording system). Both dB and linear rate of change can be designated.

-Level meter (except the recording system)

-Audio timer function. LR clock count and interrupt generation function

• On-chip 16-bit PCM input/output interface. Master/slave mode, I^{2}S support

• 12MHz oscillator XT1 + PLL dedicated for audio enable audio clock generation

 Also supports audio operations using 16.9344MHz oscillator XT2 (optional).

• Supply voltages (typical)

-LOGIC, USB PHY1, XTAL, PLL1, RTC = 1.1V (when no USB devices connected) or 1.5V (when USB devices connected)

-I/O, ADC, USB PHY2, PLL2 = 2.8V (when no USB devices connected) or 3.3V (when USB devices connected)

 *2: MPEG Layer-3 audio coding technology licensed from Fraunhofer IIS and Thomson.

Specifications

Absolute Maximum Ratings at *V$_{SS}$* = 0V

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V$_{DD}$1 V$_{DD}$RTC V$_{DD}$XT AV$_{DD}$PHY1 AV$_{DD}$PLL1		-0.3 to 1.8	V
	V$_{DD}$2 V$_{DD}$3 AV$_{DD}$ADC AV$_{DD}$PHY2 AV$_{DD}$PLL2		-0.3 to 3.96	V
Input voltage	V$_I$		-0.3 to *V$_{DD}$*+0.3 (max3.96)	V
	V$_{IUSB}$	DP and DM pins	-0.3 to 5.25	V
Operating ambient temperature	Topr		-30 to +70	°C
Storage ambient temperature	Tstg		-55 to 125	°C

Allowable Operating Range at Ta = -30 to +70°C

Parameter	Symbol	Conditions	Low Voltage Operation			High Voltage Operation			Unit
			min	typ	max	min	typ	max	
Supply voltage	$V_{DD}1$		1.05	1.1	1.2	1.35	1.5	1.65	V
	$V_{DD}XT$		1.05	1.1	1.2	1.35	1.5	1.65	V
	$AV_{DD}PLL1$		1.05	1.1	1.2	1.35	1.5	1.65	V
	$AV_{DD}PLL2$		2.7	2.8	3.3	2.7	2.8	3.6	V
	$V_{DD}RTC$		0.9	1.1	1.65	0.9	1.5	1.65	V
	$V_{DD}2$		2.7	2.8	3.3	2.7	2.8	3.6	V
	$V_{DD}3$		2.7	2.8	3.3	2.7	2.8	3.6	V
			1.7	1.8	1.95	1.7	1.8	1.95	V
	$AV_{DD}ADC$		2.7	2.8	3.3	2.7	2.8	3.6	V
	$AV_{DD}PHY1$		1.05(*1)	1.1	1.2	1.35	1.5	1.65	V
	$AV_{DD}PHY2$		2.7(*1)	2.8	3.3	3.0	3.3	3.6	V
Input voltage	V_{IN}		0		*V_{DD}*	0		*V_{DD}*	V

(*1) In the low-voltage operation state, although transition from this state to the high-voltage operation state and operation after the transition are guaranteed, all operations are not guaranteed in the low-voltage state.

(*2) The relations below are assumed in all operation states.
- $V_{DD}1=V_{DD}XT=AV_{DD}PLL1=AV_{DD}PHY1$
- $AV_{DD}PHY2>=AV_{DD}ADC$
- $V_{DD}2>=AV_{DD}PLL2$
- $V_{DD}2>=V_{DD}3$
  where,
- $V_{DD}1$, $V_{DD}XT$, and $AV_{DD}HY1$ have the same electrical potential because they are connected within the IC.
- $AV_{DD}PLL1>=V_{DD}1$
- Besides the above two points, voltage differences up to 0.1V are considered to be equal.
  Also, during RTC-only operation,
  The above $V_{DD}RTC$ voltage can be applied at BACKUPB = Low input and application of
  $V_{DD}* = 0V$ except for $V_{DD}RTC$.

(*3) Low-voltage operation: This is an operation state that enables low power consumption during music playback and other operations.
  High-voltage operation: This is an operation state on the assumption that USB is used.

Parameter	Symbol	Function	Low Voltage Operation			High Voltage Operation			Unit
			min	typ	max	min	typ	max	
Input oscillation frequency	Fxin1	ARM & Peripherals		12		12MHz±100p-pm (using USB)			MHz
	FxinRTC	RTC		32.768			32.768		kHz
	Fxin2	AUDIO		16.9344			16.9344		MHz
	Frc	RC	0.4	1	2	0.4	1	2	MHz
Internal operating frequency	Fahb	ARM AHB	0		30	0		60	MHz
	Fapb	ARM APB	0		30	0		60	MHz
	Faud	AUDIO	0	16.9344	36.864	0	16.9344	36.864	MHz
SD I/F clock frequency	Fsdclk	Normal			19			24	MHz
		High speed ($V_{DD}3>=2.7V$ SDDRV=1)			25			40	MHz
MS I/F clock frequency	Fsclk	Parallel			30			30	MHz
		Serial			20			20	MHz

DC characteristic at Ta = -30 to +70°C, $V_{DD}2$ = 2.7 to 3.6V, $V_{DD}RTC$ = 0.9 to 1.65V, $V_{DD}3$=1.7 to 1.95V, 2.7 to 3.6V

Parameter	Symbol	Pins	Conditions	Ratings			Unit
				min	typ	max	
Input high level voltage	V_{IH}	(1)		$0.7 \times V_{DD}2$			V
		(2)	Schmitt	$0.75 \times V_{DD}2$			V
		(3)		$0.7 \times V_{DD}RTC$			V
Input low level voltage	V_{IL}	(1)				$0.3 \times V_{DD}2$	V
		(2)	Schmitt			$0.25 \times V_{DD}2$	V
		(3)				$0.2 \times V_{DD}RTC$	V
Output high level voltage	V_{OH}	(4)	I_{OH}=-2mA	$V_{DD}2$-0.4			V
		(5)	I_{OH}=-4mA	$V_{DD}3$-0.34			V
		(6)	I_{OH}=-0.3mA	$V_{DD}RTC$-0.3			V
Output low level voltage	V_{OL}	(4)	I_{OL}=2mA			0.4	V
		(5)	I_{OL}=4mA			0.34	V
		(6)	I_{OL}=0.3mA			0.3	V
Output leakage current	I_{OZ}	(7)	Hi-Z output	-10		10	µA
Pull-up resistor	Rup	(8)		50	100	150	kΩ
Pull-up resistor	Rup	(9)		30	45	80	kΩ
Pull-down resistor	Rdn	(10)		40	70	160	kΩ
Pull-down resistor	Rdn	(11)		20	50	90	kΩ

(1) FD7-0, SDCMD, SDAT3-0, BCK, LRCK, MCLK, SCL, SDA, TIOCA1-0, SDI1, RXD2-0, SDO0, TXD2-0, XFCE1-0, PHI, TCK, TDI, TMS, SDI0, DIN, SDCD, SDWP

(2) TEST6-1, NTRST, NRES, EXTINT6-0, EXTFIQ, SCK1-0, XFBSY

(3) BACKUPB, VDET

(4) SCK1-0, FD7-0, EXD15-0, BCK, LRCK, MCLK, SCL, SDA, TIOCA1-0, SDI1, SDI0, RXD2-0, TXD2-0, XFCE1-0, PHI, EXTFIQ, EXTINT4-0, DOUT, RTCK, TDO, XALE, XCLE, XFRE, XFWE, XFWP

(5) SDCLK, SDCMD, SDAT3-0

(6) RTCINT

(7) SCK1-0, FD7-0, SDCMD, SDAT4-1, BCK, LRCK, MCLK, SCL, SDA, TIOCA1-0, SDI1, RXD2-0, SDO1-0, TXD2-0, XFCE1-0, PHI, EXTFIQ, EXTINT4-0, RTCK, XALE, XCLE, XFRE, XFWE, XFWP, RTCINT

(8) EXTFIQ, SCK1, SDO1, TXD2-0, RXD2-0, TIOCA1-0, SDI1, EXTINT4-0, XFCE1-0, SCL, SDA, LRCK, MCLK, PHI, SCK0, SDI0, SDO0, TCK, TDI, TMS, NTRST ,XFWE, XFRE, XALE, XCLE, XFWP

(9) SDCMD, SDAT3-0, SDCD

(10) SDAT3-0

(11) DIN, FD7-0

(Caution)

The following pins are not included in DC characteristics.

RREF, DM, DP, VCNT1, VCNT2, AN3-0, XIN1, XIN2, XIN32K, XOUT1, XOUT2, XOUT32K

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PLL1 Characteristics at Ta = -30 to +70°C

Parameter	Symbol	Conditions	$AV_{DD}PLL1$=1.05 to 1.2V			$AV_{DD}PLL1$=1.35 to 1.65V			Unit
			min	typ	max	min	typ	max	
VCO voltage	VCNT1		0		$AV_{DD}PLL1$	0		$AV_{DD}PLL1$	V
VCO maximum oscillation frequency	Fmax		90			180			MHz
VCO minimum oscillation frequency	Fmin				60			60	MHz
Phase comparison frequency	Fref				30			30	MHz
PLL lock time	Tlock			5	10		5	10	ms

PLL2 Characteristics at Ta = -30 to +70°C, $AV_{DD}PLL2$ = 2.7 to 3.6V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
VCO voltage	VCNT2		0		$AV_{DD}PLL2$	V
VCO maximum oscillation frequency	Fmax		40			MHz
VCO minimum oscillation frequency	Fmin				15 (*1)	MHz
Phase comparison frequency	Fref				17	MHz
PLL lock time	Tlock			10	15	ms

(*1) When a clock with a frequency lower than 15MHz is required, for example 12.288MHz (= 32kHz * 384, audio circuit operation clock at a sampling frequency of 32kHz), this is generated by frequency dividing the clock by 2 as follows.

12.288MHz = 24.576MHz/2

10-bit AD Converter Characteristics at Ta = 25°C, $AV_{DD}ADC$ = 3.3V, $AV_{SS}ADC$ = 0V

Parameter	Symbol	Conditions	Ratings			Unit	Pin
			min	typ	max		
ADC power supply	VAVRH		2.7		3.6	V	$AV_{DD}ADC$
ADC ground voltage	VAVRL		0			V	$AV_{SS}ADC$
Analog input voltage	VAN		VAVRL		VAVRH	V	AN3-AN0
ADC resolution	N				10	Bit	AN3-AN0
ADC operation clock	FC				16.5	MHz	
ADC conversion frequency	Fs				1.04	MHz	
ADC sample hold time	Twr		120			ns	
Differential linearity error	FDIF	NEFFECT=10			±1.5	LSB	AN3-AN0
Linearity error	FLN	NEFFECT=10			±4.0	LSB	AN3-AN0
Zero-scale offset voltage (Transit voltage from 0 to 1)	Vtz		VAVRL-0.1	VAVRL	VAVRL+0.1	V	AN3-AN0
Full-scale offset voltage (Transit voltage from 1022 to 1023)	Vtf		VAVRH-0.1	VAVRH	VAVRH+0.1	V	AN3-AN0
Ladder stabilization time (*1)	Tstr	After STBY released	1			μs	
Reference resistor (*1)	Rr			770		Ω	
Power dissipation (*1)	Pd			15		mW	

(*1) All the characteristics are design values.

USB Interface Characteristics at Ta = -30 to +70°C, $V_{DD}1$=1.35 to 1.65V, $AV_{DD}PHY1$=1.35 to 1.65V, $AV_{DD}PHY2$=3.0 to 3.6V

Parameter	Symbol	Conditions	Ratings min	Ratings typ	Ratings max	Unit
Output pin impedance	Z_{HSDRV}	Includes R_S resistor	40.5		49.5	Ω
Bus pull-up resistor on upstream forcing port	R_{PU1}	FS idle	0.900		1.575	kΩ
Bus pull-up resistor on upstream forcing port	R_{PU2}	FS receiving or transmitting	1.425		3.090	kΩ
Termination voltage for upstream forcing port pullup (full-speed)	V_{TERM}		3.15		3.45	V
Input levels for full-speed:						
High-level input voltage (drive)	V_{IH}		2.0			V
High-level input voltage (floating)	V_{IHZ}		2.7		3.6	V
Low-level input voltage	V_{IL}				0.8	V
Differential input sensitivity	V_{DI}	|(D+)-(D-)|	0.2			V
Differential common mode range	V_{CM}	Includes V_{DI} range Refer to figure 2.1	0.8		2.5	V
Output levels for full-speed:						
High-level output voltage	V_{OH}	R_L of 14.25kΩ to V_{SS}	2.8		3.6	V
Low-level output voltage	V_{OL}	R_L of 1.425kΩ to 3.6V	0.0		0.3	V
SE1	V_{OSE1}		0.8			V
Output signal crossover point voltage	V_{CRS}	Refer to figure 2.1	1.3		2.0	V
Input levels for high-speed:						
High-speed squelch detection threshold (differential signal)	V_{HSSQ}		100		150	mV
High-speed data signaling common mode voltage range	V_{HSCM}		-50		+500	mV
High-speed differential input signaling level	Refer to figure 2.2					
Output levels for high-speed:						
High-speed idle state	V_{HSOI}		-10.0		+10	mV
High-speed data signaling high	V_{HSOH}		360		440	mV
High-speed data signaling low	V_{HSOL}		-10.0		+10	mV
Chirp J level (different signal)	V_{CHIRPJ}		700		1100	mV
Chirp K level (different signal)	V_{CHIRPK}		-900		-500	mV
Time to active-state:						
Time from idle (standby/ suspend) state to active state (*)	T_{ACT}				1	ms

States identified by an asterisk (*)

- Idle (standby/suspend) state: Either one of the following 4 states:
  - Either one of $AV_{DD}PHY1$ and $AV_{DD}PHY2$ is lower than the guaranteed operating voltage.
  - (USB register) DeviceControl: SuspendSts=Susp3endSet=1 (USBPHY suspended state)
  - (USB register) DeviceControl: RstPhy=1 (USBPHY reset state)
  - (SYSCON register) USBCTL: SHSTBY=1 (USBPHY standby state)

  For details on the registers, see the LC823410-09C-E User's Manual (Expansion Module).
- Active-state: Any state in which the IC is not in any of the Idle (standby/suspend) states.

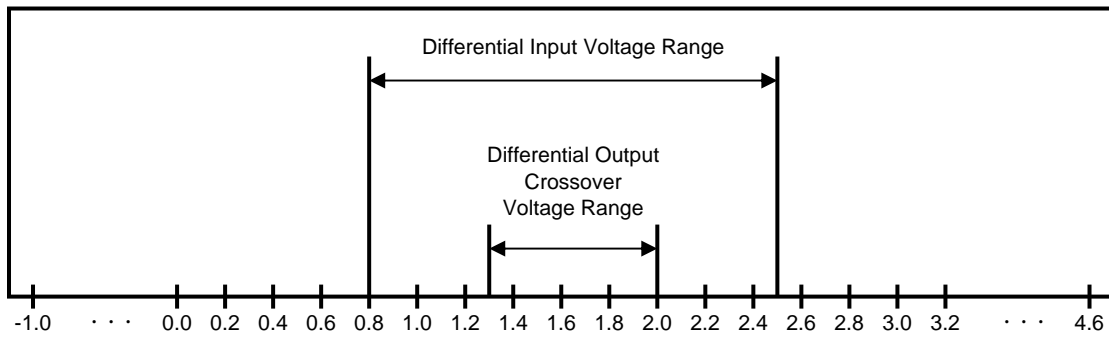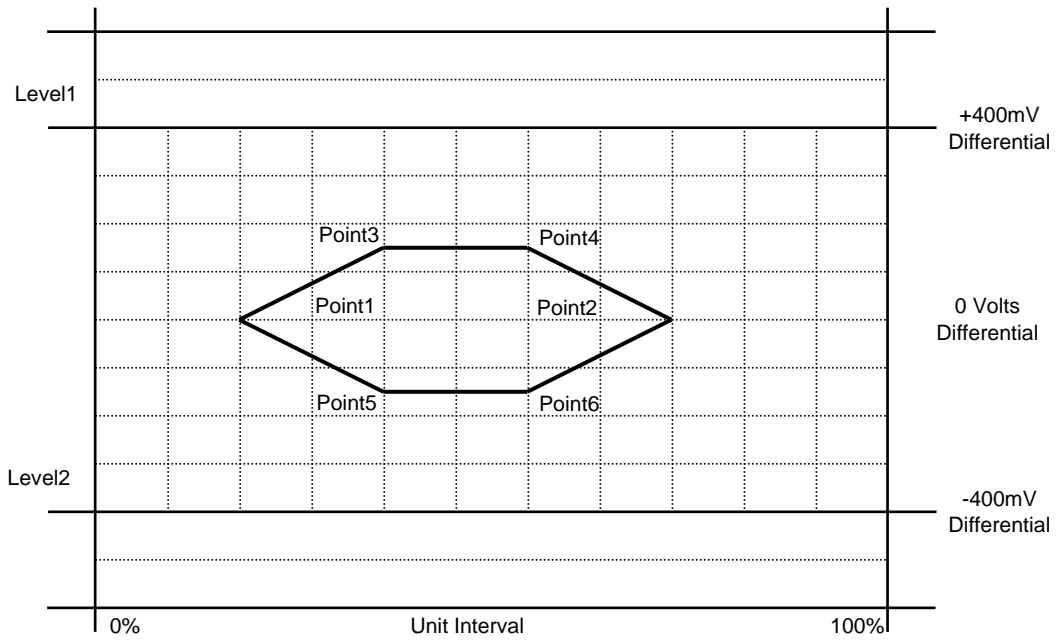Figure 2.1: Differential Input Sensitivity Range for Full-speed

Figure 2.2: Differential Input Sensitivity Range for High-speed

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AC Characteristics: Reset at Ta = -30 to +70°C, $V_{DD}1$ = 1.05 to 1.65V, $V_{DD}2$ = 2.7 to 3.6V

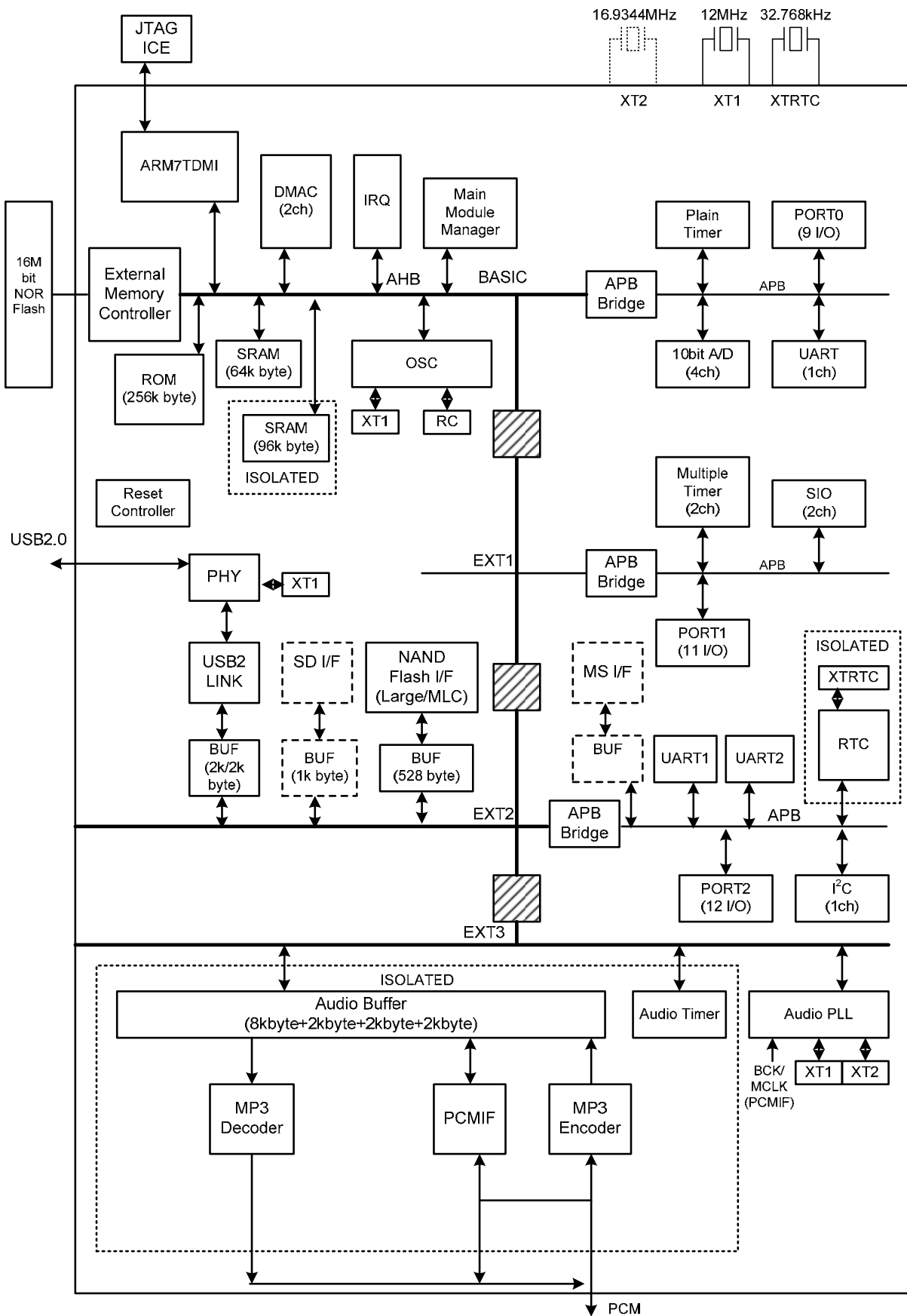| Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Reset active time	$t_{RESW}1$	Time after both of $V_{DD}1$ and $V_{DD}2$ reached within the allowable operation voltage range	10			µs
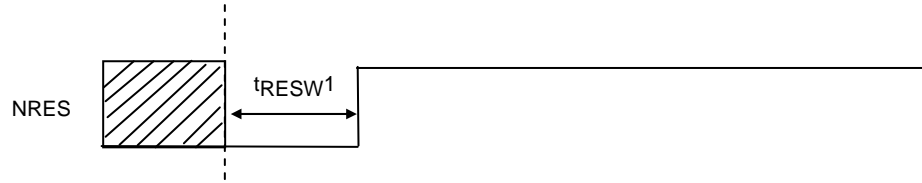
Package Dimensions

unit : mm (typ)

3257A

SANYO : TQFP120(14X14)
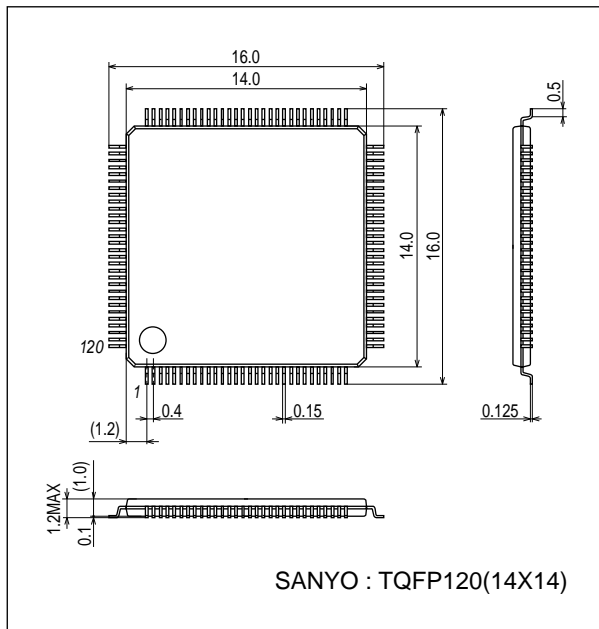
Block Diagram

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Pin Assignments

I/O			Pin Characteristics			
I	Input pin	3IC	3.3V CMOS input	1IC	1.5V CMOS input
O	Output pin	3IS	3.3V Schmitt input	1T3	1.5V 0.3mA tristate output
B	Bi-directional pin	3ICU	3.3V CMOS input pullup	X	Oscillation amplifier
P	Power supply pin	3ICD	3.3V CMOS input pulldown	3A	3.3V analog
		3ISU	3.3V Schmitt input pullup	1A	1.5V analog
		3O2	3.3V 2mA output		
		3T2	3.3V 2mA tristate output		
		3O6	3.3V 6mA output		
		3T6	3.3V 6mA tristate output		

No.	Name	I/O	Characteristic	Function
1	TEST3	I	3IS	Test pin (normally tied to low)
2	TEST4	I	3IS	Test pin (normally tied to low)
3	TEST5	I	3IS	Test pin (normally tied to low)
4	TEST6	I	3IS	Test pin (normally tied to low)
5	TCK	I	3ICU	JTAG test clock
6	RTCK	O	3O2	JTAG test returned clock
7	NTRST	I	3ISU	JTAG test reset
8	TDI	I	3ICU	JTAG test data input
9	TMS	I	3ICU	JTAG test mode select
10	TDO	O	3O2	JTAG test data output
11	NRES	I	3IS	Reset input
12	PHI(P11)	B	3ICU/3T2	AHB bus clock output/32.768kHz clock output/GPIO
13	EXTFIQ(P2F)	B	3ISU/3T2	External FIQ interrupt/GPIO
14	SCK0(P08)	B	3ISU/3T2	Serial I/F 0 clock/GPIO
15	SDO0(P09)	B	3ICU/3T2	Serial I/F 0 output data/GPIO
16	SDI0(P0A)	B	3ICU/3T2	Serial I/F 0 input data/GPIO
17	SCK1(P14)	B	3ISU/3T2	Serial I/F 1 clock/GPIO
18	SDO1(P15)	B	3ICU/3T2	Serial I/F 1 output data/GPIO
19	SDI1(P16)	B	3ICU/3T2	Serial I/F 1 input data/GPIO
20	TXD1(P2A)	B	3ICU/3T2	UART1 transmit data/GPIO
21	RXD1(P2B)	B	3ICU/3T2	UART1 receive data/GPIO
22	TI0CA0(P19)	B	3ICU/3T2	Multiple timer input capture/output compare A0/GPIO
23	TI0CA1(P1B)	B	3ICU/3T2	Multiple timer input capture/output compare A1/GPIO
24	$V_{DD}1$	P		Digital 1.5V power supply
25	$V_{DD}2$	P		Digital 3.3V power supply
26	V_{SS}	P		Digital ground
27	TXD0(P1D)	B	3ICU/3T2	UART0 transmit data/GPIO
28	RXD0(P1E)	B	3ICU/3T2	UART0 receive data/GPIO
29	XFWE(P01)	B	3ICU/3T2	NAND FLASH write enable
30	XFRE(P02)	B	3ICU/3T2	NAND FLASH read enable
31	XALE(P03)	B	3ICU/3T2	NAND FLASH address latch enable
32	XCLE(P04)	B	3ICU/3T2	NAND FLASH command latch enable
33	XFCE1(P1F)	B	3ICU/3T2	NAND FLASH chip enable 1/GPIO
34	XFCE0(P00)	B	3ICU/3T2	NAND FLASH chip enable 0/GPIO
35	XFWP(P05)	B	3ICU/3T2	NAND FLASH write protect/GPIO
36	XFBSY	I	3IS	NAND FLASH busy
37	FD0	B	3ICD/3T2	NAND FLASH data bit0
38	FD1	B	3ICD/3T2	NAND FLASH data bit1
39	$V_{DD}2$	P		Digital 3.3V power supply
40	V_{SS}	P		Digital ground

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No.		I/O	Characteristic	Function
41	FD2	B	3ICD/3T2	NAND FLASH data bit2
42	FD3	B	3ICD/3T2	NAND FLASH data bit3
43	FD4	B	3ICD/3T2	NAND FLASH data bit4
44	FD5	B	3ICD/3T2	NAND FLASH data bit5
45	FD6	B	3ICD/3T2	NAND FLASH data bit6
46	FD7	B	3ICD/3T4	NAND FLASH data bit7
47	EXTINT0(P21)	B	3ISU/3T2	External interrupt bit0/GPIO
48	EXTINT1(P22)	B	3ISU/3T2	External interrupt bit1/GPIO
49	EXTINT2(P23)	B	3ISU/3T2	External interrupt bit2/GPIO
50	EXTINT3(P24)	B	3ISU/3T2	External interrupt bit3/GPIO
51	EXTINT4(P25)	B	3ISU/3T2	External interrupt bit4/GPIO
52	$V_{DD}1$	P		Digital 1.5V power supply
53	$V_{DD}2$	P		Digital 3.3V power supply
54	V_{SS}	P		Digital ground
55	DOUT	O	3O2	PCM output data
56	DIN	I	3ICD	PCM input data
57	BCK	B	3IC/3T2	PCM bit clock
58	LRLK(P12)	B	3ICU/3T2	PCM LR clock/GPIO
59	MCLK(P13)	B	3ICU/3T2	PCM main clock/GPIO
60	SCL(P28)	B	3ICU/3T2	I^{2}C SCL clock/GPIO
61	SDA(P29)	B	3ICU/3T2	I^{2}C SDA data/GPIO
62	TXD2(P2C)	B	3ICU/3T2	UART2 transmit data/GPIO
63	RXD2(P2D)	B	3ICU/3T2	UART2 receive data/GPIO
64	TEST1	I	3IS	Test pin (normally tied to Low)
65	TEST2	I	3IS	Test pin (normally tied to Low)
66	$V_{DD}1$	P		Digital 1.5V power supply
67	SDWP	I	3IC	SD card write protect
68	SDCD/INS	I	3ICU	SD card detect/MSINS
69	SDCMD/BS	B	3ICU/3T6	SD card command/MSBS
70	SDCLK/SCLK	O	3O6	SD card clock/MS clock
71	SDAT0/DATA0	B	3ICUD/3T6	SD card data/MS data
72	V_{SS}	P		Digital ground
73	$V_{DD}3$	P		Digital 3.3V/1.8V power supply
74	SDAT1/DATA1	B	3ICUD/3T6	SD card data/MS data
75	SDAT2/DATA2	B	3ICUD/3T6	SD card data/MS data
76	SDAT3/DATA3	B	3ICUD/3T6	SD card data/MS data
77	$AV_{DD}PLL1$	P		PLL1 analog power supply
78	$AV_{SS}PLL1$	P		PLL1 analog ground
79	VCNT1	O	1A	PLL1 VCO control
80	$V_{DD}XT$	P		System /USB PHY oscillation amplifier 1.5V power supply
81	$V_{SS}XT$	P		System /USB PHY oscillation amplifier ground
82	$X_{IN}1$	I	X	System /USB PHY oscillation amplifier input
83	$X_{OUT}1$	B	X	System /USB PHY oscillation amplifier output
84	$V_{DD}RTC$	P		RTC power supply
85	$V_{SS}RTC$	P		RTC ground
86	XOUT32K	O	X	RTC 32.768kHz oscillation amplifier output
87	XIN32K	I	X	RTC 32.768kHz oscillation amplifier input
88	VDET	I	1IC	Voltage detect input
89	RTCINT	O	1T3	RTC interrupt output
90	BACKUPB	I	1IC	RTC mode (RTC only or whole IC)
91	$AV_{DD}PHY1$	P		USB PHY 1.5V power supply
92	$AV_{SS}PHY1$	P		USB PHY analog ground

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No.		I/O	Characteristic	Function
93	$AV_{SS}PHY1$	P		USB PHY analog ground
94	RREF	B	3A	USB PHY reference resistor
95	$AV_{SS}PHY2$	P		USB PHY analog ground
96	$AV_{DD}PHY2$	P		USB PHY analog 3.3V power supply
97	$AV_{DD}PHY2$	P		USB PHY analog 3.3V power supply
98	$AV_{SS}PHY2$	P		USB PHY analog ground
99	$AV_{SS}PHY2$	P		USB PHY analog ground
100	$AV_{SS}PHY2$	P		USB PHY analog ground
101	$AV_{DD}PHY2$	P		USB PHY analog 3.3V power supply
102	DP	B	3A	USB D+
103	DM	B	3A	USB D-
104	$AV_{SS}PHY2$	P		USB PHY analog ground
105	$AV_{DD}PHY2$	P		USB PHY analog 3.3V power supply
106	$AV_{DD}ADC$	P		A/D converter analog power supply
107	AN0	I	3A	A/D converter analog input Ch0
108	AN1	I	3A	A/D converter analog input Ch1
109	AN2	I	3A	A/D converter analog input Ch2
110	AN3	I	3A	A/D converter analog input Ch3
111	$AV_{SS}ADC$	P		A/D converter analog ground
112	V_{SS}	P		Digital ground
113	$X_{IN}2$	I	X	Audio 16.9344MHz oscillator input
114	$X_{OUT}2$	O	X	Audio 16.9344MHz oscillator output
115	$V_{DD}1$	P		Digital 1.5V power supply
116	$AV_{DD}PLL2$	P		PLL2 analog power supply
117	$AV_{SS}PLL2$	P		PLL2 analog ground
118	VCNT2	O	3A	PLL2 VCO control
119	$V_{DD}2$	P		Digital 3.3V power supply
120	V_{SS}	P		Digital ground

Pin Functions

I	Input pin
O	Output pin
B	Bi-directional pin
P	Power supply pin

Pin name	Direction	Count	Function
(1) Clock, reset, system pin (12 pins)			
TEST[6:1]	I	6	Test pin
NRES	I	1	Reset input
$X_{IN}1$	I	1	System/USB PHY oscillator amplifier input
$X_{OUT}1$	O	1	System/USB PHY oscillator amplifier output
$X_{IN}2$	I	1	Audio 16.9344MHz oscillator input
$X_{OUT}2$	O	1	Audio 16.9344MHz oscillator output
PHI(P11)	O(B)	1	AHB bus clock output/32.768kHz clock output Functions as P11 after hard reset
(2) Interrupt (6 pins)			
EXTFIQ(P2F)	I(B)	1	External FIQ interrupt Functions as P2F after hard reset
EXTINT[4:0] (P[25:21])	I(B)	5	External interrupt Functions as port after hard reset

Continued from preceding page.

Pin name	Direction	Count	Function
(3) NAND FLASH I/F (16 pins)			
XFCEO(P00)	O(B)	1	NAND FLASH chip enable 0 Functions as P00 after hard reset
XFCE1(P1F)	O(B)	1	NAND FLASH chip enable 1 Functions as P1F after hard reset
XFWE(P01)	O(B)	1	NAND FLASH write enable Functions as P01 after hard reset
XFRE(P02)	O(B)	1	NAND FLASH read enable Functions as P02 after hard reset
XALE(P03)	O(B)	1	NAND FLASH address latch enable Functions as P03 after hard reset
XCLE(P04)	O(B)	1	NAND FLASH command latch enable Functions as P04 after hard reset
XFWP(P05)	O(B)	1	NAND FLASH write protect Functions as P05 after hard reset
XFBSY	I	1	NAND FLASH busy
FD[7:0]	B	8	NAND FLASH data
(4) SD card I/F, MS I/F (8 pins)			
SDWP0	I	1	SD card write protect
SDCD0/INS	I	1	SD card card detect / MSINS
SDCMD0/BS	B	1	SD card command / MSBS
SDCLK0/SCLK	O	1	SD card clock / MS clock
SDAT0[3:0]/DATA[3:0]	B	4	SD card data / MS data
(5) PCM I/F (5 pins)			
DOUT	O	1	PCM output data
DIN	I	1	PCM input data
BCK	B	1	PCM bit clock
LRCK(P12)	B(B)	1	PCM LR clock Functions as LRCK after hard reset
MCLK(P13)	B(B)	1	PCM main clock Functions as MCLK after hard reset
(6) Serial I/F (14 pins)			
SCK0 (P08)	B	1	Serial I/F 0 clock Functions as P08 after hard reset
SDO0 (P09)	O (B)	1	Serial I/F 0 output data Functions as P09 after hard reset
SDI0 (P0A)	I (B)	1	Serial I/F 0 input data Functions as P0A after hard reset
SCK1 (P14)	B (B)	1	Serial I/F 1 clock Functions as P14 after hard reset
SDO1 (P15)	O (B)	1	Serial I/F 1 output data Functions as P15 after hard reset
SDI1 (P16)	I (B)	1	Serial I/F 1 input data Functions as P16 after hard reset
TXD0 (P1D)	O (B)	1	UART transmit data Functions as P1D after hard reset
RXD0 (P1E)	I (B)	1	UART receive data Functions as P1E after hard reset
TXD1 (P2A)	O (B)	1	UART1 transmit data Functions as P2A after hard reset
RXD1 (P2B)	I (B)	1	UART1 receive data Functions as P2B after hard reset
TXD2(P2C)	O (B)	1	UART2 transmit data Functions as P2C after hard reset
RXD2(P2D)	I (B)	1	UART2 receive data Functions as P2D after hard reset
SCL (P28)	B (B)	1	I^2C SCL clock (open drain output) Functions as P28 after hard reset
SDA (P29)	B (B)	1	I^2C SDA data (open drain output) Functions as P29 after hard reset

Continued from preceding page.

Pin name	Direction	Count	Function
(7)Timer (2 pins)			
TIOCA0 (P19)	B(B)	1	Multiple timer input capture/output compare A0 Functions as P19 after hard reset
TIOCA1 (P1B)	B(B)	1	Multiple timer input capture/output compare A1 Functions as P1B after hard reset
(8) JTAG (6 pins)			
TCK	I	1	JTAG test clock
RTCK	O	1	JTAG test returned clock
NTRST	I	1	JTAG test reset
TDI	I	1	JTAG test data input
TMS	I	1	JTAG test mode select
TDO	O	1	JTAG test data output
(9) RTC (5 pins)			
XOUT32K	O	1	RTC 32.768kHz oscillator amplifier output
XIN32K	I	1	RTC 32.768kHz oscillator amplifier input
VDET	I	1	Voltage detect input
RTCINT	O	1	RTC interrupt output
BACKUPB	I	1	RTC mode (RTC only or LSI whole)
(10) PLL (2 pins)			
VCNT1	O	1	PLL1 VCO control
VCNT2	O	1	PLL2 VCO control
(11) USB (3 pins)			
DP	B	1	USB D+ (Device)
DM	B	1	USB D- (Device)
RREF	B	1	USB PHY reference resistor
(12) Analog (4 pins)			
AN[3:0]	I	4	Analog input
(13) Power supply pin (37 pins)			
$V_{DD}1$	P	4	Digital 1.5V power supply
$V_{DD}2$	P	4	Digital 3.3V power supply
$V_{DD}3$	P	1	Digital 3.3V/1.8V power supply (SD card I/F, MS I/F power supply)
V_{SS}	P	6	Digital ground
$AV_{DD}PLL1$	P	1	PLL1 analog power supply
$AV_{SS}PLL1$	P	1	PLL1 analog ground
$AV_{DD}PLL2$	P	1	PLL2 analog power supply
$AV_{SS}PLL2$	P	1	PLL2 analog ground
$V_{DD}RTC$	P	1	RTC power supply
$V_{SS}RTC$	P	1	RTC ground
$V_{DD}XT$	P	1	Oscillation amplifier 1.5V power supply
$V_{SS}XT$	P	1	Oscillation amplifier ground
$AV_{DD}PHY1$	P	1	USB PHY analog 1.5V power supply
$AV_{SS}PHY1$	P	2	USB PHY analog ground
$AV_{DD}PHY2$	P	4	USB PHY analog 3.3V power supply
$AV_{SS}PHY2$	P	5	USB PHY analog ground
$AV_{DD}ADC$	P	1	A/D converter analog power supply
$AV_{SS}ADC$	P	1	A/D converter analog ground

Peripheral Circuit Example
PLL Peripheral Circuit 1 (for system)

The PLL1 circuit configuration is shown in the figure below. On the wiring board, connect the decoupling capacitors as close as possible to the pin, and separate the power line from other power supply lines to minimize noise.
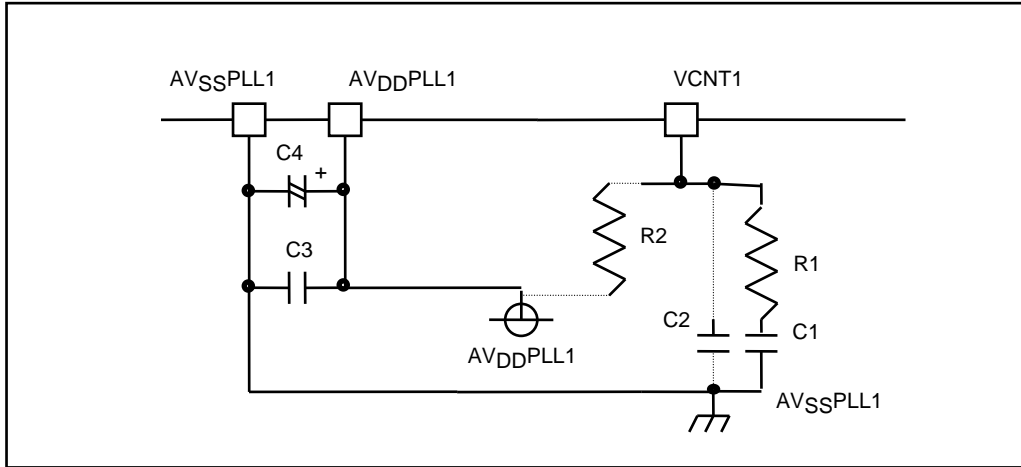
Symbol	Value	Model or Accuracy
R1	100 to 200Ω	±5%
R2	*MΩ	±5%
C1	0.1 to 0.22μF	Capacitance error: ±10%
C2	(Approx. C1/100)	Temperature characteristics: ±10%
C3	0.1μF	(-25 to +85°C)
C4	33μF	16CV33BS

* C4: This is based on SANYO Electric's Surface Mount Device Catalog (CV-BS Series).

Note:
Generally, use R2 and C2 without mounting.
However, if there is a problem that affects the PLL characteristics, the PLL characteristics may be improved by mounting R2 and C2. Therefore, be sure to prepare R2 and C2 wiring patterns beforehand.

PLL Peripheral Circuit 2 (for audio)

The PLL2 circuit configuration is shown in the figure below. On the wiring board, connect the decoupling capacitors as close as possible to the pins, and separate the power line from other power supply lines to minimize noise.
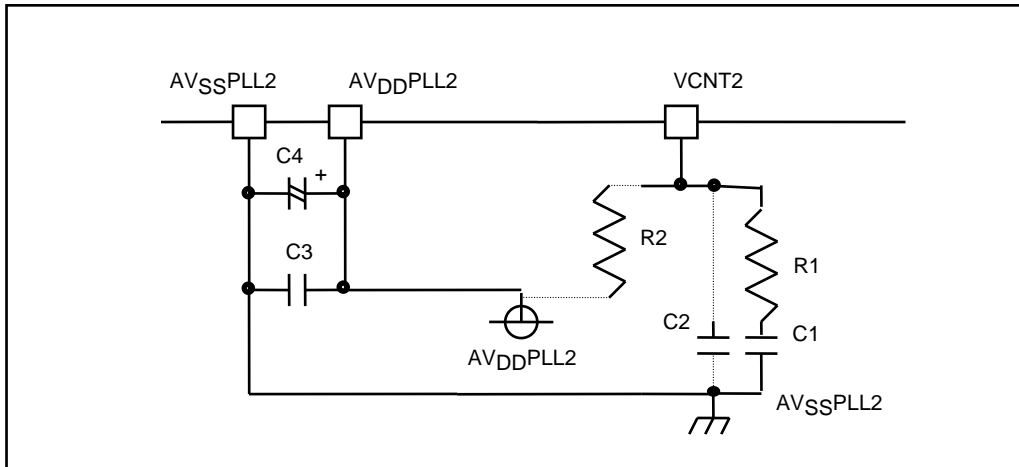
Symbol	Value	Model or Accuracy
R1	100 to 200Ω	±5%
R2	*MΩ	±5%
C1	1.0 to 2.0μF	Capacitance error: ±10%
C2	(Approx. C1/100)	Temperature characteristics: ±10%
C3	0.1μF	(-25 to +85°C)
C4	33μF	16CV33BS

* C4: This is based on SANYO Electric's Surface Mount Device Catalog (CV-BS Series).

Note:
Generally, use R2 and C2 without mounting.
However if there is a problem that affects the PLL characteristics, the PLL characteristics may be improved by mounting R2 and C2. Therefore, be sure to prepare R2 and C2 wiring patterns beforehand.

Reference
For audio applications, experiments have confirmed that
C1=1.0μF, C2=0.01μF
can be effective in maximizing the jitter reduction of the PLL output clock.
(Note that this depends on the board and other environmental conditions, and the result is not guaranteed.)

USB2.0 Peripheral Circuit

Be sure to always observe the items below when designing the circuit board.

• Differential impedance control
  The DP/DM routing width, routing clearance, and PCB layer spacing must be determined so that differential impedance of 90Ω can be achieved. We recommend a microstrip structure for realizing impedance matching.

• Power supply ($AV_{DD}PHY2$, $AV_{DD}PHY1$) and ground ($AV_{SS}PHY2$, $AV_{SS}PHY1$) lines
  The separation of the power line and ground line only for USB usage is recommended.
  At a minimum, insert 10μF, 0.1μF, and 0.01μF capacitors between the power supply and ground for filtering.
  To reject high-frequency noise, inserting the 0.01μF capacitor directly under the power pin and ground pin is recommended.
  Note that 0.1μF capacitor is also effective for latch-up protection.

• Crystal oscillator
  Use a crystal oscillator connected to the $X_{IN}1$ and $X_{OUT}1$ pins that has a fundamental wave of 12MHz, oscillation accuracy of 100p-pm or less, and place it near the IC.

• Reference resistor
  Connect the RREF pin to the ground near the IC through the 680Ω (tolerance 1% or less) reference resistor.

I^{2}C Peripheral Circuit
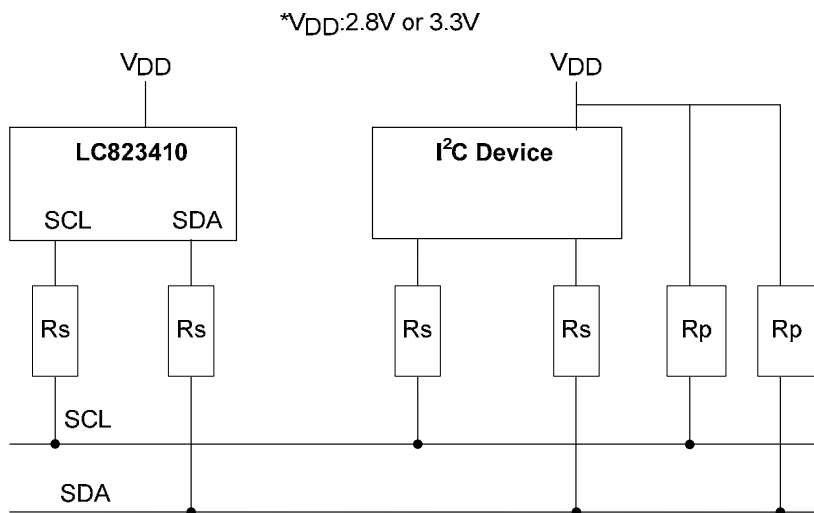
For the Rs and Rp values, see the I^{2}C standards.

XTAL Peripheral Circuit

XTAL1 (12MHz)

12MHz oscillation amplifier RC reference values → R1=1MΩ, R2=0Ω, C1=C2=22pF
Applicable pins: $X_{IN}1$, $X_{OUT}1$
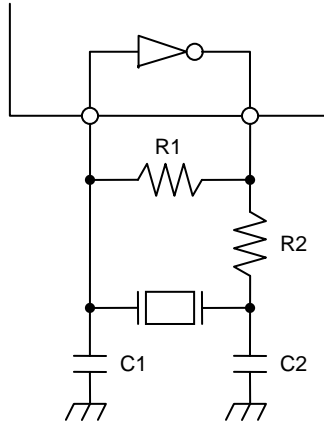
XTAL2 (16.9344MHz)

16.9344MHz oscillation amplifier RC reference values → R1=1MΩ, R2=0Ω, C1=C2=22pF
Applicable pins: $X_{IN}2$, $X_{OUT}2$
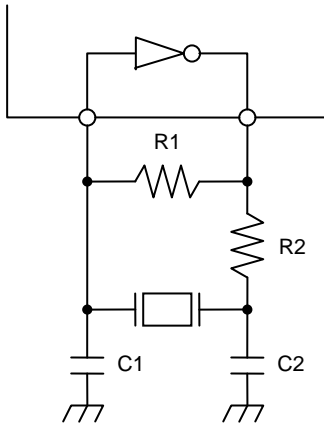
XTALRTC (32.768kHz)

32.768kHz oscillation amplifier RC reference values → R1=5.1MΩ, R2=330kΩ, C1=C2=22pF
Applicable pins: $X_{IN}32K$, $X_{OUT}32K$
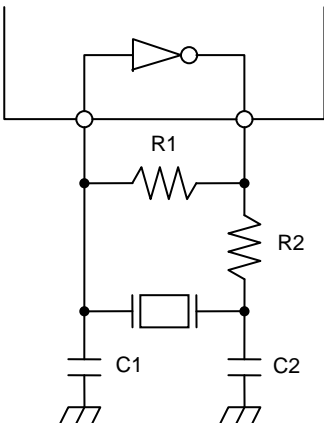
(Reference)
Oscillator product: DT-38 (DAISHINKU Corp.)

JTAG Pin Treatment Examples (both for use of ICE and non-use of ICE)
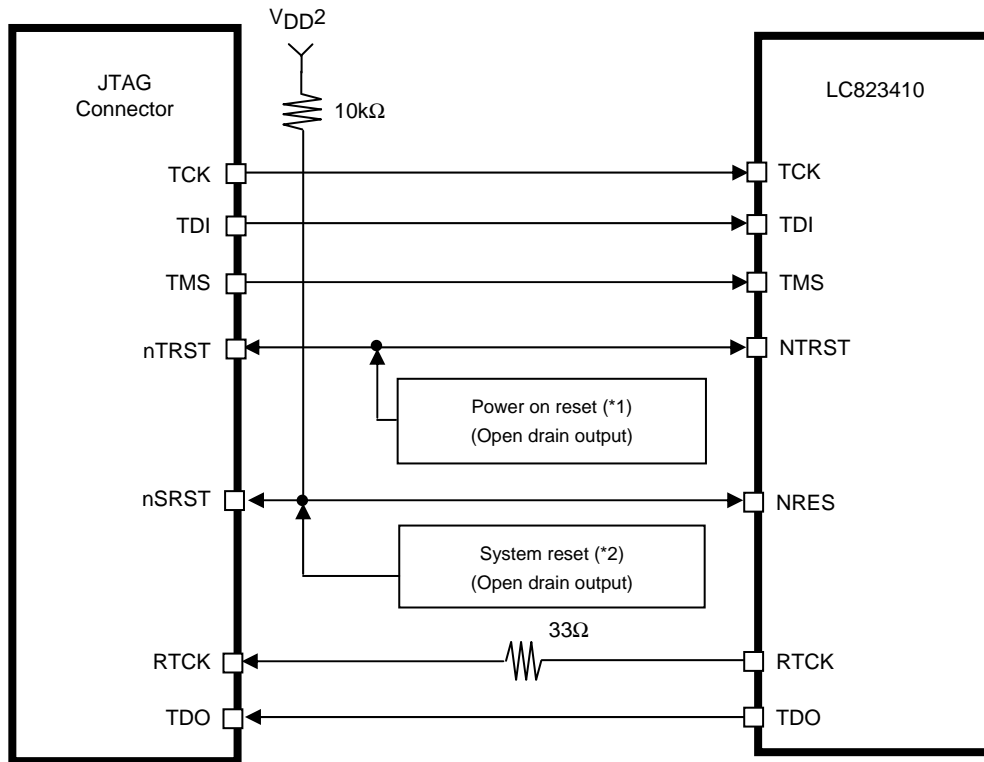
(*1) The power-on reset is a reset signal that becomes active-low only when the power is turned on. Set so that the NTRST pin is reset only by a reset from JTAG and power-on reset.

(*2) System reset includes a power-on reset and a reset signal, requested by the system, that becomes active-low by a manual reset or other means.
Set so that the NRES pin is reset by the reset from JTAG and by system reset.

See the data sheet for the NRES pin reset specifications. The NTRST pin has the same specifications as those of the NRES pin.

The power-on reset (open drain output) can be implemented, for example, by connecting it to the ground through a capacitor.

The above configuration is a peripheral circuit example that assumes the use of a JTAG ICE by YDC (Yokogawa Digital Computer) and can be applied both in cases where ICE is and is not used.
To use other products, inquire at the manufacturer.

JTAG Pin Treatment Examples (non-use of ICE)
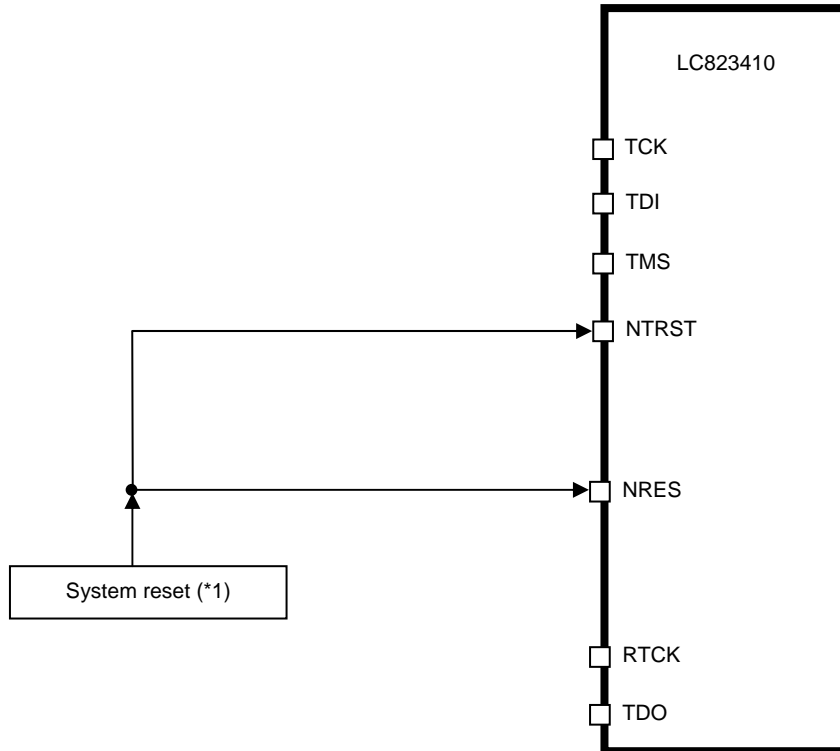
(*1) System reset includes a power-on reset that becomes active-low only when power is turned on, or a reset signal, requested by the system, that becomes active-low by a manual reset or other means.

The NTRST pin has the same specifications as those of the NRES pin, and at least a power-on reset must be implemented.
As shown in this example, system reset can be connected to the NRES pin directly.

The above configuration is a simplified example of a peripheral circuit in the case that ICE is not used.

Power-on Sequence

(1) 3.3V *1

($V_{DD}2$, $V_{DD}3$, $AV_{DD}ADC$, $AV_{DD}PHY2$, $AV_{DD}PLL2$)

3.3V

3.0V

2.8V

1.5V

(2)1.5V

($V_{DD}1$, $V_{DD}XT$, $AV_{DD}PLL1$, $V_{DD}RTC$, $AV_{DD}PHY1$)

1.35V

1.1V

Max 100ms

Min *2

Max 100ms

USB power supply cutoff (such as cable disconnection)
(when Vbus = low is detected by at the IC pin)
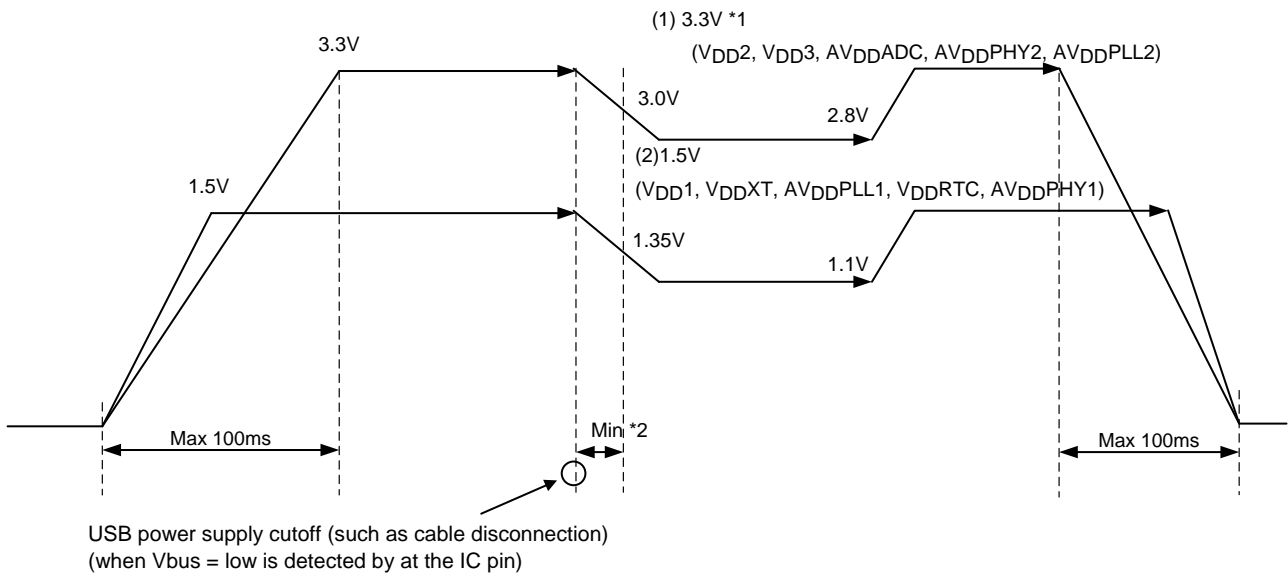
*1 The following relations must be satisfied.
- $AV_{DD}PHY2 >= AV_{DD}ADC$
  $V_{DD}2 >= AV_{DD}PLL2$
  $V_{DD}2 >= V_{DD}3$

*2
- This is a period required only when the AHB clock is operating at a frequency higher than the internal operating frequency guaranteed by $V_{DD}1 >= 1.35V$, and this is needed for switching to an operating frequency guaranteed by $V_{DD}1 >= 1.0V$. The minimum time depends on the system. For the guaranteed operating frequency at each voltage, see the data sheet.

RTC Pin Power On/Off Control Sequence

When running RTC only at power-off of the device, it is required to detect the voltage drop of $V_{DD}1$, $V_{DD}2$ and set BACKUPB to low. Determine the detection level of $V_{DD}1$ and $V_{DD}2$ according to the conditions of the device. The VDET pin needs to be set to low when the RTC power supply is cut off (when RTC operation is stopped).
Also, when drop in the RTC power supply voltage is detected, VDET must be set to low. The figure below shows the power on/off sequence when the detection level of $V_{DD}RTC$ is 0.9V or less. Determine the detection level of $V_{DD}RTC$ according to the conditions of the device.
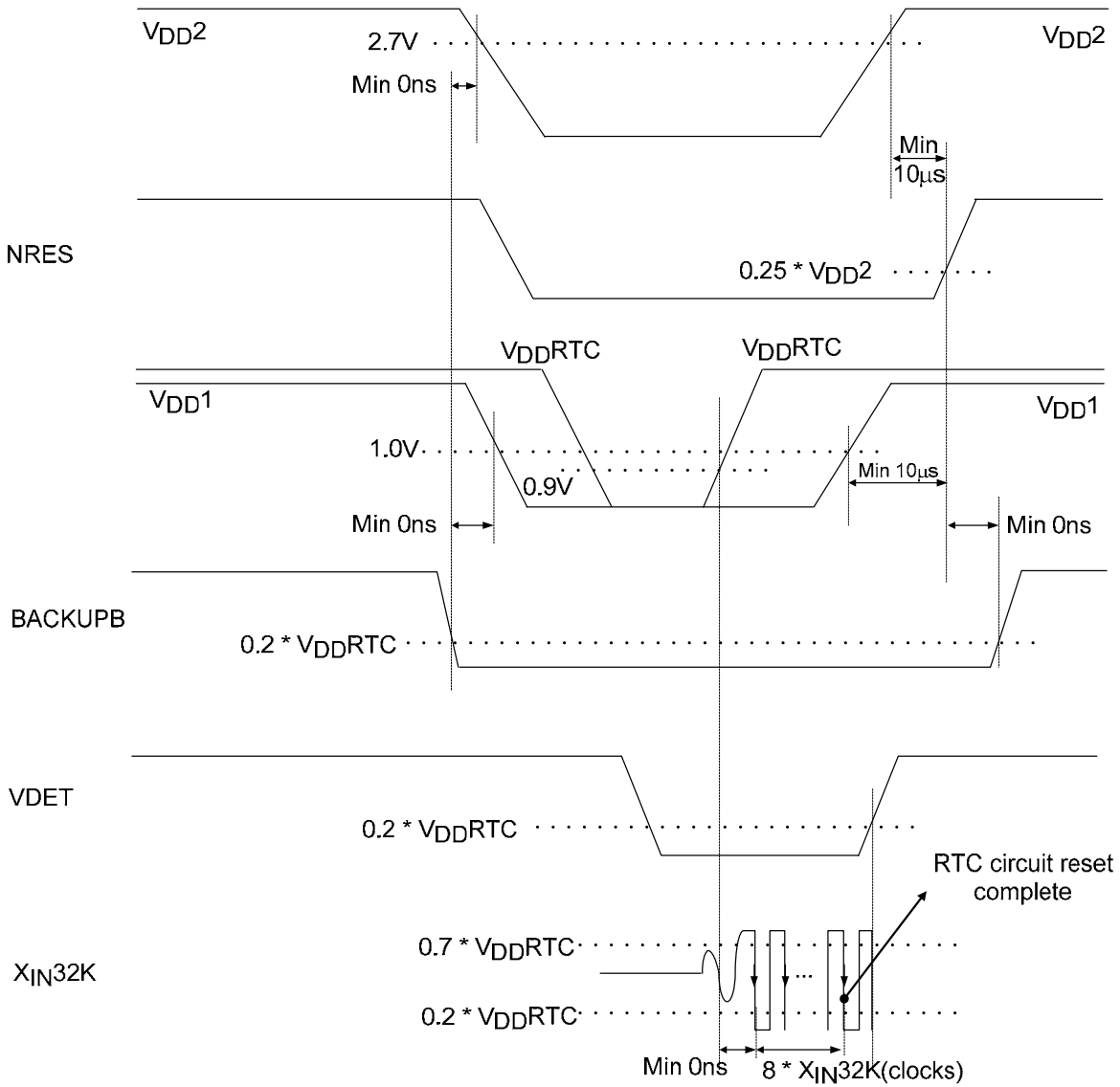
(Reference: Internal control by BACKUPB)
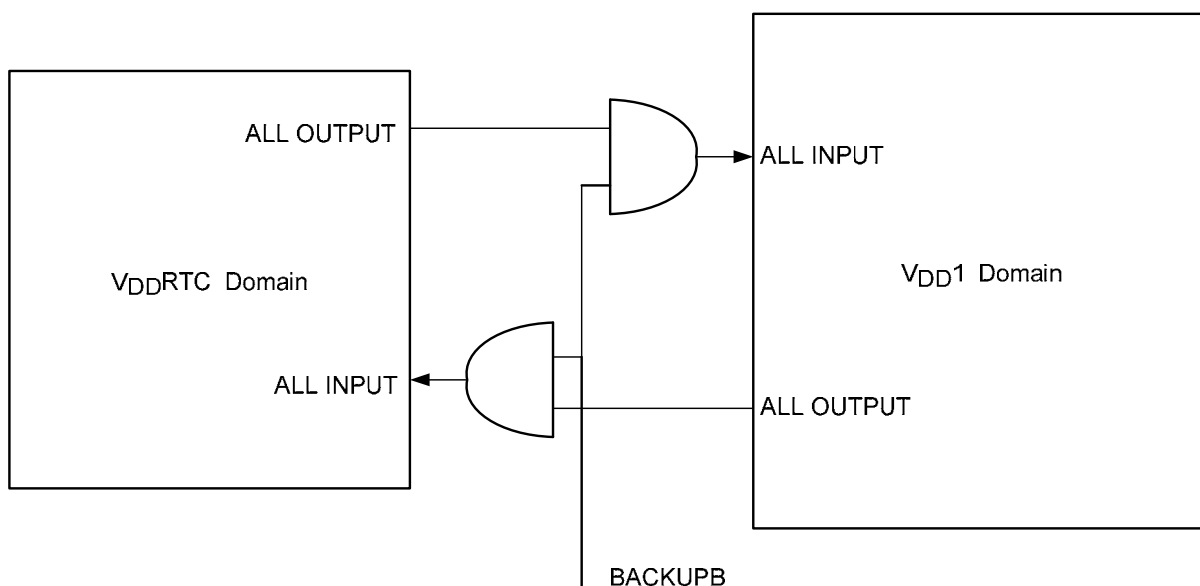
NOTE: $V_{DD}1$ can be shut down while BACKUPB=Low

This catalog provides information as of June, 2010. Specifications and information herein are subject to change without notice.