

# 16-bit Proprietary Microcontroller

CMOS

## F<sup>2</sup>MC-16LX MB90540/545 Series

### MB90F543/F549/V540

#### ■ DESCRIPTION

The MB90540/545 series with FULL-CAN\*1 and FLASH ROM is specially designed for automotive and industrial applications. Its main features are two on board CAN Interfaces (one for MB90V545 series), which conform to V2.0 Part A and Part B, supporting very flexible message buffer scheme and so offering more functions than a normal full CAN approach. The instruction set by F<sup>2</sup>MC-16LX CPU core inherits an AT architecture of the F<sup>2</sup>MC\*2 family with additional instruction sets for high-level languages, extended addressing mode, enhanced multiplication/division instructions, and enhanced bit manipulation instructions. The micro controller has a 32-bit accumulator for processing long word data. The MB90540/545 series has peripheral resources of 8/10-bit A/D converters, UART(SCI), extended I/O serial interfaces, 8/16-bit timer, I/O timer (input capture(ICU), output compare (OCU)).

\*1:Controller Area Network (CAN) - License of Robert Bosch GmbH.

\*2:F<sup>2</sup>MC stands for FUJITSU Flexible Microcontroller.

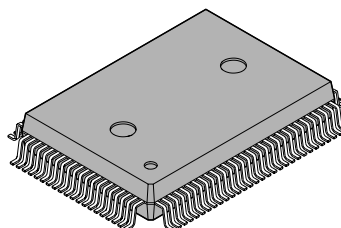
#### ■ FEATURES

- Clock  
Embedded PLL clock multiplication circuit  
Operating clock (PLL clock) can be selected from: divided-by-2 of oscillation or one to four times the oscillation  
Minimum instruction execution time: 62.5 ns (operation at oscillation of 4 MHz, four times the oscillation clock, V<sub>cc</sub> of 5.0V)  
Subsystem Clock: 32 kHz

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#### ■ PACKAGE

100-pin Plastic QFP



(FPT-100P-M06)

# MB90540/545 Series

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- Instruction set to optimize controller applications
  - Rich data types (bit, byte, word, long word)
  - Rich addressing mode (23 types)
  - Enhanced signed multiplication/division instruction and RETI instruction functions
  - Enhanced precision calculation realized by the 32-bit accumulator
- Instruction set designed for high level language (C language) and multi-task operations
  - Adoption of system stack pointer
  - Enhanced pointer indirect instructions
  - Barrel shift instructions
- Program patch function (for two address pointers)
- Enhanced execution speed: 4-byte Instruction queue
- Enhanced interrupt function: 8 levels, 34 factors
- Automatic data transmission function independent of CPU operation
  - Extended intelligent I/O service function (EI<sup>2</sup>OS)
- Embedded ROM size and types
  - Flash ROM: 128 Kbytes / 256 Kbytes
  - Embedded RAM size: 6 Kbytes / 8 Kbytes (evaluation chip)
- Flash ROM
  - Supports automatic programming, Embedded Algorithm TM\*
  - Write / Erase / Erase-Suspend / Resume commands
  - A flag indicating completion of the algorithm
  - Hard-wired reset vector available in order to point to a fixed boot sector in Flash Memory
  - Erase can be performed on each block
  - Block protection with external programming voltage
- Low-power consumption (stand-by) mode
  - Sleep mode (mode in which CPU operating clock is stopped)
  - Stop mode (mode in which oscillation is stopped)
  - CPU intermittent operation mode
  - Clock mode
  - Hardware stand-by mode
- Process
  - 0.5  $\mu$ m CMOS technology
- I/O port
  - General-purpose I/O ports: 81 ports
- Timer
  - Watchdog timer: 1 channel
  - 8/16-bit PPG timer: 8/16-bit  $\times$  4 channels
  - 16-bit re-load timer: 2 channels
- 16-bit I/O timer
  - 16-bit free-run timer: 1 channel
  - Input capture: 8 channels
  - Output compare: 4 channels
- Extended I/O serial interface: 1 channel
- UART 0
  - With full-duplex double buffer (8-bit length)
  - Clock asynchronous or clock synchronized (with start/stop bit) transmission can be selectively used.

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- UART 1
  - With full-duplex double buffer (8-bit length)
  - Clock asynchronous or clock synchronized serial (extended I/O serial) can be used.
- External interrupt circuit (8 channels)
  - A module for starting an extended intelligent I/O service (EI<sup>2</sup>OS) and generating an external interrupt which is triggered by an external input.
- Delayed interrupt generation module
  - Generates an interrupt request for switching tasks.
- 8/10-bit A/D converter (8 channels)
  - 8/10-bit resolution can be selectively used.
  - Starting by an external trigger input.
  - Conversion time: 26.3  $\mu$ s
- FULL-CAN interfaces
  - MB90540 series: 2 channel
  - MB90545 series: 1 channel
  - Conforming to Version 2.0 Part A and Part B
  - Flexible message buffering (mailbox and FIFO buffering can be mixed)
- External bus interface: Maximum address space 16 Mbytes

\*: Embedded Algorithm is a trade mark of Advanced Micro Devices Inc.

# MB90540/545 Series

## ■ PRODUCT LINEUP

The following table provides a quick outlook of the MB90540/545 Series

Features		MB90F543	MB90F549	MB90V540
Classification		Flash ROM product		Evaluation product
ROM size		128 Kbytes Boot Block	256 Kbytes Boot Block	None
ROM size		6 K		8 K
CPU functions		The number of instructions: 351 Instruction bit length: 8 bits, 16 bits Instruction length: 1 byte to 7 bytes Data bit length: 1bit, 8 bits, 16 bits Minimum execution time: 62.5 ns (at machine clock frequency of 16 MHz) Interrupt processing time: 1.5 μs (at machine clock frequency of 16 MHz, minimum value)		
UART 0		Clock synchronized transmission (500 K / 1M / 2 Mbps) Clock asynchronized transmission (4808 / 5208 / 9615 / 10417 / 19230 / 38460 / 62500 / 500000 bps at machine clock frequency of 16 MHz) Transmission can be performed by bi-directional serial transmission or by master/slave connection.		
UART 1 (SCI)		Clock synchronized transmission (62.5 K/ 12 K/ 250 K/ 500 K/ 1 Mbps) Clock asynchronized transmission (1202/ 2404/ 4808/ 9615/ 31250 bps) Transmission can be performed by bi-directional serial transmission or by master / slave connection.		
8/10-bit A/D converter		Conversion precision: 8/10-bit can be selectively used. Number of inputs: 8 One-shot conversion mode (converts selected channel once only) Scan conversion mode (converts two or more successive channels and can program up to 8 channels) Continuous conversion mode (converts selected channel continuously) Stop conversion mode (converts selected channel and stop operation repeatedly)		
8/16-bit PPG timers		Number of channels: 8/16 bit × 4 channels PPG operation of 8-bit or 16 bit A pulse wave of given intervals and given duty ratios can be output. Pulse interval: $f_{sys}$ , $f_{sys}/2^1$ , $f_{sys}/2^2$ , $f_{sys}/2^3$ , $f_{sys}/2^4$ , 128 μs (at oscillation of 4 MHz, $f_{sys}$ = machine clock frequency of 16 MHz, $f_{osc}$ = oscillation clock frequency)		
16-bit Reload timer		Number of channels:2 Operation clock frequency: $f_{sys}/2^1$ , $f_{sys}/2^3$ , $f_{sys}/2^5$ ( $f_{sys}$ = System clock frequency) Supports External Event Count function		
16-bit I/O timer	16-bit Output compares	Number of channels: 4 Pin input factor: A match signal of compare register		
	Input captures	Number of channels: 8 Rewriting a register value upon a pin input (rising, falling, or both edges)		

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# MB90540/545 Series

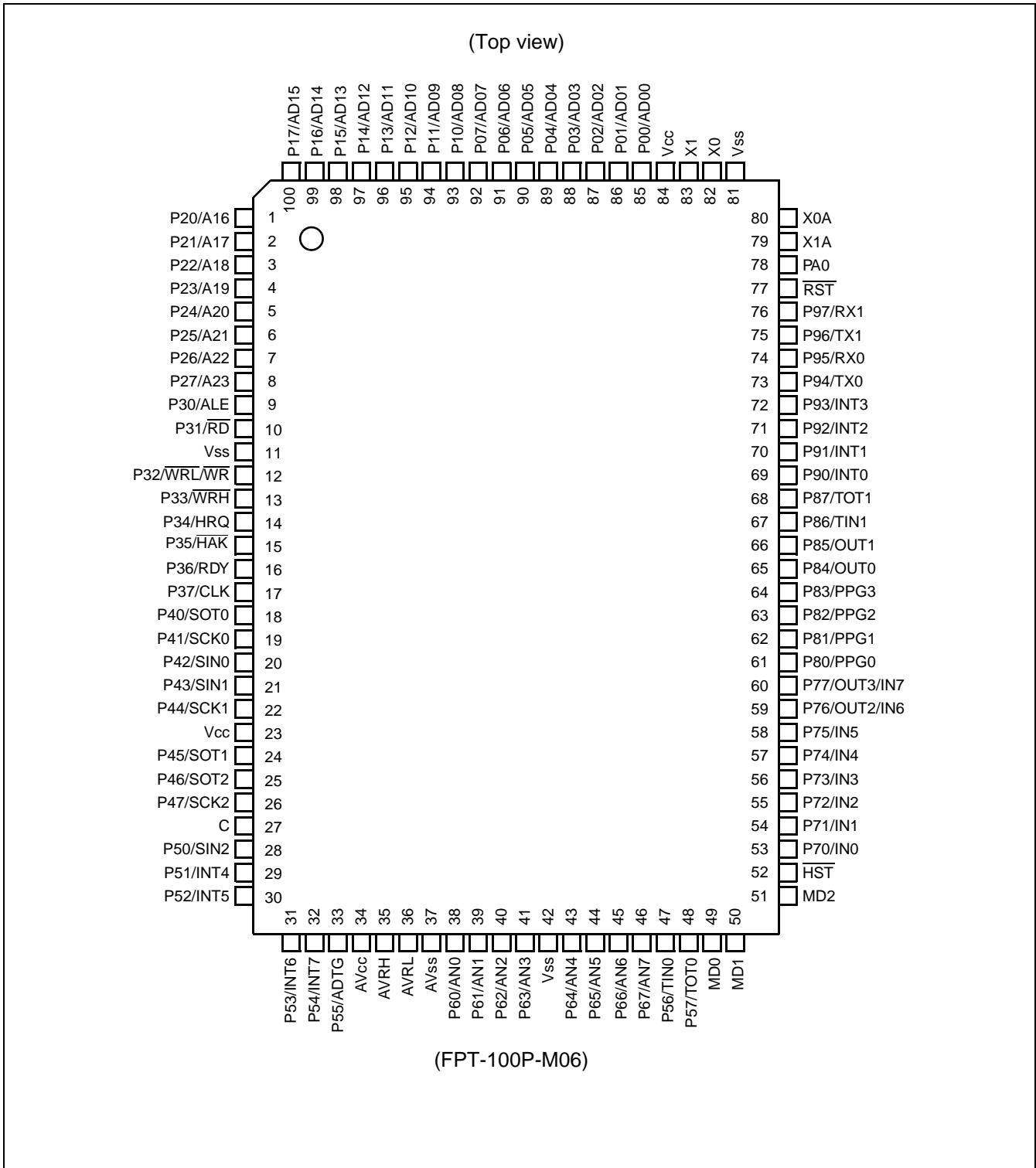
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Features	MB90F543	MB90F549	MB90V540
CAN Interface	Number of channels: 2(MB90540 series), 1(MB90545 series) Conforms to CAN Specification Version 2.0 Part A and B Automatic re-transmission in case of error Automatic transmission responding to Remote Frame Prioritized 16 message buffers for data and ID's Supports multiple messages Flexible configuration of acceptance filtering: Full bit compare / Full bit mask / Two partial bit masks Supports up to 1 Mbps		
External interrupt circuit	Number of inputs: 8 Started by a rising edge, a falling edge, an "H" level input, or an "L" level input.		
Extended I/O serial interface	Clock synchronized transmission (31.25 K / 62.5 K / 125 K / 500 K / 1 Mbps at machine clock frequency of 16 MHz) LSB first / MSB first		
Watchdog timer	Reset generation interval: 3.58 ms, 14.33 ms, 57.23 ms, 458.75 ms (at oscillation of 4 MHz, minimum value)		
Flash Memory	Supports automatic programming, Embedded Algorithm $\text{TM}$ and Write/Erase/Erase-Suspend/Resume commands A flag indicating completion of the algorithm Hard-wired reset vector available in order to point to a fixed boot sector in Flash Memory Boot block configuration Erase can be performed on each block Block protection with external programming voltage Flash Writer from Minato Electronics Inc.		
Low-power consumption (stand-by) mode	Sleep/ stop/ CPU intermittent operation/ clock timer/ hardware stand-by		
Process	CMOS		
Power supply voltage for operation	5 V $\pm$ 10 %		
Package	QFP-100		PGA-256

\*: Varies with conditions such as operating frequency. (See section "■ Electrical Characteristics".)

# MB90540/545 Series

## PIN ASSIGNMENT



(Continued)

## ■ PIN DESCRIPTION

No.	Pin name	Circuit type	Function
82 83	X0 X1	A (Oscillation)	High speed oscillator input pins
80 79	X0A X1A	A (Oscillation)	Low speed oscillator input pins
77	$\overline{\text{RST}}$	B	External reset request input
52	$\overline{\text{HST}}$	C	Hardware standby input
85 to 92	P00 to P07	I	General I/O port with programmable pullup. This function is enabled in the single-chip mode.
	AD00 to AD07		I/O pins for 8 lower bits of the external address/data bus. This function is enabled when the external bus is enabled.
93 to 100	P10 to P17	I	General I/O port with programmable pullup. This function is enabled in the single-chip mode.
	AD08 to AD15		I/O pins for 8 higher bits of the external address/data bus. This function is enabled when the external bus is enabled.
1 to 8	P20 to P27	H	General I/O port with programmable pullup. This function is enabled in the single-chip mode.
	A16 to A23		8-bit I/O pins for A16 to A23 at the external address bus. This function is enabled when the external bus is enabled.
9	P30	I	General I/O port with programmable pullup. This function is enabled in the single-chip mode.
	ALE		Address latch enable output pin. This function is enabled when the external bus is enabled.
10	P31	I	General I/O port with programmable pullup. This function is enabled in the single-chip mode.
	$\overline{\text{RD}}$		Read strobe output pin for the data bus. This function is enabled when the external bus is enabled.
12	P32	I	General I/O port with programmable pullup. This function is enabled in the single-chip mode or when the $\overline{\text{WR}}/\overline{\text{WRL}}$ pin output is disabled.
	$\overline{\text{WRL}}$		Write strobe output pin for the data bus. This function is enabled when both the external bus and the $\overline{\text{WR}}/\overline{\text{WRL}}$ pin output are enabled. $\overline{\text{WRL}}$ is write-strobe output pin for the lower 8 bits of the data bus in 16-bit access. $\overline{\text{WR}}$ is write-strobe output pin for the 8 bits of the data bus in 8-bit access.
	$\overline{\text{WR}}$		
13	P33	I	General I/O port with programmable pullup. This function is enabled in the single-chip mode or external bus 8-bit mode or when $\overline{\text{WRH}}$ pin output is disabled.
	$\overline{\text{WRH}}$		Write strobe output pin for the 8 higher bits of the data bus. This function is enabled when the external bus is enabled, when the external bus 16-bit mode is selected, and when the $\overline{\text{WRH}}$ output pin is enabled.

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# MB90540/545 Series

No.	Pin name	Circuit type	Function
14	P34	I	General I/O port with programmable pullup. This function is enabled in the single-chip mode or when the hold function is disabled.
	HRQ		Hold request input pin. This function is enabled when both the external bus and the hold functions are enabled.
15	P35	I	General I/O port with programmable pullup. This function is enabled in the single-chip mode or when the hold function is disabled.
	$\overline{\text{HAK}}$		Hold acknowledge output pin. This function is enabled when both the external bus and the hold functions are enabled.
16	P36	I	General I/O port with programmable pullup. This function is enabled in the single-chip mode or when the external ready function is disabled.
	RDY		Ready input pin. This function is enabled when both the external bus and the external ready functions are enabled.
17	P37	H	General I/O port with programmable pullup. This function is enabled in the single-chip mode or when the clock output is disabled.
	CLK		CLK output pin. This function is enabled when both the external bus and CLK outputs are enabled.
18	P40	G	General I/O port. This function is enabled when UART0 disables the serial data output.
	SOT0		Serial data output pin for UART0. This function is enabled when UART0 enables the serial data output.
19	P41	G	General I/O port. This function is enabled when UART0 disables clock output.
	SCK0		Clock I/O pin for UART0. This function is enabled when UART0 enables the clock output.
20	P42	G	General I/O port. This function is always enabled.
	SIN0		Serial data input pin for UART0. While UART0 is operating for input, the input of the pin is used as required. Except when the function is intentionally used, output from the other functions must be stopped.
21	P43	G	General I/O port. This function is always enabled.
	SIN1		Serial data input pin for UART1. While UART1 is operating for input, the input of the pin is used as required. Except when the function is intentionally used, output from the other functions must be stopped.
22	P44	G	General I/O port. This function is enabled when UART1 disables the clock output.
	SCK1		Clock pulse input/output pin for UART1. This function is enabled when UART1 enables the clock output.
24	P45	G	General I/O port. This function is enabled when UART1 disables the serial data output.
	SOT1		Serial data output pin for UART1. This function is enabled when UART1 enables the serial data output.

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# MB90540/545 Series

No.	Pin name	Circuit type	Function
25	P46	G	General I/O port. This function is enabled when the Serial IO disables the serial data output.
	SOT2		Serial data output pin for the Serial IO. This function is enabled when the Serial IO enables the serial data output.
26	P47	G	General I/O port. This function is enabled when the Serial IO disables the clock output.
	SCK2		Clock pulse input/output pin for the Serial IO. This function is enabled when the Serial IO enables the clock output.
28	P50	D	General I/O port. This function is always enabled.
	SIN2		Serial data input pin for the Serial IO. While the Serial IO is operating for input, the input of the pin is used as required. Except when the function is intentionally used, output from the other functions must be stopped.
29 to 32	P51 to P54	D	General I/O port. This function is always enabled.
	INT4 to INT7		External interrupt request input pins for INT4 to INT7. While external interrupt is allowed, the input of the pin is used as required. Except when the function is intentionally used, output from the other functions must be stopped.
33	P55	D	General I/O port. This function is always enabled.
	ADTG		Trigger input pin for the A/D converter. While the A/D converter is operating for input, the input of the pin is used as required. Except when the function is intentionally used, output from the other functions must be stopped.
38 to 41	P60 to P63	E	General I/O port. This function is enabled when the analog input enable register specifies a port.
	AN0 to AN3		Analog input pins for the 8/10-bit A/D converter. This function is enabled when the analog input enable register specifies AD.
43 to 46	P64 to P67	E	General I/O port. The function is enabled when the analog input enable register specifies a port.
	AN4 to AN7		Analog input pins for the 8/10-bit A/D converter. This function is enabled when the analog input enable register specifies AD.
47	P56	D	General I/O port. This function is always enabled.
	TIN0		Event input pin for the 16-bit reload timers 0. While the 16-bit reload timer is operating for input, the input of the pin is used as required. Except when the function is intentionally used, output from the other functions must be stopped.
48	P57	D	General I/O port. This function is enabled when the 16-bit reload timers 0 disables the output.
	TOT0		Output pin for the 16-bit reload timers 0. This function is enabled when the 16-bit reload timers 0 enables the output.

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# MB90540/545 Series

No.	Pin name	Circuit type	Function
53 to 58	P70 to P75	D	General I/O ports. This function is always enabled.
	IN0 to IN5		Data sample input pins for input captures ICU0 to ICU5. While the ICU is for input, the input of the pin is used as required. Except when the function is intentionally used, output from the other functions must be stopped.
59 to 60	P76 to P77	D	General I/O ports. This function is enabled when the OCU disables the waveform output.
	OUT2 to OUT3		Waveform output pins for output compares OCU2 and OCU3. This function is enabled when the OCU enables the waveform output.
	IN6 to IN7		Data sample input pin for input captures ICU6 and ICU7. While the ICU is for input, the input of the pin is used as required. Except when the function is intentionally used, output from the other functions must be stopped.
61 to 64	P80 to P83	D	General I/O ports. This function is enabled when 8/16-bit PPG disables the waveform output.
	PPG0 to PPG3		Output pins for 8/16-bit PPGs. This function is enabled when 8/16-bit PPG enables the waveform output.
65 to 66	P84 to P85	D	General I/O ports. This function is enabled when the OCU disables the waveform output.
	OUT0 to OUT1		Waveform output pins for output compares OCU0 and OCU1. This function is enabled when the OCU enables the waveform output.
67	P86	D	General I/O port. This function is always enabled.
	TIN1		Event input pin for the 16-bit reload timers 1. While the 16-bit reload timer is operating as an input, the input of the pin is used as required. Except when the function is intentionally used, output from the other functions must be stopped.
68	P87	D	General I/O port. This function is enabled when the 16-bit reload timers 0 disables the output.
	TOT1		Output pin for the 16-bit reload timers 1 This function is enabled when the 16-bit reload timers 1 enables the output.
69 to 72	P90 to P93	D	General I/O port. This function is always enabled.
	INT0 to INT3		External interrupt request input pins for INT0 to INT3. While external interrupt is allowed, the input of the pin is used as required. Except when the function is intentionally used, output from the other functions must be stopped.
73	P94	D	General I/O port. This function is enabled when CAN0 disables the output.
	TX0		TX Output pin for CAN0. This function is enabled when CAN0 enables the output.
74	P95	D	General I/O port. This function is always enabled.
	RX0		RX input pin for CAN0 Interface. When the CAN function is used, output from the other functions must be stopped.

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# MB90540/545 Series

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No.	Pin name	Circuit type	Function
75	P96	D	General I/O port. This function is enabled when CAN1 disables the output.
	TX1		TX Output pin for CAN1. This function is enabled when CAN1 enables the output (only MB90540 series).
76	P97	D	General I/O port. This function is always enabled.
	RX1		RX input pin for CAN1 Interface. When the CAN function is used, output from the other functions must be stopped (only MB90540 series).
78	PA0	D	General I/O port. This function is always enabled.
34	AV <sub>cc</sub>	Power supply	Power supply for the A/D Converter. This power supply must be turned on or off while a voltage higher than or equal to AV <sub>cc</sub> is applied to V <sub>cc</sub> .
37	AV <sub>ss</sub>	Power supply	Power supply for the A/D Converter.
35	AVRH	Power supply	External reference voltage input for the A/D Converter. This power supply must be turned on or off while a voltage higher than or equal to AVRH is applied to AV <sub>cc</sub> .
36	AVRL	Power supply	External reference voltage input for the A/D Converter.
49 50	MD0 MD1	C	Input pins for specifying the operating mode. The pins must be directly connected to V <sub>cc</sub> or V <sub>ss</sub> .
51	MD2	F	Input pin for specifying the operating mode. The pin must be directly connected to V <sub>cc</sub> or V <sub>ss</sub> .
27	C		This is the power supply stabilization capacitor pin. It should be connected externally to an 0.1 μF ceramic capacitor.
23, 84	V <sub>cc</sub>	Power supply	Input pin for power supply (5.0 V) .
11, 42, 81	V <sub>ss</sub>	Power supply	Input pin for power supply (0.0 V) .

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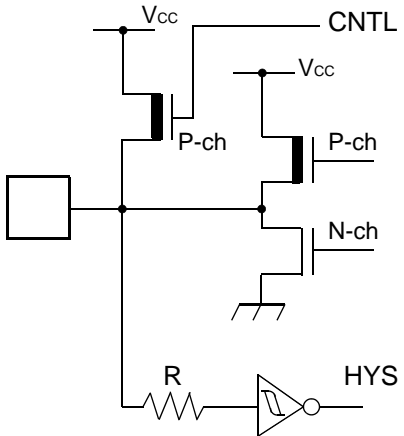
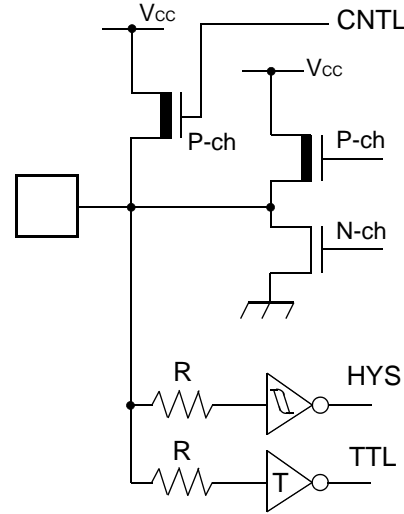
## ■ I/O CIRCUIT TYPE

Circuit type	Diagram	Remarks
A	<p>Diagram A shows a differential input circuit. Two inputs, X1 and X0, are connected to the gates of two transistors. The outputs of these transistors are connected to the gates of a second differential pair of transistors. The output of this second differential pair is connected to an inverter. A standby control signal is connected to the gates of the first differential pair through an inverter.</p>	<ul style="list-style-type: none"> <li>• Oscillation feedback resistor: 1 MΩ approx.</li> </ul>
B	<p>Diagram B shows a hysteresis input circuit. An input terminal is connected to a resistor R, which is also connected to ground. The other end of resistor R is connected to the input of an inverter. The output of the inverter is labeled HYS.</p>	<ul style="list-style-type: none"> <li>• Hysteresis input with pull-up Resistor: 50 kΩ approx.</li> </ul>
C	<p>Diagram C shows a hysteresis input circuit. An input terminal is connected to a resistor R, which is also connected to ground. The other end of resistor R is connected to the input of an inverter. The output of the inverter is labeled HYS.</p>	<ul style="list-style-type: none"> <li>• Hysteresis input</li> </ul>
D	<p>Diagram D shows a CMOS level output circuit. An input terminal is connected to the gates of a P-channel MOSFET (P-ch) and an N-channel MOSFET (N-ch). The P-ch MOSFET has its source connected to Vcc and its drain connected to the input terminal. The N-ch MOSFET has its source connected to ground and its drain connected to the input terminal. The output of the P-ch MOSFET is connected to the input of an inverter. The output of the inverter is labeled HYS.</p>	<ul style="list-style-type: none"> <li>• CMOS level output</li> <li>• Hysteresis input</li> </ul>

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Circuit type	Diagram	Remarks
E		<ul style="list-style-type: none"> <li>• CMOS level output</li> <li>• Hysteresis input</li> <li>• Analog input</li> </ul>
F		<ul style="list-style-type: none"> <li>• Hysteresis input</li> <li>• Pull-down Resistor: 50 kΩ approx. (except FLASH devices)</li> </ul>
G		<ul style="list-style-type: none"> <li>• CMOS level output</li> <li>• Hysteresis input</li> <li>• TTL input (FLASH devices only)</li> </ul>

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Circuit type	Diagram	Remarks
H		<ul style="list-style-type: none"> <li>• CMOS level output</li> <li>• Hysteresis input</li> <li>• Programmable pullup resistor: 50 kΩ approx.</li> </ul>
I		<ul style="list-style-type: none"> <li>• CMOS level output</li> <li>• Hysteresis input</li> <li>• TTL level input (FLASH devices only)</li> <li>• Programmable pullup resistor: 50 kΩ approx.</li> </ul>

## ■ HANDLING DEVICES

### (1) Preventing latch-up

CMOS IC chips may suffer latch-up under the following conditions:

- A voltage higher than  $V_{CC}$  or lower than  $V_{SS}$  is applied to an input or output pin.
- A voltage higher than the rated voltage is applied between  $V_{CC}$  and  $V_{SS}$ .
- The  $AV_{CC}$  power supply is applied before the  $V_{CC}$  voltage.

Latch-up may increase the power supply current drastically, causing thermal damage to the device.

For the same reason, care must also be taken in not allowing the analog power-supply voltage ( $AV_{CC}$ ,  $AV_{RH}$ ,  $DV_{CC}$ ) to exceed the digital power-supply voltage.

### (2) Handling unused input pins

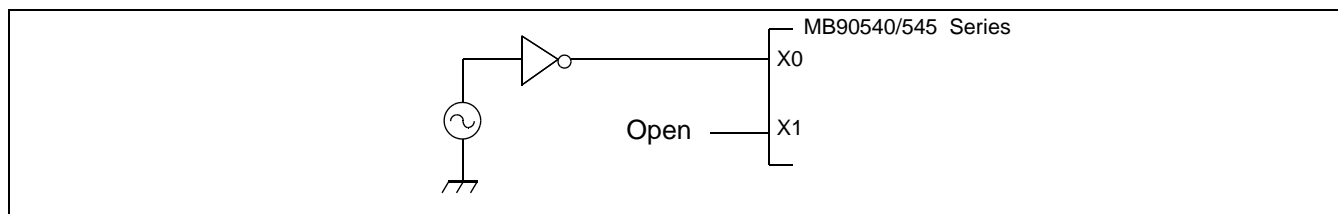
Leaving unused input pins open may result in misbehavior or latch up and possible permanent damage of the device. Therefore they must be pulled up or pulled down through resistors. In this case those resistors should be more than  $2\text{ k}\Omega$ .

Unused bi-directional pins should be set to the output state and can be left open, or the input state with the above described connection.

### (3) Using external clock

To use external clock, drive X0 pin only and leave X1 pin unconnected.

Below is a diagram of how to use external clock.



### (4) Not using subclock mode

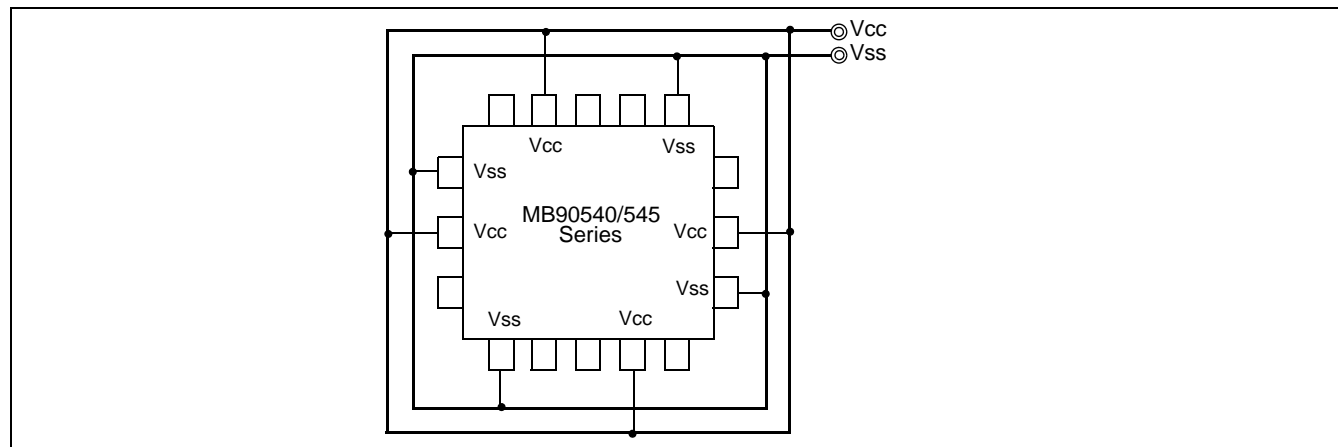
Oscillations must be connected to the X0A and X1A, even when a subclock is not used.

### (5) Power supply pins ( $V_{CC}/V_{SS}$ )

In products with multiple  $V_{CC}$  or  $V_{SS}$  pins, the pins of a same potential are internally connected in the device to avoid abnormal operations including latch-up. However you must connect the pins to an external power and a ground line to lower the electro-magnetic emission level to prevent abnormal operation of strobe signals caused by the rise in the ground level, and to conform to the total current rating.

Make sure to connect  $V_{CC}$  and  $V_{SS}$  pins via the lowest impedance to power lines.

It is recommended to provide a bypass capacitor of around  $0.1\ \mu\text{F}$  between  $V_{CC}$  and  $V_{SS}$  pins near the device.



# MB90540/545 Series

## (6) Pull-up/down resistors

The MB90540/545 Series does not support internal pull-up/down resistors (except Port0 - Port3:pull-up resistors). Use external components where needed.

## (7) Crystal Oscillator Circuit

Noises around X0 or X1 pins may be possible causes of abnormal operations. Make sure to provide bypass capacitors via the shortest distances from X0, X1 pins, crystal oscillator (or ceramic resonator) and ground lines, and make sure, to the utmost effort, that lines of oscillation circuits do not cross the lines of other circuits.

It is highly recommended to provide a printed circuit board artwork surrounding X0 and X1 pins with a grand area for stabilizing the operation.

## (8) Turning-on Sequence of Power Supply to A/D Converter and Analog Inputs

Make sure to turn on the A/D converter power supply (AV<sub>CC</sub>, AVR<sub>H</sub>, AVR<sub>L</sub>) and analog inputs (AN0 to AN7) after turning-on the digital power supply (V<sub>CC</sub>).

Turn-off the digital power after turning off the A/D converter supply and analog inputs. In this case, make sure that the voltage does not exceed AVR<sub>H</sub> or AV<sub>CC</sub> (turning on/off the analog and digital power supplies simultaneously is acceptable).

## (9) Connection of Unused Pins of A/D Converter

Connect unused pins of A/D converter to AV<sub>CC</sub> = V<sub>CC</sub>, AV<sub>SS</sub> = AVR<sub>H</sub> = V<sub>SS</sub>.

## (10) N.C. Pin

The N.C. (internally connected) pin must be opened for use.

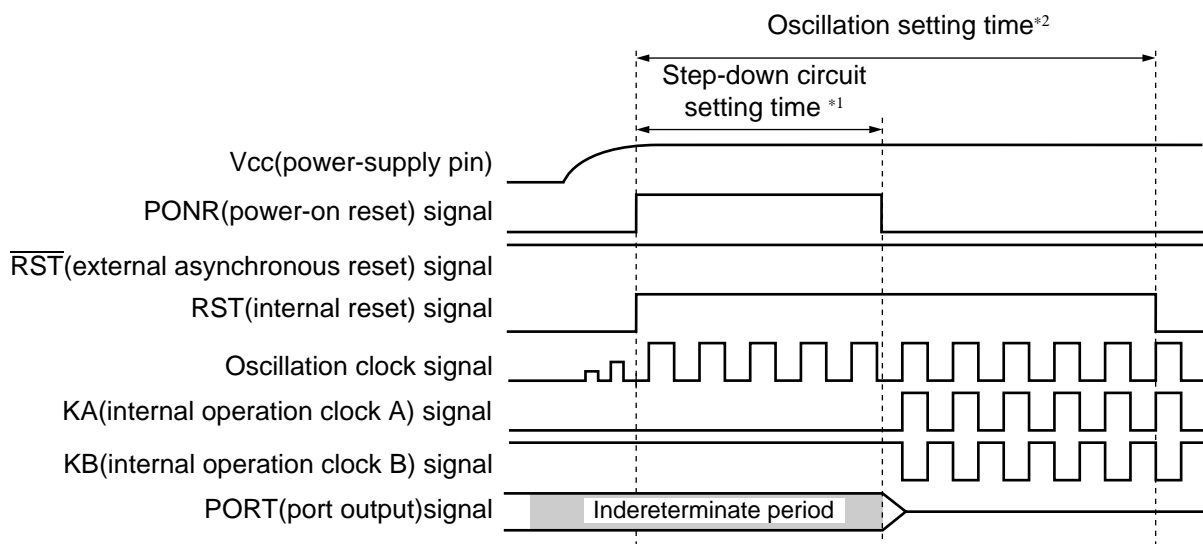
## (11) Notes on Energization

To prevent the internal regulator circuit from malfunctioning, set the voltage rise time during energization at 50 μs or more (0.2 V to 2.7 V).

## (12) Indeterminate outputs from ports 0 and 1

The outputs from 0 and 1 become indeterminate during a power-on reset after the power is turned on. Pay attention to the port output timing shown as follows.

### • Timing chart of indeterminate outputs from ports 0 and 1



\* : 1:Step-down circuit setting time :  $2^{17}$ /oscillation clock frequency (oscillation clock frequency of 16 MHz: 8.19 ms)

\* : 2:Oscillation setting time:  $2^{18}$ /oscillation clock frequency (oscillation clock frequency of 16 MHz: 16.38 ms)



## **(13) Initialization**

In the device, there are internal registers which are initialized only by a power-on reset. To initialize these registers, please turn on the power again.

## **(14) Directions of “DIV A, Ri” and “DIVW A, RWi” instructions**

In the Signed multiplication and division instructions (“DIV A, Ri” and “DIVW A, RWi”), the value of the corresponding bank register (DTB, ADB, USB, SSB) is set in “00h”.

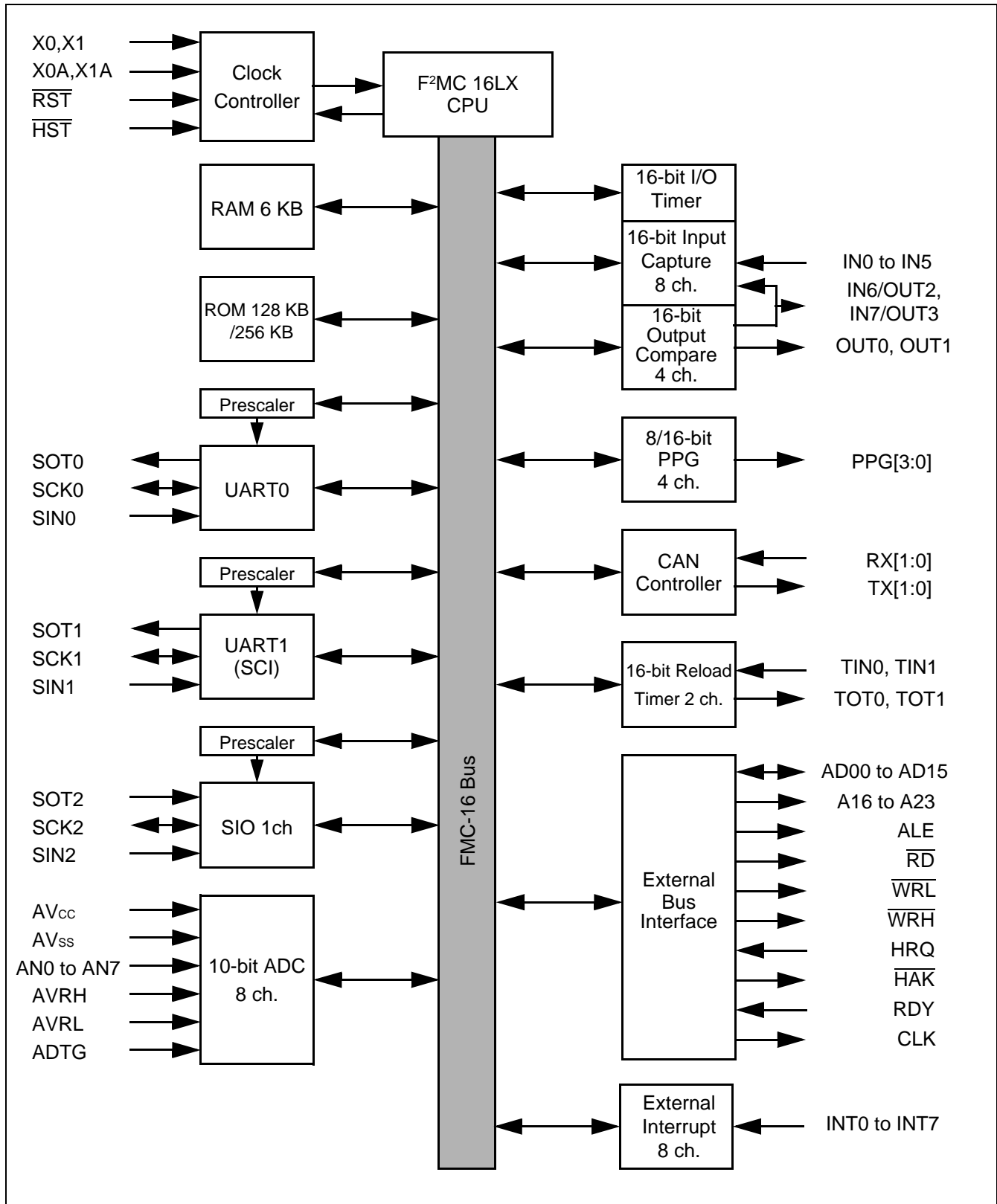
If the values of the corresponding bank registers (DTB,ADB,USB,SSB) are set to other than “00h”, the remainder by the execution result of the instruction is not stored in the register of the instruction operand.

## **(15) Using REALOS**

Extended intelligent I/O service (EI<sup>2</sup>OS) can not be used, while REALOS is used.

# MB90540/545 Series

## ■ BLOCK DIAGRAM



# MB90540/545 Series

## ■ MEMORY SPACE

The memory space of the MB90540/545 Series is shown below.

MB90V540		MB90F543		MB90F549	
FFFFFF <sub>H</sub>	ROM (FF bank)	FFFFFF <sub>H</sub>	ROM (FF bank)	FFFFFF <sub>H</sub>	ROM (FF bank)
FF0000 <sub>H</sub>		FF0000 <sub>H</sub>		FF0000 <sub>H</sub>	
FEFFFF <sub>H</sub>	ROM (FE bank)	FEFFFF <sub>H</sub>	ROM (FE bank)	FEFFFF <sub>H</sub>	ROM (FE bank)
FE0000 <sub>H</sub>		FE0000 <sub>H</sub>		FE0000 <sub>H</sub>	
FDFFFF <sub>H</sub>	ROM (FD bank)		External	FDFFFF <sub>H</sub>	ROM (FD bank)
FD0000 <sub>H</sub>				FD0000 <sub>H</sub>	
FCFFFF <sub>H</sub>	ROM (FC bank)			FCFFFF <sub>H</sub>	ROM (FC bank)
FC0000 <sub>H</sub>				FC0000 <sub>H</sub>	
	External				External
00FFFF <sub>H</sub>	ROM (Image of FF bank)	00FFFF <sub>H</sub>	ROM (Image of FF bank)	00FFFF <sub>H</sub>	ROM (Image of FF bank)
004000 <sub>H</sub>		004000 <sub>H</sub>		004000 <sub>H</sub>	
003FFF <sub>H</sub>	Peripheral	003FFF <sub>H</sub>	Peripheral	003FFF <sub>H</sub>	Peripheral
003900 <sub>H</sub>		003900 <sub>H</sub>		003900 <sub>H</sub>	
	External		External		External
0020FF <sub>H</sub>					
001FF5 <sub>H</sub>	ROM correction	0018FF <sub>H</sub>		0018FF <sub>H</sub>	
001FF0 <sub>H</sub>			RAM 6K		RAM 6K
	RAM 8K				
000100 <sub>H</sub>		000100 <sub>H</sub>		000100 <sub>H</sub>	
	External		External		External
0000BF <sub>H</sub>	Peripheral	0000BF <sub>H</sub>	Peripheral	0000BF <sub>H</sub>	Peripheral
000000 <sub>H</sub>		000000 <sub>H</sub>		000000 <sub>H</sub>	

The high-order portion of bank 00 gives the image of the FF bank ROM to make the small model of the C compiler effective. Since the low-order 16 bits are the same, the table in ROM can be referenced without using the “far” specification in the pointer declaration.

For example, an attempt to access 00C000<sub>H</sub> accesses the value at FFC000<sub>H</sub> in ROM. The ROM area in bank FF exceeds 48 Kbytes, and its entire image cannot be shown in bank 00. The image between FF4000<sub>H</sub> and FFFFFFF<sub>H</sub> is visible in bank 00, while the image between FF0000<sub>H</sub> and FF3FFF<sub>H</sub> is visible only in bank FF.

# MB90540/545 Series

## ■ I/O MAP

Address	Register	Abbreviation	Access	Peripheral	Initial value
00 <sub>H</sub>	Port 0 data register	PDR0	R/W	Port 0	XXXXXXXX <sub>B</sub>
01 <sub>H</sub>	Port 1 data register	PDR1	R/W	Port 1	XXXXXXXX <sub>B</sub>
02 <sub>H</sub>	Port 2 data register	PDR2	R/W	Port 2	XXXXXXXX <sub>B</sub>
03 <sub>H</sub>	Port 3 data register	PDR3	R/W	Port 3	XXXXXXXX <sub>B</sub>
04 <sub>H</sub>	Port 4 data register	PDR4	R/W	Port 4	XXXXXXXX <sub>B</sub>
05 <sub>H</sub>	Port 5 data register	PDR5	R/W	Port 5	XXXXXXXX <sub>B</sub>
06 <sub>H</sub>	Port 6 data register	PDR6	R/W	Port 6	XXXXXXXX <sub>B</sub>
07 <sub>H</sub>	Port 7 data register	PDR7	R/W	Port 7	XXXXXXXX <sub>B</sub>
08 <sub>H</sub>	Port 8 data register	PDR8	R/W	Port 8	XXXXXXXX <sub>B</sub>
09 <sub>H</sub>	Port 9 data register	PDR9	R/W	Port 9	XXXXXXXX <sub>B</sub>
0A <sub>H</sub>	Port A data register	PDRA	R/W	Port A	_____X <sub>B</sub>
0B <sub>H</sub> to 0F <sub>H</sub>	Reserved				
10 <sub>H</sub>	Port 0 direction register	DDR0	R/W	Port 0	0 0 0 0 0 0 0 0 <sub>B</sub>
11 <sub>H</sub>	Port 1 direction register	DDR1	R/W	Port 1	0 0 0 0 0 0 0 0 <sub>B</sub>
12 <sub>H</sub>	Port 2 direction register	DDR2	R/W	Port 2	0 0 0 0 0 0 0 0 <sub>B</sub>
13 <sub>H</sub>	Port 3 direction register	DDR3	R/W	Port 3	0 0 0 0 0 0 0 0 <sub>B</sub>
14 <sub>H</sub>	Port 4 direction register	DDR4	R/W	Port 4	0 0 0 0 0 0 0 0 <sub>B</sub>
15 <sub>H</sub>	Port 5 direction register	DDR5	R/W	Port 5	0 0 0 0 0 0 0 0 <sub>B</sub>
16 <sub>H</sub>	Port 6 direction register	DDR6	R/W	Port 6	0 0 0 0 0 0 0 0 <sub>B</sub>
17 <sub>H</sub>	Port 7 direction register	DDR7	R/W	Port 7	0 0 0 0 0 0 0 0 <sub>B</sub>
18 <sub>H</sub>	Port 8 direction register	DDR8	R/W	Port 8	0 0 0 0 0 0 0 0 <sub>B</sub>
19 <sub>H</sub>	Port 9 direction register	DDR9	R/W	Port 9	0 0 0 0 0 0 0 0 <sub>B</sub>
1A <sub>H</sub>	Port A direction register	DDRA	R/W	Port A	_____0 <sub>B</sub>
1B <sub>H</sub>	Analog Input Enable	ADER	R/W	Port 6, A/D	1 1 1 1 1 1 1 1 <sub>B</sub>
1C <sub>H</sub>	Port 0 Pullup control register	PUCR0	R/W	Port 0	0 0 0 0 0 0 0 0 <sub>B</sub>
1D <sub>H</sub>	Port 1 Pullup control register	PUCR1	R/W	Port 1	0 0 0 0 0 0 0 0 <sub>B</sub>
1E <sub>H</sub>	Port 2 Pullup control register	PUCR2	R/W	Port 2	0 0 0 0 0 0 0 0 <sub>B</sub>
1F <sub>H</sub>	Port 3 Pullup control register	PUCR3	R/W	Port 3	0 0 0 0 0 0 0 0 <sub>B</sub>
20 <sub>H</sub>	Serial Mode Control Register 0	UMC0	R/W	UART0	0 0 0 0 0 1 0 0 <sub>B</sub>
21 <sub>H</sub>	Serial Status Register 0	USR0	R/W		0 0 0 1 0 0 0 0 <sub>B</sub>
22 <sub>H</sub>	Serial Input/Output data register 0	UIDR0/ UODR0	R/W		XXXXXXXX <sub>B</sub>
23 <sub>H</sub>	Rate and data register 0	URD0	R/W		0 0 0 0 0 0 0 X <sub>B</sub>

(Continued)

# MB90540/545 Series

Address	Register	Abbreviation	Access	Peripheral	Initial value
24 <sub>H</sub>	Serial mode register 1	SMR1	R/W	UART1	0 0 0 0 0 0 0 0 <sub>B</sub>
25 <sub>H</sub>	Serial control register 1	SCR1	R/W		0 0 0 0 0 1 0 0 <sub>B</sub>
26 <sub>H</sub>	Serial input/output data register 1	SIDR1/ SODR1	R/W		XXXXXXXX <sub>B</sub>
27 <sub>H</sub>	Serial status register 1	SSR1	R/W		0 0 0 0 1 _ 0 0 <sub>B</sub>
28 <sub>H</sub>	UART1 prescaler control register	U1CDCR	R/W		0 _ _ _ 1 1 1 1 <sub>B</sub>
29 <sub>H</sub>	Edge selector	SES1	R/W		_ _ _ _ _ _ 0 <sub>B</sub>
2A <sub>H</sub>	Reserved				
2B <sub>H</sub>	Serial IO prescaler	SCDCR	R/W	Serial IO	0 _ _ _ 1 1 1 1 <sub>B</sub>
2C <sub>H</sub>	Serial mode control register	SMCS	R/W		_ _ _ _ 0 0 0 0 <sub>B</sub>
2D <sub>H</sub>	Serial mode control register	SMCS	R/W		0 0 0 0 0 0 1 0 <sub>B</sub>
2E <sub>H</sub>	Serial data register	SDR	R/W		XXXXXXXX <sub>B</sub>
2F <sub>H</sub>	Edge selector	SES2	R/W		_ _ _ _ _ _ 0 <sub>B</sub>
30 <sub>H</sub>	External interrupt enable register	ENIR	R/W	External Interrupt	0 0 0 0 0 0 0 0 <sub>B</sub>
31 <sub>H</sub>	External interrupt request register	EIRR	R/W		XXXXXXXX <sub>B</sub>
32 <sub>H</sub>	External interrupt level register	ELVR	R/W		0 0 0 0 0 0 0 0 <sub>B</sub>
33 <sub>H</sub>	External interrupt level register	ELVR	R/W		0 0 0 0 0 0 0 0 <sub>B</sub>
34 <sub>H</sub>	A/D control status register 0	ADCS0	R/W	A/D Converter	0 0 0 0 0 0 0 0 <sub>B</sub>
35 <sub>H</sub>	A/D control status register 1	ADCS1	R/W		0 0 0 0 0 0 0 0 <sub>B</sub>
36 <sub>H</sub>	A/D data register 0	ADCR0	R		XXXXXXXX <sub>B</sub>
37 <sub>H</sub>	A/D data register 1	ADCR1	R/W		0 0 0 0 1 _ XX <sub>B</sub>
38 <sub>H</sub>	PPG0 operation mode control register	PPGC0	R/W	16-bit Programmable Pulse Generator 0/1	0 _ 0 0 0 _ _ 1 <sub>B</sub>
39 <sub>H</sub>	PPG1 operation mode control register	PPGC1	R/W		0 _ 0 0 0 0 0 1 <sub>B</sub>
3A <sub>H</sub>	PPG0 and PPG1 clock select register	PPG01	R/W		0 0 0 0 0 0 _ _ <sub>B</sub>
3B <sub>H</sub>	Reserved				
3C <sub>H</sub>	PPG2 operation mode control register	PPGC2	R/W	16-bit Programmable Pulse Generator 2/3	0 _ 0 0 0 _ _ 1 <sub>B</sub>
3D <sub>H</sub>	PPG3 operation mode control register	PPGC3	R/W		0 _ 0 0 0 0 0 1 <sub>B</sub>
3E <sub>H</sub>	PPG2 and PPG3 Clock Select Register	PPG23	R/W		0 0 0 0 0 0 _ _ <sub>B</sub>
3F <sub>H</sub>	Reserved				
40 <sub>H</sub>	PPG4 operation mode control register	PPGC4	R/W	16-bit Programmable Pulse Generator 4/5	0 _ 0 0 0 _ _ 1 <sub>B</sub>
41 <sub>H</sub>	PPG5 operation mode control register	PPGC5	R/W		0 _ 0 0 0 0 0 1 <sub>B</sub>
42 <sub>H</sub>	PPG4 and PPG5 clock select register	PPG45	R/W		0 0 0 0 0 0 _ _ <sub>B</sub>
43 <sub>H</sub>	Reserved				
44 <sub>H</sub>	PPG6 operation mode control register	PPGC6	R/W	16-bit Programmable Pulse Generator 6/7	0 _ 0 0 0 _ _ 1 <sub>B</sub>
45 <sub>H</sub>	PPG7 operation mode control register	PPGC7	R/W		0 _ 0 0 0 0 0 1 <sub>B</sub>
46 <sub>H</sub>	PPG6 and PPG7 output pin control register	PPG67	R/W		0 0 0 0 0 0 _ _ <sub>B</sub>

(Continued)

# MB90540/545 Series

Address	Register	Abbreviation	Access	Peripheral	Initial value
47 <sub>H</sub> to 4B <sub>H</sub>	Reserved				
4C <sub>H</sub>	Input capture control status register 0/1	ICS01	R/W	Input Capture 0/1	0 0 0 0 0 0 0 0 <sub>B</sub>
4D <sub>H</sub>	Input capture control status register 2/3	ICS23	R/W	Input Capture 2/3	0 0 0 0 0 0 0 0 <sub>B</sub>
4E <sub>H</sub>	Input capture control status register 4/5	ICS45	R/W	Input Capture 4/5	0 0 0 0 0 0 0 0 <sub>B</sub>
4F <sub>H</sub>	Input capture control status register 6/7	ICS67	R/W	Input Capture 6/7	0 0 0 0 0 0 0 0 <sub>B</sub>
50 <sub>H</sub>	Timer control status register 0	TMCSR0	R/W	16-bit Reload Timer 0	0 0 0 0 0 0 0 0 <sub>B</sub>
51 <sub>H</sub>	Timer control status register 0	TMCSR0	R/W		__ __ __ 0 0 0 0 <sub>B</sub>
52 <sub>H</sub>	Timer register 0/reload register 0	TMR0/ TMRLR0	R/W		XXXXXXXX <sub>B</sub>
53 <sub>H</sub>	Timer register 0/reload register 0	TMR0/ TMRLR0	R/W		XXXXXXXX <sub>B</sub>
54 <sub>H</sub>	Timer control status register 1	TMCSR1	R/W	16-bit Reload Timer 1	0 0 0 0 0 0 0 0 <sub>B</sub>
55 <sub>H</sub>	Timer control status register 1	TMCSR1	R/W		__ __ __ 0 0 0 0 <sub>B</sub>
56 <sub>H</sub>	Timer register 1/reload register 1	TMR1/ TMRLR1	R/W		XXXXXXXX <sub>B</sub>
57 <sub>H</sub>	Timer register 1/reload register 1	TMR1/ TMRLR1	R/W		XXXXXXXX <sub>B</sub>
58 <sub>H</sub>	Output compare control status register 0	OCS0	R/W	Output Compare 0/1	0 0 0 0 __ _ 0 0 <sub>B</sub>
59 <sub>H</sub>	Output compare control status register 1	OCS1	R/W		__ _ 0 0 0 0 0 0 <sub>B</sub>
5A <sub>H</sub>	Output compare control status register 2	OCS2	R/W	Output Compare 2/3	0 0 0 0 __ _ 0 0 <sub>B</sub>
5B <sub>H</sub>	Output compare control status register 3	OCS3	R/W		__ _ 0 0 0 0 0 0 <sub>B</sub>
5C <sub>H</sub> to 6B <sub>H</sub>	Reserved				
6C <sub>H</sub>	Timer Data register	TCDDT	R/W	I/O Timer	0 0 0 0 0 0 0 0 <sub>B</sub>
6D <sub>H</sub>	Timer Data register	TCDDT	R/W		0 0 0 0 0 0 0 0 <sub>B</sub>
6E <sub>H</sub>	Timer Control register	TCCS	R/W		0 0 0 0 0 0 0 0 <sub>B</sub>
6F <sub>H</sub>	ROM mirror register	ROMM	R/W	ROM Mirror	__ __ __ __ __ 1 <sub>B</sub>
70 <sub>H</sub> to 7F <sub>H</sub>	Reserved for CAN 0 Interface. Refer to "CAN Controller Hardware Manual"				
80 <sub>H</sub> to 8F <sub>H</sub>	Reserved for CAN 1 Interface. Refer to "CAN Controller Hardware Manual"				
90 <sub>H</sub> to 9D <sub>H</sub>	Reserved				
9E <sub>H</sub>	ROM correction control status register	PACSR	R/W	ROM Correction	0 0 0 0 0 0 0 0 <sub>B</sub>
9F <sub>H</sub>	Delayed interrupt/release register	DIRR	R/W	Delayed Interrupt	__ __ __ __ __ 0 <sub>B</sub>
A0 <sub>H</sub>	Low-power mode register	LPMCR	R/W	Low Power Controller	0 0 0 1 1 0 0 0 <sub>B</sub>
A1 <sub>H</sub>	Clock selector register	CKSCR	R/W	Low Power Controller	1 1 1 1 1 1 0 0 <sub>B</sub>
A2 <sub>H</sub> to A4 <sub>H</sub>	Reserved				

(Continued)

# MB90540/545 Series

(Continued)

Address	Register	Abbreviation	Access	Peripheral	Initial value
A5 <sub>H</sub>	Automatic ready function select register	ARSR	W	External Memory Access	0 0 1 1 _ _ 0 0 <sub>B</sub>
A6 <sub>H</sub>	External address output control register	HACR	W		0 0 0 0 0 0 0 0 <sub>B</sub>
A7 <sub>H</sub>	Bus control signal select register	ECSR	W		0 0 0 0 0 0 0 _ <sub>B</sub>
A8 <sub>H</sub>	Watchdog control register	WDTC	R/W	Watchdog Timer	XXXXX 1 1 1 <sub>B</sub>
A9 <sub>H</sub>	Time Base Timer Control	TBTC	R/W	Time Base Timer	1 - - 0 0 1 0 0 <sub>B</sub>
AA <sub>H</sub>	Watch timer control register	WTC	R/W	Watch Timer	1 X 0 0 0 0 0 0 <sub>B</sub>
AB <sub>H</sub> to AD <sub>H</sub>	Reserved				
AE <sub>H</sub>	Flash control status register (Flash only, otherwise reserved)	FMCS	R/W	Flash Memory	0 0 0 X 0 _ _ 0 <sub>B</sub>
AF <sub>H</sub>	Reserved				
B0 <sub>H</sub>	Interrupt control register 00	ICR00	R/W	Interrupt controller	0 0 0 0 0 1 1 1 <sub>B</sub>
B1 <sub>H</sub>	Interrupt control register 01	ICR01	R/W		0 0 0 0 0 1 1 1 <sub>B</sub>
B2 <sub>H</sub>	Interrupt control register 02	ICR02	R/W		0 0 0 0 0 1 1 1 <sub>B</sub>
B3 <sub>H</sub>	Interrupt control register 03	ICR03	R/W		0 0 0 0 0 1 1 1 <sub>B</sub>
B4 <sub>H</sub>	Interrupt control register 04	ICR04	R/W		0 0 0 0 0 1 1 1 <sub>B</sub>
B5 <sub>H</sub>	Interrupt control register 05	ICR05	R/W		0 0 0 0 0 1 1 1 <sub>B</sub>
B6 <sub>H</sub>	Interrupt control register 06	ICR06	R/W		0 0 0 0 0 1 1 1 <sub>B</sub>
B7 <sub>H</sub>	Interrupt control register 07	ICR07	R/W		0 0 0 0 0 1 1 1 <sub>B</sub>
B8 <sub>H</sub>	Interrupt control register 08	ICR08	R/W		0 0 0 0 0 1 1 1 <sub>B</sub>
B9 <sub>H</sub>	Interrupt control register 09	ICR09	R/W		0 0 0 0 0 1 1 1 <sub>B</sub>
BA <sub>H</sub>	Interrupt control register 10	ICR10	R/W		0 0 0 0 0 1 1 1 <sub>B</sub>
BB <sub>H</sub>	Interrupt control register 11	ICR11	R/W		0 0 0 0 0 1 1 1 <sub>B</sub>
BC <sub>H</sub>	Interrupt control register 12	ICR12	R/W		0 0 0 0 0 1 1 1 <sub>B</sub>
BD <sub>H</sub>	Interrupt control register 13	ICR13	R/W		0 0 0 0 0 1 1 1 <sub>B</sub>
BE <sub>H</sub>	Interrupt control register 14	ICR14	R/W		0 0 0 0 0 1 1 1 <sub>B</sub>
BF <sub>H</sub>	Interrupt control register 15	ICR15	R/W		0 0 0 0 0 1 1 1 <sub>B</sub>
CO <sub>H</sub> to FF <sub>H</sub>	External				

Address	Register	Abbreviation	Access	Peripheral	Initial value
1FF0 <sub>H</sub>	ROM Correction Address 0	PADR0	R/W	ROM correction	XXXXXXXX <sub>B</sub>
1FF1 <sub>H</sub>	ROM Correction Address 1	PADR0	R/W		XXXXXXXX <sub>B</sub>
1FF2 <sub>H</sub>	ROM Correction Address 2	PADR0	R/W		XXXXXXXX <sub>B</sub>
1FF3 <sub>H</sub>	ROM Correction Address 3	PADR1	R/W		XXXXXXXX <sub>B</sub>
1FF4 <sub>H</sub>	ROM Correction Address 4	PADR1	R/W		XXXXXXXX <sub>B</sub>
1FF5 <sub>H</sub>	ROM Correction Address 5	PADR1	R/W		XXXXXXXX <sub>B</sub>

# MB90540/545 Series

Address	Register	Abbreviation	Access	Peripheral	Initial value
3900 <sub>H</sub>	Reload L	PRL0	R/W	16-bit Programmable Pulse Generator 0/1	XXXXXXXX <sub>B</sub>
3901 <sub>H</sub>	Reload H	PRLH0	R/W		XXXXXXXX <sub>B</sub>
3902 <sub>H</sub>	Reload L	PRL1	R/W		XXXXXXXX <sub>B</sub>
3903 <sub>H</sub>	Reload H	PRLH1	R/W		XXXXXXXX <sub>B</sub>
3904 <sub>H</sub>	Reload L	PRL2	R/W	16-bit Programmable Pulse Generator 2/3	XXXXXXXX <sub>B</sub>
3905 <sub>H</sub>	Reload H	PRLH2	R/W		XXXXXXXX <sub>B</sub>
3906 <sub>H</sub>	Reload L	PRL3	R/W		XXXXXXXX <sub>B</sub>
3907 <sub>H</sub>	Reload H	PRLH3	R/W		XXXXXXXX <sub>B</sub>
3908 <sub>H</sub>	Reload L	PRL4	R/W	16-bit Programmable Pulse Generator 4/5	XXXXXXXX <sub>B</sub>
3909 <sub>H</sub>	Reload H	PRLH4	R/W		XXXXXXXX <sub>B</sub>
390A <sub>H</sub>	Reload L	PRL5	R/W		XXXXXXXX <sub>B</sub>
390B <sub>H</sub>	Reload H	PRLH5	R/W		XXXXXXXX <sub>B</sub>
390C <sub>H</sub>	Reload L	PRL6	R/W	16-bit Programmable Pulse Generator 6/7	XXXXXXXX <sub>B</sub>
390D <sub>H</sub>	Reload H	PRLH6	R/W		XXXXXXXX <sub>B</sub>
390E <sub>H</sub>	Reload L	PRL7	R/W		XXXXXXXX <sub>B</sub>
390F <sub>H</sub>	Reload H	PRLH7	R/W		XXXXXXXX <sub>B</sub>
3910 <sub>H</sub> to 3917 <sub>H</sub>	Reserved				
3918 <sub>H</sub>	Input Capture 0	ICP0	R	Input Capture 0/1	XXXXXXXX <sub>B</sub>
3919 <sub>H</sub>	Input Capture 0	ICP0	R		XXXXXXXX <sub>B</sub>
391A <sub>H</sub>	Input Capture 1	ICP1	R		XXXXXXXX <sub>B</sub>
391B <sub>H</sub>	Input Capture 1	ICP1	R		XXXXXXXX <sub>B</sub>
391C <sub>H</sub>	Input Capture 2	ICP2	R	Input Capture 2/3	XXXXXXXX <sub>B</sub>
391D <sub>H</sub>	Input Capture 2	ICP2	R		XXXXXXXX <sub>B</sub>
391E <sub>H</sub>	Input Capture 3	ICP3	R		XXXXXXXX <sub>B</sub>
391F <sub>H</sub>	Input Capture 3	ICP3	R		XXXXXXXX <sub>B</sub>
3920 <sub>H</sub>	Input Capture 4	ICP4	R	Input Capture 4/5	XXXXXXXX <sub>B</sub>
3921 <sub>H</sub>	Input Capture 4	ICP4	R		XXXXXXXX <sub>B</sub>
3922 <sub>H</sub>	Input Capture 5	ICP5	R		XXXXXXXX <sub>B</sub>
3923 <sub>H</sub>	Input Capture 5	ICP5	R		XXXXXXXX <sub>B</sub>
3924 <sub>H</sub>	Input Capture 6	ICP6	R	Input Capture 6/7	XXXXXXXX <sub>B</sub>
3925 <sub>H</sub>	Input Capture 6	ICP6	R		XXXXXXXX <sub>B</sub>
3926 <sub>H</sub>	Input Capture 7	ICP7	R		XXXXXXXX <sub>B</sub>
3927 <sub>H</sub>	Input Capture 7	ICP7	R		XXXXXXXX <sub>B</sub>

(Continued)



# MB90540/545 Series

(Continued)

Address	Register	Abbreviation	Access	Peripheral	Initial value
3928 <sub>H</sub>	Output Compare 0	OCCP0	R/W	Output Compare 0/1	XXXXXXXX <sub>B</sub>
3929 <sub>H</sub>	Output Compare 0	OCCP0	R/W		XXXXXXXX <sub>B</sub>
392A <sub>H</sub>	Output Compare 1	OCCP1	R/W		XXXXXXXX <sub>B</sub>
392B <sub>H</sub>	Output Compare 1	OCCP1	R/W		XXXXXXXX <sub>B</sub>
392C <sub>H</sub>	Output Compare 2	OCCP2	R/W	Output Compare 2/3	XXXXXXXX <sub>B</sub>
392D <sub>H</sub>	Output Compare 2	OCCP2	R/W		XXXXXXXX <sub>B</sub>
392E <sub>H</sub>	Output Compare 3	OCCP3	R/W		XXXXXXXX <sub>B</sub>
392F <sub>H</sub>	Output Compare 3	OCCP3	R/W		XXXXXXXX <sub>B</sub>
3930 <sub>H</sub> to 39FF <sub>H</sub>	Reserved				
3A00 <sub>H</sub> to 3AFF <sub>H</sub>	Reserved for CAN 0 Interface. Refer to “CAN Controller Hardware Manual”				
3B00 <sub>H</sub> to 3BFF <sub>H</sub>	Reserved for CAN 0 Interface. Refer to “CAN Controller Hardware Manual”				
3C00 <sub>H</sub> to 3CFF <sub>H</sub>	Reserved for CAN 1 Interface. Refer to “CAN Controller Hardware Manual”				
3D00 <sub>H</sub> to 3DFF <sub>H</sub>	Reserved for CAN 1 Interface. Refer to “CAN Controller Hardware Manual”				
3E00 <sub>H</sub> to 3FFF <sub>H</sub>	Reserved				

Note Initial value of “\_” represents unused bit, “X” represents unknown value.  
Addresses in the range 0000<sub>H</sub> to 00FF<sub>H</sub>, which are not listed in the table, are reserved for the primary functions of the MCU. A read access to these reserved addresses results in an “X” reading and any write access should not be performed.

# MB90540/545 Series

## ■ CAN CONTROLLER

The MB90540 series contains two CAN controllers (CAN0 and CAN1), the MB90545 series contains only one (CAN0). The Evaluation Chip MB90V540 also has two CAN controllers.

The CAN controller has the following features:

- Conforms to CAN Specification Version 2.0 Part A and B
  - Supports transmission/reception in standard frame and extended frame formats
- Supports transmission of data frames by receiving remote frames
- 16 transmitting/receiving message buffers
  - 29-bit ID and 8-byte data
  - Multi-level message buffer configuration
- Provides full-bit comparison, full-bit mask, acceptance register 0/acceptance register 1 for each message buffer as 1D acceptance mask
  - Two acceptance mask registers in either standard frame format or extended frame formats
- Bit rate programmable from 10 Kbit/s to 1 Mbit/s (when input clock is at 16 MHz)

**List of Control Registers**

Address		Register	Abbreviation	Access	Initial Value
CAN0	CAN1				
000070 <sub>H</sub>	000080 <sub>H</sub>	Message buffer valid register	BVALR	R/W	00000000 00000000 <sub>B</sub>
000071 <sub>H</sub>	000081 <sub>H</sub>				
000072 <sub>H</sub>	000082 <sub>H</sub>	Transmit request register	TREQR	R/W	00000000 00000000 <sub>B</sub>
000073 <sub>H</sub>	000083 <sub>H</sub>				
000074 <sub>H</sub>	000084 <sub>H</sub>	Transmit cancel register	TCANR	W	00000000 00000000 <sub>B</sub>
000075 <sub>H</sub>	000085 <sub>H</sub>				
000076 <sub>H</sub>	000086 <sub>H</sub>	Transmit complete register	TCR	R/W	00000000 00000000 <sub>B</sub>
000077 <sub>H</sub>	000087 <sub>H</sub>				
000078 <sub>H</sub>	000088 <sub>H</sub>	Receive complete register	RCR	R/W	00000000 00000000 <sub>B</sub>
000079 <sub>H</sub>	000089 <sub>H</sub>				
00007A <sub>H</sub>	00008A <sub>H</sub>	Remote request receiving register	RRTRR	R/W	00000000 00000000 <sub>B</sub>
00007B <sub>H</sub>	00008B <sub>H</sub>				
00007C <sub>H</sub>	00008C <sub>H</sub>	Receive overrun register	ROVRR	R/W	00000000 00000000 <sub>B</sub>
00007D <sub>H</sub>	00008D <sub>H</sub>				
00007E <sub>H</sub>	00008E <sub>H</sub>	Receive interrupt enable register	RIER	R/W	00000000 00000000 <sub>B</sub>
00007F <sub>H</sub>	00008F <sub>H</sub>				

# MB90540/545 Series

List of Control Registers

Address		Register	Abbreviation	Access	Initial Value
CAN0	CAN1				
003B00 <sub>H</sub>	003D00 <sub>H</sub>	Control status register	CSR	R/W, R	00---000 0----0-1 <sub>B</sub>
003B01 <sub>H</sub>	003D01 <sub>H</sub>				
003B02 <sub>H</sub>	003D02 <sub>H</sub>	Last event indicator register	LEIR	R/W	----- 000-0000 <sub>B</sub>
003B03 <sub>H</sub>	003D03 <sub>H</sub>				
003B04 <sub>H</sub>	003D04 <sub>H</sub>	Receive/transmit error counter	RTEC	R	00000000 00000000 <sub>B</sub>
003B05 <sub>H</sub>	003D05 <sub>H</sub>				
003B06 <sub>H</sub>	003D06 <sub>H</sub>	Bit timing register	BTR	R/W	-11111111 11111111 <sub>B</sub>
003B07 <sub>H</sub>	003D07 <sub>H</sub>				
003B08 <sub>H</sub>	003D08 <sub>H</sub>	IDE register	IDER	R/W	XXXXXXXX XXXXXXXX <sub>B</sub>
003B09 <sub>H</sub>	003D09 <sub>H</sub>				
003B0A <sub>H</sub>	003D0A <sub>H</sub>	Transmit RTR register	TRTRR	R/W	00000000 00000000 <sub>B</sub>
003B0B <sub>H</sub>	003D0B <sub>H</sub>				
003B0C <sub>H</sub>	003D0C <sub>H</sub>	Remote frame receive waiting register	RFWTR	R/W	XXXXXXXX XXXXXXXX <sub>B</sub>
003B0D <sub>H</sub>	003D0D <sub>H</sub>				
003B0E <sub>H</sub>	003D0E <sub>H</sub>	Transmit interrupt enable register	TIER	R/W	00000000 00000000 <sub>B</sub>
003B0F <sub>H</sub>	003D0F <sub>H</sub>				
003B10 <sub>H</sub>	003D10 <sub>H</sub>	Acceptance mask select register	AMSR	R/W	XXXXXXXX XXXXXXXX <sub>B</sub>
003B11 <sub>H</sub>	003D11 <sub>H</sub>				XXXXXXXX XXXXXXXX <sub>B</sub>
003B12 <sub>H</sub>	003D12 <sub>H</sub>				XXXXXXXX XXXXXXXX <sub>B</sub>
003B13 <sub>H</sub>	003D13 <sub>H</sub>	Acceptance mask register 0	AMR0	R/W	XXXXXXXX XXXXXXXX <sub>B</sub>
003B14 <sub>H</sub>	003D14 <sub>H</sub>				XXXXXXXX XXXXXXXX <sub>B</sub>
003B15 <sub>H</sub>	003D15 <sub>H</sub>				XXXXX--- XXXXXXXX <sub>B</sub>
003B16 <sub>H</sub>	003D16 <sub>H</sub>				XXXXXXXX XXXXXXXX <sub>B</sub>
003B17 <sub>H</sub>	003D17 <sub>H</sub>	Acceptance mask register 1	AMR1	R/W	XXXXXXXX XXXXXXXX <sub>B</sub>
003B18 <sub>H</sub>	003D18 <sub>H</sub>				XXXXXXXX XXXXXXXX <sub>B</sub>
003B19 <sub>H</sub>	003D19 <sub>H</sub>				XXXXX--- XXXXXXXX <sub>B</sub>
003B1A <sub>H</sub>	003D1A <sub>H</sub>				XXXXXXXX XXXXXXXX <sub>B</sub>
003B1B <sub>H</sub>	003D1B <sub>H</sub>				

# MB90540/545 Series

List of Message Buffers (ID Registers) (1)

Address		Register	Abbreviation	Access	Initial Value
CAN0	CAN1				
003A00 <sub>H</sub> to 003A1F <sub>H</sub>	003C00 <sub>H</sub> to 003C1F <sub>H</sub>	General-purpose RAM	—	R/W	XXXXXXXX <sub>B</sub> to XXXXXXXX <sub>B</sub>
003A20 <sub>H</sub>	003C20 <sub>H</sub>	ID register 0	IDR0	R/W	XXXXXXXX XXXXXXXX <sub>B</sub>
003A21 <sub>H</sub>	003C21 <sub>H</sub>				XXXXX--- XXXXXXXX <sub>B</sub>
003A22 <sub>H</sub>	003C22 <sub>H</sub>				
003A23 <sub>H</sub>	003C23 <sub>H</sub>				
003A24 <sub>H</sub>	003C24 <sub>H</sub>	ID register 1	IDR1	R/W	XXXXXXXX XXXXXXXX <sub>B</sub>
003A25 <sub>H</sub>	003C25 <sub>H</sub>				XXXXX--- XXXXXXXX <sub>B</sub>
003A26 <sub>H</sub>	003C26 <sub>H</sub>				
003A27 <sub>H</sub>	003C27 <sub>H</sub>				
003A28 <sub>H</sub>	003C28 <sub>H</sub>	ID register 2	IDR2	R/W	XXXXXXXX XXXXXXXX <sub>B</sub>
003A29 <sub>H</sub>	003C29 <sub>H</sub>				XXXXX--- XXXXXXXX <sub>B</sub>
003A2A <sub>H</sub>	003C2A <sub>H</sub>				
003A2B <sub>H</sub>	003C2B <sub>H</sub>				
003A2C <sub>H</sub>	003C2C <sub>H</sub>	ID register 3	IDR3	R/W	XXXXXXXX XXXXXXXX <sub>B</sub>
003A2D <sub>H</sub>	003C2D <sub>H</sub>				XXXXX--- XXXXXXXX <sub>B</sub>
003A2E <sub>H</sub>	003C2E <sub>H</sub>				
003A2F <sub>H</sub>	003C2F <sub>H</sub>				
003A30 <sub>H</sub>	003C30 <sub>H</sub>	ID register 4	IDR4	R/W	XXXXXXXX XXXXXXXX <sub>B</sub>
003A31 <sub>H</sub>	003C31 <sub>H</sub>				XXXXX--- XXXXXXXX <sub>B</sub>
003A32 <sub>H</sub>	003C32 <sub>H</sub>				
003A33 <sub>H</sub>	003C33 <sub>H</sub>				
003A34 <sub>H</sub>	003C34 <sub>H</sub>	ID register 5	IDR5	R/W	XXXXXXXX XXXXXXXX <sub>B</sub>
003A35 <sub>H</sub>	003C35 <sub>H</sub>				XXXXX--- XXXXXXXX <sub>B</sub>
003A36 <sub>H</sub>	003C36 <sub>H</sub>				
003A37 <sub>H</sub>	003C37 <sub>H</sub>				
003A38 <sub>H</sub>	003C38 <sub>H</sub>	ID register 6	IDR6	R/W	XXXXXXXX XXXXXXXX <sub>B</sub>
003A39 <sub>H</sub>	003C39 <sub>H</sub>				XXXXX--- XXXXXXXX <sub>B</sub>
003A3A <sub>H</sub>	003C3A <sub>H</sub>				
003A3B <sub>H</sub>	003C3B <sub>H</sub>				

# MB90540/545 Series

List of Message Buffers (ID Registers) (2)

Address		Register	Abbreviation	Access	Initial Value
CAN0	CAN1				
003A3C <sub>H</sub>	003C3C <sub>H</sub>	ID register 7	IDR7	R/W	XXXXXXXX XXXXXXXX <sub>B</sub>
003A3D <sub>H</sub>	003C3D <sub>H</sub>				XXXXX--- XXXXXXXX <sub>B</sub>
003A3E <sub>H</sub>	003C3E <sub>H</sub>				
003A3F <sub>H</sub>	003C3F <sub>H</sub>				
003A40 <sub>H</sub>	003C40 <sub>H</sub>	ID register 8	IDR8	R/W	XXXXXXXX XXXXXXXX <sub>B</sub>
003A41 <sub>H</sub>	003C41 <sub>H</sub>				XXXXX--- XXXXXXXX <sub>B</sub>
003A42 <sub>H</sub>	003C42 <sub>H</sub>				
003A43 <sub>H</sub>	003C43 <sub>H</sub>				
003A44 <sub>H</sub>	003C44 <sub>H</sub>	ID register 9	IDR9	R/W	XXXXXXXX XXXXXXXX <sub>B</sub>
003A45 <sub>H</sub>	003C45 <sub>H</sub>				XXXXX--- XXXXXXXX <sub>B</sub>
003A46 <sub>H</sub>	003C46 <sub>H</sub>				
003A47 <sub>H</sub>	003C47 <sub>H</sub>				
003A48 <sub>H</sub>	003C48 <sub>H</sub>	ID register 10	IDR10	R/W	XXXXXXXX XXXXXXXX <sub>B</sub>
003A49 <sub>H</sub>	003C49 <sub>H</sub>				XXXXX--- XXXXXXXX <sub>B</sub>
003A4A <sub>H</sub>	003C4A <sub>H</sub>				
003A4B <sub>H</sub>	003C4B <sub>H</sub>				
003A4C <sub>H</sub>	003C4C <sub>H</sub>	ID register 11	IDR11	R/W	XXXXXXXX XXXXXXXX <sub>B</sub>
003A4D <sub>H</sub>	003C4D <sub>H</sub>				XXXXX--- XXXXXXXX <sub>B</sub>
003A4E <sub>H</sub>	003C4E <sub>H</sub>				
003A4F <sub>H</sub>	003C4F <sub>H</sub>				
003A50 <sub>H</sub>	003C50 <sub>H</sub>	ID register 12	IDR12	R/W	XXXXXXXX XXXXXXXX <sub>B</sub>
003A51 <sub>H</sub>	003C51 <sub>H</sub>				XXXXX--- XXXXXXXX <sub>B</sub>
003A52 <sub>H</sub>	003C52 <sub>H</sub>				
003A53 <sub>H</sub>	003C53 <sub>H</sub>				
003A54 <sub>H</sub>	003C54 <sub>H</sub>	ID register 13	IDR13	R/W	XXXXXXXX XXXXXXXX <sub>B</sub>
003A55 <sub>H</sub>	003C55 <sub>H</sub>				XXXXX--- XXXXXXXX <sub>B</sub>
003A56 <sub>H</sub>	003C56 <sub>H</sub>				
003A57 <sub>H</sub>	003C57 <sub>H</sub>				
003A58 <sub>H</sub>	003C58 <sub>H</sub>	ID register 14	IDR14	R/W	XXXXXXXX XXXXXXXX <sub>B</sub>
003A59 <sub>H</sub>	003C59 <sub>H</sub>				XXXXX--- XXXXXXXX <sub>B</sub>
003A5A <sub>H</sub>	003C5A <sub>H</sub>				
003A5B <sub>H</sub>	003C5B <sub>H</sub>				
003A5C <sub>H</sub>	003C5C <sub>H</sub>	ID register 15	IDR15	R/W	XXXXXXXX XXXXXXXX <sub>B</sub>
003A5D <sub>H</sub>	003C5D <sub>H</sub>				XXXXX--- XXXXXXXX <sub>B</sub>
003A5E <sub>H</sub>	003C5E <sub>H</sub>				
003A5F <sub>H</sub>	003C5F <sub>H</sub>				

# MB90540/545 Series

List of Message Buffers (DLC Registers and Data Registers) (1)

Address		Register	Abbreviation	Access	Initial Value
CAN0	CAN1				
003A60 <sub>H</sub>	003C60 <sub>H</sub>	DLC register 0	DLCR0	R/W	----XXXX <sub>B</sub>
003A61 <sub>H</sub>	003C61 <sub>H</sub>				
003A62 <sub>H</sub>	003C62 <sub>H</sub>	DLC register 1	DLCR1	R/W	----XXXX <sub>B</sub>
003A63 <sub>H</sub>	003C63 <sub>H</sub>				
003A64 <sub>H</sub>	003C64 <sub>H</sub>	DLC register 2	DLCR2	R/W	----XXXX <sub>B</sub>
003A65 <sub>H</sub>	003C65 <sub>H</sub>				
003A66 <sub>H</sub>	003C66 <sub>H</sub>	DLC register 3	DLCR3	R/W	----XXXX <sub>B</sub>
003A67 <sub>H</sub>	003C67 <sub>H</sub>				
003A68 <sub>H</sub>	003C68 <sub>H</sub>	DLC register 4	DLCR4	R/W	----XXXX <sub>B</sub>
003A69 <sub>H</sub>	003C69 <sub>H</sub>				
003A6A <sub>H</sub>	003C6A <sub>H</sub>	DLC register 5	DLCR5	R/W	----XXXX <sub>B</sub>
003A6B <sub>H</sub>	003C6B <sub>H</sub>				
003A6C <sub>H</sub>	003C6C <sub>H</sub>	DLC register 6	DLCR6	R/W	----XXXX <sub>B</sub>
003A6D <sub>H</sub>	003C6D <sub>H</sub>				
003A6E <sub>H</sub>	003C6E <sub>H</sub>	DLC register 7	DLCR7	R/W	----XXXX <sub>B</sub>
003A6F <sub>H</sub>	003C6F <sub>H</sub>				

# MB90540/545 Series

List of Message Buffers (DLC Registers and Data Registers) (2)

Address		Register	Abbreviation	Access	Initial Value
CAN0	CAN1				
003A70 <sub>H</sub>	003C70 <sub>H</sub>	DLC register 8	DLCR8	R/W	----XXXX
003A71 <sub>H</sub>	003C71 <sub>H</sub>				
003A72 <sub>H</sub>	003C72 <sub>H</sub>	DLC register 9	DLCR9	R/W	----XXXX <sub>B</sub>
003A73 <sub>H</sub>	003C73 <sub>H</sub>				
003A74 <sub>H</sub>	003C74 <sub>H</sub>	DLC register 10	DLCR10	R/W	----XXXX <sub>B</sub>
003A75 <sub>H</sub>	003C75 <sub>H</sub>				
003A76 <sub>H</sub>	003C76 <sub>H</sub>	DLC register 11	DLCR11	R/W	----XXXX <sub>B</sub>
003A77 <sub>H</sub>	003C77 <sub>H</sub>				
003A78 <sub>H</sub>	003C78 <sub>H</sub>	DLC register 12	DLCR12	R/W	----XXXX <sub>B</sub>
003A79 <sub>H</sub>	003C79 <sub>H</sub>				
003A7A <sub>H</sub>	003C7A <sub>H</sub>	DLC register 13	DLCR13	R/W	----XXXX <sub>B</sub>
003A7B <sub>H</sub>	003C7B <sub>H</sub>				
003A7C <sub>H</sub>	003C7C <sub>H</sub>	DLC register 14	DLCR14	R/W	----XXXX <sub>B</sub>
003A7D <sub>H</sub>	003C7D <sub>H</sub>				
003A7E <sub>H</sub>	003C7E <sub>H</sub>	DLC register 15	DLCR15	R/W	----XXXX <sub>B</sub>
003A7F <sub>H</sub>	003C7F <sub>H</sub>				
003A80 <sub>H</sub> to 003A87 <sub>H</sub>	003C80 <sub>H</sub> to 003C87 <sub>H</sub>	Data register 0 (8 bytes)	DTR0	R/W	XXXXXXXX <sub>B</sub> to XXXXXXXX <sub>B</sub>
003A88 <sub>H</sub> to 003A8F <sub>H</sub>	003C88 <sub>H</sub> to 003C8F <sub>H</sub>	Data register 1 (8 bytes)	DTR1	R/W	XXXXXXXX <sub>B</sub> to XXXXXXXX <sub>B</sub>
003A90 <sub>H</sub> to 003A97 <sub>H</sub>	003C90 <sub>H</sub> to 003C97 <sub>H</sub>	Data register 2 (8 bytes)	DTR2	R/W	XXXXXXXX <sub>B</sub> to XXXXXXXX <sub>B</sub>
003A98 <sub>H</sub> to 003A9F <sub>H</sub>	003C98 <sub>H</sub> to 003C9F <sub>H</sub>	Data register 3 (8 bytes)	DTR3	R/W	XXXXXXXX <sub>B</sub> to XXXXXXXX <sub>B</sub>
003AA0 <sub>H</sub> to 003AA7 <sub>H</sub>	003CA0 <sub>H</sub> to 003CA7 <sub>H</sub>	Data register 4 (8 bytes)	DTR4	R/W	XXXXXXXX <sub>B</sub> to XXXXXXXX <sub>B</sub>
003AA8 <sub>H</sub> to 003AAF <sub>H</sub>	003CA8 <sub>H</sub> to 003CAF <sub>H</sub>	Data register 5 (8 bytes)	DTR5	R/W	XXXXXXXX <sub>B</sub> to XXXXXXXX <sub>B</sub>
003AB0 <sub>H</sub> to 003AB7 <sub>H</sub>	003CB0 <sub>H</sub> to 003CB7 <sub>H</sub>	Data register 6 (8 bytes)	DTR6	R/W	XXXXXXXX <sub>B</sub> to XXXXXXXX <sub>B</sub>

# MB90540/545 Series

List of Message Buffers (DLC Registers and Data Registers) (3)

Address		Register	Abbreviation	Access	Initial Value
CAN0	CAN1				
003AB8H to 003ABFH	003CB8H to 003CBFH	Data register 7 (8 bytes)	DTR7	R/W	XXXXXXXX <sub>B</sub> to XXXXXXXX <sub>B</sub>
003AC0H to 003AC7H	003CC0H to 003CC7H	Data register 8 (8 bytes)	DTR8	R/W	XXXXXXXX <sub>B</sub> to XXXXXXXX <sub>B</sub>
003AC8H to 003ACFH	003CC8H to 003CCFH	Data register 9 (8 bytes)	DTR9	R/W	XXXXXXXX <sub>B</sub> to XXXXXXXX <sub>B</sub>
003AD0H to 003AD7H	003CD0H to 003CD7H	Data register 10 (8 bytes)	DTR10	R/W	XXXXXXXX <sub>B</sub> to XXXXXXXX <sub>B</sub>
003AD8H to 003ADFH	003CD8H to 003CDFH	Data register 11 (8 bytes)	DTR11	R/W	XXXXXXXX <sub>B</sub> to XXXXXXXX <sub>B</sub>
003AE0H to 003AE7H	003CE0H to 003CE7H	Data register 12 (8 bytes)	DTR12	R/W	XXXXXXXX <sub>B</sub> to XXXXXXXX <sub>B</sub>
003AE8H to 003AEFH	003CE8H to 003CEFH	Data register 13 (8 bytes)	DTR13	R/W	XXXXXXXX <sub>B</sub> to XXXXXXXX <sub>B</sub>
003AF0H to 003AF7H	003CF0H to 003CF7H	Data register 14 (8 bytes)	DTR14	R/W	XXXXXXXX <sub>B</sub> to XXXXXXXX <sub>B</sub>
003AF8H to 003AFFH	003CF8H to 003CFFH	Data register 15 (8 bytes)	DTR15	R/W	XXXXXXXX <sub>B</sub> to XXXXXXXX <sub>B</sub>



## ■ INTERRUPT MAP

Interrupt cause	EI <sup>2</sup> OS clear	Interrupt vector		Interrupt control register	
		Number	Address	Number	Address
Reset	N/A	#08	FFFFDC <sub>H</sub>	—	—
INT9 instruction	N/A	#09	FFFFD8 <sub>H</sub>	—	—
Exception	N/A	#10	FFFFD4 <sub>H</sub>	—	—
CAN 0 RX	N/A	#11	FFFFD0 <sub>H</sub>	ICR00	0000B0 <sub>H</sub>
CAN 0 TX/NS	N/A	#12	FFFFCC <sub>H</sub>		
CAN 1 RX	N/A	#13	FFFFC8 <sub>H</sub>	ICR01	0000B1 <sub>H</sub>
CAN 1 TX/NS	N/A	#14	FFFFC4 <sub>H</sub>		
External Interrupt INT0/INT1	*1	#15	FFFFC0 <sub>H</sub>	ICR02	0000B2 <sub>H</sub>
Time Base Timer	N/A	#16	FFFFBC <sub>H</sub>		
16-bit Reload Timer 0	*1	#17	FFFFB8 <sub>H</sub>	ICR03	0000B3 <sub>H</sub>
8/10-bit A/D Converter	*1	#18	FFFFB4 <sub>H</sub>		
I/O Timer	N/A	#19	FFFFB0 <sub>H</sub>	ICR04	0000B4 <sub>H</sub>
External Interrupt INT2/INT3	*1	#20	FFFFAC <sub>H</sub>		
Serial I/O	*1	#21	FFFFA8 <sub>H</sub>	ICR05	0000B5 <sub>H</sub>
8/16-bit PPG 0/1	N/A	#22	FFFFA4 <sub>H</sub>		
Input Capture 0	*1	#23	FFFFA0 <sub>H</sub>	ICR06	0000B6 <sub>H</sub>
External Interrupt INT4/INT5	*1	#24	FFFF9C <sub>H</sub>		
Input Capture 1	*1	#25	FFFF98 <sub>H</sub>	ICR07	0000B7 <sub>H</sub>
8/16-bit PPG 2/3	N/A	#26	FFFF94 <sub>H</sub>		
External Interrupt INT6/INT7	*1	#27	FFFF90 <sub>H</sub>	ICR08	0000B8 <sub>H</sub>
Watch Timer	N/A	#28	FFFF8C <sub>H</sub>		
8/16-bit PPG 4/5	N/A	#29	FFFF88 <sub>H</sub>	ICR09	0000B9 <sub>H</sub>
Input Capture 2/3	*1	#30	FFFF84 <sub>H</sub>		
8/16-bit PPG 6/7	N/A	#31	FFFF80 <sub>H</sub>	ICR10	0000BA <sub>H</sub>
Output Compare 0	*1	#32	FFFF7C <sub>H</sub>		
Output Compare 1	*1	#33	FFFF78 <sub>H</sub>	ICR11	0000BB <sub>H</sub>
Input Capture 4/5	*1	#34	FFFF74 <sub>H</sub>		
Output Compare 2/3 - Input Capture 6/7	*1	#35	FFFF70 <sub>H</sub>	ICR12	0000BC <sub>H</sub>
16-bit Reload Timer 1	*1	#36	FFFF6C <sub>H</sub>		
UART 0 RX	*2	#37	FFFF68 <sub>H</sub>	ICR13	0000BD <sub>H</sub>
UART 0 TX	*1	#38	FFFF64 <sub>H</sub>		
UART 1 RX	*2	#39	FFFF60 <sub>H</sub>	ICR14	0000BE <sub>H</sub>
UART 1 TX	*1	#40	FFFF5C <sub>H</sub>		
Flash Memory	N/A	#41	FFFF58 <sub>H</sub>	ICR15	0000BF <sub>H</sub>
Delayed interrupt	N/A	#42	FFFF54 <sub>H</sub>		

# MB90540/545 Series

\*1: The interrupt request flag is cleared by the EI<sup>2</sup>OS interrupt clear signal.

\*2: The interrupt request flag is cleared by the EI<sup>2</sup>OS interrupt clear signal. A stop request is available.

N/A: The interrupt request flag is not cleared by the EI<sup>2</sup>OS interrupt clear signal.

Note: • For a peripheral module with two interrupt causes for a single interrupt number, both interrupt request flags are cleared by the EI<sup>2</sup>OS interrupt clear signal.

- At the end of EI<sup>2</sup>OS, the EI<sup>2</sup>OS clear signal will be asserted for all the interrupt flags assigned to the same interrupt number. If one interrupt flag starts the EI<sup>2</sup>OS and in the meantime another interrupt flag is set by a hardware event, the later event is lost because the flag is cleared by the EI<sup>2</sup>OS clear signal caused by the first event. So it is recommended not to use the EI<sup>2</sup>OS for this interrupt number.

- If EI<sup>2</sup>OS is enabled, EI<sup>2</sup>OS is initiated when one of the two interrupt signals in the same interrupt control register (ICR) is asserted. This means that different interrupt sources share the same EI<sup>2</sup>OS Descriptor which should be unique for each interrupt source. For this reason, when one interrupt source uses the EI<sup>2</sup>OS, the other interrupt should be disabled.

## ■ ELECTRICAL CHARACTERISTICS

### 1. Absolute Maximum Ratings

( $V_{SS} = AV_{SS} = 0V$ )

Parameter	Symbol	Value		Units	Remarks
		Min.	Max.		
Power supply voltage	$V_{CC}$	$V_{SS} - 0.3$	$V_{SS} + 6.0$	V	
	$AV_{CC}$	$V_{SS} - 0.3$	$V_{SS} + 6.0$	V	$V_{CC} = AV_{CC}$ *1
	AVRH, AVRL	$V_{SS} - 0.3$	$V_{SS} + 6.0$	V	$AV_{CC} \geq AVRH/AVRL$ , $AVRH \geq AVRL$ *1
Input voltage	$V_I$	$V_{SS} - 0.3$	$V_{SS} + 6.0$	V	*2
Output voltage	$V_O$	$V_{SS} - 0.3$	$V_{SS} + 6.0$	V	*2
Clamp Current	$I_{CLAMP}$	-2.0	2.0	mA	
"L" level max. output current	$I_{OL}$	—	15	mA	*3
"L" level avg. output current	$I_{OLAV}$	—	4	mA	*4
"L" level max. overall output current	$\Sigma I_{OL}$	—	100	mA	
"L" level avg. overall output current	$\Sigma I_{OLAV}$	—	50	mA	*5
"H" level max. output current	$I_{OH}$	—	-15	mA	*3
"H" level avg. output current	$I_{OHAV}$	—	-4	mA	*4
"H" level max. overall output current	$\Sigma I_{OH}$	—	-100	mA	
"H" level avg. overall output current	$\Sigma I_{OHAV}$	—	-50	mA	*5
Power consumption	$P_D$	—	500	mW	MB90F543/F549
Operating temperature	$T_A$	-40	+85	°C	
Storage temperature	$T_{STG}$	-55	+150	°C	

\*1:  $AV_{CC}$ , AVRH and AVRL should not exceed  $V_{CC}$ , and AVRL should not exceed AVRH.

\*2:  $V_I$  and  $V_O$  should not exceed  $V_{CC} + 0.3V$ .  $V_I$  should not exceed the specified ratings. However if the maximum current to/from an input is limited by some means with external components, the  $I_{CLAMP}$  rating supercedes the  $V_I$  rating.

\*3: The maximum output current is a peak value for a corresponding pin.

\*4: Average output current is an average current value observed for a 100 ms period for a corresponding pin.

\*5: Total average current is an average current value observed for a 100 ms period for all corresponding pins.

Note: Average output current = operating current × operating efficiency

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

# MB90540/545 Series

## 2. Recommended Conditions

( $V_{SS} = AV_{SS} = 0V$ )

Parameter	Symbol	Value			Units	Remarks
		Min.	Typ.	Max.		
Power supply voltage	$V_{CC}$	4.5	5.0	5.5	V	
Smooth capacitor	$C_S$	0.022	0.1	1.0	$\mu F$	*
Operating temperature	$T_A$	-40		+85	$^{\circ}C$	

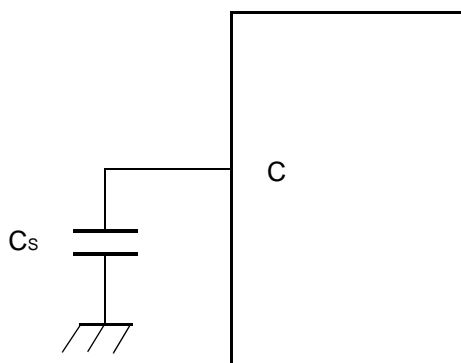
\*: Use a ceramic capacitor or a capacitor of better AC characteristics. The  $V_{CC}$  Capacitor should be greater than this capacitor.

**WARNING:** The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

### • C Pin Connection Diagram



# MB90540/545 Series

## 3. DC Characteristics

( $V_{CC} = 5.0\text{ V} \pm 10\%$ ,  $V_{SS} = AV_{SS} = 0\text{V}$ ,  $T_A = -40\text{ }^\circ\text{C}$  to  $+85\text{ }^\circ\text{C}$ )

Parameter	Symbol	Pin	Condition	Value			Units	Remarks
				Min.	Typ.	Max.		
Input H voltage	$V_{IHS}$	CMOS hysteresis input pin	—	$0.8 V_{CC}$	—	$V_{CC} + 0.3$	V	
	$V_{IHM}$	MD input pin	—	$V_{CC} - 0.3$	—	$V_{CC} + 0.3$	V	
Input L voltage	$V_{ILS}$	CMOS hysteresis input pin	—	$V_{CC} - 0.3$	—	$0.2 V_{CC}$	V	
	$V_{ILM}$	MD input pin	—	$V_{CC} - 0.3$	—	$V_{CC} + 0.3$	V	
Output H voltage	$V_{OH}$	All output pins	$V_{CC} = 4.5\text{V}$ , $I_{OH} = -4.0\text{mA}$	$V_{CC} - 0.5$	—	—	V	
Output L voltage	$V_{OL}$	All output pins	$V_{CC} = 4.5\text{V}$ , $I_{OL} = 4.0\text{mA}$	—	—	0.4	V	
Input leak current	$I_{IL}$		$V_{CC} = 5.5\text{V}$ , $V_{SS} < V_i < V_{CC}$	-5	—	5	$\mu\text{A}$	
Power supply current*	$I_{CC}$	$V_{CC}$	$V_{CC} = 5.0\text{ V} \pm 10\%$ , Internal frequency: 16 MHz, At normal operation	—	45	60	mA	MB90F543/F549
	$I_{CCS}$		$V_{CC} = 5.0\text{V} \pm 10\%$ , Internal frequency: 16 MHz, At sleep	—	13	22	mA	MB90F543/F549
	$I_{CCL}$		$V_{CC} = 5.0\text{V}$ , Internal frequency: 8 kHz, At sub operation	—	0.2	1	mA	MB90F543/F549
	$I_{CCLS}$		$V_{CC} = 5.0\text{V}$ , Internal frequency: 8 kHz, At sub sleep	—	10	50	$\mu\text{A}$	MB90F543/F549
	$I_{CCT}$		$V_{CC} = 5.0\text{V}$ , Internal frequency: 8 kHz, At watch mode	—	10	50	$\mu\text{A}$	MB90F543/F549
	$I_{CCH1}$		$V_{CC} = 5.0\text{ V} \pm 10\%$ , At stop, $T_A = 25\text{ }^\circ\text{C}$	—	5	20	$\mu\text{A}$	MB90F543/F549
	$I_{CCH2}$		$V_{CC} = 5.0\text{ V} \pm 10\%$ , At hardware standby mode, $T_A = 25\text{ }^\circ\text{C}$	—	50	100	$\mu\text{A}$	MB90F543/F549
Input capacity	$C_{IN}$	Other than $AV_{CC}$ , $AV_{SS}$ , $AVRH$ , $AVRL$ , C, $V_{CC}$ , $V_{SS}$	—	—	10	80	pF	

\*: Current values are tentative. They are subject to change without notice according to improvements in the characteristics. The power supply current testing conditions are when using the external clock.

# MB90540/545 Series

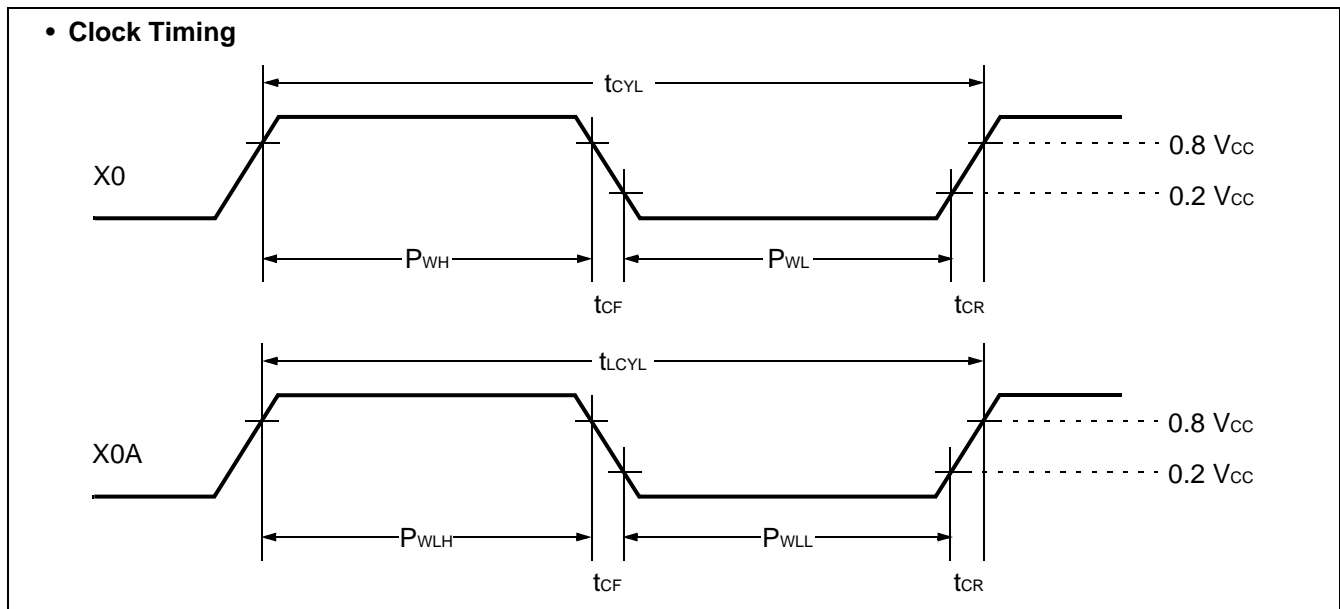
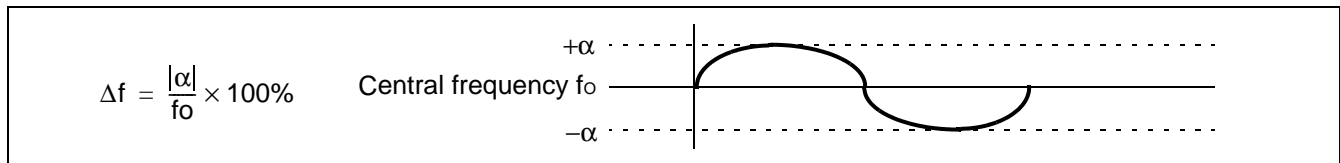
## 4. AC Characteristics

### (1) Clock Timing

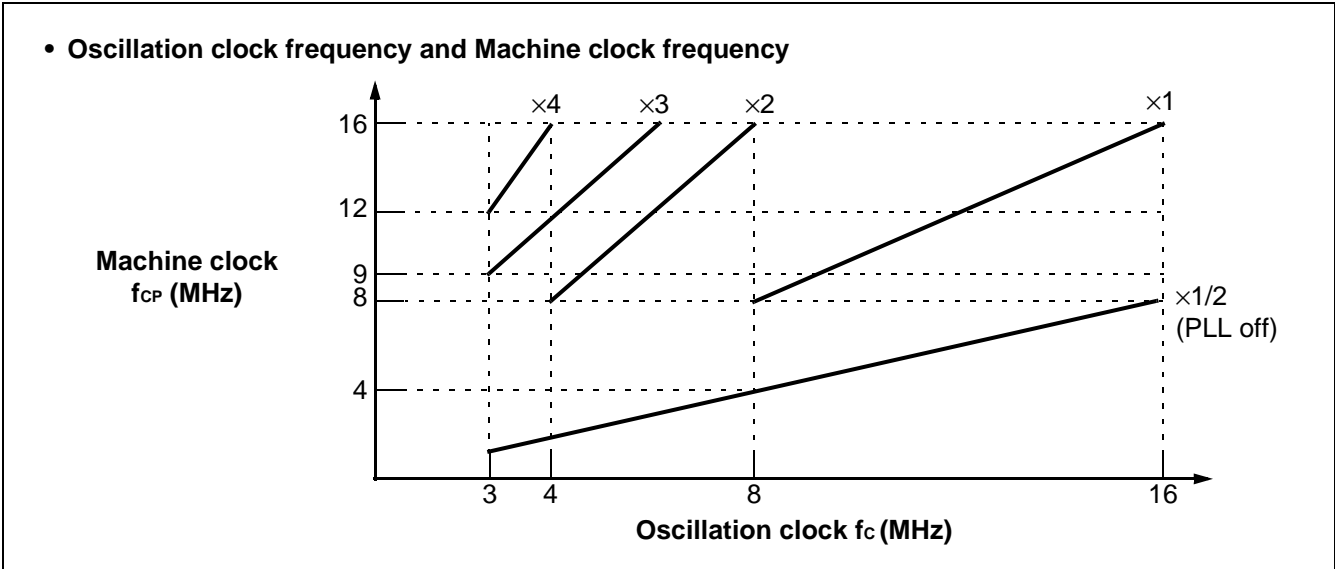
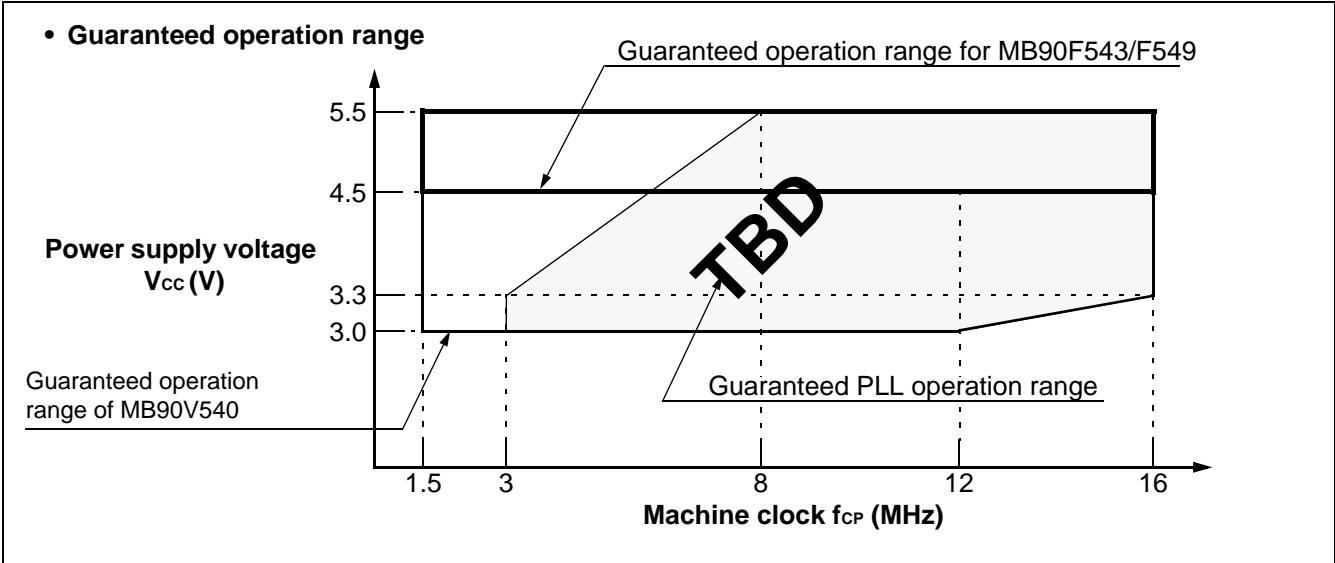
( $V_{CC} = 5.0\text{ V} \pm 10\%$ ,  $V_{SS} = AV_{SS} = 0\text{ V}$ ,  $T_A = -40\text{ }^\circ\text{C}$  to  $+85\text{ }^\circ\text{C}$ )

Parameter	Symbol	Pin	Value			Units	Remarks
			Min.	Typ.	Max.		
Oscillation frequency	$f_c$	X0, X1	3	—	16	MHz	
	$f_{CL}$	X0A, X1A	—	32.768	—	kHz	
Oscillation cycle time	$t_{CYL}$	X0, X1	62.5	—	333	ns	
	$t_{LCYL}$	X0A, X1A	—	30.5	—	$\mu\text{s}$	
Frequency deviation with PLL *	$\Delta f$	—	—	—	5	%	
Input clock pulse width	$P_{WH}, P_{WL}$	X0	10	—	—	ns	Duty ratio is about 30 to 70%.
	$P_{WLH}, P_{WLL}$	X0A	—	15.2	—	$\mu\text{s}$	
Input clock rise and fall time	$t_{CR}, t_{CF}$	X0	—	—	5	ns	When using external clock
Machine clock frequency	$f_{CP}$	—	1.5	—	16	MHz	When using main clock
	$f_{LCP}$	—	—	8.192	—	kHz	When using sub-clock
Machine clock cycle time	$t_{CP}$	—	62.5	—	666	ns	When using main clock
	$t_{LCP}$	—	—	122.1	—	$\mu\text{s}$	When using sub-clock

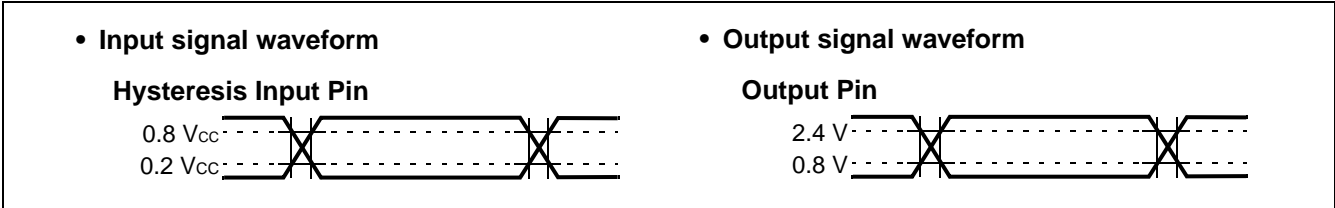
\* : Frequency deviation indicates the maximum frequency difference from the target frequency when using a multiplied clock.



# MB90540/545 Series



AC characteristics are set to the measured reference voltage values below.

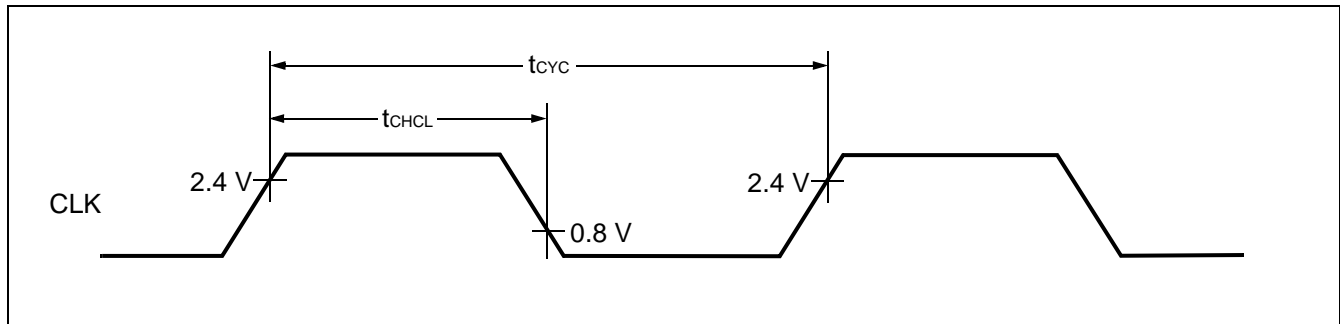


# MB90540/545 Series

## (2) Clock Output Timing

( $V_{CC} = 5.0\text{ V} \pm 10\%$ ,  $V_{SS} = AV_{SS} = 0.0\text{ V}$ ,  $T_A = -40\text{ }^\circ\text{C}$  to  $+85\text{ }^\circ\text{C}$ )

Parameter	Symbol	Pin	Condition	Value		Units	Remarks
				Min.	Max.		
Cycle time	$t_{CYC}$	CLK	$V_{CC} = 5\text{ V} \pm 10\%$	62.5	—	ns	
CLK $\uparrow \Rightarrow$ CLK $\downarrow$	$t_{CHCL}$			20	—	ns	



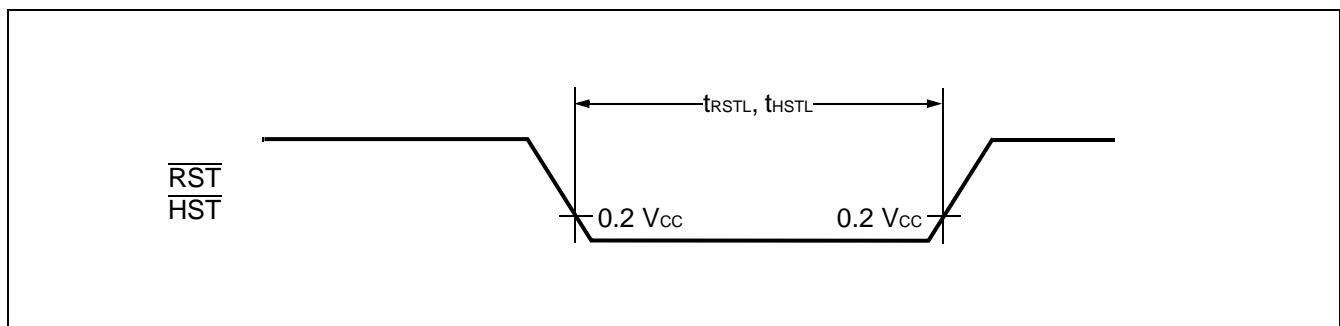
## (3) Reset and Hardware Standby Input

( $V_{CC} = 5.0\text{ V} \pm 10\%$ ,  $V_{SS} = AV_{SS} = 0.0\text{ V}$ ,  $T_A = -40\text{ }^\circ\text{C}$  to  $+85\text{ }^\circ\text{C}$ )

Parameter	Symbol	Pin	Value		Units	Remarks
			Min.	Max.		
Reset input time	$t_{RSTL}$	$\overline{\text{RST}}$	$16 t_{CP}$	—	ns	
Hardware standby input time	$t_{HSTL}$	$\overline{\text{HST}}$	$16 t_{CP}$	—	ns	

" $t_{CP}$ " represents one cycle time of the machine clock.

Any reset can not fully initialize the Flash Memory if it is performing the automatic algorithm.



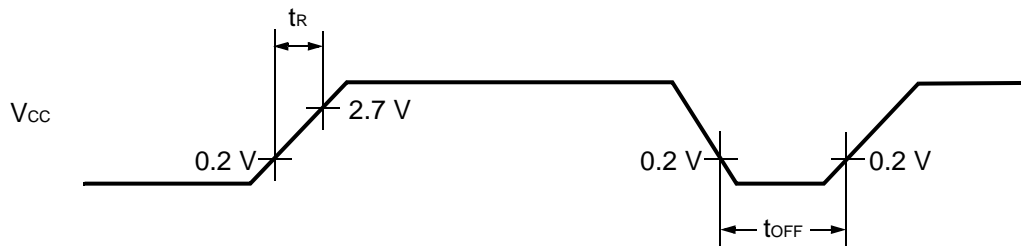


## (4) Power On Reset

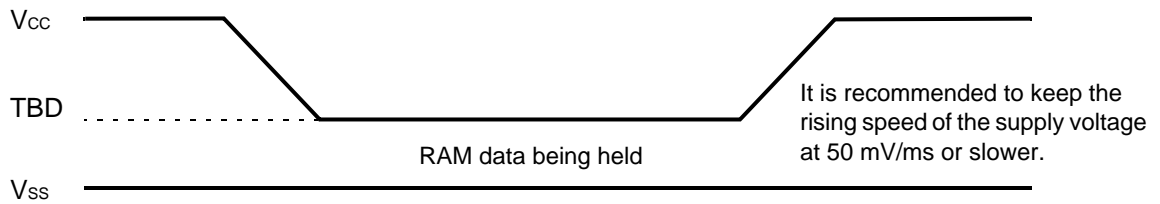
( $V_{CC} = 5.0\text{ V} \pm 10\%$ ,  $V_{SS} = AV_{SS} = 0.0\text{ V}$ ,  $T_A = -40\text{ }^\circ\text{C}$  to  $+85\text{ }^\circ\text{C}$ )

Parameter	Symbol	Pin	Condition	Value		Units	Remarks
				Min.	Max.		
Power on rise time	$t_R$	$V_{CC}$	—	0.05	30	ms	
Power off time	$t_{OFF}$	$V_{CC}$		50	—	ms	Due to repetitive operation

- Note
- $V_{CC}$  must be kept lower than 0.2 V before power-on.
  - The above values are used for creating a power-on reset.
  - Some registers in the device are initialized only upon a power-on reset. To initialize these register, turn on the power supply using the above values.



Sudden changes in the power supply voltage may cause a power-on reset. To change the power supply voltage while the device is in operation, it is recommended to raise the voltage smoothly to suppress fluctuations as shown below. In this case, change the supply voltage with the PLL clock not used. If the voltage drop is 1 V or fewer per second, however, you can use the PLL clock.



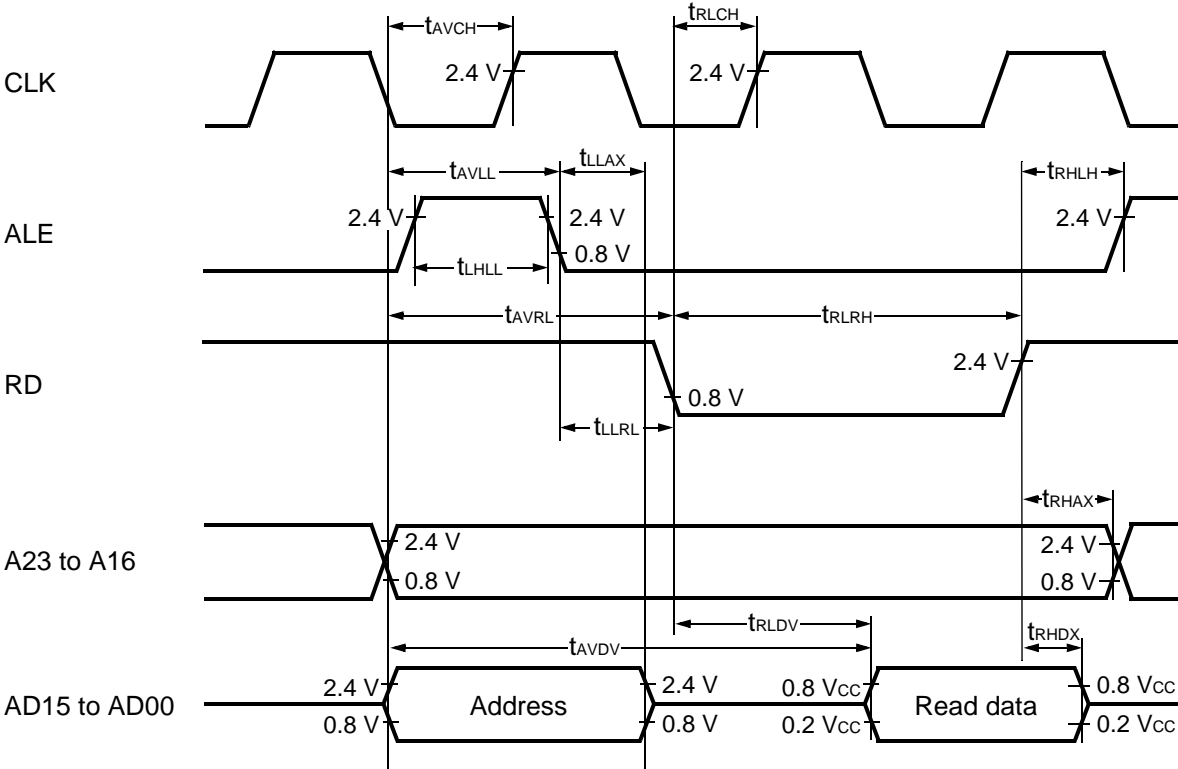
# MB90540/545 Series

## (5) Bus Timing (Read)

( $V_{CC} = 4.5\text{ V to }5.5\text{ V}$ ,  $V_{SS} = 0\text{ V}$ ,  $T_A = -40\text{ }^\circ\text{C to }+85\text{ }^\circ\text{C}$ )

Parameter	Symbol	Pin	Condition	Value		Units	Remarks
				Min.	Max.		
ALE pulse width	$t_{LHLL}$	ALE	—	$t_{CP}/2 - 20$		ns	
Valid address $\Rightarrow$ ALE $\downarrow$ time	$t_{AVLL}$	ALE, A23 to A16, AD15 to AD00		$t_{CP}/2 - 20$	—	ns	
ALE $\downarrow \Rightarrow$ Address valid time	$t_{LLAX}$	ALE, AD15 to AD00		$t_{CP}/2 - 15$	—	ns	
Valid address $\Rightarrow \overline{RD} \downarrow$ time	$t_{AVRL}$	A23 to A16, AD15 to AD00, $\overline{RD}$		$t_{CP} - 15$	—	ns	
Valid address $\Rightarrow$ Valid data input	$t_{AVDV}$	A23 to A16, AD15 to AD00		—	$5 t_{CP}/2 - 60$	ns	
$\overline{RD}$ pulse width	$t_{RLRH}$	$\overline{RD}$		$3 t_{CP}/2 - 20$	—	ns	
$\overline{RD} \downarrow \Rightarrow$ Valid data input	$t_{RLDV}$	$\overline{RD}$ , AD15 to AD00		—	$3 t_{CP}/2 - 60$	ns	
$\overline{RD} \uparrow \Rightarrow$ Data hold time	$t_{RHDX}$	$\overline{RD}$ , AD15 to AD00		0	—	ns	
$\overline{RD} \downarrow \Rightarrow$ ALE $\uparrow$ time	$t_{RHLH}$	$\overline{RD}$ , ALE		$t_{CP}/2 - 15$	—	ns	
$\overline{RD} \uparrow \Rightarrow$ Address valid time	$t_{RHAX}$	$\overline{RD}$ , A23 to A16		$t_{CP}/2 - 10$	—	ns	
Valid address $\Rightarrow$ CLK $\uparrow$ time	$t_{AVCH}$	A23 to A16, AD15 to AD00, CLK		$t_{CP}/2 - 20$	—	ns	
$\overline{RD} \downarrow \Rightarrow$ CLK $\uparrow$ time	$t_{RLCH}$	$\overline{RD}$ , CLK		$t_{CP}/2 - 20$	—	ns	
ALE $\downarrow \Rightarrow \overline{RD} \downarrow$ time	$t_{LLRL}$	ALE, $\overline{RD}$		$t_{CP}/2 - 15$	—	ns	

• Bus Timing (Read)

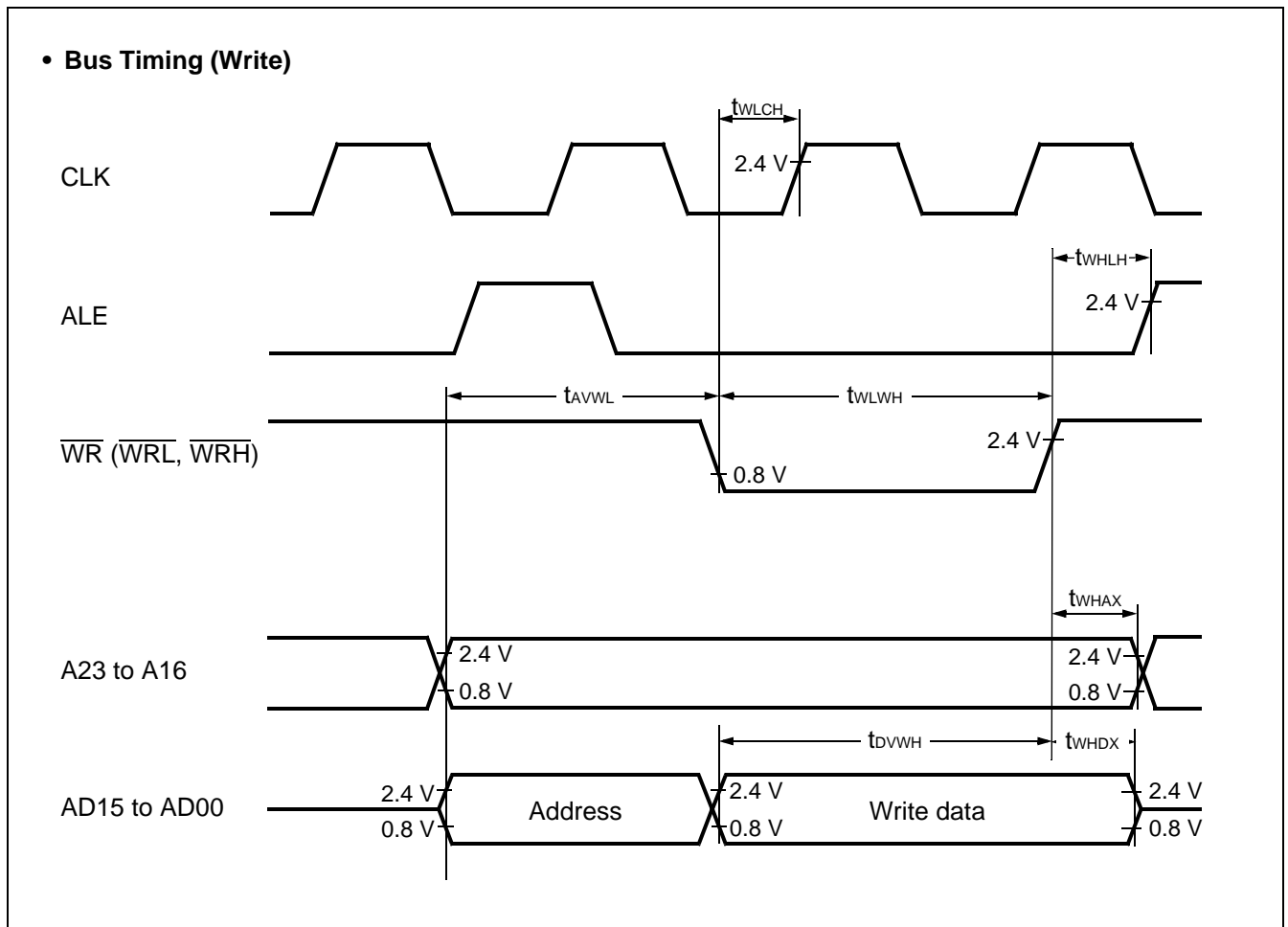


# MB90540/545 Series

## (6) Bus Timing (Write)

( $V_{CC} = 4.5\text{ V to }5.5\text{ V}$ ,  $V_{SS} = 0\text{ V}$ ,  $T_A = -40\text{ }^\circ\text{C to }+85\text{ }^\circ\text{C}$ )

Parameter	Symbol	Pin	Condition	Value		Units	Remarks
				Min.	Max.		
Valid address $\Rightarrow \overline{WR} \downarrow$ time	$t_{AVWL}$	A23 to A16, AD15 to AD00, $\overline{WR}$	—	$t_{CP} - 15$	—	ns	
$\overline{WR}$ pulse width	$t_{WLWH}$	$\overline{WR}$		$3 t_{CP}/2 - 20$	—	ns	
Valid data output $\Rightarrow \overline{WR} \uparrow$ time	$t_{DVWH}$	AD15 to AD00, $\overline{WR}$		$3 t_{CP}/2 - 20$	—	ns	
$\overline{WR} \uparrow \Rightarrow$ Data hold time	$t_{WHDX}$	AD15 to AD00, $\overline{WR}$		20	—	ns	
$\overline{WR} \uparrow \Rightarrow$ Address valid time	$t_{WHAX}$	A23 to A16, $\overline{WR}$		$t_{CP}/2 - 10$	—	ns	
$\overline{WR} \uparrow \Rightarrow$ ALE $\uparrow$ time	$t_{WHLH}$	$\overline{WR}$ , ALE		$t_{CP}/2 - 15$	—	ns	
$\overline{WR} \downarrow \Rightarrow$ CLK $\uparrow$ time	$t_{WLCH}$	$\overline{WR}$ , CLK		$t_{CP}/2 - 20$	—	ns	



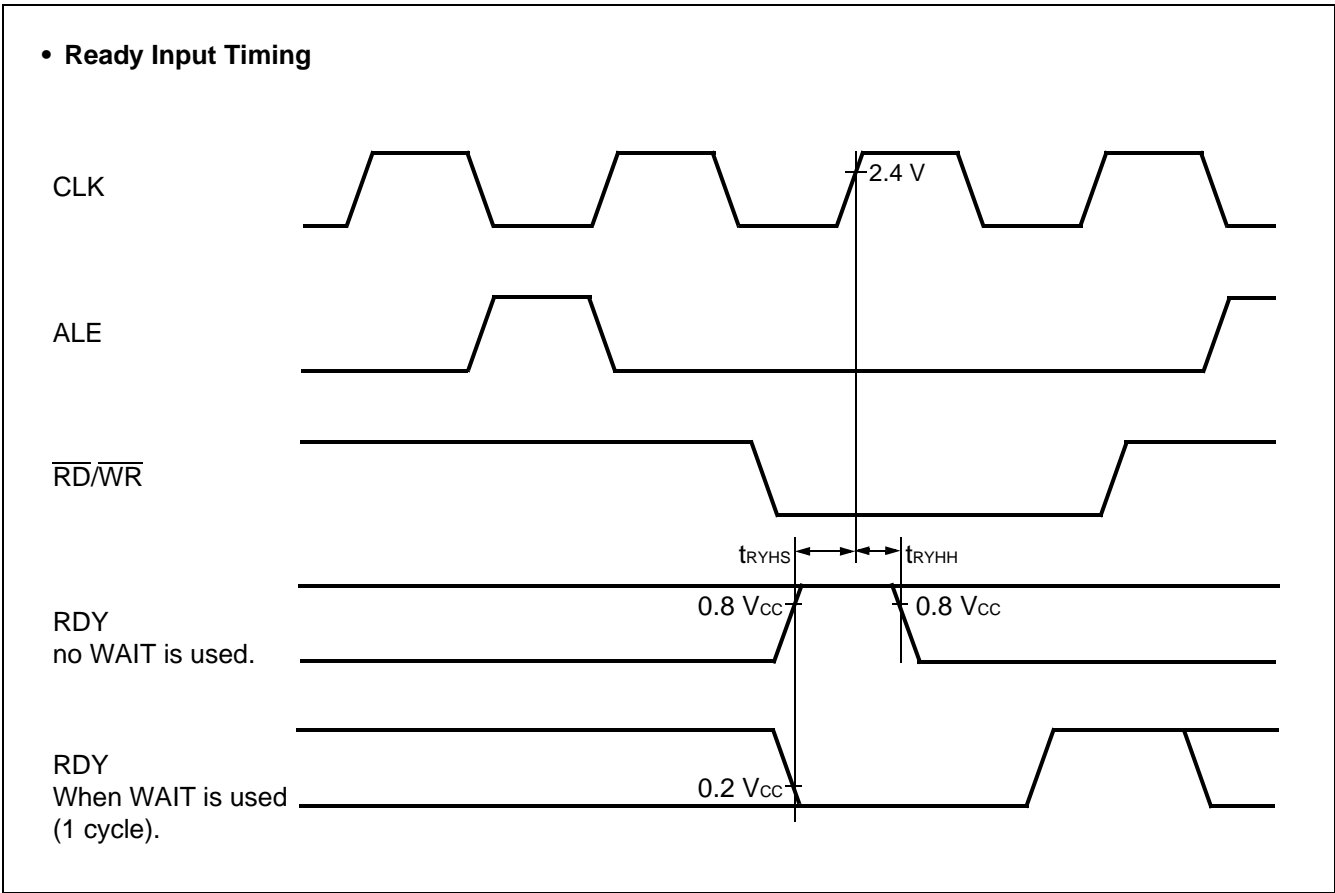
# MB90540/545 Series

## (7) Ready Input Timing

( $V_{CC} = 4.5\text{ V to }5.5\text{ V}$ ,  $V_{SS} = 0\text{ V}$ ,  $T_A = -40\text{ }^\circ\text{C to }+85\text{ }^\circ\text{C}$ )

Parameter	Symbol	Pin	Condition	Value		Units	Remarks
				Min.	Max.		
RDY setup time	$t_{RYHS}$	RDY	—	45	—	ns	
RDY hold time	$t_{RYHH}$	RDY		0	—	ns	

Note: If the RDY setup time is insufficient, use the auto-ready function.



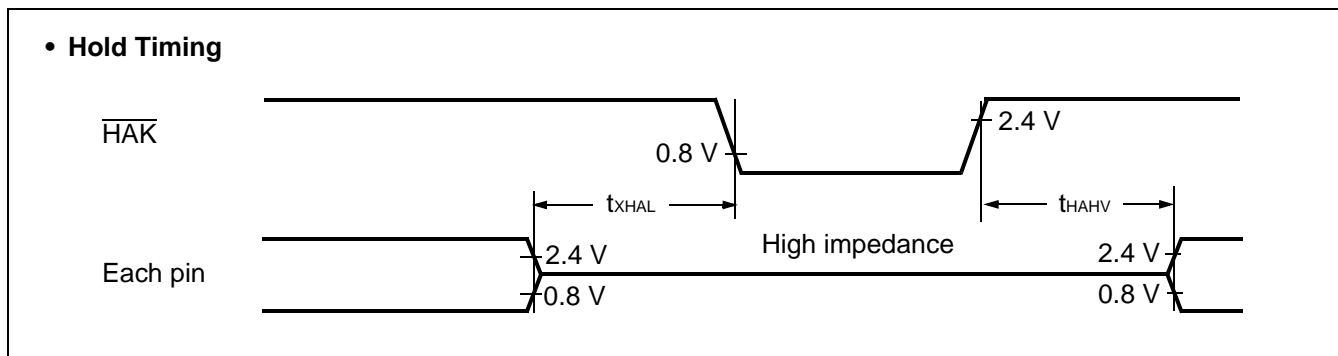
# MB90540/545 Series

## (8) Hold Timing

( $V_{CC} = 4.5\text{ V to }5.5\text{ V}$ ,  $V_{SS} = 0\text{ V}$ ,  $T_A = -40\text{ }^\circ\text{C to }+85\text{ }^\circ\text{C}$ )

Parameter	Symbol	Pin	Condition	Value		Units	Remarks
				Min.	Max.		
Pin floating $\Rightarrow \overline{\text{HAK}} \downarrow$ time	$t_{XHAL}$	$\overline{\text{HAK}}$	—	30	$t_{CP}$	ns	
$\overline{\text{HAK}} \uparrow$ time $\Rightarrow$ Pin valid time	$t_{HAHV}$	$\overline{\text{HAK}}$		$t_{CP}$	$2 t_{CP}$	ns	

Note: There is more than 1 cycle from the time HRQ is read to the time the  $\overline{\text{HAK}}$  is changed.



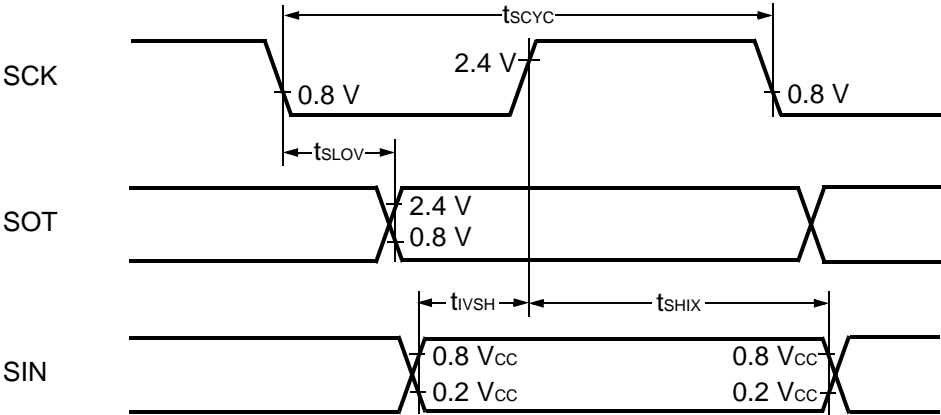
## (9) UART0/1, Serial I/O Timing

( $V_{CC} = 4.5\text{ V to }5.5\text{ V}$ ,  $V_{SS} = 0\text{ V}$ ,  $T_A = -40\text{ }^\circ\text{C to }+85\text{ }^\circ\text{C}$ )

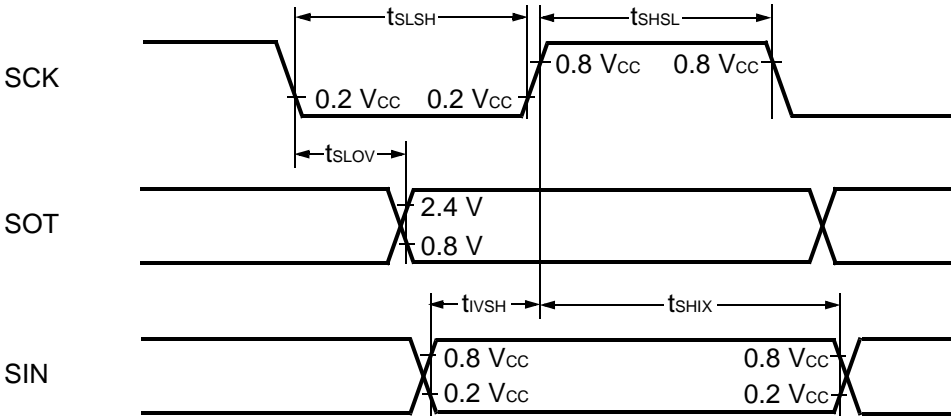
Parameter	Symbol	Pin Symbol	Condition	Value		Units	Remarks
				Min.	Max.		
Serial clock cycle time	$t_{SCYC}$	SCK0 to SCK2	Internal clock operation output pins are $C_L = 80\text{ pF} + 1\text{ TTL}$ .	$8 t_{CP}$	—	ns	
SCK $\downarrow \Rightarrow$ SOT delay time	$t_{SLOV}$	SCK0 to SCK2, SOT0 to SOT2		-80	80	ns	
Valid SIN $\Rightarrow$ SCK $\uparrow$	$t_{IVSH}$	SCK0 to SCK2, SIN0 to SIN2		100	—	ns	
SCK $\uparrow \Rightarrow$ Valid SIN hold time	$t_{SHIX}$	SCK0 to SCK2, SIN0 to SIN2		60	—	ns	
Serial clock "H" pulse width	$t_{SHSL}$	SCK0 to SCK2	External clock operation output pins are $C_L = 80\text{ pF} + 1\text{ TTL}$ .	$4 t_{CP}$	—	ns	
Serial clock "L" pulse width	$t_{LSLH}$	SCK0 to SCK2		$4 t_{CP}$	—	ns	
SCK $\downarrow \Rightarrow$ SOT delay time	$t_{SLOV}$	SCK0 to SCK2, SOT0 to SOT2		—	150	ns	
Valid SIN $\Rightarrow$ SCK $\uparrow$	$t_{IVSH}$	SCK0 to SCK2, SIN0 to SIN2		60	—	ns	
SCK $\uparrow \Rightarrow$ Valid SIN hold time	$t_{SHIX}$	SCK0 to SCK2, SIN0 to SIN2		60	—	ns	

Note: 1. AC characteristic in CLK synchronized mode.  
 2.  $C_L$  is load capacity value of pins when testing.  
 3.  $t_{CP}$  is the machine cycle (Unit: ns).

• Internal Shift Clock Mode



• External Shift Clock Mode



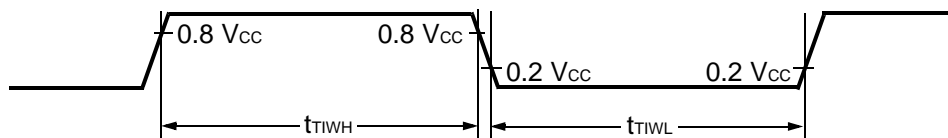
# MB90540/545 Series

## (10) Timer Related Resource Input Timing

( $V_{CC} = 4.5\text{ V to }5.5\text{ V}$ ,  $V_{SS} = 0\text{ V}$ ,  $T_A = -40\text{ }^\circ\text{C to }+85\text{ }^\circ\text{C}$ )

Parameter	Symbol	Pin	Condition	Value		Units	Remarks
				Min.	Max.		
Input pulse width	$t_{TIWH}$	TIN0, TIN1	—	4 $t_{CP}$	—	ns	
	$t_{TIWL}$	IN0 to IN7					

### • Timer Input Timing

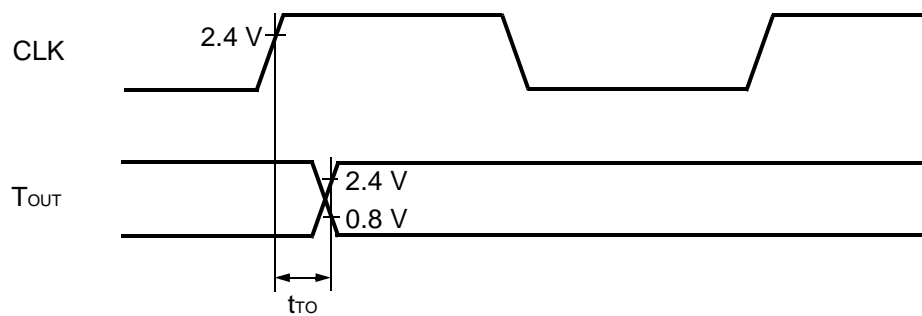


## (11) Timer Related Resource Output Timing

( $V_{CC} = 4.5\text{ V to }5.5\text{ V}$ ,  $V_{SS} = 0\text{ V}$ ,  $T_A = -40\text{ }^\circ\text{C to }+85\text{ }^\circ\text{C}$ )

Parameter	Symbol	Pin	Condition	Value		Units	Remarks
				Min.	Max.		
CLK $\uparrow$ $\Rightarrow$ $T_{OUT}$ change time	$t_{TO}$	TOT0 to TOT1, PPG0 to PPG3	—	30	—	ns	

### • Timer Output Timing



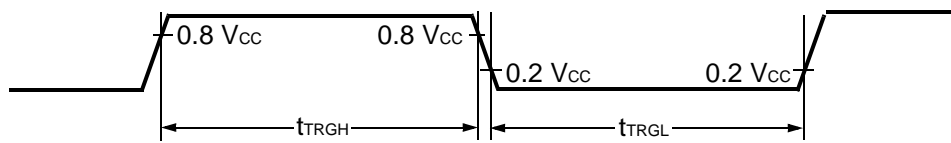


## (12) Trigger Input Timing

( $V_{CC} = 4.5$  to  $5.5$  V,  $V_{SS} = 0$  V,  $T_A = -40$  °C to  $+85$  °C)

Parameter	Symbol	Pin	Condition	Value		Units	Remarks
				Min.	Max.		
Input pulse width	$t_{TRGH}$ $t_{TRGL}$	INT0 to INT7, ADTG	—	5 $t_{CP}$	—	ns	

### • Trigger Input Timing



# MB90540/545 Series

## 5. A/D Converter

( $V_{CC} = AV_{CC} = 5.0 V \pm 10\%$ ,  $V_{SS} = AV_{SS} = 0 V$ ,  $3.0 V \leq AVRH - AVRL$ ,  $T_A = -40\text{ }^\circ\text{C}$  to  $+85\text{ }^\circ\text{C}$ )

Parameter	Symbol	Pin	Rated Value			Units	Remarks
			Min.	Typ.	Max.		
Resolution	—	—	—		10	bit	
Conversion error	—	—	—	—	$\pm 5.0$	LSB	
Nonlinearity error	—	—	—	—	$\pm 2.5$	LSB	
Differential nonlinearity error	—	—	—	—	$\pm 1.9$	LSB	
Zero reading voltage	$V_{OT}$	AN0 to AN7	$AVRL - 3.5$	$AVRL + 0.5$	$AVRL + 4.5$	mV	
Full scale reading voltage	$V_{FST}$	AN0 to AN7	$AVRH - 6.5$	$AVRH - 1.5$	$AVRH + 1.5$	mV	
Conversion time	—	—	—	$352t_{CP}$	—	ns	
Sampling time	—	—	—	$64t_{CP}$	—	ns	
Analog port input current	$I_{AIN}$	AN0 to AN7	-10	—	10	$\mu\text{A}$	
Analog input voltage range	$V_{AIN}$	AN0 to AN7	AVRL	—	AVRH	V	
Reference voltage range	—	AVRH	$AVRL + 2.7$	—	$AV_{CC}$	V	
	—	AVRL	0	—	$AVRH - 2.7$	V	
Power supply current	$I_A$	$AV_{CC}$	—	5	—	mA	
	$I_{AH}$	$AV_{CC}$	—	—	5	$\mu\text{A}$	*
Reference voltage current	$I_R$	AVRH	200	400	600	$\mu\text{A}$	
	$I_{RH}$	AVRH	—	—	5	$\mu\text{A}$	*
Offset between input channels	—	AN0 to AN7	—	—	4	LSB	

\*: When not using an A/D converter, this is the current ( $V_{CC} = AV_{CC} = AVRH = 5.0 V$ ) when the CPU is stopped.

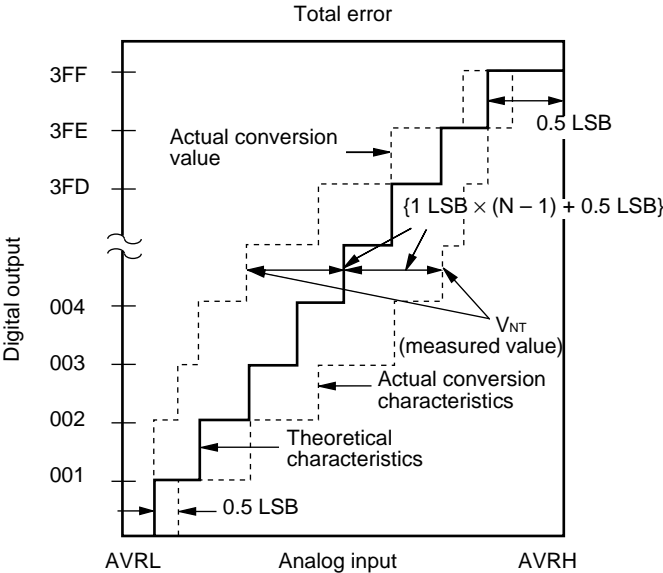
## 6. A/D Converter Glossary

**Resolution:** Analog changes that are identifiable with the A/D converter

**Linearity error:** The deviation of the straight line connecting the zero transition point (“00 0000 0000” ↔ “00 0000 0001”) with the full-scale transition point (“11 1111 1110” ↔ “11 1111 1111”) from actual conversion characteristics

**Differential linearity error:** The deviation of input voltage needed to change the output code by 1 LSB from the theoretical value

**Total error:** The total error is defined as a difference between the actual value and the theoretical value, which includes zero-transition error/full-scale transition error and linearity error.



$$1 \text{ LSB} = (\text{Theoretical value}) \frac{\text{AVRH} - \text{AVRL}}{1024} \text{ [V]}$$

$$\text{Total error for digital output } N = \frac{V_{NT} - \{1 \text{ LSB} \times (N - 1) + 0.5 \text{ LSB}\}}{1 \text{ LSB}} \text{ [LSB]}$$

$$V_{0T} (\text{Theoretical value}) = \text{AVRL} + 0.5 \text{ LSB [V]}$$

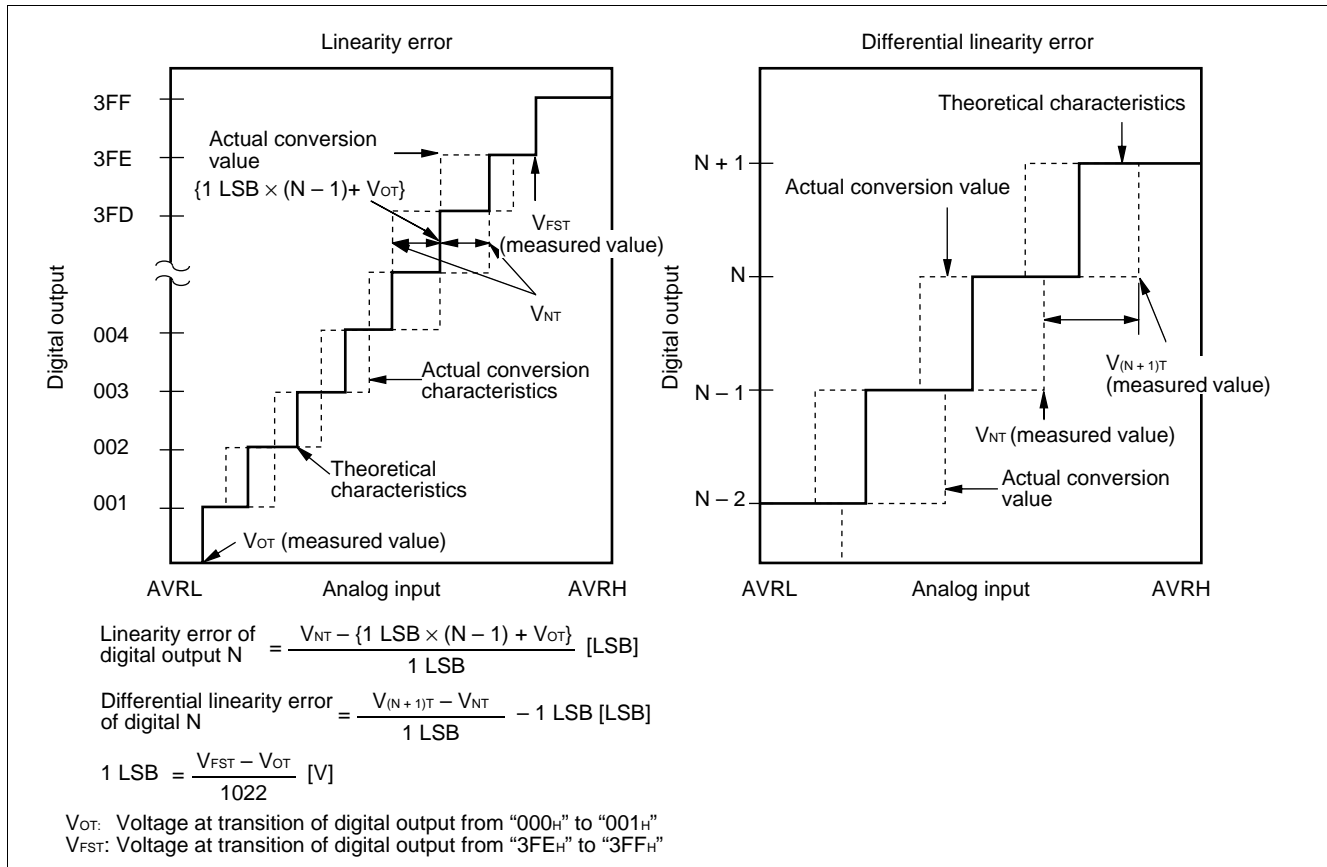
$V_{NT}$ : Voltage at a transition of digital output from (N - 1) to N

$$V_{FST} (\text{Theoretical value}) = \text{AVRH} - 1.5 \text{ LSB [V]}$$

(Continued)

# MB90540/545 Series

(Continued)



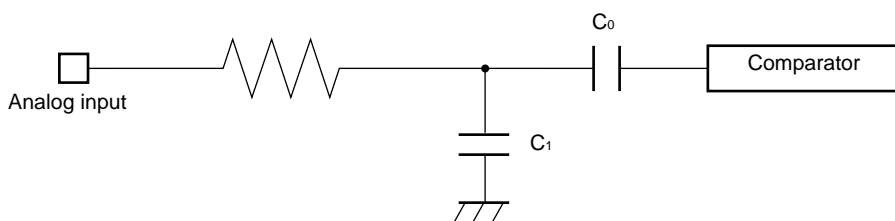
## 7. Notes on Using A/D Converter

Select the output impedance value for the external circuit of analog input according to the following conditions, :

- Output impedance values of the external circuit of 15 kΩ or lower are recommended.
- When capacitors are connected to external pins, the capacitance of several thousand times the internal capacitor value is recommended to minimized the effect of voltage distribution between the external capacitor and internal capacitor.

When the output impedance of the external circuit is too high, the sampling period for analog voltages may not be sufficient (sampling period = 4.00 μs @ machine clock of 16 MHz).

### • Equipment of analog input circuit model



Note: Listed values must be considered as standards.

### • Error

The smaller the  $|AVRH - AVRL|$ , the greater the error would become relatively.

# MB90540/545 Series

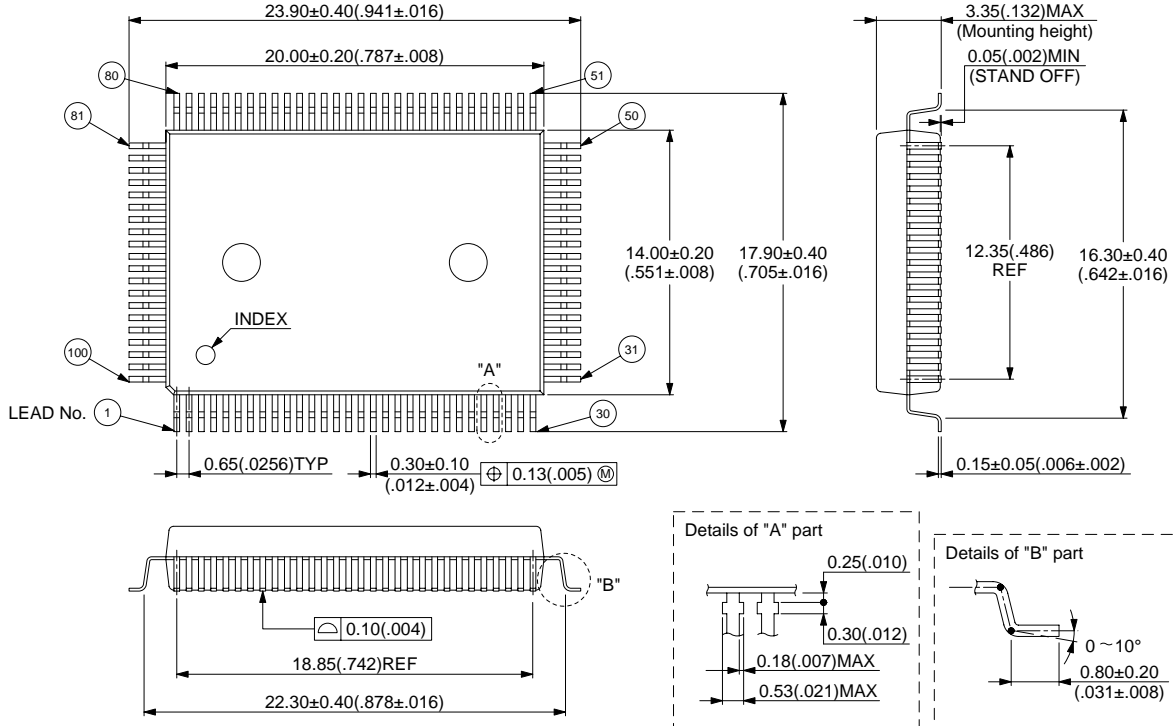
## ■ ORDERING INFORMATION

Part number	Package	Remarks
MB90F543PF MB90F549PF	100-pin Plastic QFP (FPT-100P-M06)	
MB90V540CR	256-pin Ceramic PGA (PGA-256C-A01)	For evaluation

# MB90540/545 Series

## PACKAGE DIMENSIONS

100-pin Plastic QFP  
(FPT-100P-M06)

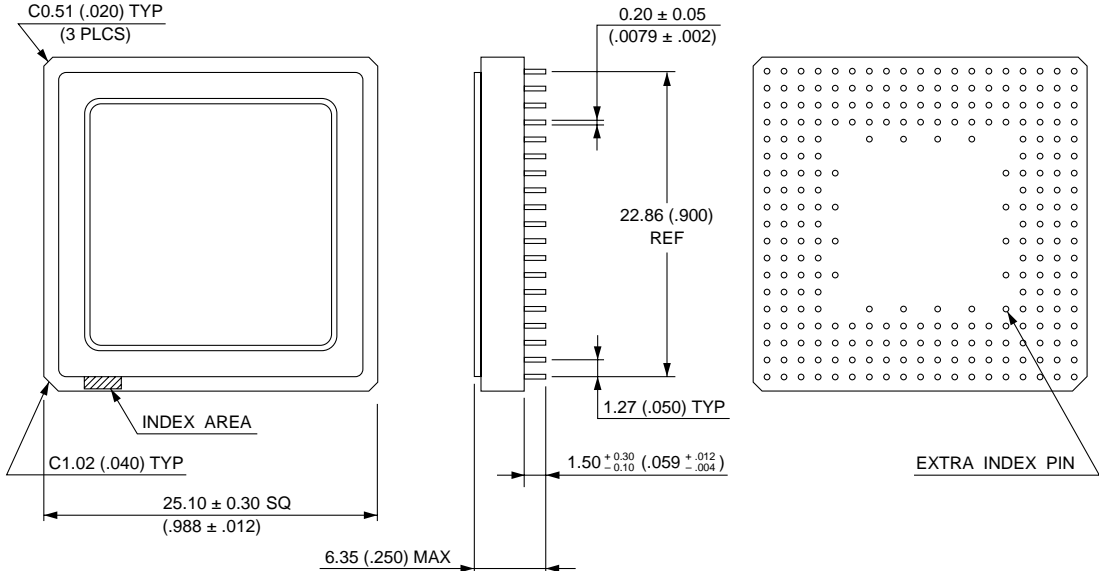


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Dimensions in mm (inches)

# MB90540/545 Series

250-pin Ceramic PGA  
(PGA-256C-A01)



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Dimensions in mm (inches)

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