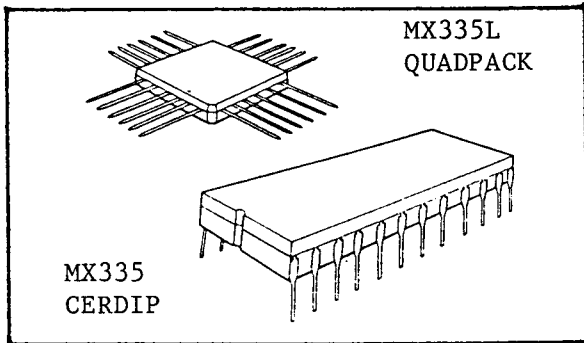


MX335
MX335L

Preliminary
January, 1984

CTCSS ENCODER/DECODER



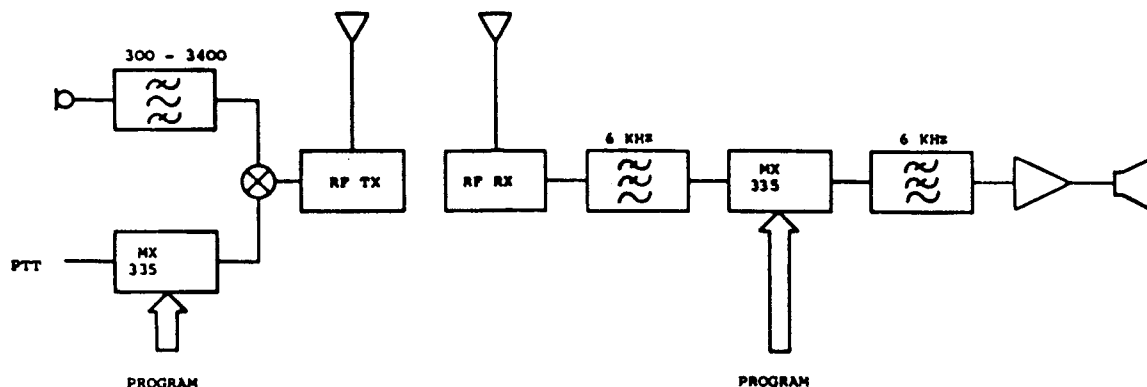
Features:

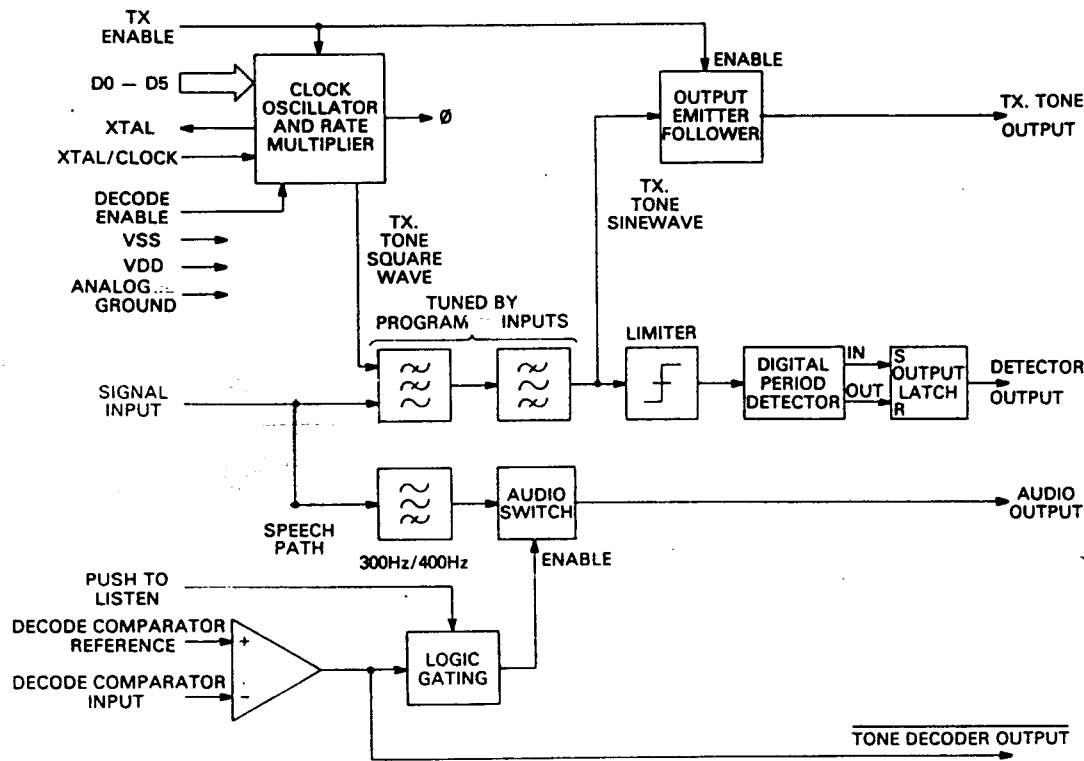
- * Encodes & Decodes 38 CTCSS Tones
- * On-Chip HPF Attenuates Tones 40 dB
- * Meets EIA RS220A (USA), MPT 1306 (UK)
- * Programmable Tones, Crystal Controlled
- * Choice of Quadpack or DIP Packages

CTCSS Operation:

In Continuous Tone-Control Squelch Systems (CTCSS), a radio's voice modulation is multiplexed continuously with a discrete "subaudible" tone. Associated receivers demodulate the tone/voice mixture, decoding the tone to unmute the speaker. Thirty-eight receiver subgroups, may then be segregated by their discrete CTCSS tone assignments. Thirty-seven tones in the 67-250Hz range are established by EIA RS220A standard, but in practice a 38th tone at 97.4Hz is commonly used. Typically, a microphone "hookswitch" is used to unmute the speaker for channel monitoring prior to the origination of calls.

Transmitter microphone audio should be rolled off below 300Hz to prevent voice from falsing the CTCSS Decoder. And, to reduce the audibility of the tone in speech, its modulation index should be held to $\frac{1}{4}$ th that of speech--down 10 to 15 dB. A further 40 dB attenuation is provided on-chip by a fifth order high pass filter for a net end-to-end reduction of at least 50 dB. The use of carrier squelch is beneficial in reducing CTCSS Decoder falsing due to in-band components present in white noise.



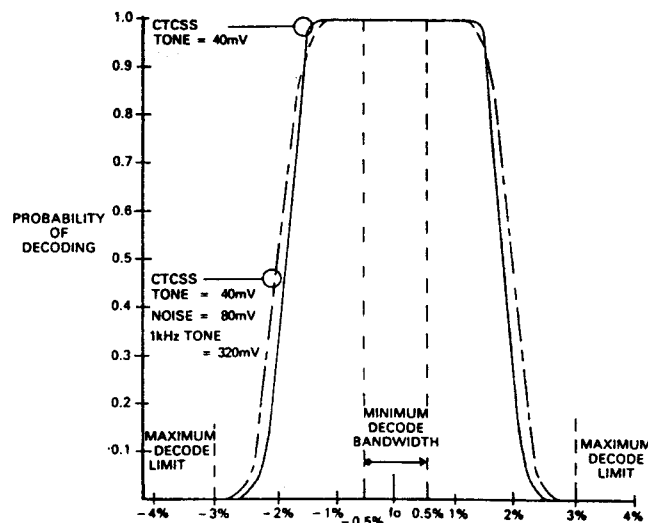


MX335 Operation:

Figure 2. Functional Block Diagram

Tones are detected in four stages. Switched-capacitor elements, tuned by the code programmed at D0-D5, filter the input signal. Their output is squared by the limiter. The period of the resulting squarewave is then measured by digital techniques, also under D0-D5 control, to set or reset an output latch. This output is externally integrated and input to the comparator. When the integral voltage exceeds a preset reference the TONE DECODER OUTPUT switches low and speech is output through the high pass filter.

Figure 3. Typical Decode Bandwidth



The resulting detector bandwidth is expressed in figure 3 as a typical decode probability against the input frequency, (f_0) programmed. The min/max decode limits are those specified by CTCSS convention. The effect of noise and speech (1kHz @ 320mVRMS) is shown by the curve with a broken line.

Figure 4. Decoder Response/Deresponse Sequence

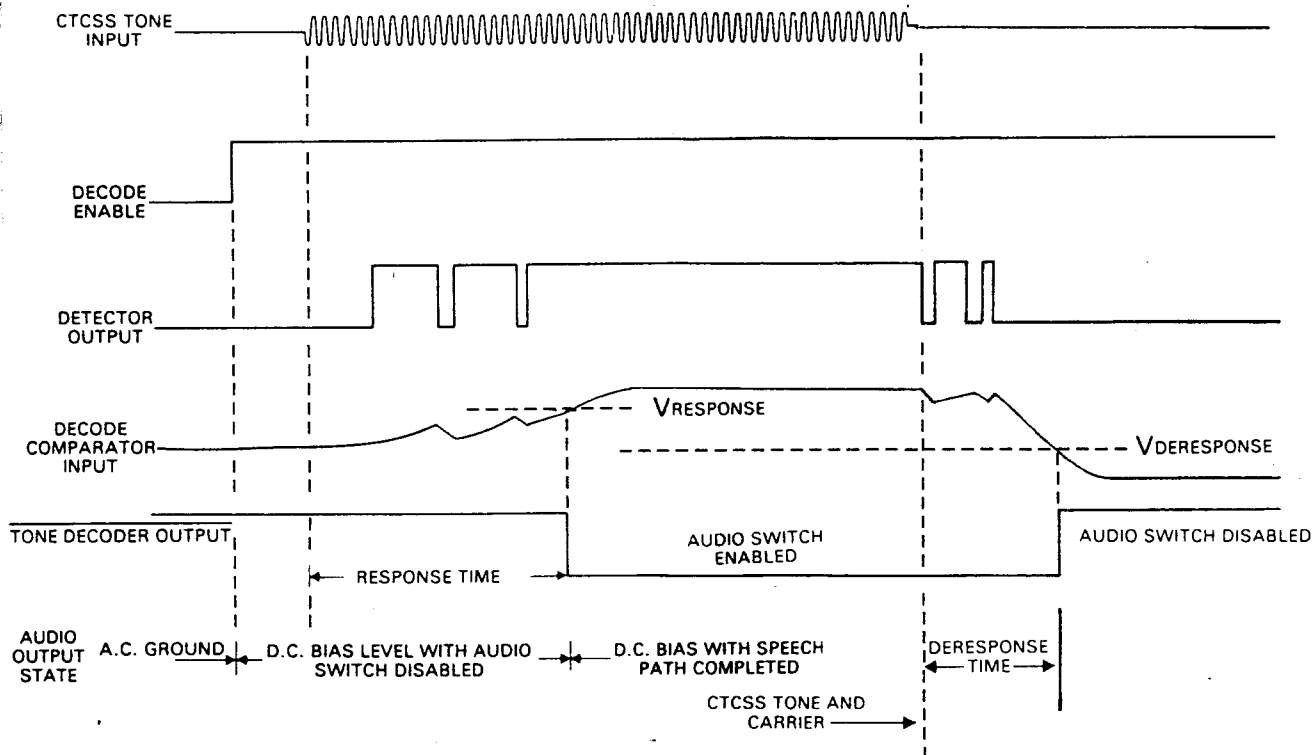
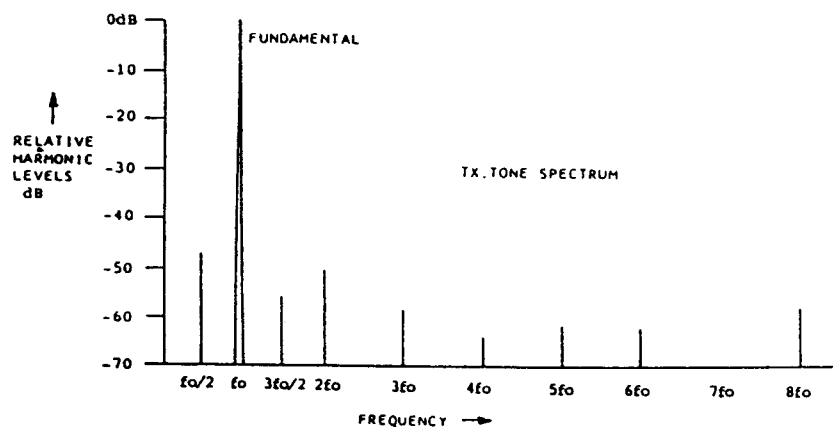


Figure 4 is a typical decoder response and deresponse sequence. As shown the Decoder is being enabled by a Carrier Detect Logic Level. This protects the Decoder from white noise when no carrier is present while also reducing quiescent current drain to the minimum. Note that a Logic 1 on the DECODE ENABLE line causes the Audio Output to switch from VSS to $V_{dd}/2$, establishing an analog ground reference.

The deresponse sequence shown presumes that the transmitting station's CTCSS Tone is removed prior to the termination of the RF carrier in a simplex release-to-listen exchange. The timing of this sequence avoids a "squelch tail" by muting the speaker before the onrush of white noise.

An alternative approach in common practice uses a phase reversal technique. Instead of terminating the tone, its phase is reversed the transmitting station just before the carrier is terminated. The MX335 responds to the phase reversal, blanking the squelch tail.

Figure 5. Tx Tone Spectrum



A logic 0 on the TX ENABLE line switches the MX335 out of receive into a transmit mode irrespective of the logic state on the DECODE ENABLE INPUT. A low distortion sinewave is generated on the TX TONE OUTPUT (an emitter follower able to source 1mW into a 600 ohm load). Invalid programs produce a 4081Hz output frequency.

Figure 6. HPF Frequency Response

The frequency response of the high pass filter in the speech path is shown in Figure 6. The programming of tone 186.2Hz or lower produces the response of the solid line. The dashed line results from programming tones above 186.2Hz. (Input level set to -6 dBV for Figure 6)

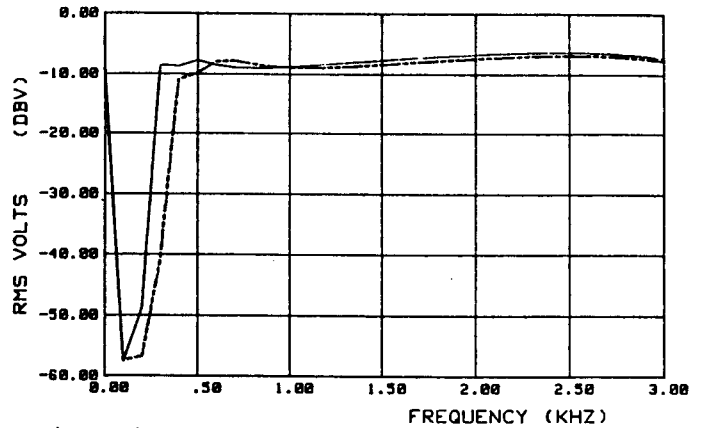
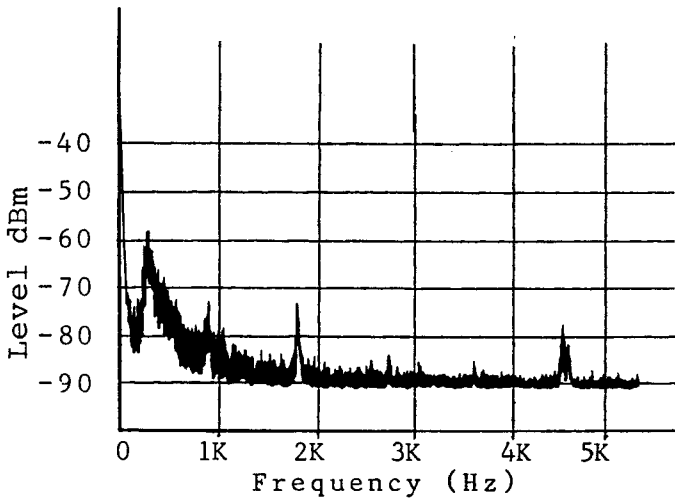


Figure 7. Output Noise Spectrum

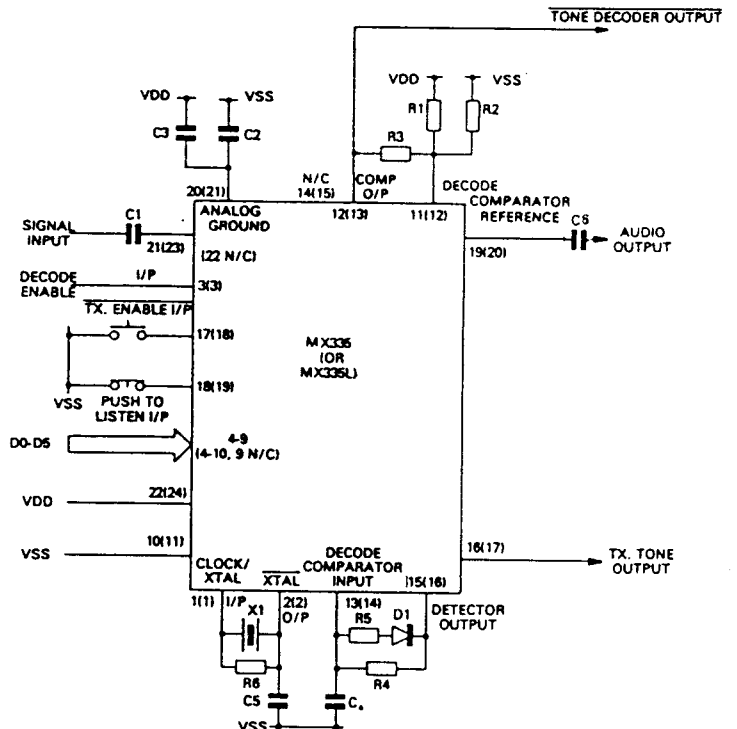


Unwanted spectral components, characteristic of switched-capacitor filters, appear on the AUDIO OUTPUT, see Figure 7. The majority of these are attenuated by the roll-off inherent in most radio audio amplifiers and are therefore unnoticed. A simple low pass filter comprising a 22k ohm resistor and 0.001 mfd capacitor can be added if due allowance is made for insertion loss.

Figure 8. Component Connections

External Components

Component	Value	Tolerance
R1	43kΩ	10%
R2	56kΩ	10%
R3	43kΩ	10%
R4	820kΩ	5%
R5	100kΩ	5%
R6	1MΩ	10%
C1	0.01μF	20%
C2	0.47μF	20%
C3	0.47μF	20%
C4	0.1μF	10%
C5	33pF	20%
C6	1.0μF	20%
X1	1MHz quartz	
D1	1N914 or similar	

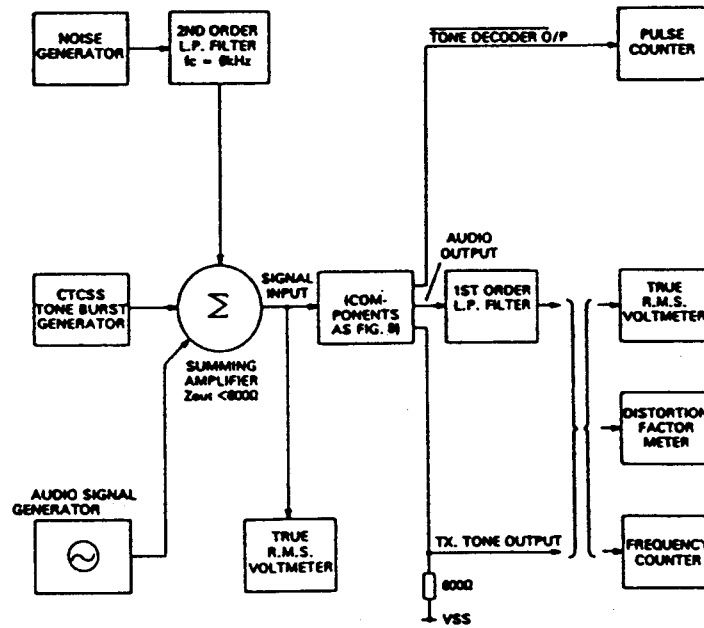


Pin	FUNCTION	Pin
1	1MHz XTAL INPUT: Can also be used to apply an externally derived 1MHz clock input (Clock I/P). The external crystal determines the frequency accuracy of all internal functions.	1
2	$\overline{\text{XTAL OSCILLATOR OUTPUT}}$: (Clock O/P).	2
3	DECODE ENABLE INPUT. A logic 0 applied to this input will disable the decoder. This can be connected to carrier squelch, if required.	3
4	D5: These six data input lines (D0-D5) are used to program the encode/	4
5	D4: decode tone frequencies and are internally pulled high to VDD via	5
6	D3: resistors.	6
7	D2:	7
8	D1:	8
-	No connection.	9
9	D0:	10
10	VSS: Negative supply.	11
11	DECODE COMPARATOR REF: A split resistor network connected to this input sets the threshold level of the comparator. An additional resistor connected between this input and the comparator output allows for hysteresis which reduces jitter under marginal conditions.	12
12	$\overline{\text{TONE DECODER O/P}}$: This is the output of the comparator used to open the analog gate and can also be used to flag the successful detection of the correct CTCSS tone. NOTE: This output is active LOW (for decode).	13
13	DECODE COMPARATOR I/P: The tone detector output, when integrated, is applied to this input. A voltage, present at this input, which is higher than the threshold voltage (Pin 11) will cause the comparator output to go low and hence open the audio gate, i.e. indicating a successful decode.	14
14	No connection.	15
15	DETECTOR OUTPUT: This logic output is set high by the successful detection of the correct CTCSS tone. To avoid any chatter on this output being superimposed on the audio output, this output is integrated and then applied to the comparator input.	16
16	TX TONE O/P: The generated sub-audible tone sine wave is transmitted from this output.	17
17	$\overline{\text{TX ENABLE I/P}}$: A logic 0 applied to this input will enable the transmitter.	18
18	PUSH TO LISTEN I/P: This input is internally pulled to VDD. Normally this input would be externally tied to VSS for normal decode operation. Open circuiting this input will manually override the decoder and open the audio gate.	19
19	AUDIO O/P: Should be capacitively coupled to Audio Amplifier.	20
20	ANALOG GROUND: Externally decoupled by C ₂ and C ₃ .	21
-	No connection.	22
21	SIGNAL INPUT: Signals above 6KHz should be externally attenuated by a 6KHz 2 pole LPF. C ₁ A.C. couples the signals into the device. To avoid injecting unwanted signals into this pin, keep wiring short.	23
22	VDD: Positive supply..	24

Truth Table Code Programming

Nominal Freq. (Hz)	MX335 Frequency	$\Delta f\%$	Program D ₀	D ₁	D ₂	D ₃	D ₄	D ₅	Nominal Freq. (Hz)	MX335 Frequency	$\Delta f\%$	Program D ₀	D ₁	D ₂	D ₃	D ₄	D ₅
67.0	67.05	+0.07	1	1	1	1	1	1	131.8	131.67	-0.10	1	0	0	1	0	0
71.9	71.90	0.0	1	1	1	1	1	0	136.5	136.61	+0.08	0	0	0	1	1	0
74.4	74.35	-0.07	0	1	1	1	1	1	141.3	141.32	+0.02	0	0	0	1	0	0
77.0	76.96	-0.05	1	1	1	1	0	0	146.2	146.37	+0.12	1	1	1	0	1	0
79.7	79.77	+0.09	1	0	1	1	1	1	151.4	151.09	-0.20	1	1	1	0	0	0
82.5	82.59	+0.10	0	1	1	1	1	0	156.7	156.88	+0.11	0	1	1	0	1	0
85.4	85.38	-0.02	0	0	1	1	1	1	162.2	162.31	+0.07	0	1	1	0	0	0
88.5	88.61	+0.13	0	1	1	1	0	0	167.9	168.14	+0.14	1	0	1	0	1	0
91.5	91.58	+0.09	1	1	0	1	1	1	173.8	173.48	-0.19	1	0	1	0	0	0
94.8	94.76	-0.04	1	0	1	1	1	0	179.9	180.15	+0.14	0	0	1	0	1	0
97.4	97.29	-0.11	0	1	0	1	1	1	186.2	186.29	+0.05	0	0	1	0	0	0
100.0	99.96	-0.04	1	0	1	1	0	0	192.8	192.86	+0.03	1	1	0	0	1	0
103.5	103.43	-0.07	0	0	1	1	1	0	203.5	203.65	+0.07	1	1	0	0	0	0
107.2	107.15	-0.05	0	0	1	1	0	0	210.7	210.17	-0.25	0	1	0	0	1	0
110.9	110.77	-0.12	1	1	0	1	1	0	218.1	218.58	+0.22	0	1	0	0	0	0
114.8	114.64	-0.14	1	1	0	1	0	0	225.7	226.12	+0.18	1	0	0	0	1	0
118.8	118.80	0.0	0	1	0	1	1	0	233.6	234.19	+0.25	1	0	0	0	0	0
123.0	122.80	-0.17	0	1	0	1	0	0	241.8	241.08	-0.30	0	0	0	0	1	0
127.3	127.08	-0.17	1	0	0	1	1	0	250.3	250.28	-0.01	0	0	0	0	0	0

Figure 9. Test Set Up



Specifications subject to change without notice.

Specification

Absolute Maximum Ratings

Exceeding the maximum rating can result in device damage. Operation of the device outside the operating limits is not implied.

Supply voltage	-0.3V to 7.0V
Input voltage at any pin (ref VSS = 0V)	-0.3V to (VDD + 0.3V)
Output sink/source current (total)	20mA
Operating temperature range	MX335 -30°C to +85°C
	MX335L -30°C to +70°C
Storage temperature range	MX335 -55°C to 125°C
	MX335L -40°C to +85°C
Maximum device dissipation	100mW

Operating Limits

VDD = 5V, T_A = 25°C, O = 1MHz, Δf_o = 0.

All characteristics measured using the standard test circuit (figure 9) with the following test parameters, and is valid for all tones unless otherwise stated: -

OdB reference	= 300mVRMS
Composite input signal	= OdB 1kHz tone
	- 12dB noise (band limited 6kHz gaussian white noise)
	- 20dB fo CTCSS tone

Characteristic	See Note	Min	Typ	Max	Unit
Static Characteristics					
Supply volts		4.5	5.0	5.5	V
Supply current (decoding)			2.5	-	mA
Supply current (transmitting)			3.5	-	mA
Supply current (standby)			0.6	-	mA
Signal input impedance			3	-	MΩ
Audio output impedance			3	-	kΩ
Input impedance	1	-	500	-	kΩ
Input logic '1'	1	3.5	-	-	V
Input logic '0'	1	-	-	1.5	V
Logic '1' output I _{source} = 0.1mA	2	4.0	-	-	V
Logic '0' output I _{sink} = 0.1 mA	2	-	-	1.0	V
Dynamic Characteristics					
Decoder					
Decode input signal level	3	-20	-	-	dB
Decode response time	3,6	-	-	250	ms
Deresponse time	3,6	-	-	250	ms
Decode selectivity	3	± 0.5	-	± 3	% fo
Encoder					
Tone output level (relative 775mVRMS)		-3	0	-	dB
Tone frequency accuracy (Δf _o error)			± 0.3	-	%fo
Risetime to 90% nominal o/p: fo > 100 Hz	4	-	15	-	ms
fo < 100 Hz	4	-	45	-	ms
Tone output load current			-	5	mA
Total harmonic distortion			2	5	%
Output level variation between tones			0.1	-	dB
Audio Filter					
Total harmonic distortion	5	-	2	5	%
Output noise level (input a.c. short circuit, audio switch enabled)	-	-	-60	-50	dB
Audio Filter (fo < 186Hz)					
Cutoff frequency	-	-	300	-	Hz
Bandpass ripple (300 - 3.4kHz)	5	-2	-	+2	dB
Stopband attenuation (f < 186Hz)	5	36	40	-	dB
Passband gain at 1kHz		-3	-2	-	dB
Audio Filter (fo > 186Hz)					
Cutoff frequency	-	-	410	-	Hz
Bandpass ripple (410 - 3.4kHz)	5	-2	-	+2	dB
Stopband attenuation (f < 250Hz)	5	36	40	-	dB
Passband gain at 1kHz	-	-3	-2	-	dB
Audio switch					
Isolation	5	-	60	-	dB

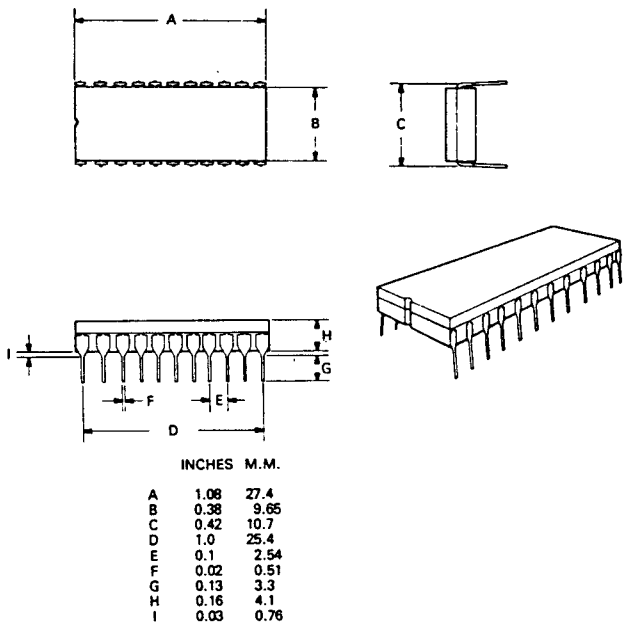
- Notes**
1. Refers to Decode Enable, Tx Enable, PTL, Decode Comparator Input, D0, D1, D2, D3, D4, D5.
 2. Tone Decoder and Detector Outputs.
 3. Composite Signal Test Condition.
 4. Any program tone and R_L = 600
 5. 1kHz Reference = 0dB.
 6. fo ≥ 100 Hz, (for 100 Hz > fo > 67 Hz: t = $\frac{100}{fo (Hz)} \times 250ms$).

DECODE TRUTH TABLE
(Positive Logic)

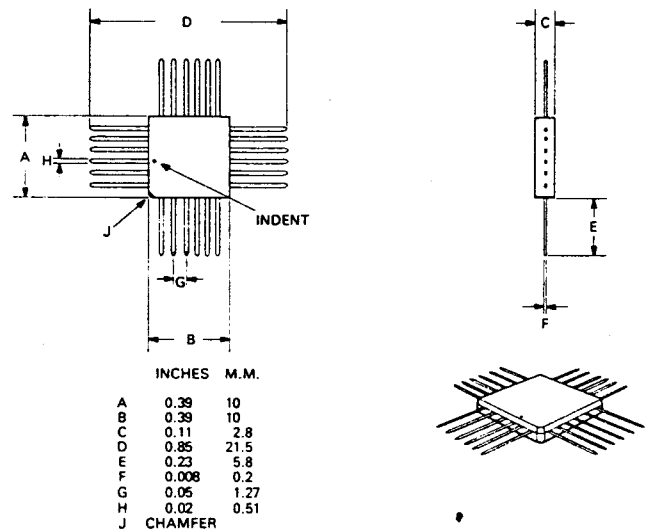
DECODE ENABLE INPUT	TX ENABLE	P.T.L. INPUT	<u>TONE</u> DECODER OUTPUT	AUDIO OUTPUT	TX. TONE OUTPUT	TYP. POWER CONSUMPTION(mA)	COMMENT
0	1	0	1	VDD/2	VSS	0.6	Standby
0	1	1	1	AUDIO	VSS	2.5	Manual channel monitoring
0	0	0	1	VDD/2	Tone	3.5	Encoding programmed tone
0	0	1	1	AUDIO	Tone	3.5	Encoding with high pass filter enabled
1	1	0	0	AUDIO	VSS	2.5	Decoding, valid tone present
1	1	1	0	AUDIO	VSS	2.5	Decoding plus P.T.L. activated
1	0	0	1	VDD/2	Tone	3.5	Simplex Tx
1	0	1	1	AUDIO	Tone	3.5	Simplex Tx
1	1	0	1	VDD/2	VSS	2.5	Valid tone not present
1	1	1	1	AUDIO	VSS	2.5	Valid tone not present

PACKAGE OUTLINES

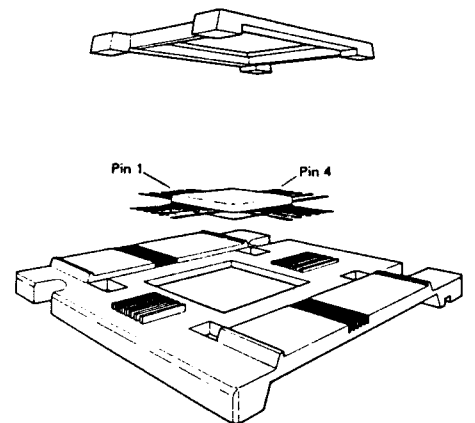
MX335 Cerdip



MX335L Quadpack



Shipping/Test Carrier



Handling Precautions

The MX335/L is a CMOS LSI integrated circuit which includes input protection. However, precautions should be taken to prevent static discharges which can cause damage.



CML Microcircuits

COMMUNICATION SEMICONDUCTORS

CML Product Data

In the process of creating a more global image, the three standard product semiconductor companies of CML Microsystems Plc (*Consumer Microcircuits Limited (UK)*, *MX-COM, Inc (USA)* and *CML Microcircuits (Singapore) Pte Ltd*) have undergone name changes and, whilst maintaining their separate new names (*CML Microcircuits (UK) Ltd*, *CML Microcircuits (USA) Inc* and *CML Microcircuits (Singapore) Pte Ltd*), now operate under the single title **CML Microcircuits**.

These companies are all 100% owned operating companies of the CML Microsystems Plc Group and these changes are purely changes of name and do not change any underlying legal entities and hence will have no effect on any agreements or contacts currently in force.

CML Microcircuits Product Prefix Codes

Until the latter part of 1996, the differentiator between products manufactured and sold from MXCOM, Inc. and Consumer Microcircuits Limited were denoted by the prefixes MX and FX respectively. These products use the same silicon etc. and today still carry the same prefixes. In the latter part of 1996, both companies adopted the common prefix: CMX.

This notification is relevant product information to which it is attached.

CML Microcircuits (USA) [formerly MX-COM, Inc.] Product Textual Marking

On CML Microcircuits (USA) products, the '**MX-COM**' textual logo is being replaced by a '**CML**' textual logo.

Company contact information is as below:



**CML Microcircuits
(UK) Ltd**

COMMUNICATION SEMICONDUCTORS

Oval Park, Langford, Maldon,
Essex, CM9 6WG, England
Tel: +44 (0)1621 875500
Fax: +44 (0)1621 875600
uk.sales@cmlmicro.com
www.cmlmicro.com



**CML Microcircuits
(USA) Inc.**

COMMUNICATION SEMICONDUCTORS

4800 Bethania Station Road,
Winston-Salem, NC 27105, USA
Tel: +1 336 744 5050,
0800 638 5577
Fax: +1 336 744 5054
us.sales@cmlmicro.com
www.cmlmicro.com



**CML Microcircuits
(Singapore) Pte Ltd**

COMMUNICATION SEMICONDUCTORS

No 2 Kallang Pudding Road, 09-05/
06 Mactech Industrial Building,
Singapore 349307
Tel: +65 7450426
Fax: +65 7452917
sg.sales@cmlmicro.com
www.cmlmicro.com