R1610I
Brief Sheet
16-BIT RISC MICROCONTROLLER

1. Features

l CPU Core

- RDC's proprietary RISC architecture
- Five-stage pipeline architecture
- Operation frequency: 100MHz
- Supports an 8K-byte uniform cache
- Supports CPU ID
- Software is compatible with the 80C186 microprocessor

l Bus interface

- 8-bit or 16-bit external bus dynamic access
- Supports a glue-less and simplified 16-bit PCMCIA bus interface

l ROM/RAM/SDRAM Controller and Addressing Space

- Supports 16-bit data bus width
- 16-bit SDRAM control Interface
- 1M addressing space / A[19:0]
- 64K-byte I/O space
- With 8-bit or 16-bit boot ROM bus size
- Supports an independent data / address bus for the external I/O device

l Two Independent DMA Channels

l Interrupt Controller

- Provides 5 maskable external interrupts and 1 non-maskable external interrupt

l General Programmable I/O

- Supports 18 PIO pins
- Programmable chip-select logic for memory or I/O bus cycle decoder

l Counter/Timers

- 3 independent 16-bit timers
- 1 independent programmable watchdog timer

l High Performance UART Ports

- Supports two 16550 UART serial channels with 16-byte FIFO and hardware flow control
- Programmable wait-state generators

l Fast Ethernet MAC Ports

- 1-port Fast Ethernet MAC with MII interface

l Operating Voltage Range

- Core voltage: 2.5V ± 5%
- I/O voltage: 3.3V ± 10%

l Package Information

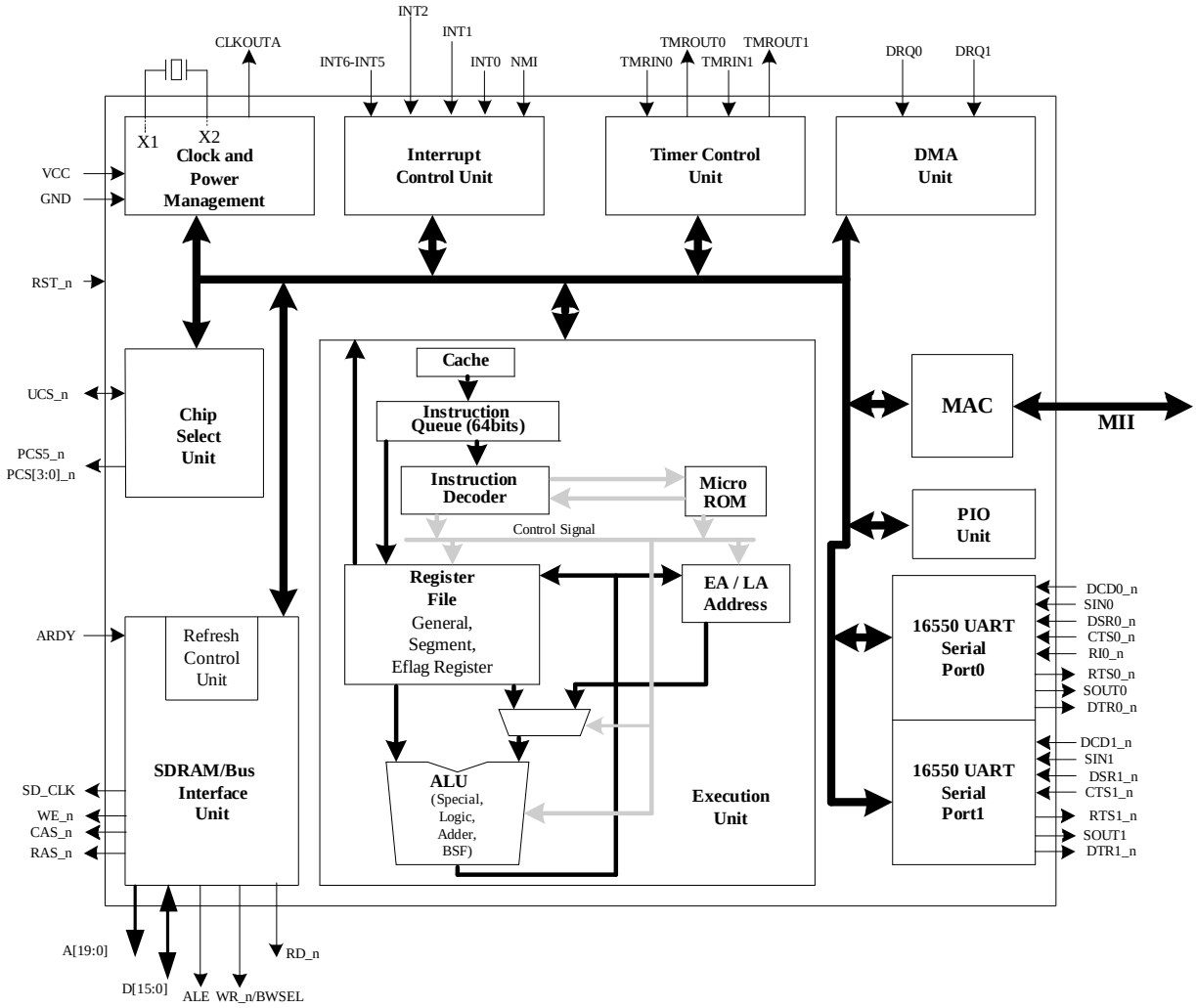
- 128-pin PQFP

l A Product of Industrial Spec

- Operation frequency: 75MHz
- Ambient temperature: -40 ~ 80℃

l A Green Product

2. Block Diagram



3. Package Information

PQFP 128 pins