DATASHEET

Programmable Timing Control Hub™ for Mobile P4™ Systems

954226

Recommended Application:

CK410M Compatible Main Clock

Output Features:

- 2 - 0.7V current-mode differential CPU pairs
- 4 - 0.7V current-mode differential PCI Express* pairs
- 1 - 0.7V current-mode differential CPU/PCI Express selectable pair
- 1 - 0.7V current-mode differential SATA pair
- 1 - 0.7V current-mode differential LCDCLK/PCI Express selectable pair
- 4 - PCI (33MHz)
- 2 - PCICLK_F, (33MHz) free-running
- 1 - USB, 48MHz
- 1 - DOT, 96MHz, 0.7V current differential pair
- 2 - REF, 14.318MHz

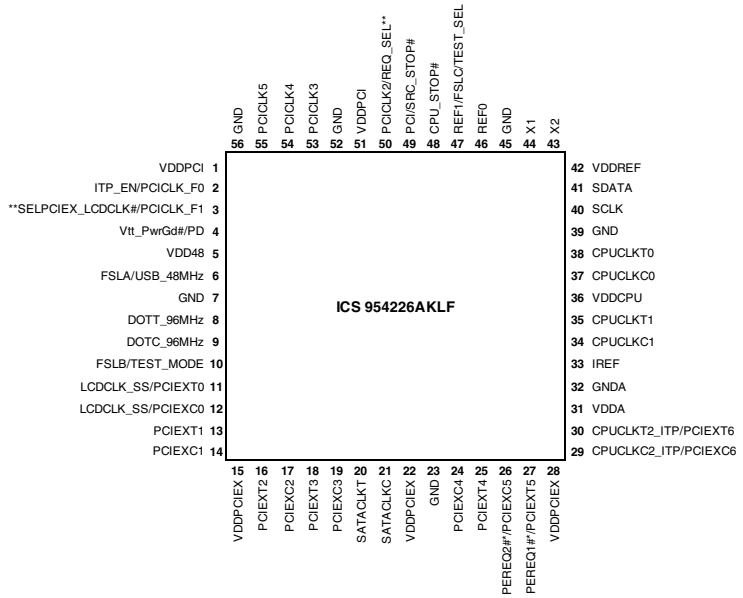
Key Specifications:

- CPU outputs cycle-cycle jitter < 85ps
- PCI Express outputs cycle-cycle jitter < 125ps
- SATA outputs cycle-cycle jitter < 125ps
- PCI outputs cycle-cycle jitter < 500ps
- +/- 300ppm frequency accuracy on CPU, PCI Express and SATA clocks
- +/- 100ppm frequency accuracy on USB clocks

Features/Benefits:

- Supports tight ppm accuracy clocks for Serial-ATA and PCI Express
- Supports programmable spread percentage and frequency
- Uses external 14.318MHz crystal, external crystal load caps are required for frequency tuning
- Supports undriven differential CPU, PCI Express pair in PD for power management.
- PEREQ# pins to support PCI Express and SATA power management.

MLF Pin Configuration

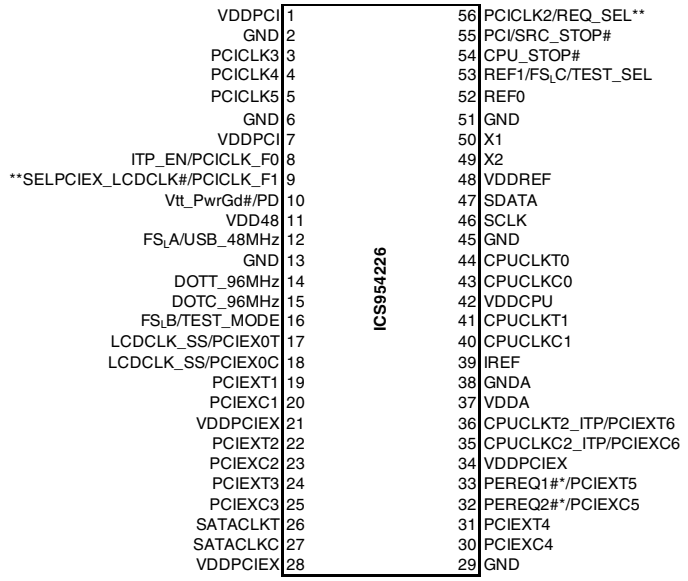


56-MLF

* Internal Pull-Up Resistor

** Internal Pull-Down Resistor

TSSOP Pin Configuration



56-TSSOP

* Internal Pull-Up Resistor

** Internal Pull-Down Resistor

Table 1: Frequency Selection Table

FS_LC B6b2	FS_LB B6b1	FS_LA B6b0	CPU MHz	PCIEX MHz	PCI MHz	REF MHz	USB MHz	DOT MHz	Spread %
0	0	0	266.66	100.00	33.33	14.318	48.00	96.00	0.5% Down
0	0	1	133.33	100.00	33.33	14.318	48.00	96.00	0.5% Down
0	1	0	200.00	100.00	33.33	14.318	48.00	96.00	0.5% Down
0	1	1	166.66	100.00	33.33	14.318	48.00	96.00	0.5% Down
1	0	0	333.33	100.00	33.33	14.318	48.00	96.00	0.5% Down
1	0	1	100.00	100.00	33.33	14.318	48.00	96.00	0.5% Down
1	1	0	400.00	100.00	33.33	14.318	48.00	96.00	0.5% Down
1	1	1	200.00	100.00	33.33	14.318	48.00	96.00	0.5% Down

TSSOP Pin Description

PIN #	PIN NAME	TYPE	DESCRIPTION
1	VDDPCI	PWR	Power supply for PCI clocks, nominal 3.3V
2	GND	PWR	Ground pin.
3	PCICLK3	OUT	PCI clock output.
4	PCICLK4	OUT	PCI clock output.
5	PCICLK5	OUT	PCI clock output.
6	GND	PWR	Ground pin.
7	VDDPCI	PWR	Power supply for PCI clocks, nominal 3.3V
8	ITP_EN/PCICLK_F0	I/O	Free running PCI clock not affected by PCI_STOP# through I2C . ITP_EN: latched input to select pin functionality 1 = CPU_2_ITP pair 0 = PCIEX_6 pair
9	**SELPCIEX_LCDCLK#/PCICLK_F1	I/O	Latched select input for LCDCLK/PCIEX output 0 = LCDCLK, 1 = PCIEX / Free running 3.3V PCI clock output.
10	Vtt_PwrGd#/PD	IN	Vtt_PwrGd# is an active low input used to determine when latched inputs are ready to be sampled. PD is an asynchronous active high input pin used to put the device into a low power state. The internal clocks, PLLs and the crystal oscillator are stopped.
11	VDD48	PWR	Power pin for the 48MHz output.3.3V
12	FSLA/USB_48MHz	I/O	3.3V tolerant input for CPU frequency selection. Refer to input electrical characteristics for Vil_FS and Vih_FS values. / Fixed 48MHz USB clock output. 3.3V.
13	GND	PWR	Ground pin.
14	DOTT_96MHz	OUT	True clock of differential pair for 96.00MHz DOT clock.
15	DOTC_96MHz	OUT	Complement clock of differential pair for 96.00MHz DOT clock.
16	FSLB/TEST_MODE	IN	3.3V tolerant input for CPU frequency selection. Refer to input electrical characteristics for Vil_FS and Vih_FS values. TEST_MODE is a real time input to select between Hi-Z and REF/N divider mode while in test mode. Refer to Test Clarification Table.
17	LCDCLK_SS/PCIEX0T	OUT	True clock of LCDCLK_SS output / True clock of PCI Express differential pair. Selected by SELPCIEX_LCDCLK#
18	LCDCLK_SS/PCIEX0C	OUT	Complementary clock of LCDCLK_SS output / Complementary clock of PCI Express differential pair. Selected by SELPCIEX_LCDCLK#
19	PCIEXT1	OUT	True clock of differential PCI_Express pair.
20	PCIEXC1	OUT	Complement clock of differential PCI_Express pair.
21	VDDPCIEX	PWR	Power supply for PCI Express clocks, nominal 3.3V
22	PCIEXT2	OUT	True clock of differential PCI_Express pair.
23	PCIEXC2	OUT	Complement clock of differential PCI_Express pair.
24	PCIEXT3	OUT	True clock of differential PCI_Express pair.
25	PCIEXC3	OUT	Complement clock of differential PCI_Express pair.
26	SATACLKT	OUT	True clock of differential SATA pair.
27	SATACLKC	OUT	Complement clock of differential SATA pair.
28	VDDPCIEX	PWR	Power supply for PCI Express clocks, nominal 3.3V

TSSOP Pin Description (cont.)

PIN #	PIN NAME	TYPE	DESCRIPTION
29	GND	PWR	Ground pin.
30	PCIEXC4	OUT	Complement clock of differential PCI_Express pair.
31	PCIEXT4	OUT	True clock of differential PCI_Express pair.
32	PEREQ2#*/PCIEXC5	I/O	Real-time input pin that controls SATACLK and PCIEXCLK outputs that are selected through the I2c. 1 = disabled, 0 = enabled. / Complement clock of differential PCI Express output.
33	PEREQ1#*/PCIEXT5	I/O	Real-time input pin that controls SATACLK and PCIEXCLK outputs that are selected through the I2c. 1 = disabled, 0 = enabled. / True clock of differential PCI Express output.
34	VDDPCIEX	PWR	Power supply for PCI Express clocks, nominal 3.3V
35	CPUCLKC2_ITP/PCIEXC6	OUT	Complementary clock of CPU_ITP/PCIEX differential pair CPU_ITP/PCIEX output. These are current mode outputs. External resistors are required for voltage bias. Selected by ITP_EN input.
36	CPUCLKT2_ITP/PCIEXT6	OUT	True clock of differential pair CPU outputs. These are current mode outputs. External resistors are required for voltage bias. / True clock of differential PCIEX pair
37	VDDA	PWR	3.3V power for the PLL core.
38	GNDA	PWR	Ground pin for the PLL core.
39	IREF	OUT	This pin establishes the reference current for the differential current-mode output pairs. This pin requires a fixed precision resistor tied to ground in order to establish the appropriate current. 475 ohms is the standard value.
40	CPUCLKC1	OUT	Complementary clock of differential pair CPU outputs. These are current mode outputs. External resistors are required for voltage bias.
41	CPUCLKT1	OUT	True clock of differential pair CPU outputs. These are current mode outputs. External resistors are required for voltage bias.
42	VDDCPU	PWR	Supply for CPU clocks, 3.3V nominal
43	CPUCLKC0	OUT	Complementary clock of differential pair CPU outputs. These are current mode outputs. External resistors are required for voltage bias.
44	CPUCLKT0	OUT	True clock of differential pair CPU outputs. These are current mode outputs. External resistors are required for voltage bias.
45	GND	PWR	Ground pin.
46	SCLK	IN	Clock pin of SMBus circuitry, 5V tolerant.
47	SDATA	I/O	Data pin for SMBus circuitry, 5V tolerant.
48	VDDREF	PWR	Ref, XTAL power supply, nominal 3.3V
49	X2	OUT	Crystal output, Nominally 14.318MHz
50	X1	IN	Crystal input, Nominally 14.318MHz.
51	GND	PWR	Ground pin.
52	REF0	OUT	14.318 MHz reference clock.
53	REF1/FSLC/TEST_SEL	I/O	14.318 MHz reference clock./ 3.3V tolerant input for CPU frequency selection. Refer to input electrical characteristics for Vil_FS and Vih_FS values. /TEST_Sel: 3-level latched input to enable test mode. Refer to Test Clarification Table
54	CPU_STOP#	IN	Stops all CPUCLK, except those set to be free running clocks
55	PCI/SRC_STOP#	IN	Stops all PCICLKs and SRCCLKs besides the free-running clocks at logic 0 level, when input low
56	PCICLK2/REQ_SEL**	I/O	3.3V PCI clock output / Latch select input pin. 0 = PCIEXCLK, 1 = PEREQ#

MLF Pin Description

PIN #	PIN NAME	TYPE	DESCRIPTION
1	VDDPCI	PWR	Power supply for PCI clocks, nominal 3.3V
2	ITP_EN/PCICLK_F0	I/O	Free running PCI clock not affected by PCI_STOP#. ITP_EN: latched input to select pin functionality 1 = CPU_ITP pair 0 = SRC pair
3	**SELPCIEX_LCDCLK#/PCICLK_F1	I/O	Latched select input for LCDCLK/PCIEX output 0 = LCDCLK, 1 = PCIEX / Free running 3.3V PCI clock output.
4	Vtt_PwrGd#/PD	IN	Vtt_PwrGd# is an active low input used to determine when latched inputs are ready to be sampled. PD is an asynchronous active high input pin used to put the device into a low power state. The internal clocks, PLLs and the crystal oscillator are stopped.
5	VDD48	PWR	Power pin for the 48MHz output.3.3V
6	FSLA/USB_48MHz	I/O	3.3V tolerant input for CPU frequency selection. Refer to input electrical characteristics for Vil_FS and Vih_FS values. / Fixed 48MHz USB clock output. 3.3V.
7	GND	PWR	Ground pin.
8	DOTT_96MHz	OUT	Free running PCI clock not affected by PCI_STOP# through I2C . ITP_EN: latched input to select pin functionality 1 = CPU_2_ITP pair 0 = PCIEX_6 pair
9	DOTC_96MHz	OUT	Complement clock of differential pair for 96.00MHz DOT clock.
10	FSLB/TEST_MODE	IN	3.3V tolerant input for CPU frequency selection. Refer to input electrical characteristics for Vil_FS and Vih_FS values. TEST_MODE is a real time input to select between Hi-Z and REF/N divider mode while in test mode. Refer to Test Clarification Table.
11	LCDCLK_SS/PCIEXT0	OUT	True clock of LCDCLK_SS output / True clock of PCI Express differential pair. Selected by SELPCIEX_LCDCLK#
12	LCDCLK_SS/PCIEXC0	OUT	Complementary clock of LCDCLK_SS output / Complementary clock of PCI Express differential pair. Selected by SELPCIEX_LCDCLK#
13	PCIEXT1	OUT	True clock of differential PCI_Express pair.
14	PCIEXC1	OUT	Complement clock of differential PCI_Express pair.
15	VDDPCIEX	PWR	Power supply for PCI Express clocks, nominal 3.3V
16	PCIEXT2	OUT	True clock of differential PCI_Express pair.
17	PCIEXC2	OUT	Complement clock of differential PCI_Express pair.
18	PCIEXT3	OUT	True clock of differential PCI_Express pair.
19	PCIEXC3	OUT	Complement clock of differential PCI_Express pair.
20	SATACLKT	OUT	True clock of differential SATA pair.
21	SATACLKC	OUT	Complement clock of differential SATA pair.
22	VDDPCIEX	PWR	Power supply for PCI Express clocks, nominal 3.3V
23	GND	PWR	Ground pin.
24	PCIEXC4	OUT	Complement clock of differential PCI_Express pair.
25	PCIEXT4	OUT	True clock of differential PCI_Express pair.
26	PEREQ2#*/PCIEXC5	I/O	Real-time input pin that controls SATACLK and PCIEXCLK outputs that are selected through the I2c. 1 = disabled, 0 = enabled. / Complement clock of differential PCI Express output.
27	PEREQ1#*/PCIEXT5	I/O	Real-time input pin that controls SATACLK and PCIEXCLK outputs that are selected through the I2c. 1 = disabled, 0 = enabled. / True clock of differential PCI Express output.
28	VDDPCIEX	PWR	Power supply for PCI Express clocks, nominal 3.3V

MLF Pin Description (Continued)

PIN #	PIN NAME	TYPE	DESCRIPTION
29	CPUCLKC2_ITP/PCIEXC6	OUT	Complementary clock of CPU_ITP/PCIEX differential pair CPU_ITP/PCIEX output. These are current mode outputs. External resistors are required for voltage bias. Selected by ITP_EN input.
30	CPUCLKT2_ITP/PCIEXT6	OUT	True clock of differential pair CPU outputs. These are current mode outputs. External resistors are required for voltage bias. / True clock of differential PCIEX pair
31	VDDA	PWR	3.3V power for the PLL core.
32	GNDA	PWR	Ground pin for the PLL core.
33	IREF	OUT	This pin establishes the reference current for the differential current-mode output pairs. This pin requires a fixed precision resistor tied to ground in order to establish the appropriate current. 475 ohms is the standard value.
34	CPUCLKC1	OUT	Complementary clock of differential pair CPU outputs. These are current mode outputs. External resistors are required for voltage bias.
35	CPUCLKT1	OUT	True clock of differential pair CPU outputs. These are current mode outputs. External resistors are required for voltage bias.
36	VDDCPU	PWR	Supply for CPU clocks, 3.3V nominal
37	CPUCLKC0	OUT	Complementary clock of differential pair CPU outputs. These are current mode outputs. External resistors are required for voltage bias.
38	CPUCLKT0	OUT	True clock of differential pair CPU outputs. These are current mode outputs. External resistors are required for voltage bias.
39	GND	PWR	Ground pin.
40	SCLK	IN	Clock pin of SMBus circuitry, 5V tolerant.
41	SDATA	I/O	Data pin for SMBus circuitry, 5V tolerant.
42	VDDREF	PWR	Ref, XTAL power supply, nominal 3.3V
43	X2	OUT	Crystal output, Nominally 14.318MHz
44	X1	IN	Crystal input, Nominally 14.318MHz.
45	GND	PWR	Ground pin.
46	REF0	OUT	14.318 MHz reference clock.
47	REF1/FSLC/TEST_SEL	I/O	14.318 MHz reference clock./ 3.3V tolerant input for CPU frequency selection. Refer to input electrical characteristics for Vil_FS and Vih_FS values. /TEST_Sel: 3-level latched input to enable test mode. Refer to Test Clarification Table
48	CPU_STOP#	IN	Stops all CPUCLK, except those set to be free running clocks
49	PCI/SRC_STOP#	IN	Stops all PCICLKs and SRCCLKs besides the free-running clocks at logic 0 level, when input low
50	PCICLK2/REQ_SEL**	I/O	3.3V PCI clock output / Latch select input pin. 0 = PCIEXCLK, 1 = PEREQ#
51	VDDPCI	PWR	Power supply for PCI clocks, nominal 3.3V
52	GND	PWR	Ground pin.
53	PCICLK3	OUT	PCI clock output.
54	PCICLK4	OUT	PCI clock output.
55	PCICLK5	OUT	PCI clock output.
56	GND	PWR	Ground pin.

General Description

The **ICS954226** is a CK410M compatible clock synthesizer. It provides a single-chip solution for mobile systems built with Intel P4-M processors and Intel mobile chipsets. The device is driven with a 14.318MHz crystal and generates CPU outputs up to 400MHz. It provides the tight ppm accuracy required by Serial ATA and PCI Express.

Block Diagram

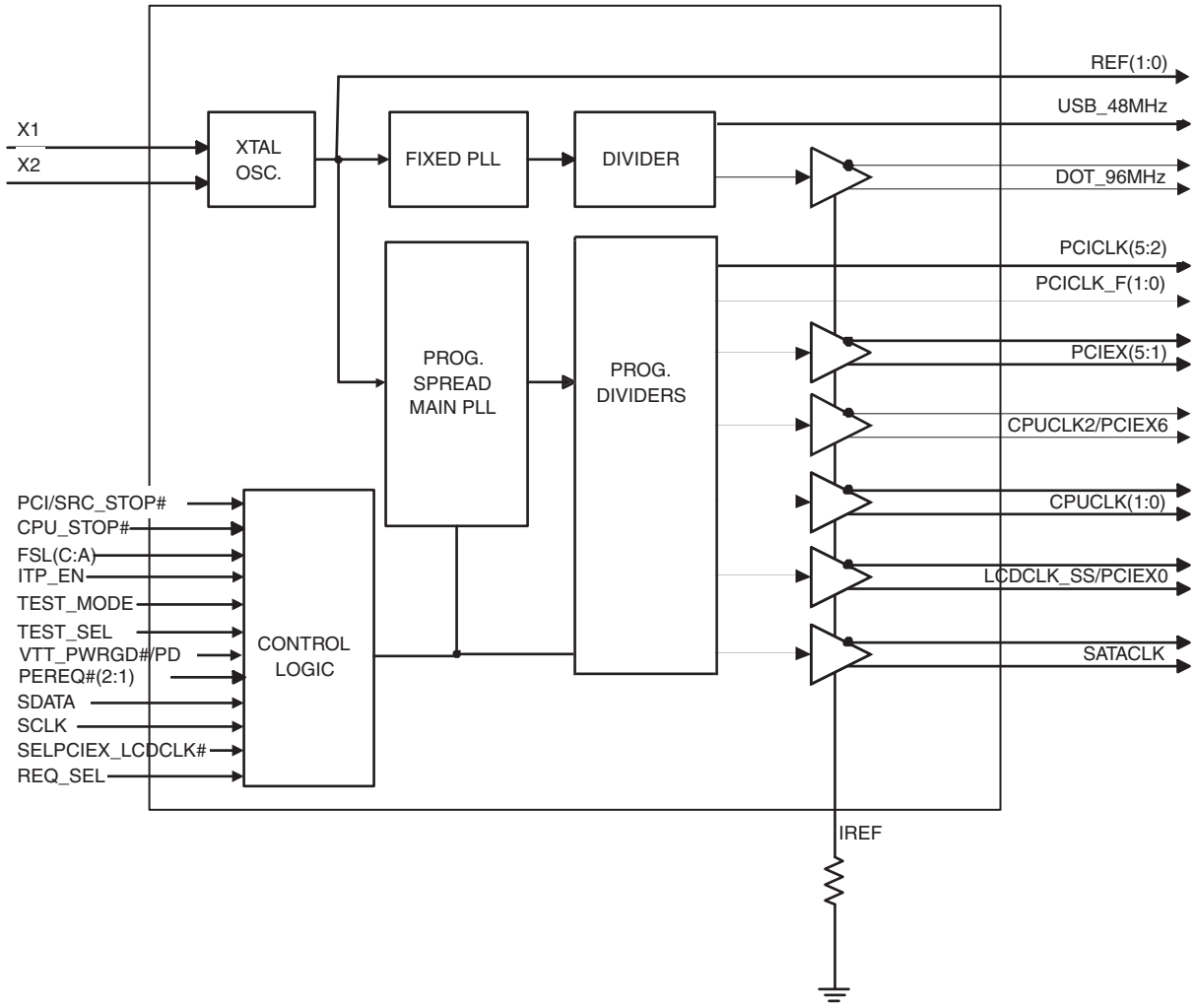


Table2: LCDCLK Spread and Frequency Selection Table

Byte 6b7	Byte 6b6	Byte 6b5	Byte 6b4	Byte 6b3	Pin 17/18	Spread
					MHz	%
0	0	0	0	0	96.00	0.8 Down
0	0	0	0	1	96.00	1 Down
0	0	0	1	0	96.00	1.25 Down
0	0	0	1	1	96.00	1.5 Down
0	0	1	0	0	96.00	1.75 Down
0	0	1	0	1	96.00	2 Down
0	0	1	1	0	96.00	2.5 Down
0	0	1	1	1	96.00	3 Down
0	1	0	0	0	96.00	+/-0.3 Center
0	1	0	0	1	96.00	+/-0.4 Center
0	1	0	1	0	96.00	+/-0.5 Center
0	1	0	1	1	96.00	+/-0.6 Center
0	1	1	0	0	96.00	+/-0.8 Center
0	1	1	0	1	96.00	+/-1.0 Center
0	1	1	1	0	96.00	+/-1.25 Center
0	1	1	1	1	96.00	+/-1.5 Center
1	0	0	0	0	100.00	0.8 Down
1	0	0	0	1	100.00	1 Down
1	0	0	1	0	100.00	1.25 Down
1	0	0	1	1	100.00	1.5 Down
1	0	1	0	0	100.00	1.75 Down
1	0	1	0	1	100.00	2 Down
1	0	1	1	0	100.00	2.5 Down
1	0	1	1	1	100.00	3 Down
1	1	0	0	0	100.00	+/-0.3 Center
1	1	0	0	1	100.00	+/-0.4 Center
1	1	0	1	0	100.00	+/-0.5 Center
1	1	0	1	1	100.00	+/-0.6 Center
1	1	1	0	0	100.00	+/-0.8 Center
1	1	1	0	1	100.00	+/-1.0 Center
1	1	1	1	0	100.00	+/-1.25 Center
1	1	1	1	1	100.00	+/-1.5 Center

General SMBus serial interface information for the 954226

How to Write:

- Controller (host) sends a start bit.
- Controller (host) sends the write address D2 $_{(H)}$
- ICS clock will ***acknowledge***
- Controller (host) sends the begining byte location = N
- ICS clock will ***acknowledge***
- Controller (host) sends the data byte count = X
- ICS clock will ***acknowledge***
- Controller (host) starts sending ***Byte N through Byte N + X -1***
  (see Note 2)
- ICS clock will ***acknowledge*** each byte ***one at a time***
- Controller (host) sends a Stop bit

How to Read:

- Controller (host) will send start bit.
- Controller (host) sends the write address D2 $_{(H)}$
- ICS clock will ***acknowledge***
- Controller (host) sends the begining byte location = N
- ICS clock will ***acknowledge***
- Controller (host) will send a separate start bit.
- Controller (host) sends the read address D3 $_{(H)}$
- ICS clock will ***acknowledge***
- ICS clock will send the data byte count = X
- ICS clock sends ***Byte N + X -1***
- ICS clock sends ***Byte 0 through byte X (if X$_{(H)}$ was written to byte 8)***.
- Controller (host) will need to acknowledge each byte
- Controllor (host) will send a not acknowledge bit
- Controller (host) will send a stop bit

Index Block Write Operation

Controller (Host)			ICS (Slave/Receiver)
T	starT bit		
Slave Address D2$_{(H)}$			
WR	WRite		
			ACK
Beginning Byte = N			
			ACK
Data Byte Count = X			
			ACK
Beginning Byte N		X Byte	
			ACK
	○		
	○		○
	○		○
			○
Byte N + X - 1			
			ACK
P	stoP bit		

Index Block Read Operation

Controller (Host)		ICS (Slave/Receiver)	
T	starT bit		
Slave Address D2$_{(H)}$			
WR	WRite		
		ACK	
Beginning Byte = N			
		ACK	
RT	Repeat starT		
Slave Address D3$_{(H)}$			
RD	ReaD		
		ACK	
		Data Byte Count = X	
ACK			
		X Byte	Beginning Byte N
ACK			
			○
○			○
○			○
○			
			Byte N + X - 1
N	Not acknowledge		
P	stoP bit		

* By default, SMBADR = 0,
therefore, SMBus WRITE/READ address is D0/D1.
Please see SMBus Address Selection table on page 1.

SMBus Table: Output Control Register

Byte 0	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	CPUCLK2_ITP/PCIEX6 Enable	Output Enable	RW	Disable	Enable	1
Bit 6	-	PCIEX5 Enable	Output Enable	RW	Disable	Enable	1
Bit 5	-	PCIEX4 Enable	Output Enable	RW	Disable	Enable	1
Bit 4	-	SATACLK Enable	Output Enable	RW	Disable	Enable	1
Bit 3	-	PCIEX3 Enable	Output Enable	RW	Disable	Enable	1
Bit 2	-	PCIEX2 Enable	Output Enable	RW	Disable	Enable	1
Bit 1	-	PCIEX1 Enable	Output Enable	RW	Disable	Enable	1
Bit 0	-	LCDCLK/PCIEX0 Enable	Output Enable	RW	Disable	Enable	1

SMBus Table: Spread and Output Control Register

Byte 1	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	Test Clock Mode Entry	Test Mode	RW	Disable	Enable	0
Bit 6	-	DOT_96MHz Enable	Output Enable	RW	Disable	Enable	1
Bit 5	-	USB_48MHz Enable	Output Enable	RW	Disable	Enable	1
Bit 4	-	REF_0 Enable	Output Enable	RW	Disable	Enable	1
Bit 3	-	LCDCLK/PCIEX0 Spectrum Mode	Spread Control	RW	OFF	ON	1
Bit 2	-	CPUCLK1	Output Enable	RW	Disable	Enable	1
Bit 1	-	CPUCLK0	Output Enable	RW	Disable	Enable	1
Bit 0	-	Spread Spectrum Mode	Spread Control for PLL1	RW	OFF	ON	0

SMBus Table: Output Control Register

Byte 2	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	PCICLK5	Output Enable	RW	Disable	Enable	1
Bit 6	-	PCICLK4	Output Enable	RW	Disable	Enable	1
Bit 5	-	PCICLK3	Output Enable	RW	Disable	Enable	1
Bit 4	-	PCICLK2	Output Enable	RW	Disable	Enable	1
Bit 3	-	Test Mode Selection	Test Mode Selection	RW	Hi-Z	REF/N	0
Bit 2	-	PCI_STOP	Stop all PCI, PCIEX and SATA clocks	RW	Enable	Disable	1
Bit 1	-	PCI_F0 Enable	Output Enable	RW	Disable	Enable	1
Bit 0	-	PCI_F1 Enable	Output Enable	RW	Disable	Enable	1

SMBus Table: Output Control Register

Byte 3	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	PCIEX6	Allow assertion of PCI_STOP# or setting of PCI_STOP control bit in SMBus register to stop PCIEX clocks	RW	Free Running	Stoppable	0
Bit 6	-	PCIEX5		RW	Free Running	Stoppable	0
Bit 5	-	PCIEX4		RW	Free Running	Stoppable	0
Bit 4	-	SATACLK		RW	Free Running	Stoppable	0
Bit 3	-	PCIEX3		RW	Free Running	Stoppable	0
Bit 2	-	PCIEX2		RW	Free Running	Stoppable	0
Bit 1	-	PCIEX1		RW	Free Running	Stoppable	0
Bit 0	-	PCIEX0		RW	Free Running	Stoppable	0

SMBus Table: Output Control Register

Byte 4	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	REF_1 Enable	Output Enable	RW	Disable	Enable	1
Bit 6	-	96MHz	Driven in PD	RW	Driven	Hi-Z	1
Bit 5	-	REF_0 STRENGTH	Strength Programming	RW	1X	2X	1
Bit 4	-	PCI_F1	Allow assertion of PCI_STOP# or setting of	RW	Free Running	Stoppable	0
Bit 3	-	PCI_F0		RW	Free Running	Stoppable	0
Bit 2	-	CPUCLK2_ITP	Allow assertion of CPU_STOP# to stop CPUCLK outputs	RW	Free Running	Stoppable	1
Bit 1	-	CPUCLK1		RW	Free Running	Stoppable	1
Bit 0	-	CPUCLK0		RW	Free Running	Stoppable	1

SMBus Table: Output Control Register

Byte 5	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	PCI_STOP Drive Mode	Driven in PCI_STOP#	RW	Driven	Hi-Z	0
Bit 6	-	CPUCLK2_ITP_STOP Drive Mode	Driven in CPU_STOP#	RW	Driven	Hi-Z	0
Bit 5	-	CPUCLK1_STOP Drive Mode		RW	Driven	Hi-Z	0
Bit 4	-	CPUCLK0_STOP Drive Mode		RW	Driven	Hi-Z	0
Bit 3	-	PCIEX (6:0) Drive Mode	Driven in Powerdown (PD)	RW	Driven	Hi-Z	0
Bit 2	-	CPUCLK2_ITP_PD Drive Mode		RW	Driven	Hi-Z	0
Bit 1	-	CPUCLK[1:0] PD Drive Mode		RW	Driven	Hi-Z	0
Bit 0	-	ITP_EN	PCIEX/CPU_ITP select	RW	PCIEX	CPU_ITP	latch

SMBus Table: Output Control Register

Byte 6	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	SS4	LCDCLK Spread Prog Bit 4	RW	96Mhz	100Mhz	0
Bit 6	-	SS3	LCDCLK Spread Prog Bit 3	RW	See Table 2: LCDCLK Freq Sel		1
Bit 5	-	SS2	LCDCLK Spread Prog Bit 2	RW			0
Bit 4	-	SS1	LCDCLK Spread Prog Bit 1	RW			0
Bit 3	-	SS0	LCDCLK Spread Prog Bit 0	RW			0
Bit 2	-	FSLC	Freq Select Bit 2	RW	See Table 1: PLL1 Frequency Selection Table		Latched
Bit 1	-	FSLB	Freq Select Bit 1	RW			Latched
Bit 0	-	FSLA	Freq Select Bit 0	RW			Latched

SMBus Table: Vendor & Revision ID Register

Byte 7	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	RID3	REVISION ID	R	-	-	x
Bit 6	-	RID2		R	-	-	x
Bit 5	-	RID1		R	-	-	x
Bit 4	-	RID0		R	-	-	x
Bit 3	-	VID3	VENDOR ID	R	-	-	0
Bit 2	-	VID2		R	-	-	0
Bit 1	-	VID1		R	-	-	0
Bit 0	-	VID0		R	-	-	1

SMBus Table: Byte Count Register

Byte 8	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	BC7	Byte Count Programming b(7:0)	RW	Writing to this register will configure how many bytes will be read back, default is 0F = 15 bytes.		0
Bit 6	-	BC6		RW			0
Bit 5	-	BC5		RW			0
Bit 4	-	BC4		RW			0
Bit 3	-	BC3		RW			1
Bit 2	-	BC2		RW			1
Bit 1	-	BC1		RW			1
Bit 0	-	BC0		RW			1

SMBus Table: Watchdog Timer Register

Byte 9	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	WDH_EN	Watchdog Hard Alarm Enable	RW	Disable	Enable	0
Bit 6	-	WDS_EN	Watchdog Soft Alarm Enable	RW	Disable	Enable	0
Bit 5	-	WD Hard Status	WD Hard Alarm Status	R	Normal	Alarm	X
Bit 4	-	WD Soft Status	WD Soft Alarm Status	R	Normal	Alarm	X
Bit 3	-	WDTCtrl	Watch Dog Time base Control	RW	290ms Base	1160ms Base	0
Bit 2	-	WD2	WD Timer Bit 2	RW	These bits represent X*290ms (or 1.16S) the watchdog timer waits before it goes to alarm mode. Default is 7 X 290ms = 2s.		1
Bit 1	-	WD1	WD Timer Bit 1	RW			1
Bit 0	-	WD0	WD Timer Bit 0	RW			1

SMBus Table: VCO Control Select Bit & WD Timer Control Register

Byte 10	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	M/N_EN	PLLM/N Programming Enable	RW	Disable	Enable	0
Bit 6	-	LCDCLK/PCIEX0 SEL	SELPCIEX0/LCDCLK#	RW	LCDCLK	PCIEX0	latch
Bit 5	-	REQ_SEL	REQ_SEL	RW	PCIEX5	PEREQ	latch
Bit 4	-	LCDCLK/PCIEX0	Driven in PD	RW	Driven	Hi-Z	0
Bit 3	-	WD Safe Freq Source	WD Safe Freq Source	RW	Latch Inputs/Byte6[2:0]	B10b(2:0)	0
Bit 2	-	WD SFC	Watch Dog Safe Freq Programming bits	RW	Writing to these bit will configure the safe frequency as Byte0 bit (4:0).		0
Bit 1	-	WD SFB		RW			0
Bit 0	-	WD SFA		RW			0

SMBus Table: VCO Frequency Control Register

Byte 11	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	N Div8	N Divider Prog bit 8	RW	The decimal representation of M and N Divier in Byte 11 and 12 will configure the VCO frequency. Default at power up = latch-in or Byte 0 Rom table. VCO Frequency = 14.318 x [NDiv(9:0)+8] / [MDiv(5:0)+2]		X
Bit 6	-	N Div 9	N Divider Prog bit 9	RW			X
Bit 5	-	M Div5	M Divider Programming bits	RW			X
Bit 4	-	M Div4		RW			X
Bit 3	-	M Div3		RW			X
Bit 2	-	M Div2		RW			X
Bit 1	-	M Div1		RW			X
Bit 0	-	M Div0		RW			X

SMBus Table: VCO Frequency Control Register

Byte 12	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	N Div7	N Divider Programming b(8:0)	RW	The decimal representation of M and N Divier in Byte 11 and 12 will configure the VCO frequency. Default at power up = latch-in or Byte 0 Rom table. VCO Frequency = 14.318 x [NDiv(9:0)+8] / [MDiv(5:0)+2]		X
Bit 6	-	N Div6		RW			X
Bit 5	-	N Div5		RW			X
Bit 4	-	N Div4		RW			X
Bit 3	-	N Div3		RW			X
Bit 2	-	N Div2		RW			X
Bit 1	-	N Div1		RW			X
Bit 0	-	N Div0		RW			X

SMBus Table: Spread Spectrum Control Register

Byte 13	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	SSP7	Spread Spectrum Programming b(7:0)	RW	These Spread Spectrum bits in Byte 13 and 14 will program the spread pecentage. It is recommended to use ICS Spread % table for spread programming.		X
Bit 6	-	SSP6		RW			X
Bit 5	-	SSP5		RW			X
Bit 4	-	SSP4		RW			X
Bit 3	-	SSP3		RW			X
Bit 2	-	SSP2		RW			X
Bit 1	-	SSP1		RW			X
Bit 0	-	SSP0		RW			X

SMBus Table: Spread Spectrum Control Register

Byte 14	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	Reserved	Reserved	R	-	-	0
Bit 6	-	SSP14	Spread Spectrum Programming b(14:8)	RW	These Spread Spectrum bits in Byte 13 and 14 will program the spread pecentage. It is recommended to use ICS Spread % table for spread programming.		X
Bit 5	-	SSP13		RW			X
Bit 4	-	SSP12		RW			X
Bit 3	-	SSP11		RW			X
Bit 2	-	SSP10		RW			X
Bit 1	-	SSP9		RW			X
Bit 0	-	SSP8		RW			X

SMBus Table: Output Divider Control Register

Byte 15	Pin #	Name	Control Function	Type	0		1		PWD
Bit 7	-	PCIEX Div3	PCIEX Divider Ratio Programming Bits	RW	0000:/2	0100:/4	1000:/8	1100:/16	X
Bit 6	-	PCIEX Div2		RW	0001:/3	0101:/6	1001:/12	1101:/24	X
Bit 5	-	PCIEX Div1		RW	0010:/5	0110:/10	1010:/20	1110:/40	X
Bit 4	-	PCIEX Div0		RW	0011:/15	0111:/30	1011:/60	1111:/120	X
Bit 3	-	CPU Div3	CPUDivider Ratio Programming Bits	RW	0000:/2	0100:/4	1000:/8	1100:/16	X
Bit 2	-	CPU Div2		RW	0001:/3	0101:/6	1001:/12	1101:/24	X
Bit 1	-	CPU Div1		RW	0010:/5	0110:/10	1010:/20	1110:/40	X
Bit 0	-	CPU Div0		RW	0011:/15	0111:/30	1011:/60	1111:/120	X

SMBus Table: PEREQ# Control Register

Byte 16	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	Reserved	Reserved	RW	-	-	0
Bit 6	-	PEREQ2# controls selected outputs. Outputs controlled by this pin will be Hi-Z when PEREQ2# is high.	PCIEX4 is controlled	RW	Not Controlled	Controlled	0
Bit 5	-		PCIEX3 is controlled	RW	Not Controlled	Controlled	0
Bit 4	-		PCIEX1 is controlled	RW	Not Controlled	Controlled	0
Bit 3	-	Reserved	Reserved	RW	-	-	0
Bit 2	-	PEREQ1# controls selected outputs. Outputs controlled by this pin will be Hi-Z when PEREQ1# is high.	SATACLK is controlled	RW	Not Controlled	Controlled	0
Bit 1	-		PCIEX2 is controlled	RW	Not Controlled	Controlled	0
Bit 0	-		PCIEX0 is controlled	RW	Not Controlled	Controlled	0

SMBus Table: PLL 2 VCO Frequency Control Register

Byte 17	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	N Div8	N Divider Prog bit 8	RW	The decimal representation of M and N Divier in Byte 17 and 18 will configure the VCO frequency. Default at power up = Byte 0 Rom table. VCO Frequency = 14.318 x [NDiv(9:0)+8] / [MDiv(5:0)+2]		X
Bit 6	-	N Div9	N Divider Prog bit 9	RW			X
Bit 5	-	M Div5	M Divider Programming bits	RW			X
Bit 4	-	M Div4		RW			X
Bit 3	-	M Div3		RW			X
Bit 2	-	M Div2		RW			X
Bit 1	-	M Div1		RW			X
Bit 0	-	M Div0		RW			X

SMBus Table: PLL 2 VCO Frequency Control Register

Byte 18	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	N Div7	N Divider Programming b(8:0)	RW	The decimal representation of M and N Divier in Byte 17 and 18 will configure the VCO frequency. Default at power up = Byte 0 Rom table. VCO Frequency = 14.318 x [NDiv(9:0)+8] / [MDiv(5:0)+2]		X
Bit 6	-	N Div6		RW			X
Bit 5	-	N Div5		RW			X
Bit 4	-	N Div4		RW			X
Bit 3	-	N Div3		RW			X
Bit 2	-	N Div2		RW			X
Bit 1	-	N Div1		RW			X
Bit 0	-	N Div0		RW			X

SMBus Table: PLL 2 Spread Spectrum Control Register

Byte 19	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	SSP7	Spread Spectrum Programming b(7:0)	RW	These Spread Spectrum bits in Byte 19 and 20 will program the spread pecentage. It is recommended to use ICS Spread % table for spread programming.		X
Bit 6	-	SSP6		RW			X
Bit 5	-	SSP5		RW			X
Bit 4	-	SSP4		RW			X
Bit 3	-	SSP3		RW			X
Bit 2	-	SSP2		RW			X
Bit 1	-	SSP1		RW			X
Bit 0	-	SSP0		RW			X

SMBus Table: PLL2 Spread Spectrum Control Register

Byte 20	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	Reserved	Reserved	R	-	-	0
Bit 6	-	SSP14	Spread Spectrum Programming b(14:8)	RW	These Spread Spectrum bits in Byte 19 and 20 will program the spread pecentage. It is recommended to use ICS Spread % table for spread programming.		X
Bit 5	-	SSP13		RW			X
Bit 4	-	SSP12		RW			X
Bit 3	-	SSP11		RW			X
Bit 2	-	SSP10		RW			X
Bit 1	-	SSP9		RW			X
Bit 0	-	SSP8		RW			X

Absolute Maximum Rating

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	Notes
3.3V Core Supply Voltage	VDDA	-			4.6	V	1
3.3V Logic Input Supply Voltage	VDD	-			4.6	V	1
Storage Temperature	Ts	-	-65		150	°C	1
Ambient Operating Temp	Tambient	-	0		70	°C	1
Junction Temperature	Tj	-			125	°C	1
Input ESD protection HBM	ESD prot	-	2000			V	1

[1]Guaranteed by design and characterization, not 100% tested in production.

Electrical Characteristics - Input/Supply/Common Output Parameters

PARAMETER	SYMBOL	CONDITIONS*	MIN	TYP	MAX	UNITS	Notes
Input High Voltage	V_{IH}	3.3 V +/-5%	2		V_{DD} + 0.3	V	1
Input Low Voltage	V_{IL}	3.3 V +/-5%	V_{SS} - 0.3		0.8	V	1
Input High Current	I_{IH}	$V_{IN} = V_{DD}$	-5		5	uA	1
Input Low Current	I_{IL1}	V_{IN} = 0 V; Inputs with no pull-up resistors	-5			uA	1
	I_{IL2}	V_{IN} = 0 V; Inputs with pull-up resistors	-200			uA	1
Low Threshold Input-High Voltage	V_{IH_FSL}	3.3 V +/-5%	0.7		1.7	V	1
Low Threshold Input-Low Voltage	V_{IL_FSL}	3.3 V +/-5%	V_{SS} - 0.3		0.35	V	1
Operating Supply Current	$I_{DD3.3OP}$	Full Active, C_L = Full load;			400	mA	1
Powerdown Current	$I_{DD3.3PD}$	all diff pairs driven			70	mA	1
		all differential pairs tri-stated			12	mA	1
Input Frequency	F_i	V_{DD} = 3.3 V		14.31818		MHz	2
Pin Inductance	L_{pin}				7	nH	1
Input Capacitance	C_{IN}	Logic Inputs			5	pF	1
	C_{OUT}	Output pin capacitance			6	pF	1
	C_{INX}	X1 & X2 pins			5	pF	1
Clk Stabilization	T_{STAB}	From V_{DD} Power-Up or de-assertion of PD# to 1st clock			1.8	ms	1
Modulation Frequency		Triangular Modulation	30		33	kHz	1
Tdrive_PD#		CPU output enable after PD# de-assertion			300	us	1
Tfall_Pd#		PD# fall time of			5	ns	1
Trise_Pd#		PD# rise time of			5	ns	1
SMBus Voltage	V_{DD}		2.7		5.5	V	1
Low-level Output Voltage	V_{OL}	@ I_{PULLUP}			0.4	V	1
Current sinking at V_{OL} = 0.4 V	I_{PULLUP}		4			mA	1
SCLK/SDATA Clock/Data Rise Time	T_{RI2C}	(Max VIL - 0.15) to (Min VIH + 0.15)			1000	ns	1
SCLK/SDATA Clock/Data Fall Time	T_{FI2C}	(Min VIH + 0.15) to (Max VIL - 0.15)			300	ns	1

*TA = 0 - 70°C; Supply Voltage VDD = 3.3 V +/-5%

[1]Guaranteed by design and characterization, not 100% tested in production.

[2] Input frequency should be measured at the REF pin and tuned to ideal 14.31818MHz to meet ppm frequency accuracy on PLL outputs.

Electrical Characteristics - CPUCLKT/C -- 0.7V Current Mode Differential Pair

PARAMETER	SYMBOL	CONDITIONS*	MIN	TYP	MAX	UNITS	Notes
Current Source Output Impedance	Zo	VO = Vx	3000			Ω	1
Voltage High	VHigh	Statistical measurement on single ended signal	660		850	mV	1,3
Voltage Low	VLow		-150		150	mV	1,3
Max Voltage	Vovs	Measurement on single ended signal using absolute value.			1150	mV	1
Min Voltage	Vuds		-300			mV	1
Crossing Voltage (abs)	Vx(abs)		250		550	mV	1
Crossing Voltage (var)	d-Vx	Variation of crossing over all edges			140	mV	1
Long Accuracy	ppm	see Tperiod min-max values	-300		300	ppm	1,2
Average period	Tperiod	400MHz nominal	2.4993		2.5008	ns	2
		400MHz spread	2.4993		2.5133	ns	2
		333.33MHz nominal	2.9991		3.0009	ns	2
		333.33MHz spread	2.9991		3.016	ns	2
		266.66MHz nominal	3.7489		3.7511	ns	2
		266.66MHz spread	3.7489		3.77	ns	2
		200MHz nominal	4.9985		5.0015	ns	2
		200MHz spread	4.9985		5.0266	ns	2
		166.66MHz nominal	5.9982		6.0018	ns	2
		166.66MHz spread	5.9982		6.0320	ns	2
		133.33MHz nominal	7.4978		7.5023	ns	2
		133.33MHz spread	7.4978		7.5400	ns	2
		100.00MHz nominal	9.9970		10.0030	ns	2
		100.00MHz spread	9.9970		10.0533	ns	2
Absolute min period	Tabsmin	400MHz nominal/spread	2.4143			ns	1,2
		333.33MHz nominal/spread	2.9141			ns	1,2
		266.66MHz nominal/spread	3.6639			ns	1,2
		200MHz nominal/spread	4.8735			ns	1,2
		166.66MHz nominal/spread	5.8732			ns	1,2
		133.33MHz nominal/spread	7.3728			ns	1,2
		100.00MHz nominal/spread	9.8720			ns	1,2
Rise Time	tr	VOL = 0.175V, VOH = 0.525V	175		700	ps	1
Fall Time	tf	VOH = 0.525V VOL = 0.175V	175		700	ps	1
Rise Time Variation	d-tr	VOL = 0.175V, VOH = 0.525V			125	ps	1
Fall Time Variation	d-tf	VOH = 0.525V VOL = 0.175V			125	ps	1
Rise/Fall Matching	trfm				20	%	1
Duty Cycle	dt3	Measurement from differential wavefrom	45		55	%	1
Skew	tsk3	CPU(1:0), VT = 50%			100	ps	1
Skew	tsk4	CPU(1:0) to CPU2_ITP, VT = 50%			150	ps	1
Jitter, Cycle to cycle	tjcyc-cyc	Measurement from differential wavefrom (CPU2_ITP)			125	ps	1
Jitter, Cycle to cycle	tjcyc-cyc	Measurement from differential wavefrom, (CPU(1:0))			85	ps	1

*T_A = 0 - 70°C; V_{DD} = 3.3 V +/-5%; C_L =2pF, R_S=33.2Ω, R_P=49.9Ω, I_{REF} = 475Ω

[1]Guaranteed by design and characterization, not 100% tested in production.

[2] All Long Term Accuracy and Clock Period specifications are guaranteed assuming that REFOUT is at 14.31818MHz

[3]$I_{REF} = V_{DD}/(3xR_R)$. For R_R = 475Ω (1%), I_{REF} = 2.32mA. I_{OH} = 6 x I_{REF} and V_{OH} = 0.7V @ Z_O=50Ω.

Electrical Characteristics - SATA/PCIEX/LCDCLK_SS@100M 0.7V Current Mode Differential Pair

PARAMETER	SYMBOL	CONDITIONS*	MIN	TYP	MAX	UNITS	Notes
Current Source Output Impedance	Zo	VO = Vx	3000			Ω	1
Voltage High	VHigh	Statistical measurement on single ended signal	660		850	mV	1,3
Voltage Low	VLow		-150		150	mV	1,3
Max Voltage	Vovs	Measurement on single ended signal using absolute value.			1150	mV	1
Min Voltage	Vuds		-300			mV	1
Crossing Voltage (abs)	Vx(abs)		250		550	mV	1
Crossing Voltage (var)	d-Vx	Variation of crossing over all edges			140	mV	1
Long Accuracy	ppm	see Tperiod min-max values	-300		300	ppm	1,2
Average period	Tperiod	100.00MHz nominal	9.9970		10.0030	ns	2
		100.00MHz spread	9.9970		10.0533	ns	2
Absolute min period	Tabsmin	100.00MHz nominal/spread	9.8720			ns	1,2
Rise Time	tr	VOL = 0.175V, VOH = 0.525V	175		700	ps	1
Fall Time	tf	VOH = 0.525V VOL = 0.175V	175		700	ps	1
Rise Time Variation	d-tr	VOL = 0.175V, VOH = 0.525V			125	ps	1
Fall Time Variation	d-tf	VOH = 0.525V VOL = 0.175V			125	ps	1
Rise/Fall Matching	trfm				20	%	1
Duty Cycle	dt3	Measurement from differential wavefrom	45		55	%	1
Skew	tsk3	VT = 50%			250	ps	1
Jitter, Cycle to cycle	tjcyc-cyc	Measurement from differential wavefrom			125	ps	1

*T_A = 0 - 70°C; V_{DD} = 3.3 V +/-5%; C_L =2pF, R_S=33.2Ω, R_P=49.9Ω and I_{REF} = 475Ω

[1]Guaranteed by design and characterization, not 100% tested in production.

[2] All Long Term Accuracy and Clock Period specifications are guaranteed assuming that REFOUT is at 14.31818MHz

[3]$I_{REF} = V_{DD}/(3xR_R)$. For R_R = 475Ω (1%), I_{REF} = 2.32mA. I_{OH} = 6 x I_{REF} and V_{OH} = 0.7V @ Z_O=50Ω.

Electrical Characteristics - DOT_96MHz/LCDCLK_SS@96M 0.7V Current Mode Differential Pair

PARAMETER	SYMBOL	CONDITIONS*	MIN	TYP	MAX	UNITS	Notes
Current Source Output Impedance	Zo	VO = Vx	3000			Ω	1
Voltage High	VHigh	Statistical measurement on single ended signal	660		850	mV	1,3
Voltage Low	VLow		-150		150	mV	1,3
Max Voltage	Vovs	Measurement on single ended signal using absolute value.			1150	mV	1
Min Voltage	Vuds		-300			mV	1
Crossing Voltage (abs)	Vx(abs)		250		550	mV	1
Crossing Voltage (var)	d-Vcross	Variation of crossing over all edges			140	mV	1
Long Accuracy	ppm	see Tperiod min-max values	-100		100	ppm	1,2
Average period	Tperiod	96.00MHz nominal	10.4135		10.4198	ns	2
Absolute min period	Tabsmin	96.00MHz nominal	10.1635			ns	1,2
Rise Time	tr	VOL = 0.175V, VOH = 0.525V	175		700	ps	1
Fall Time	tf	VOH = 0.525V VOL = 0.175V	175		700	ps	1
Rise Time Variation	d-tr	VOL = 0.175V, VOH = 0.525V			125	ps	1
Fall Time Variation	d-tf	VOH = 0.525V VOL = 0.175V			125	ps	1
Rise/Fall Matching	trfm				20	%	1
Duty Cycle	dt3	Measurement from differential wavefrom	45		55	%	1
Jitter, Cycle to cycle	tjcyc-cyc	Measurement from differential wavefrom			250	ps	1

*T_A = 0 - 70°C; V_{DD} = 3.3 V +/-5%; C_L =2pF, R_S=33.2Ω, R_P=49.9Ω and I_{REF} = 475Ω

[1]Guaranteed by design and characterization, not 100% tested in production.

[2] All Long Term Accuracy and Clock Period specifications are guaranteed assuming that REFOUT is at 14.31818MHz

[3]$I_{REF} = V_{DD}/(3xR_R)$. For R_R = 475Ω (1%), I_{REF} = 2.32mA. I_{OH} = 6 x I_{REF} and V_{OH} = 0.7V @ Z_O=50Ω.

Electrical Characteristics - PCICLK/PCICLK_F

PARAMETER	SYMBOL	CONDITIONS*	MIN	TYP	MAX	UNITS	Notes
Output Impedance	R_{DSP}	$V_O = V_{DD}*(0.5)$	12		55	Ω	1
Output High Voltage	V_{OH}	I_{OH} = -1 mA	2.4			V	1
Output Low Voltage	V_{OL}	I_{OL} = 1 mA			0.55	V	1
Output High Current	I_{OH}	V_{OH} @MIN = 1.0 V	-33			mA	1
		V_{OH}@MAX = 3.135 V			-33	mA	1
Output Low Current	I_{OL}	V_{OL} @ MIN = 1.95 V	30			mA	1
		V_{OL} @ MAX = 0.4 V			38	mA	1
Edge Rate	$t_{slewr/f}$	Rising/Falling edge rate VOL = 0.4 V, VOH = 2.4 V	1		4	V/ns	1
Duty Cycle	d_{t1}	V_T = 1.5 V	45		55	%	1
Group Skew	t_{skew}	V_T = 1.5 V			500	ps	1
Jitter, Cycle to cycle	$t_{jcyc-cyc}$	V_T = 1.5 V			250	ps	1

*TA = 0 - 70°C; Supply Voltage VDD = 3.3 V +/-5%, CL = 5 pF with Rs = 33Ω (unless otherwise specified)

[1]Guaranteed by design and characterization, not 100% tested in production.

Electrical Characteristics - 48MHz

PARAMETER	SYMBOL	CONDITIONS*	MIN	TYP	MAX	UNITS	Notes
Long Accuracy	ppm	see Tperiod min-max values	-100		100	ppm	1
Clock period	T_{period}	48.00MHz output nominal	20.8313		20.8354	ns	
Output Impedance	R_{DSP}	$V_O = V_{DD}*(0.5)$	12		55	Ω	1
Output High Voltage	V_{OH}	I_{OH} = -1 mA	2.4			V	1
Output Low Voltage	V_{OL}	I_{OL} = 1 mA			0.55	V	1
Output High Current	I_{OH}	V_{OH} @MIN = 1.0 V	-33			mA	1
		V_{OH}@MAX = 3.135 V			-33	mA	1
Output Low Current	I_{OL}	V_{OL} @ MIN = 1.95 V	30			mA	1
		V_{OL} @ MAX = 0.4 V			38	mA	1
Edge Rate	t_{slewr/f_48}	48M Rising/Falling edge rate VOL = 0.4 V, VOH = 2.4 V	1		2	V/ns	1
Duty Cycle	d_{t1}	V_T = 1.5 V	45		55	%	1
Jitter, Cycle to cycle	$t_{jcyc-cyc}$	V_T = 1.5 V			500	ps	1

*TA = 0 - 70°C; Supply Voltage VDD = 3.3 V +/-5%, CL = 5 pF with Rs = 33Ω

[1]Guaranteed by design and characterization, not 100% tested in production.

Electrical Characteristics - REF-14.318MHz

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	Notes
Long Accuracy	ppm	see Tperiod min-max values	-300		300	ppm	1,2
Clock period	Tperiod	14.318MHz output nominal	69.8270		69.8550	ns	2
Output High Voltage	VOH	IOH = -1 mA	2.4			V	1
Output Low Voltage	VOL	IOL = 1 mA			0.4	V	1
Output High Current	IOH	VOH @MIN = 1.0 V, VOH@MAX = 3.135 V	-29		-23	mA	1
Output Low Current	IOL	VOL @MIN = 1.95 V, VOL @MAX = 0.4 V	29		27	mA	1
Edge Rate	tslewr/f	Rising/Falling edge rate VOL = 0.4 V, VOH = 2.4 V	1		4	V/ns	1
Duty Cycle	dt1	VT = 1.5 V	45		55	%	1
Jitter	tjcyc-cyc	VT = 1.5 V			1000	ps	1

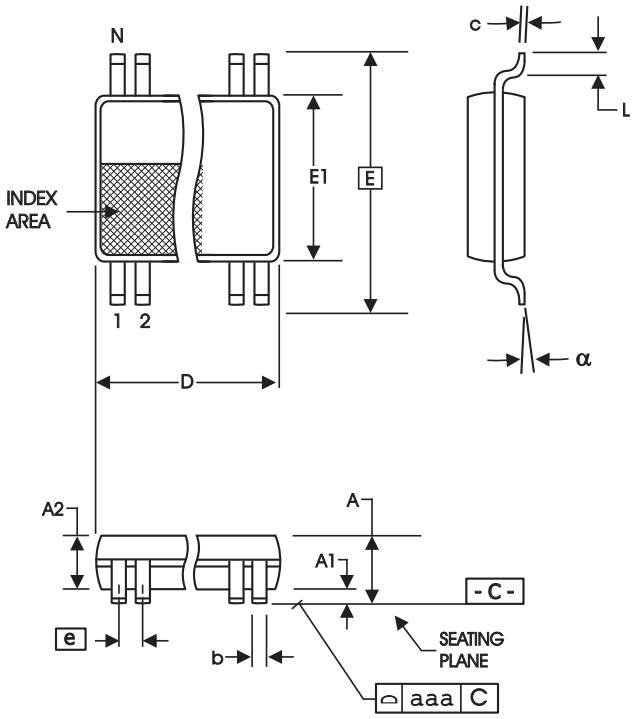
*TA = 0 - 70°C; Supply Voltage VDD = 3.3 V +/-5%, CL = 5 pF with Rs = 39Ω

[1]Guaranteed by design and characterization, not 100% tested in production.

[2] All Long Term Accuracy and Clock Period specifications are guaranteed assuming that REFOUT is at 14.31818MHz

Test Clarification Table

Comments	HW		SW		
	FSLC/TEST_SEL HW PIN	FSLB/TEST_MODE HW PIN	TEST ENTRY BIT W1b7	REF/N or HI-Z W2b3	OUTPUT
	0	X	0	X	NORMAL
· **FS_C/TEST_SEL is a 3-level latched input.** o Power-up w/ V >= 2.0V to select TEST o Power-up w/ V < 2.0V to have pin function as FS_C.	1	0	X	0	HI-Z
	1	0	X	1	REF/N
	1	1	X	0	REF/N
· **When pin is FS_C, VIH_FS and VIL_FS levels apply.** · **FS_B/TEST_MODE is a low-threshold input** o VIH_FS and VIL_FS levels apply. o TEST_MODE is a real time input	1	1	X	1	REF/N
	0	X	1	0	HI-Z
· **TEST_SEL can be invoked after power up through SMBus B1b7.** o If TEST is selected by B1b7, only B2b3 controls TEST_MODE. The FS_B/TEST_Mode pin is not used. · **Power must be cycled to exit TEST.**	0	X	1	1	REF/N
W1b7: 1= ENTER TEST MODE, Default = 0 (NORMAL OPERATION)					
W2b3: 1= REF/N, Default = 0 (HI-Z)					



56-Lead 6.10 mm. Body, 0.50 mm. Pitch TSSOP
(240 mil) (20 mil)

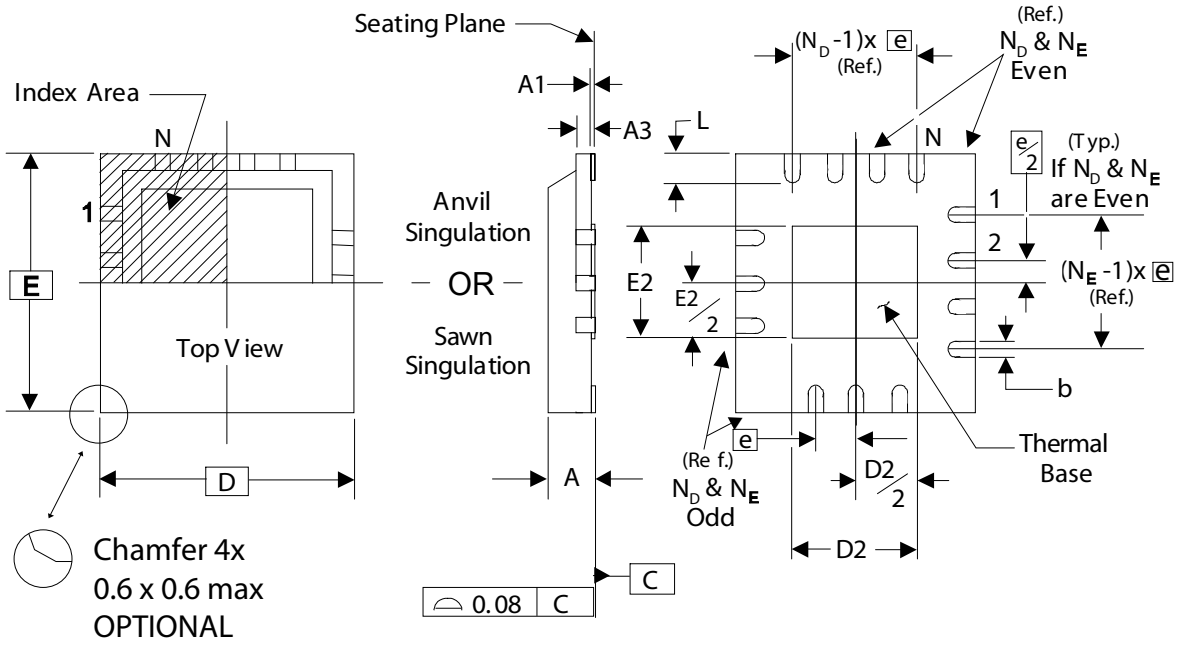
SYMBOL	In Millimeters COMMON DIMENSIONS		In Inches COMMON DIMENSIONS	
	MIN	MAX	MIN	MAX
A	--	1.20	--	.047
A1	0.05	0.15	.002	.006
A2	0.80	1.05	.032	.041
b	0.17	0.27	.007	.011
c	0.09	0.20	.0035	.008
D	SEE VARIATIONS		SEE VARIATIONS	
E	8.10 BASIC		0.319 BASIC	
E1	6.00	6.20	.236	.244
e	0.50 BASIC		0.020 BASIC	
L	0.45	0.75	.018	.030
N	SEE VARIATIONS		SEE VARIATIONS	
a	0°	8°	0°	8°
aaa	--	0.10	--	.004

VARIATIONS

N	D mm.		D (inch)	
	MIN	MAX	MIN	MAX
56	13.90	14.10	.547	.555

Reference Doc.: JEDEC Publication 95, MO-153

10-0039



THERMALLY ENHANCED, VERY THIN, FINE PITCH
QUAD FLAT / NO LEAD PLASTIC PACKAGE

DIMENSIONS

SYMBOL	MIN.	MAX.
A	0.8	1.0
A1	0	0.05
A3	0.25 Reference	
b	0.18	0.3
e	0.50 BASIC	

DIMENSIONS

SYMBOL	VLLD-2 / -5	ICS 56L TOLERANCE
N	56	56
N_D	14	14
N_E	14	14
D x E BASIC	8.00 x 8.00	8.00 x 8.00
D2 MIN. / MAX.	2.75 / 6.80	4.35 / 4.65
E2 MIN. / MAX.	2.75 / 6.80	5.05 / 5.35
L MIN. / MAX.	0.30 / 0.50	0.30 / 0.50

Ordering Information

Part / Order Number	Shipping Packaging	Package	Temperature
954226AGLF	Tubes	56-pin TSSOP	0 to +70° C
954226AGLFT	Tape and Reel	56-pin TSSOP	0 to +70° C
954226AKLF	Tubes	56-pin MLF	0 to +70° C
954226AKLFT	Tape and Reel	56-pin MLF	0 to +70° C

"LF" to the suffix are the Pb-Free configuration and are RoHS compliant.
"A" is the device revision designator (will not correlate with the datasheet revision).

Revision History

Rev.	Issue Date	Who	Description	Page #
0.1	3/29/2005	JC	Updated Ordering Information from "Lead Free" to "Annealed Lead Free"	18
0.2	7/14/2006	DC	Added MLF Pinout, Pin Description and Ordering Information.	1, 4, 5, 21
A	4/12/2010	RDW	1. Clean up Electrical Tables 2. Corrected Test Clarification Table 3. Move to final	