

SANYO

No.2330D

LC7942A

CMOS LSI

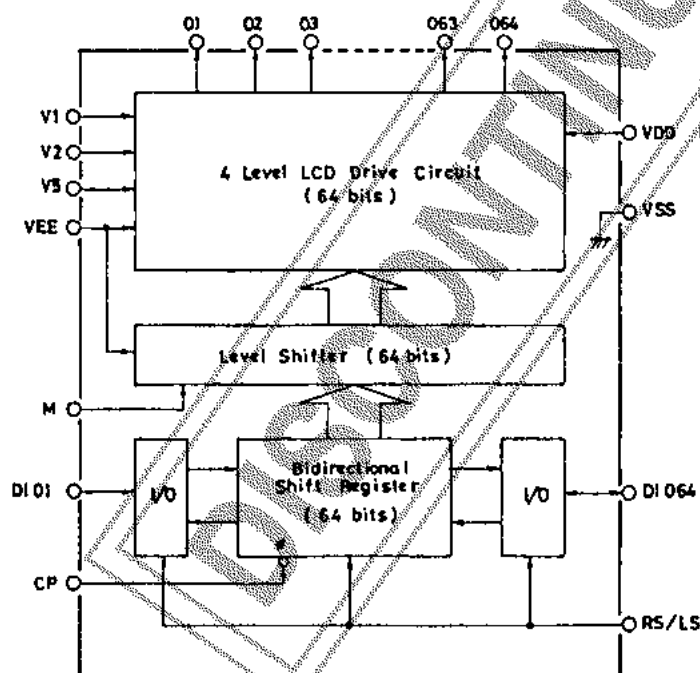
Dot Matrix LCD Drivers

Overview

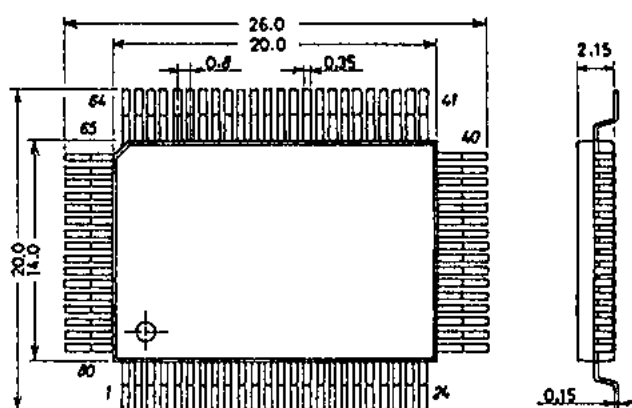
The LC7942A is a large-scale dot matrix LCD segment driver LSI. The LC7942A contains a 64-bit bidirectional shift register and a 4-level LCD driver. The input/output pins for cascade connection can be used to further increase the number of bits. The LC7942A can be used in conjunction with segment driver LC7940A or LC7941A (QIP100) to drive a wide-screen LCD panel and provide high-density packaging.

Features

- On-chip LCD drive circuit (64 bits)
- Display duty : 1/64 to 1/128
- On-chip input/output pins used to further increase the number of bits
- Possible to apply the bias voltage externally
- Operating voltage/operating temperature
 - V_{DD} (logic section) : $5V \pm 10\%$ / -20 to $+85^{\circ}\text{C}$
 - $V_{DD} - V_{EE}$ (LCD section) : V_{DD} to $20V$ / -20 to $+85^{\circ}\text{C}$
- CMOS process
- 80-pin flat plastic package

Equivalent Circuit Block Diagram**Package Dimensions 3044B**

(unit : mm)



Specifications and information herein are subject to change without notice.

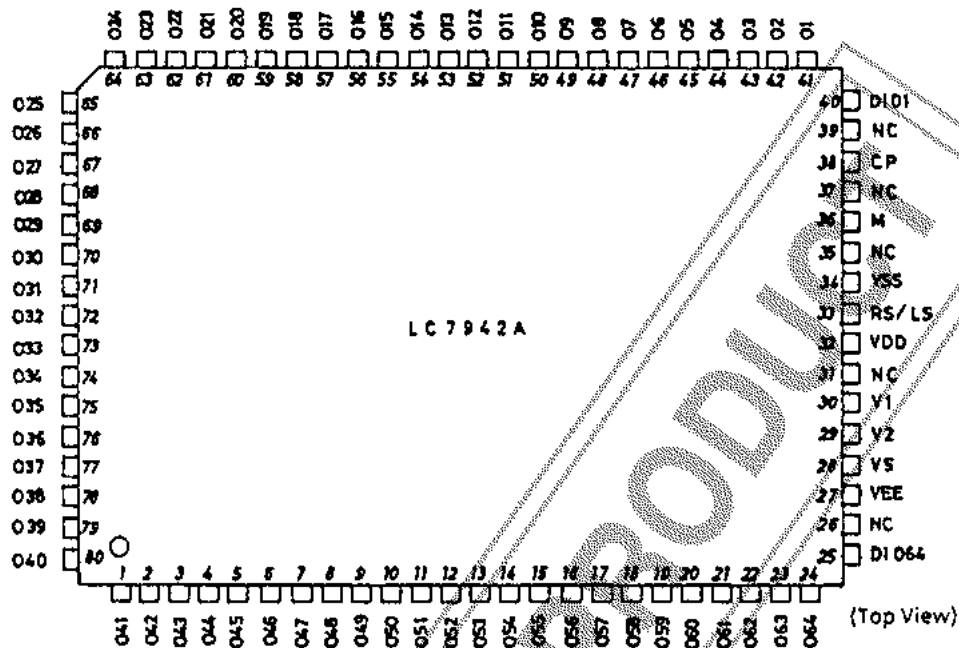
SANYO Electric Co., Ltd. Semiconductor Business Headquarters

TOKYO OFFICE Tokyo Bldg., 1-10, 1 Chome, Ueno, Taito-ku, TOKYO, 110 JAPAN

91494TH/2270TA/1118AT/N136KI,TS No.2230-1/4

LC7942A

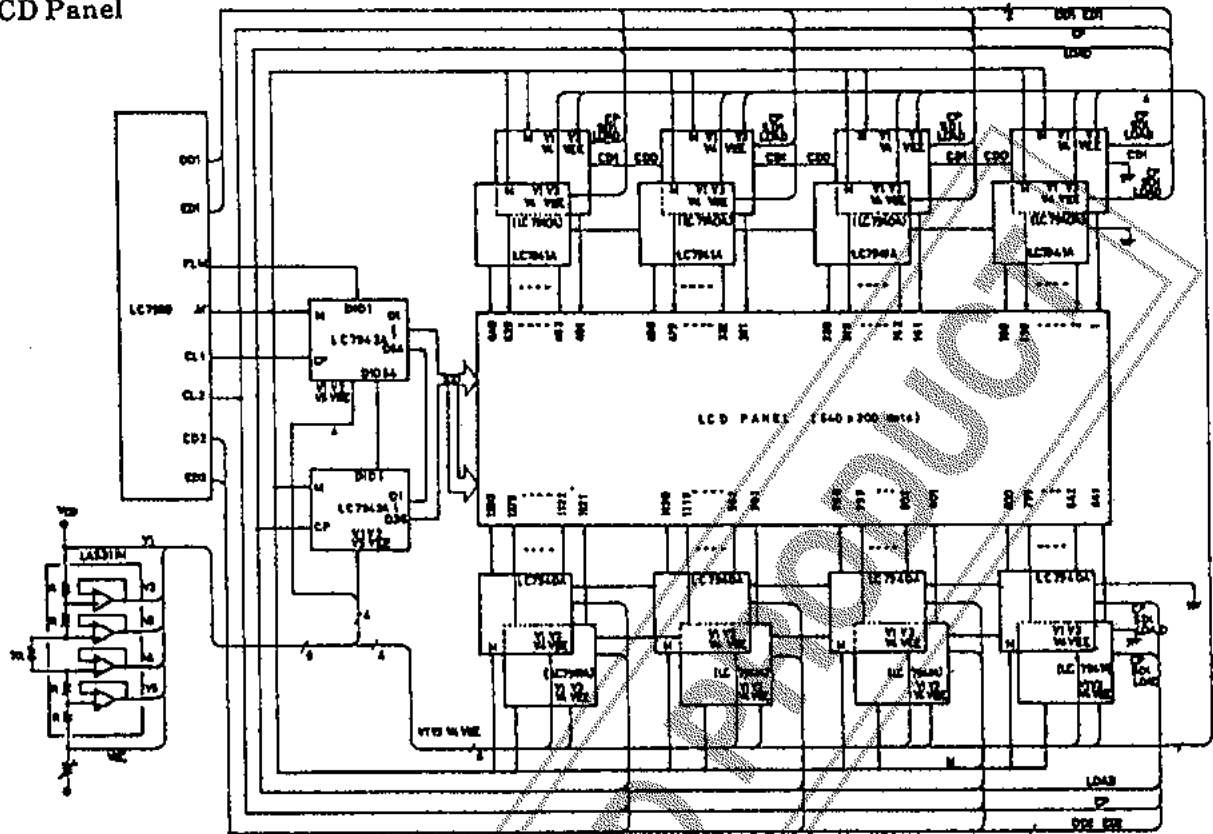
Pin Assignment



Pin Description

Pin Number	Pin Name	Input/Output	Function												
32 34 27	VDD VSS VEE	Power supply	VDD to VSS Power supply for logic section VDD to VEE Power supply for LCD section												
30 29 28	V1 V2 V5	Power supply	Power supply for LCD drive level V1, VEE : Select level V2, V5 : Nonselect level												
38	CP	Input	Bidirectional shift register shift clock (triggering on the trailing edge)												
40 25 33	D101 D1064 RS/LS	Input/output Input	<table><tr><th>RS/LS</th><th>D101</th><th>D1064</th><th>Shift direction</th></tr><tr><td>L</td><td>Input</td><td>Output</td><td>O1→O64</td></tr><tr><td>H</td><td>Output</td><td>Input</td><td>O64→O1</td></tr></table>	RS/LS	D101	D1064	Shift direction	L	Input	Output	O1→O64	H	Output	Input	O64→O1
RS/LS	D101	D1064	Shift direction												
L	Input	Output	O1→O64												
H	Output	Input	O64→O1												
36	M	Input	Signal to cause LCD drive output to alternate												
41 to 80 1 to 24	O1 to O40 O41 to O64	Output	LCD driver output The combination of scan data and M signal provides the following output levels. <table><tr><th>Data \ M</th><th>"H"</th><th>"L"</th></tr><tr><th>"H"</th><td>V1</td><td>VEE</td></tr><tr><th>"L"</th><td>V5</td><td>V2</td></tr></table>	Data \ M	"H"	"L"	"H"	V1	VEE	"L"	V5	V2			
Data \ M	"H"	"L"													
"H"	V1	VEE													
"L"	V5	V2													

LCD Panel



Absolute Maximum Ratings at $T_a = 25 \pm 2^\circ\text{C}$, $V_{SS} = 0\text{V}$

			unit
Maximum Supply Voltage (LOGIC)	$V_{DD \text{ max}}$	-0.3 to +7.0	V
Maximum Supply Voltage (LCD)	$V_{DD} - V_{EE \text{ max}}$	0 to 22	V
Maximum Input Voltage	$V_{I \text{ max}}$	-0.3 to $V_{DD} + 0.3$	V
Operating Temperature	T_{opg}	-20 to +85	$^\circ\text{C}$
Storage Temperature	T_{stg}	-40 to +125	$^\circ\text{C}$

Note: With $V_{DD} \geq V_1 > V_2 > V_5 > V_{EE}$ held

When mounting the QIP package on the board, do not dip it in solder.

Allowable Operating Conditions at $T_a = -20$ to $+85^\circ\text{C}$, $V_{SS} = 0\text{V}$

		min	typ	max	unit
Supply Voltage (LOGIC)	V_{DD}	4.5		5.5	V
Supply Voltage (LCD)	$V_{DD} - V_{EE}$			20	V
Input 'H'-Level Voltage	V_{IH}	$0.8V_{DD}$			V
Input 'L'-Level Voltage	V_{IL}		$0.2V_{DD}$		V
CP (Shift) Clock	f_{CP}			1	MHz
CP Pulse Width	t_{WC}	125			ns
Setup Time	t_{SETUP}	100			ns
Hold Time	t_{HOLD}	100			ns
Rise/Fall Time	t_R			50	ns
	t_F			50	ns

Electrical Characteristics at $T_a = 25 \pm 2^\circ\text{C}$, $V_{SS} = 0\text{V}$, $V_{DD} = 5\text{V} \pm 0\%$

		min	typ	max	unit
Input 'H'-Level Current	I_{IH}			1	μA
	$V_{IN} = V_{DD}$				
	DIO1, DIO64, CP, M, RS/LS				
Input 'L'-Level Current	I_{IL}	-1			μA
	$V_{IN} = V_{SS}$				
	DIO1, DIO64, CP, M, RS/LS				
Output 'H'-Level Voltage	V_{OH}		$V_{DD} - 0.4$		V
	$I_{OH} = -0.4\text{mA}$,				
	DIO1, DIO64				
Output 'L'-Level Voltage	V_{OL}			0.4	V
	$I_{OL} = 0.4\text{mA}$,				
	DIO1, DIO64				

Continued on next page.

LC7942A

Continued from preceding page.

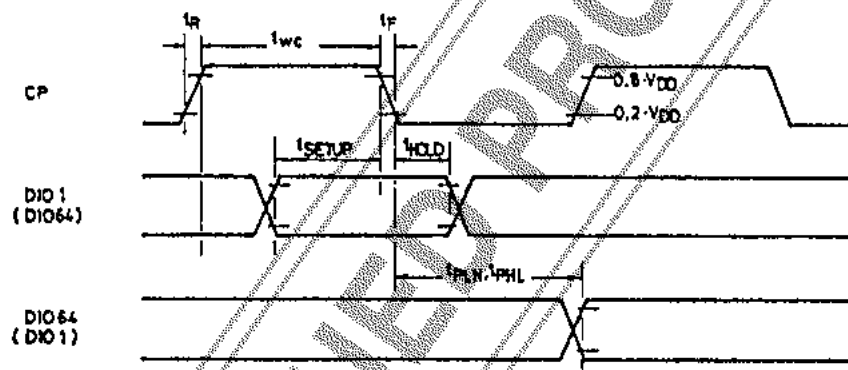
			min	typ	max	unit
Driver ON-State Resistance	R_{ON}	$V_{DD} - V_{EE} = 18V$, $ V_{DE} - V_O = 0.25V$ (Note) (O1 to O64)			1.5	$k\Omega$
Quiescent Current	I_{DD}	$V_{DD} - V_{EE} = 18V$, CP = DC			100	μA
Input Capacitance	C_I	$f = 1MHz$		5		pF

(Note) : $V_{DE} = V_{DD}$ to V_{EE} , $V_1 = V_{DD}$, $V_2 = 10/11 (V_{DD} - V_{EE})$, $V_5 = 1/11 (V_{DD} - V_{EE})$

Switching Characteristics

		min	typ	max	unit
Output Delay Time	t_{PLH}			250	ns
	t_{PHL}			250	ns

Switching Characteristic



Information (including circuit diagrams and circuit parameters) herein is for example only; it is not guaranteed for volume production. SANYO believes information herein is accurate and reliable, but no guarantees are made or implied regarding its use or any infringements of intellectual property rights or other rights of third parties.