



SANYO Semiconductors

DATA SHEET

An ON Semiconductor Company

LV8729V — Bi-CMOS LSI PWM Constant-Current Control Stepping Motor Driver

Overview

The LV8729V is a PWM current-controlled microstep bipolar stepping motor driver.

This driver can perform eight times of excitation of the second phase to 32W1-second phase and can drive simply by the CLK input.

Features

- Single-channel PWM current control stepping motor driver.
- BiCDMOS process IC.
- Output on-resistance (upper side : 0.35Ω ; lower side : 0.3Ω ; total of upper and lower : 0.65Ω ; Ta = 25°C, IO = 1.8A)
- 2-phase, 1-2 phase, W1-2 phase, 2W1-2 phase, 4W1-2 phase, 8W1-2 phase, 16W1-2 phase, 32W1-2 phase excitation are selectable.
- Advance the excitation step with the only step signal input.
- Available forward reverse control.
- Over current protection circuit.
- Thermal shutdown circuit.
- Input pull down resistance
- With reset pin and enable pin.

Specifications

Absolute Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	VM max		36	V
Maximum output peak current	IO max		1.8	A
Maximum logic input voltage	VIN max		6	V
Maximum VREF input voltage	VREF max		6	V
Maximum MO input voltage	VMO max		6	V

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Parameter	Symbol	Conditions	Ratings	Unit
Maximum DOWN input voltage	$V_{\text{DOWN max}}$		6	V
Allowable power dissipation	$P_{\text{d max}}$	*	3.85	W
Operating temperature	T_{opr}		-30 to +85	°C
Storage temperature	T_{stg}		-55 to +150	°C

* Specified circuit board : 90.0mm×90.0mm×1.6mm, glass epoxy 2-layer board, with backside mounting.

Allowable Operating Ratings at $T_a = 25^\circ\text{C}$

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage range	V_M		9 to 32	V
Logic input voltage	V_{IN}		0 to 5	V
VREF input voltage range	V_{REF}		0 to 3	V

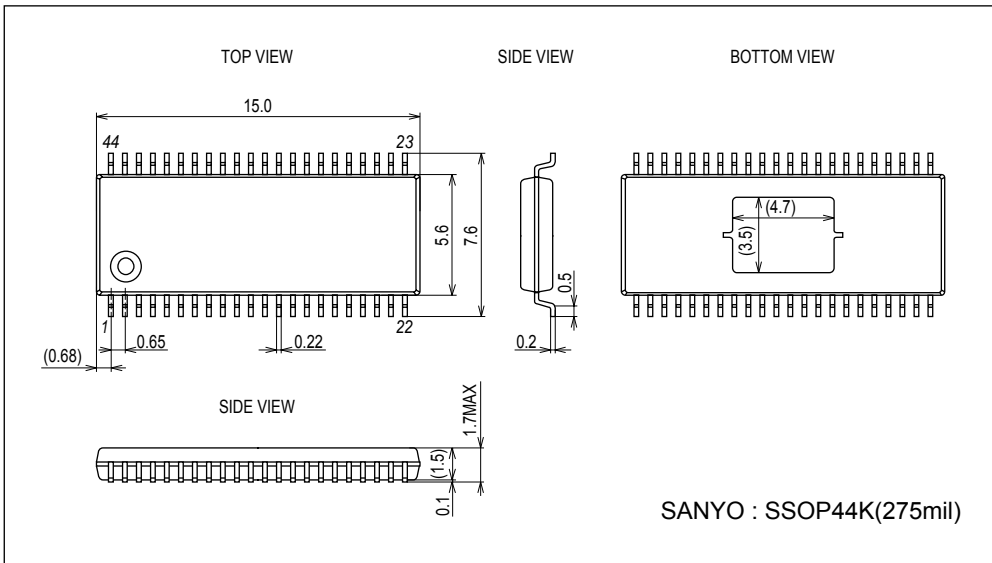
Electrical Characteristics at $T_a = 25^\circ\text{C}$, $V_M = 24\text{V}$, $V_{\text{REF}} = 1.5\text{V}$

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Standby mode current drain	I_{Mst}	ST = "L"		70	100	μA
Current drain	I_{M}	ST = "H", OE = "H", no load		3.3	4.6	mA
Thermal shutdown temperature	TSD	Design guarantee	150	180	200	°C
Thermal hysteresis width	ΔTSD	Design guarantee		40		°C
Logic pin input current	I_{INL}	$V_{\text{IN}} = 0.8\text{V}$	3	8	15	μA
	I_{INH}	$V_{\text{IN}} = 5\text{V}$	30	50	70	μA
Logic high-level input voltage	V_{INH}		2.0			V
Logic low-level input voltage	V_{INL}				0.8	V
Chopping frequency	F_{ch}	$\text{Cosc1} = 100\text{pF}$	70	100	130	kHz
OSC1 pin charge/discharge current	I_{osc1}		7	10	13	μA
Chopping oscillation circuit threshold voltage	V_{tup1}		0.8	1	1.2	V
	V_{tdown1}		0.3	0.5	0.7	V
VREF pin input voltage	I_{ref}	$V_{\text{REF}} = 1.5\text{V}$	-0.5			μA
DOWN output residual voltagr	V_{O1DOWN}	$I_{\text{down}} = 1\text{mA}$		40	100	mV
MO pin residual voltage	V_{O1MO}	$I_{\text{mo}} = 1\text{mA}$		40	100	mV
Hold current switching frequency	F_{down}	$\text{Cosc2} = 1500\text{pF}$	1.12	1.6	2.08	Hz
Hold current switching frequency threshold voltage	V_{tup2}		0.8	1	1.2	V
	V_{tdown2}		0.3	0.5	0.7	V
VREG1 output voltage	V_{reg1}		4.7	5	5.3	V
VREG2 output voltage	V_{reg2}	V_M	18	19	20	V
Output on-resistance	R_{onU}	$I_{\text{O}} = 1.8\text{A}$, high-side ON resistance		0.35	0.455	Ω
	R_{onD}	$I_{\text{O}} = 1.8\text{A}$, low-side ON resistance		0.3	0.39	Ω
Output leakage current	I_{Oleak}	$V_M = 36\text{V}$			50	μA
Diode forward voltage	V_{D}	$I_{\text{D}} = -1.8\text{A}$		1	1.4	V
Current setting reference voltage	V_{RF}	$V_{\text{REF}} = 1.5\text{V}$, Current ratio 100%	0.285	0.3	0.315	V

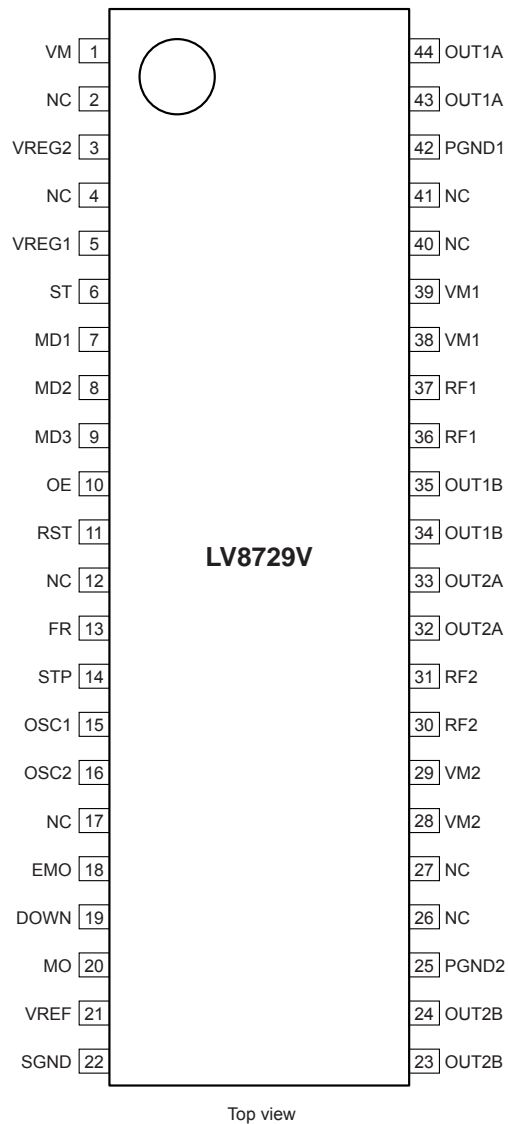
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Package Dimensions

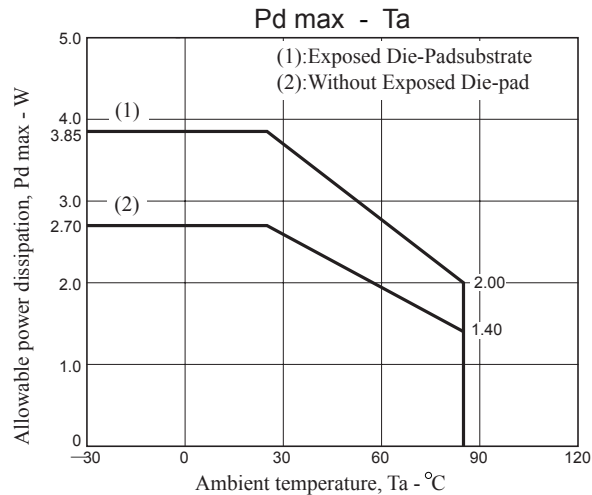
unit : mm (typ)
3333



Pin Assignment

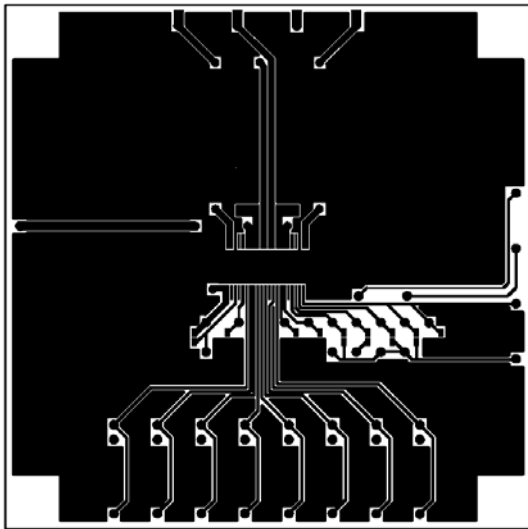


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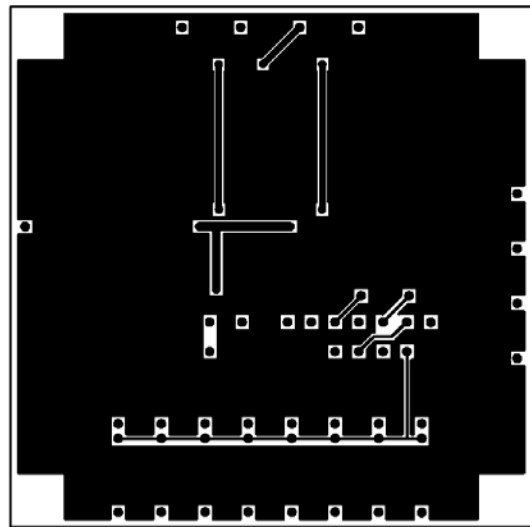


Substrate Specifications (Substrate recommended for operation of LV8729V)

Size : 90mm × 90mm × 1.6mm (two-layer substrate [2S0P])
Material : Glass epoxy
Copper wiring density : L1 = 85% / L2 = 90%



L1 : Copper wiring pattern diagram



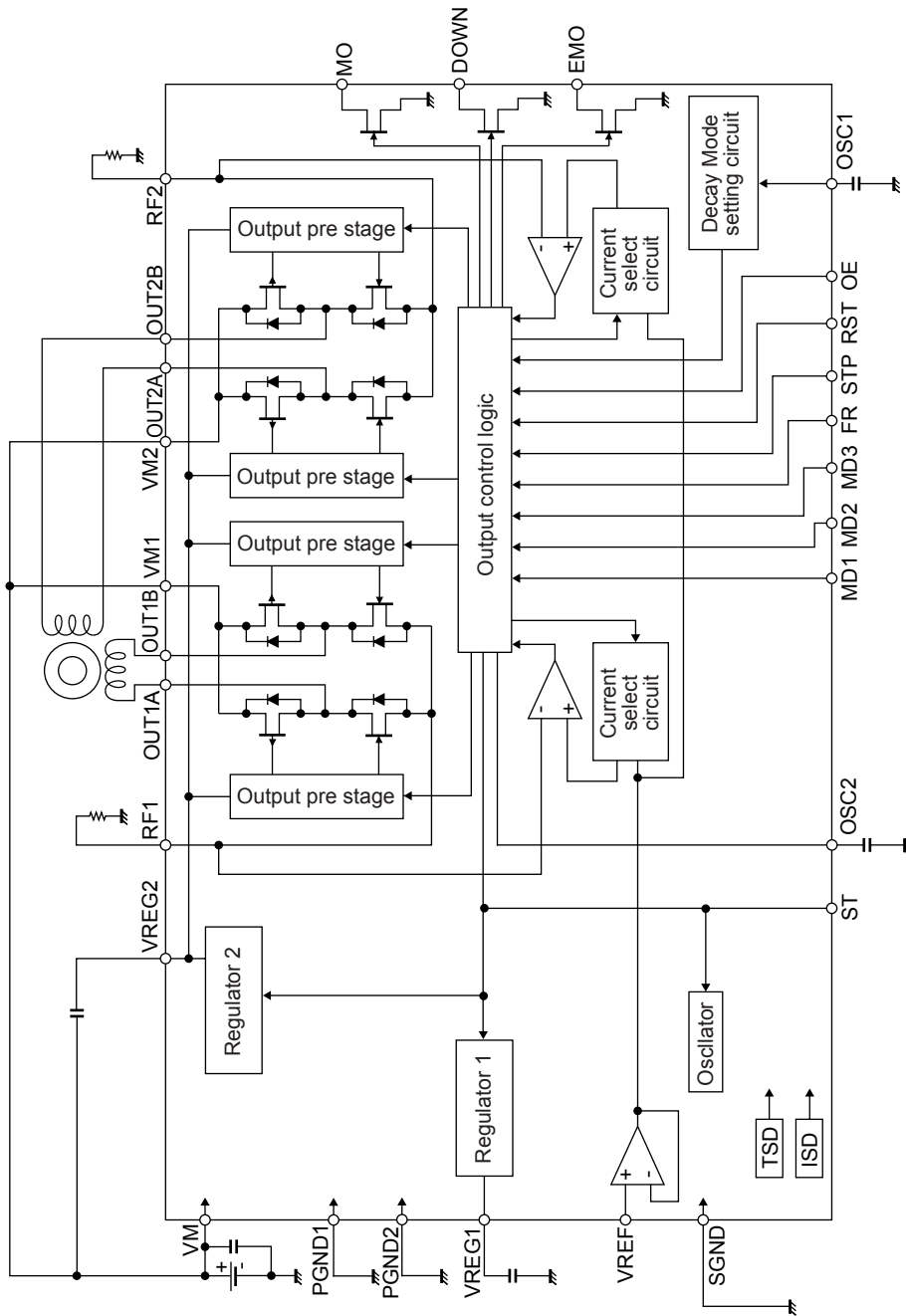
L2 : Copper wiring pattern diagram

Cautions

- 1) The data for the case with the Exposed Die-Pad substrate mounted shows the values when 90% or more of the Exposed Die-Pad is wet.
- 2) For the set design, employ the derating design with sufficient margin.
Stresses to be derated include the voltage, current, junction temperature, power loss, and mechanical stresses such as vibration, impact, and tension.
Accordingly, the design must ensure these stresses to be as low or small as possible.
The guideline for ordinary derating is shown below :
 - (1) Maximum value 80% or less for the voltage rating
 - (2) Maximum value 80% or less for the current rating
 - (3) Maximum value 80% or less for the temperature rating
- 3) After the set design, be sure to verify the design with the actual product.
Confirm the solder joint state and verify also the reliability of solder joint for the Exposed Die-Pad, etc.
Any void or deterioration, if observed in the solder joint of these parts, causes deteriorated thermal conduction, possibly resulting in thermal destruction of IC.

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Block Diagram



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Pin Functions

Pin No.	Pin Name	Pin Function	Equivalent Circuit
7 8 9 10 11 13 14	MD1 MD2 MD3 OE RST FR STP	Excitation mode switching pin Excitation mode switching pin Excitation mode switching pin Output enable signal input pin Reset signal input pin Forward / Reverse signal input pin Step clock pulse signal input pin	
6	ST	Chip enable pin.	
23, 24 25 28, 29 30, 31 32, 33 34, 35 36, 37 38, 39 42 43, 44	OUT2B PGND2 VM2 RF2 OUT2A OUT1B RF1 VM1 PGND1 OUT1A	Channel 2 OUTB output pin. Channel 2 Power system ground Channel 2 motor power supply connection pin. Channel 2 current-sense resistor connection pin. Channel 2 OUTA output pin. Channel 1 OUTB output pin. Channel 1 current-sense resistor connection pin. Channel 1 motor power supply pin. Channel 1 Power system ground Channel 1 OUTA output pin.	
21	VREF	Constant-current control reference voltage input pin.	

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
Pin No.	Pin Name	Pin Function	Equivalent Circuit
3	VREG2	Internal regulator capacitor connection pin.	
5	VREG1	Internal regulator capacitor connection pin.	
18 19 20	EMO DOWN MO	Over-current detection alarm output pin. Holding current output pin. Position detecting monitor pin.	
15 16	OSC1 OSC2	Copping frequency setting capacitor connection pin. Holding current detection time setting capacitor connection pin.	

Reference describing operation

(1) Stand-by function

When ST pin is at low levels, the IC enters stand-by mode, all logic is reset and output is turned OFF.
When ST pin is at high levels, the stand-by mode is released.

(2) STEP pin function

Input		Operating mode
ST	STP	
Low	*	Standby mode
High		Excitation step proceeds
High		Excitation step is kept

(3) Excitation setting method

Set the excitation setting as shown in the following table by setting MD1 pin, MD2 pin and MD3 pin.

Input			Mode (Excitation)	Initial position	
MD3	MD2	MD1		1ch current	2ch current
Low	Low	Low	2 phase	100%	-100%
Low	Low	High	1-2 phase	100%	0%
Low	High	Low	W1-2 phase	100%	0%
Low	High	High	2W1-2 phase	100%	0%
High	Low	Low	4W1-2 phase	100%	0%
High	Low	High	8W1-2 phase	100%	0%
High	High	Low	16W1-2 phase	100%	0%
High	High	High	32W1-2 phase	100%	0%

The initial position is also the default state at start-up and excitation position at counter-reset in each excitation mode.

(4) Output current setting

Output current is set shown below by the VREF pin (applied voltage) and a resistance value between RF1(2) pin and GND.

$$I_{OUT} = (V_{REF} / 5) / R_{F1(2)} \text{ resistance}$$

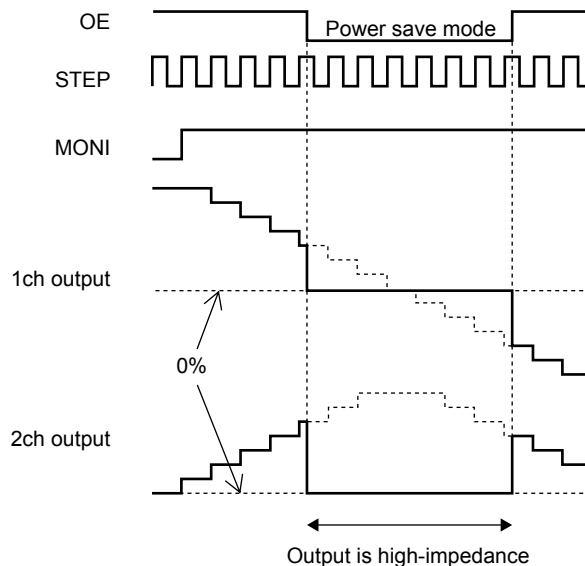
* The setting value above is a 100% output current in each excitation mode.

(Example) When $V_{REF} = 1.1V$ and $R_{F1(2)}$ resistance is 0.22Ω , the setting is shown below.

$$I_{OUT} = (1.1V / 5) / 0.22\Omega = 1.0A$$

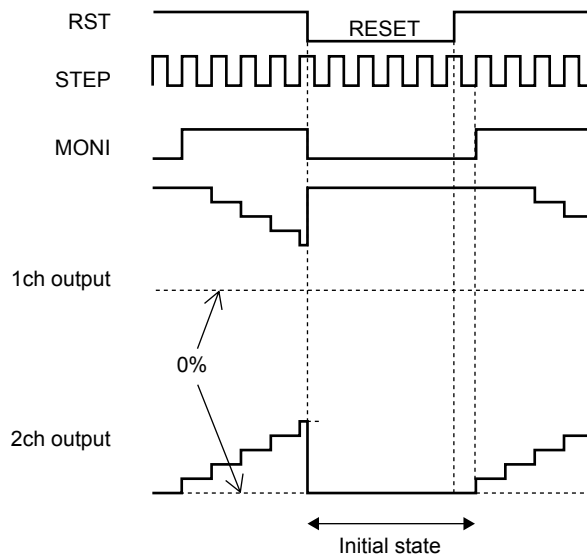
(5) Output enable function

When the OE pin is set Low, the output is forced OFF and goes to high impedance. However, the internal logic circuits are operating, so the excitation position proceeds when the STP is input. Therefore, when OE pin is returned to High, the output level conforms to the excitation position proceeded by the STP input.



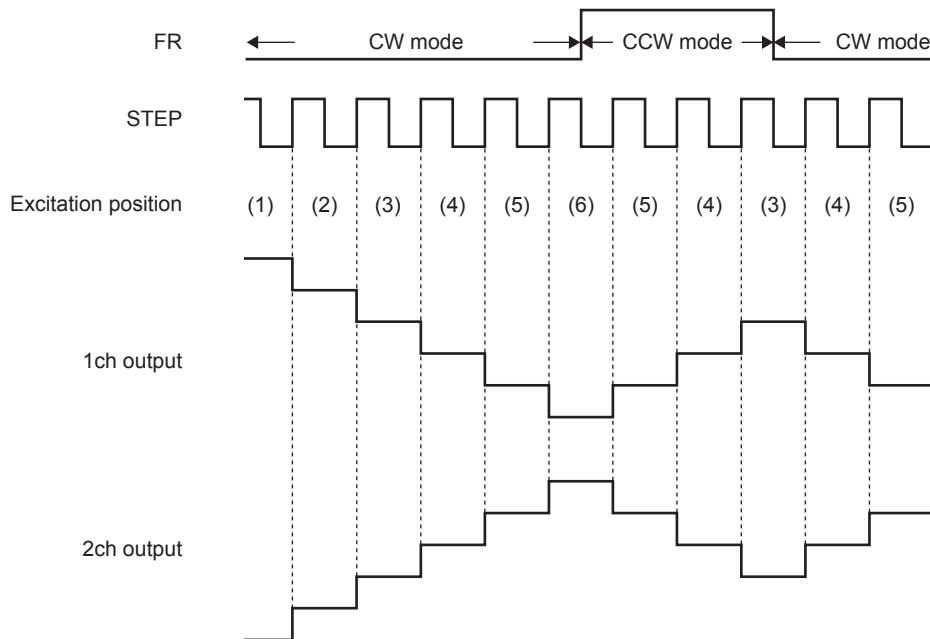
(6) Reset function

When the RST pin is set Low, the output goes to initial mode and excitation position is fixed in the initial position for STP pin and FR pin input. MO pin outputs at low levels at the initial position. (Open drain connection)



(7) Forward / reverse switching function

FR	Operating mode
Low	Clockwise (CW)
High	Counter-clockwise (CCW)



The internal D/A converter proceeds by a bit on the rising edge of the step signal input to the STP pin. In addition, CW and CCW mode are switched by FR pin setting.

In CW mode, the channel 2 current phase is delayed by 90° relative to the channel 1 current.

In CCW mode, the channel 2 current phase is advanced by 90° relative to the channel 1 current.

(8) EMO, DOWN, MO output pin

The output pin is open -drain connection. When it becomes prescribed, it turns on, and each pin outputs the Low level.

Pin state	EMO	DOWN	MO
Low	At detection of over-current	Holding current state	Initial position
OFF	Normal state	Normal state	Non initial position

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(9) Chopping frequency setting function

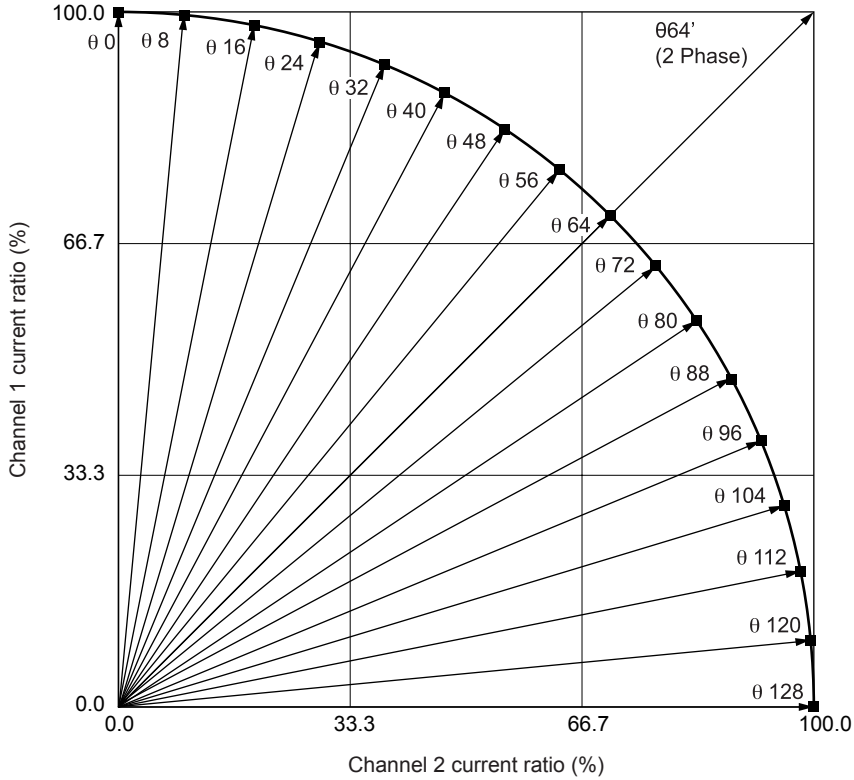
Chopping frequency is set as shown below by a capacitor between OSC1 pin and GND.

$$F_{cp} = 1 / (C_{osc1} / 10 \times 10^{-6}) \text{ (Hz)}$$

(Example) When $C_{osc1} = 200\text{pF}$, the chopping frequency is shown below.

$$F_{cp} = 1 / (200 \times 10^{-12} / 10 \times 10^{-6}) = 50\text{(kHz)}$$

(10) Output current vector locus (one step is normalized to 90 degrees)



Current setting ratio in each excitation mode

STEP	32W1-2 phase(%)		16W1-2 phase(%)		8W1-2 phase(%)		4W1-2 phase(%)		2W1-2 phase (%)		W1-2 phase (%)		1-2 phase (%)		2 phase (%)	
	1ch	2ch	1ch	2ch	1ch	2ch	1ch	2ch	1ch	2ch	1ch	2ch	1ch	2ch	1ch	2ch
00	100	0	100	0	100	0	100	0	100	0	100	0	100	0		
01	100	1														
02	100	2	100	2												
03	100	4														
04	100	5	100	5	100	5										
05	100	6														
06	100	7	100	7												
07	100	9														
08	100	10	100	10	100	10	100	10								
09	99	11														
010	99	12	99	12												
011	99	13														
012	99	15	99	15	99	15										
013	99	16														
014	99	17	99	17												
015	98	18														
016	98	20	98	20	98	20	98	20	98	20						
017	98	21														
018	98	22	98	22												
019	97	23														
020	97	24	97	24	97	24										
021	97	25														
022	96	27	96	27												
023	96	28														
024	96	29	96	29	96	29	96	29								
025	95	30														

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STEP	32W1-2 phase		16W1-2 phase		8W1-2 phase		4W1-2 phase		2W1-2 phase		W1-2 phase (%)		1-2 phase (%)		2 phase (%)	
	1ch	2ch	1ch	2ch	1ch	2ch	1ch	2ch	1ch	2ch	1ch	2ch	1ch	2ch	1ch	2ch
026	95	31	95	31												
027	95	33														
028	94	34	94	34	94	34										
029	94	35														
030	93	36	93	36												
031	93	37														
032	92	38	92	38	92	38	92	38	92	38	92	38				
033	92	39														
034	91	41	91	41												
035	91	42														
036	90	43	90	43	90	43										
037	90	44														
038	89	45	89	45												
039	89	46														
040	88	47	88	47	88	47	88	47								
041	88	48														
042	87	49	87	49												
043	86	50														
044	86	51	86	51	86	51										
045	85	52														
046	84	53	84	53												
047	84	55														
048	83	56	83	56	83	56	83	56	83	56						
049	82	57														
050	82	58	82	58												
051	81	59														
052	80	60	80	60	80	60										
053	80	61														
054	79	62	79	62												
055	78	62														
056	77	63	77	63	77	63	77	63								
057	77	64														
058	76	65	76	65												
059	75	66														
060	74	67	74	67	74	67										
061	73	68														
062	72	69	72	69												
063	72	70														
064	71	71	71	71	71	71	71	71	71	71	71	71	71	71	100	100
065	70	72														
066	69	72	69	72												
067	68	73														
068	67	74	67	74	67	74										
069	66	75														
070	65	76	65	76												
071	64	77														
072	63	77	63	77	63	77	63	77								
073	62	78														
074	62	79	62	79												
075	61	80														
076	60	80	60	80	60	80										
077	59	81														
078	58	82	58	82												
079	57	82														
080	56	83	56	83	56	83	56	83	56	83						
081	55	84														
082	53	84	53	84												
083	52	85														
084	51	86	51	86	51	86										
085	50	86														
086	49	87	49	87												
087	48	88														
088	47	88	47	88	47	88	47	88								
089	46	89														
090	45	89	45	89												

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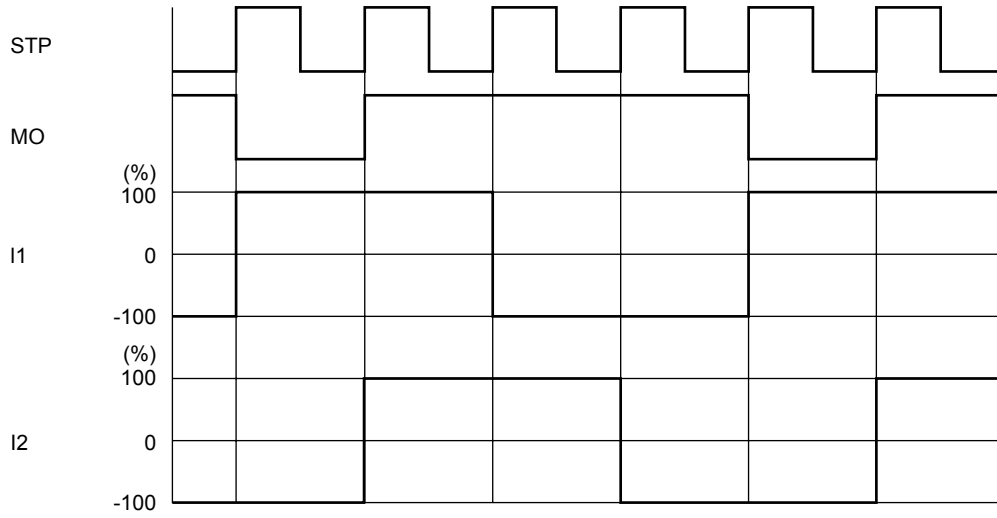
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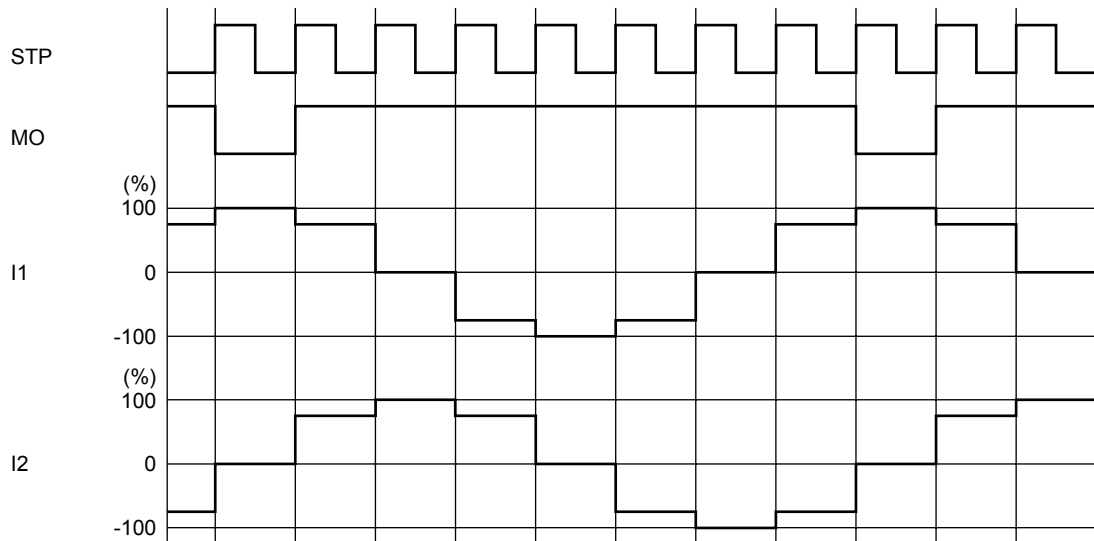
STEP	32W1-2 phase		16W1-2 phase		8W1-2 phase		4W1-2 phase		2W1-2 phase		W1-2 phase (%)		1-2 phase (%)		2 phase (%)	
	1ch	2ch	1ch	2ch	1ch	2ch	1ch	2ch	1ch	2ch	1ch	2ch	1ch	2ch	1ch	2ch
091	44	90														
092	43	90	43	90	43	90										
093	42	91														
094	41	91	41	91												
095	39	92														
096	38	92	38	92	38	92	38	92	38	92	38	92				
097	37	93														
098	36	93	36	93												
099	35	94														
0100	34	94	34	94	34	94										
0101	33	95														
0102	31	95	31	95												
0103	30	95														
0104	29	96	29	96	29	96	29	96								
0105	28	96														
0106	27	96	27	96												
0107	25	97														
0108	24	97	24	97	24	97										
0109	23	97														
0110	22	98	22	98												
0111	21	98														
0112	20	98	20	98	20	98	20	98	20	98						
0113	18	98														
0114	17	99	17	99												
0115	16	99														
0116	15	99	15	99	15	99										
0117	13	99														
0118	12	99	12	99												
0119	11	99														
0120	10	100	10	100	10	100	10	100								
0121	9	100														
0122	7	100	7	100												
0123	6	100														
0124	5	100	5	100	5	100										
0125	4	100														
0126	2	100	2	100												
0127	1	100														
0128	0	100	0	100	0	100	0	100	0	100	0	100	0	100		

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(11) Current wave example in each excitation mode (2 phase, 1-2 phase, 4W1-2 phase, 32W1-2 phase)
2-phase excitation (CW mode)

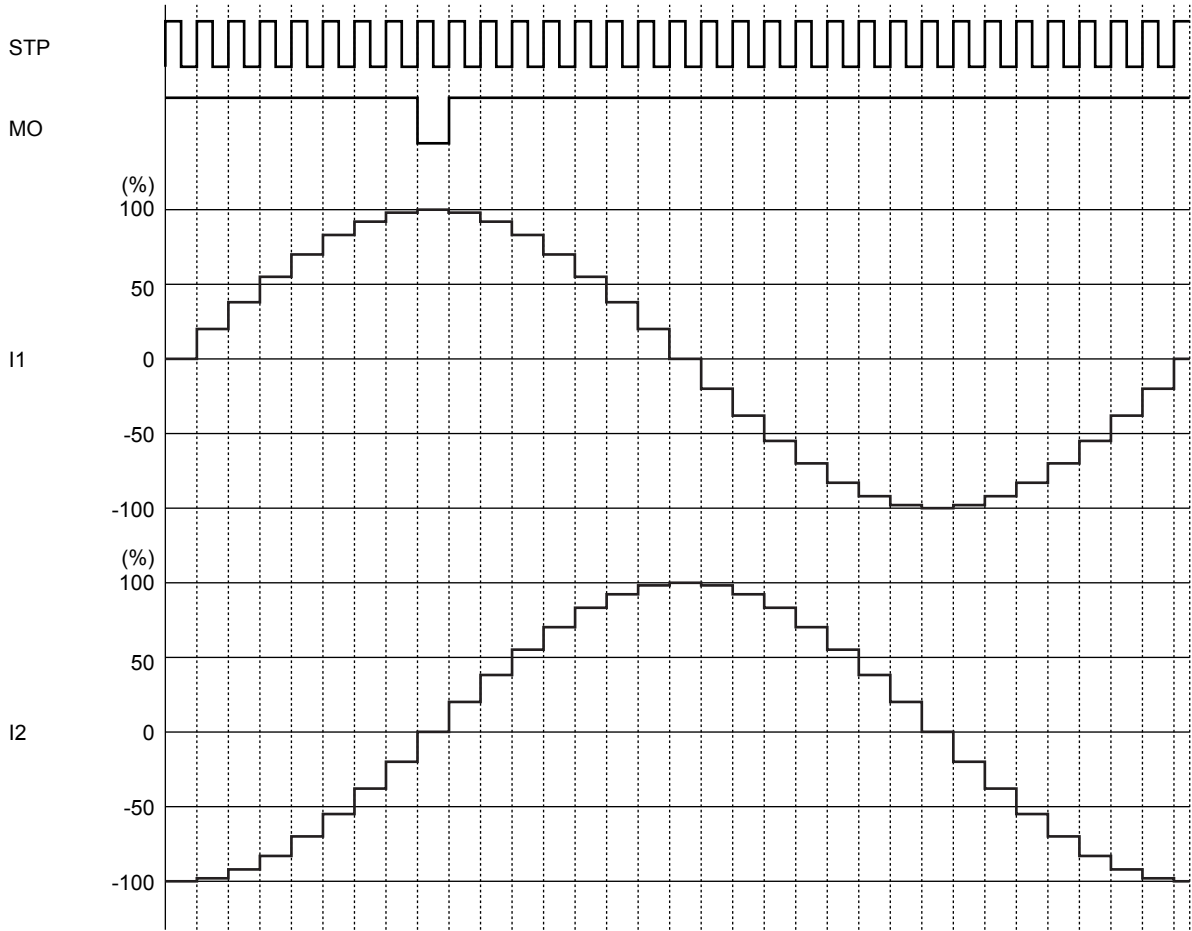


1-2 phase excitation (CW mode)

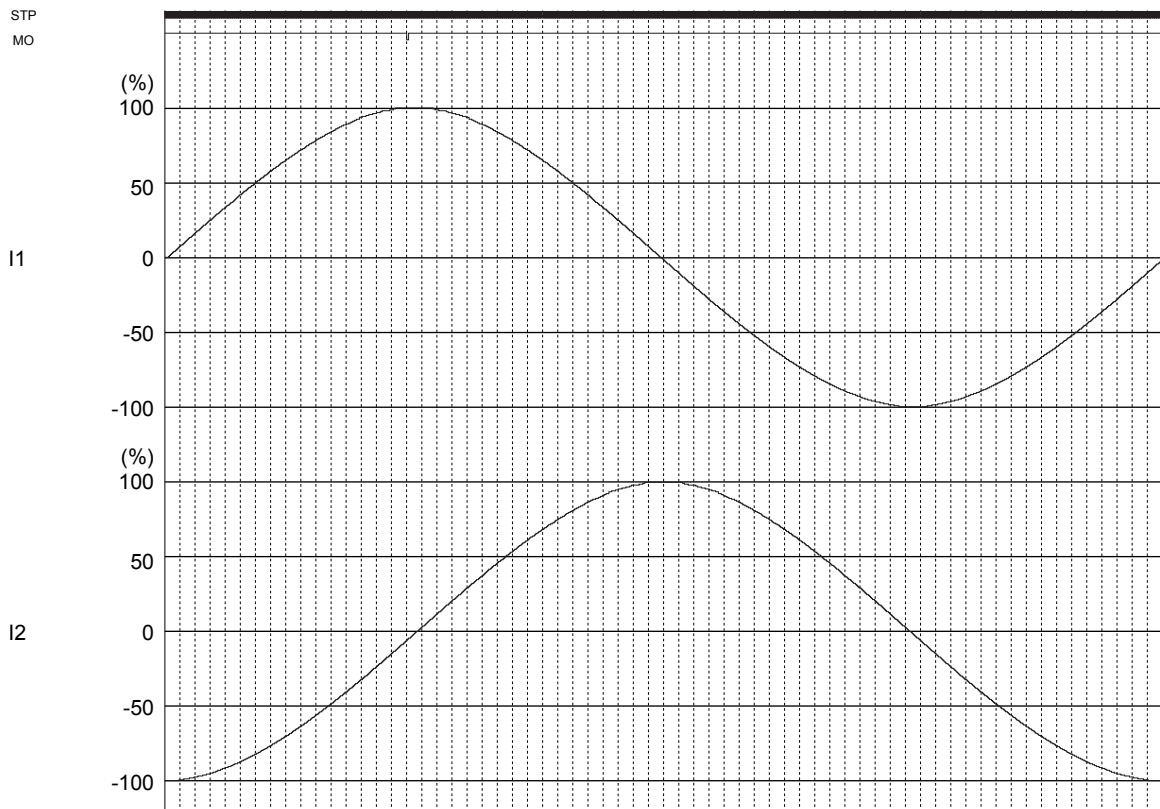


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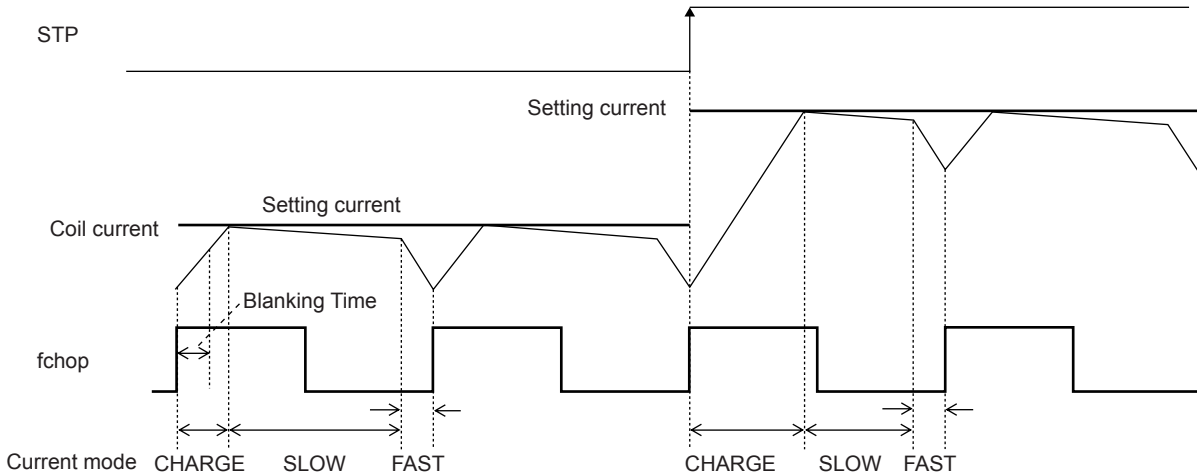
4W1-2 phase excitation (CW mode)



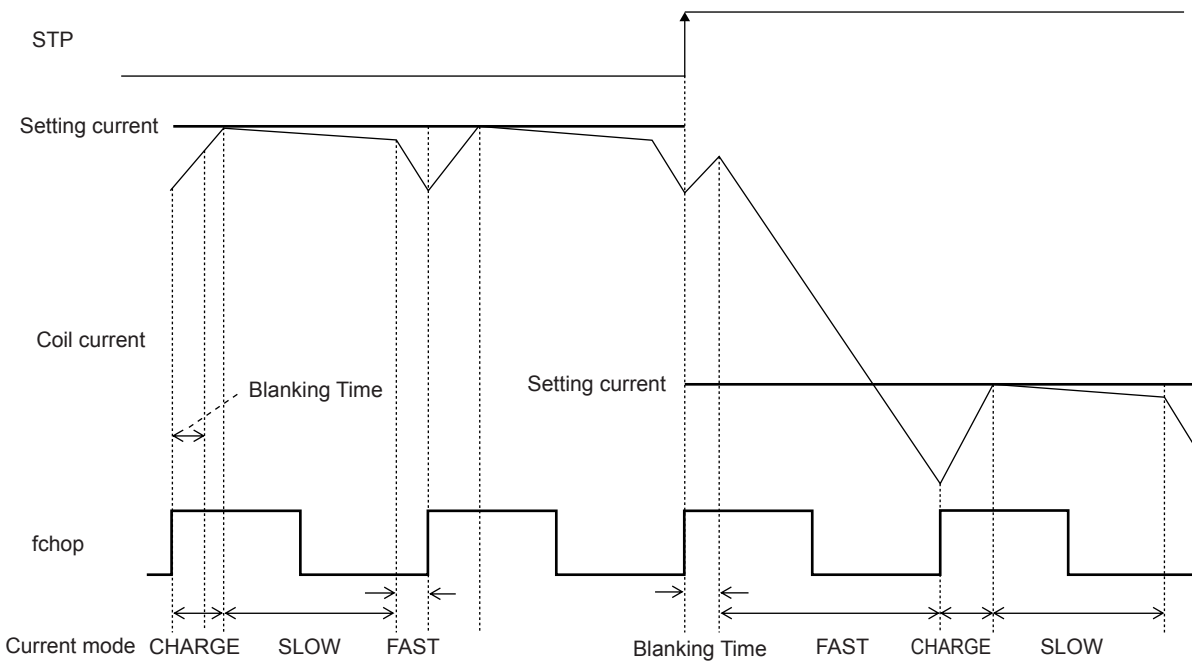
32W1-2 phase excitation (CW mode)



(12) Current control operation
(Sine-wave increasing direction)



(Sine-wave decreasing direction)



Each of current modes operates with the follow sequence.

- The IC enters CHARGE mode at a rising edge of the chopping oscillation. (A period of CHARGE mode (Blanking Time) is forcibly present in approximately $1\mu\text{s}$, regardless of the current value of the coil current (ICOIL) and set current (IREF)).
- In a period of Blanking Time, the coil current (ICOIL) and the setting current (IREF) are compared.
 - If an $\text{ICOIL} < \text{IREF}$ state exists during the charge period:
 - The IC operates in CHARGE mode until $\text{ICOIL} \geq \text{IREF}$. After that, it switches to SLOW DECAAY mode and then switches to FAST DECAAY mode in the last approximately $1\mu\text{s}$ of the period.
 - If no $\text{ICOIL} < \text{IREF}$ state exists during the charge period:
 - The IC switches to FAST DECAAY mode and the coil current is attenuated with the FAST DECAAY operation until the end of a chopping period.

The above operation is repeated. Normally, in the sine wave increasing direction the IC operates in SLOW (+ FAST) DECAAY mode, and in the sine wave decreasing direction the IC operates in FAST DECAAY mode until the current is attenuated and reaches the set value and the IC operates in SLOW (+ FAST) DECAAY mode.

(13) Output short-circuit protection circuit

Built-in output short-circuit protection circuit makes output to enter in stand-by mode. This function prevents the IC from damaging when the output shorts circuit by a voltage short or a ground short, etc. When output short state is detected, short-circuit detection circuit state the operating and output is once turned OFF. Subsequently, the output is turned ON again after the timer latch period (typ. 256 μ s). If the output remains in the short-circuit state, turn OFF the output, fix the output to the wait mode, and turn ON the EMO output.

When output is fixed in stand-by mode by output short protection circuit, output is released the latch by setting ST = "L".

(14) Open-drain pin for switching holding current

The output pin is an open-drain connection.

This pin is turned ON when no rising edge of STP between the input signals while a period determined by a capacitor between OSC2 and GND, and outputs at low levels.

The open-drain output in once turned ON, is turned OFF at the next rising edge of STP.

Holding current switching time (Tdown) is set as shown below by a capacitor between OSC2 pin and GND.

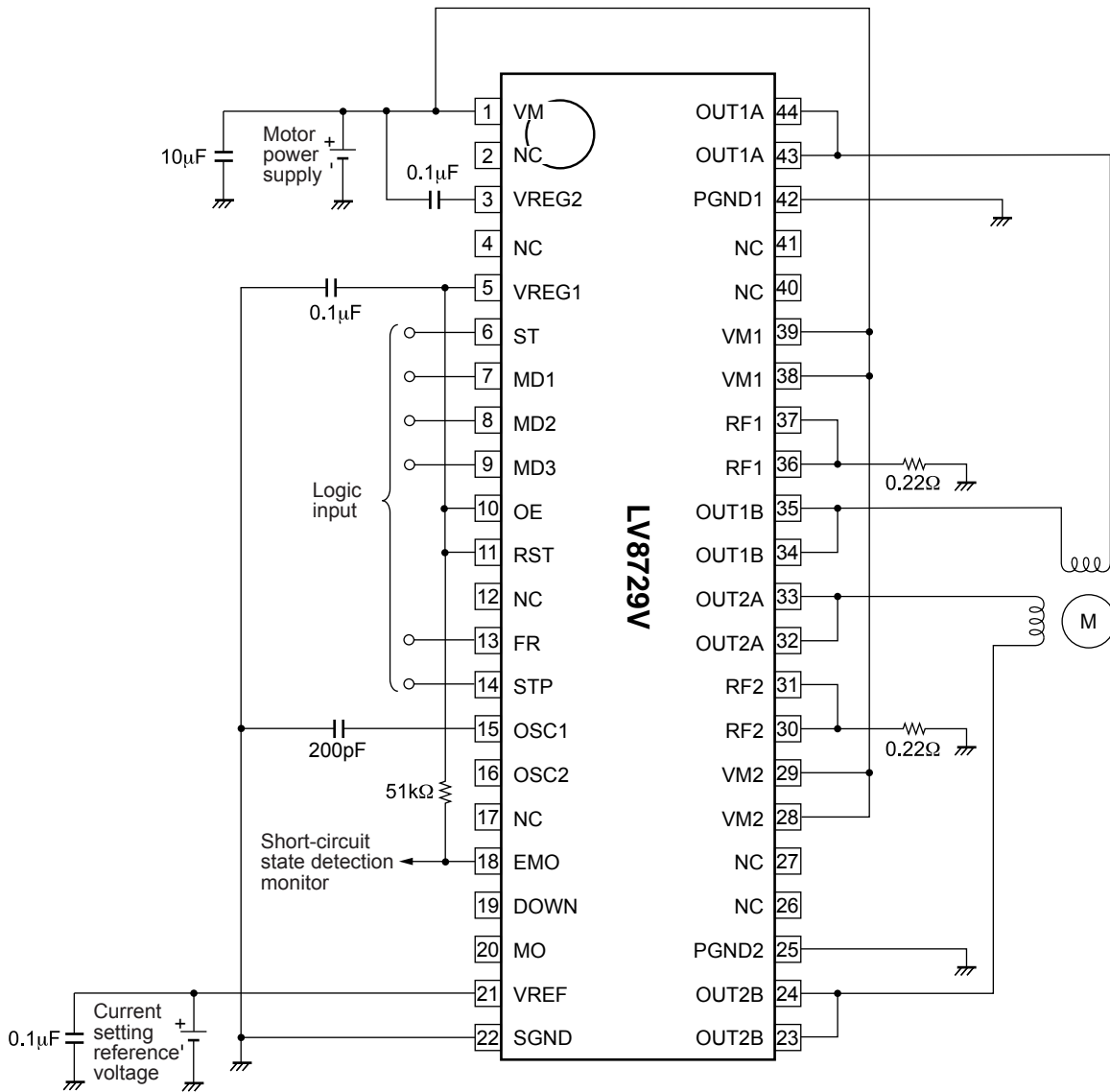
$$T_{\text{down}} = C_{\text{osc2}} \times 0.4 \times 10^9 \text{ (s)}$$

(Example) When C_{osc2} = 1500pF, the holding current switching time is shown below.

$$T_{\text{down}} = 1500\text{pF} \times 0.4 \times 10^9 = 0.6 \text{ (s)}$$

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Application Circuit Example



The above sample application circuit is set to the following conditions:

- Output enable function fixed to the output state (OE = "H")
- Reset function fixed to the output state (RST = "H")
- Chopping frequency : 50kHz (Cosc1 = 200pF)

The set current value is as follows :

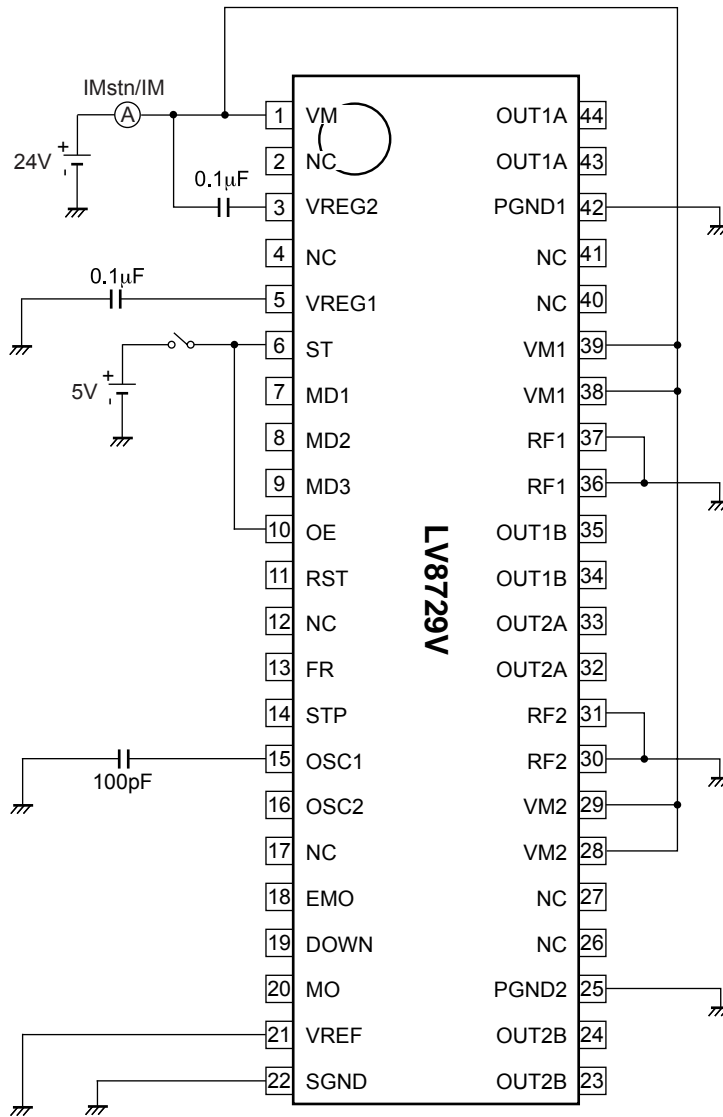
$$I_{OUT} = (\text{Current setting reference voltage} / 5) / 0.22\Omega$$

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Measurement circuit diagram

Stand-by mode current drain : I_{Mstn}

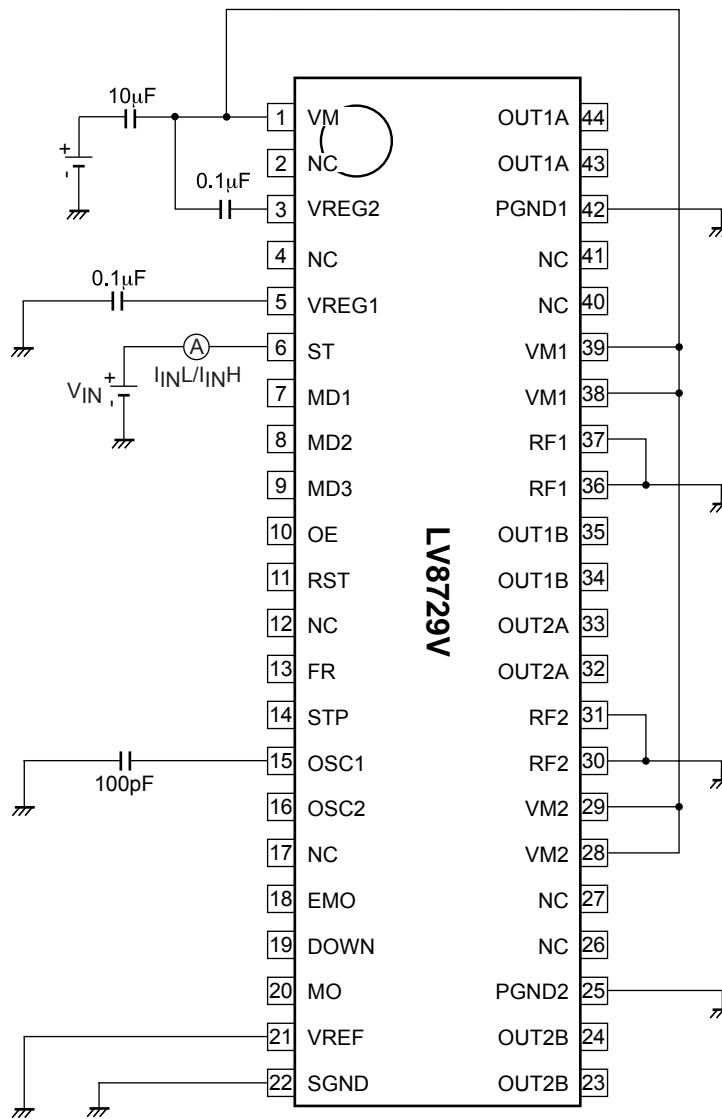
Current drain : I_M



Turn OFF SW when measuring I_{Mstn} .
Turn ON SW when measuring I_M

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Logic pin input current : I_{INL} , I_{INH}



Set $V_{IN} = 0.8V$ when measuring I_{INL} .

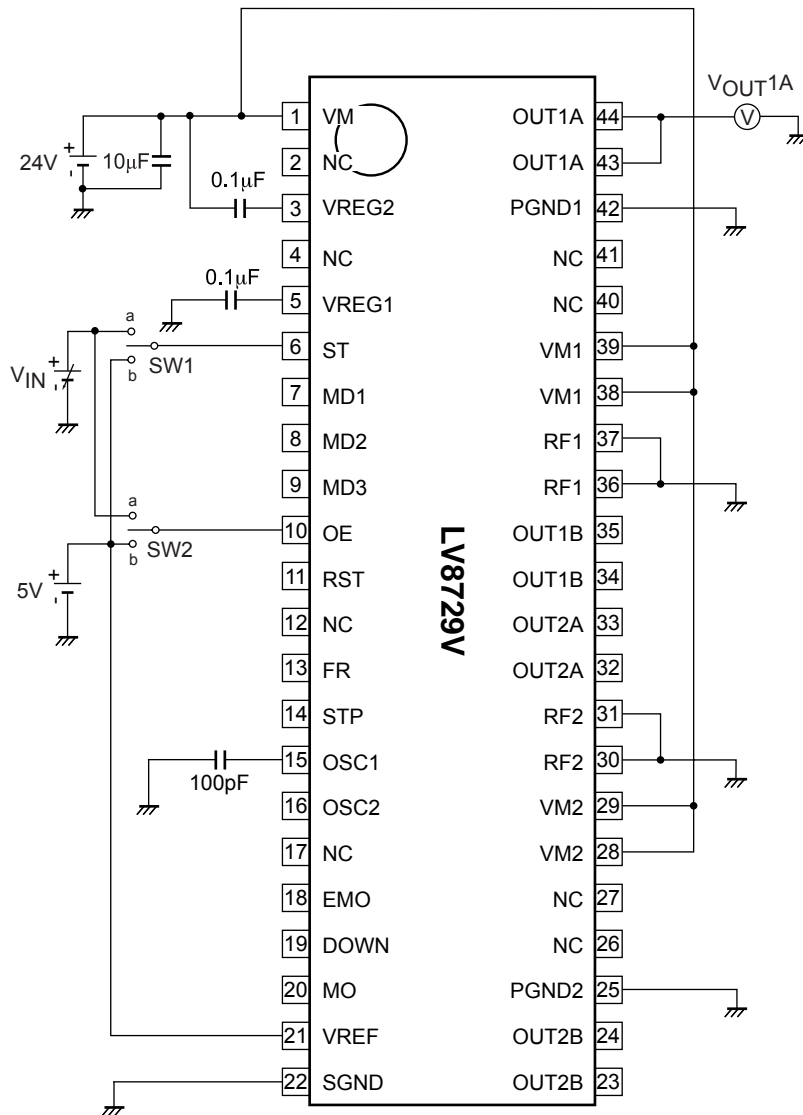
Set $V_{IN} = 5V$ when measuring I_{INH}

This measurement is related to the ST pin. Take the same procedure for measurement of other pins.

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Logic input high-level voltage : V_{INH} (ST, OE)

Logic input low-level voltage : V_{INL} (ST, OE)



To measure the ST pin, set SW1 to the "a" side and SW2 to the "b" side.

To measure the OE pin, set SW1 to the "b" side and SW2 to the "a" side.

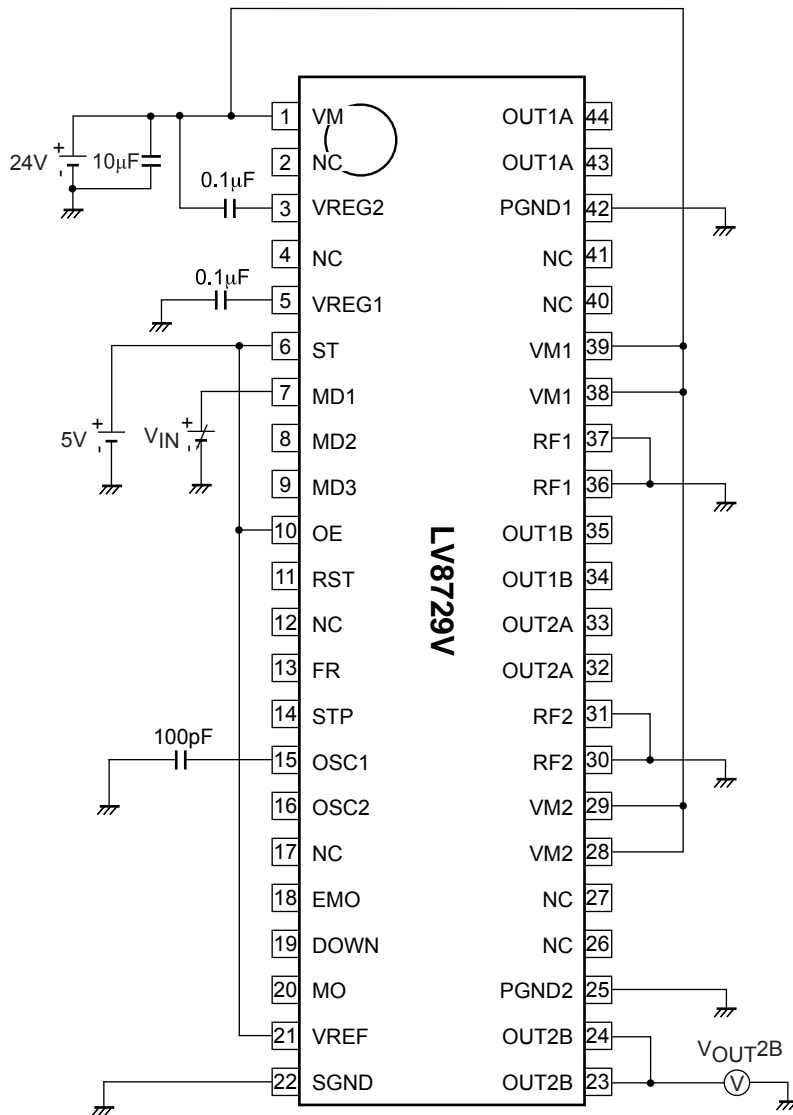
V_{INH} : When V_{IN} is raised gradually from 0V, the V_{OUT1A} voltage changes from "L" to "H". The V_{IN} voltage at which the voltage changes from "L" to "H" is the V_{INH} voltage.

V_{INL} : When V_{IN} is raised gradually from 3V, the V_{OUT1A} voltage changes from "H" to "L". The V_{IN} voltage at which the voltage changes from "H" to "L" is the V_{INL} voltage.

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Logic input high-level voltage : V_{INH} (MD1, MD2, MD3)

Logic input low-level voltage : V_{INL} (MD1, MD2, MD3)



V_{INH} : When V_{IN} is raised gradually from 0V, the V_{OUT2B} voltage changes from "H" to "L". The V_{IN} voltage at which the voltage changes from "H" to "L" is the V_{INH} voltage.

V_{INL} : When V_{IN} is raised gradually from 3V, the V_{OUT2B} voltage changes from "L" to "H". The V_{IN} voltage at which the voltage changes from "L" to "H" is the V_{INL} voltage.

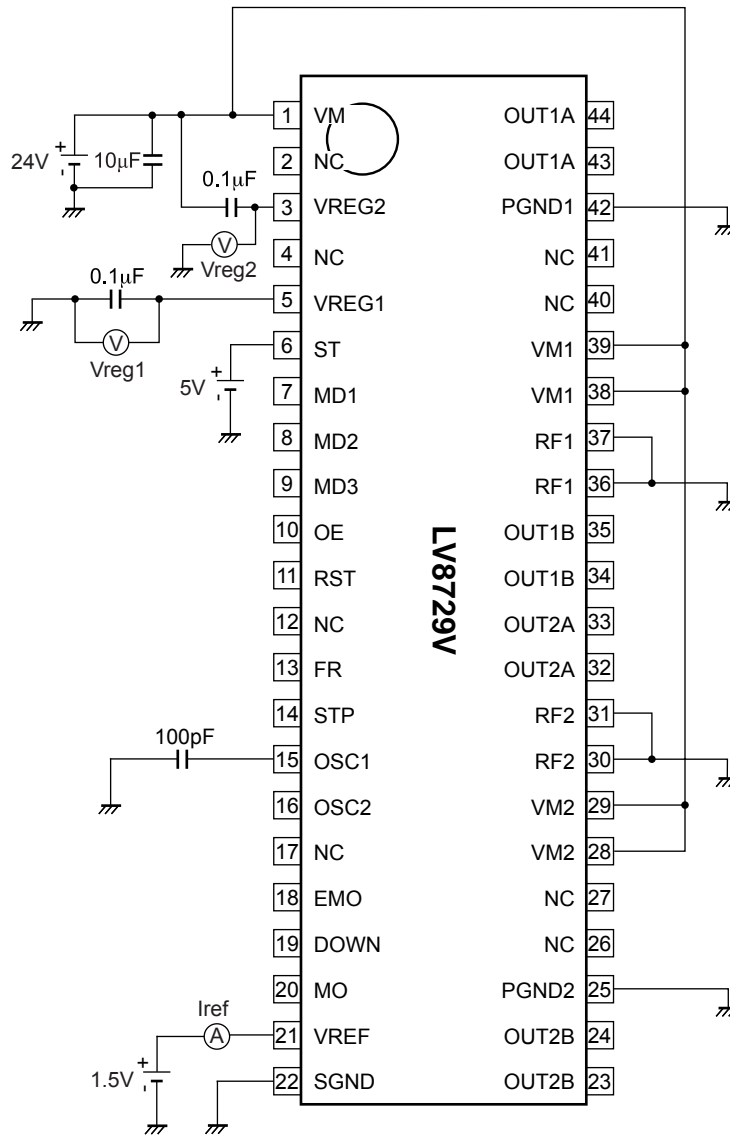
This measurement is related to the MD1 pin. Take the same procedure for measurement of MD2 and MD3 pins.

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REG1 output voltage : Vreg1

REG2 output voltage : Vreg2

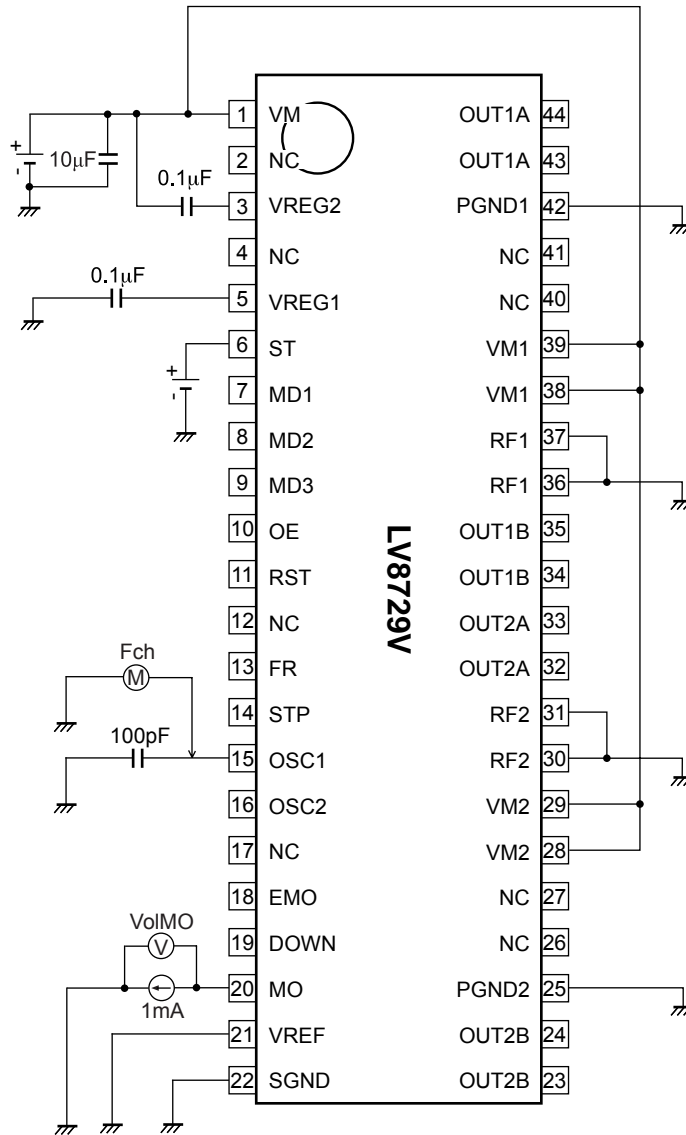
VREF pin input voltage : Iref



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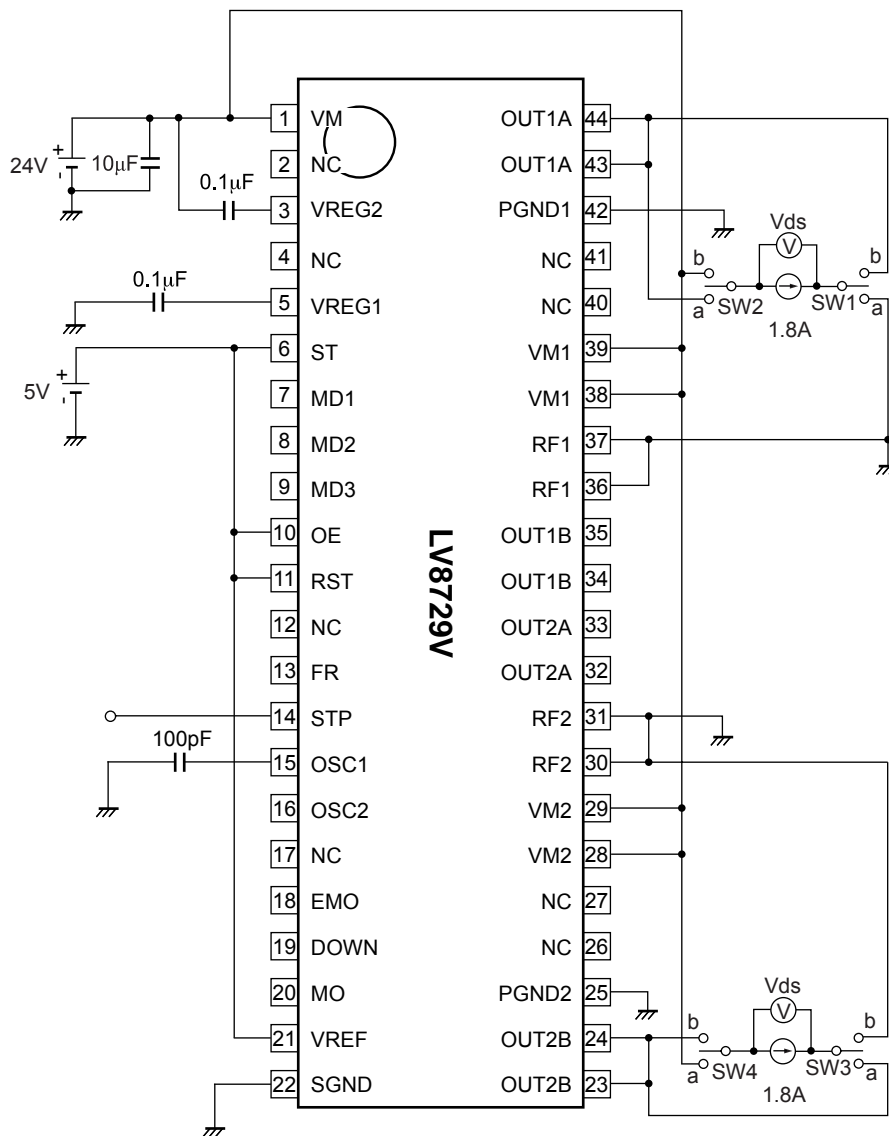
Copping frequency : Fch

MO pin residual voltage : V_{OIMO}



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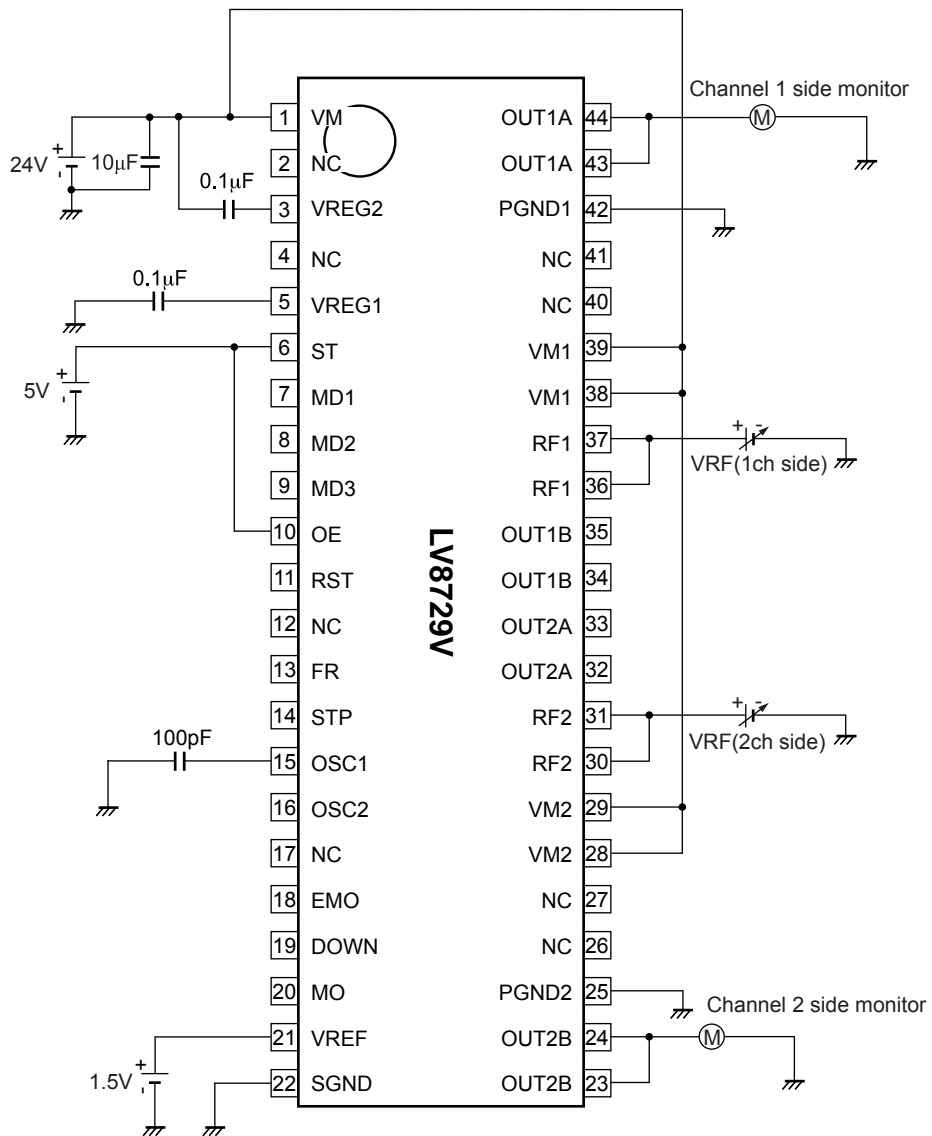
Output on-resistance : Ronu,Rond



When measuring OUT1A upper and OUT2B upper FETs, set SW1 to 4 to the "a" side.
 When measuring OUT1A lower and OUT2B lower FETs, set SW1 to 4 to the "b" side.
 This measurement is related to OUT1A and OUT2B. To measure OUT2A and OUT1B, enter two rectangular waves to the STP pin and carry out the procedure for measurement.

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Current setting reference voltage : VRF



Raise the RF1 (2) pin voltage from 0V. The RF1 (2) voltage at which the OUT voltage changes from "H" to "L" is VRF.

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