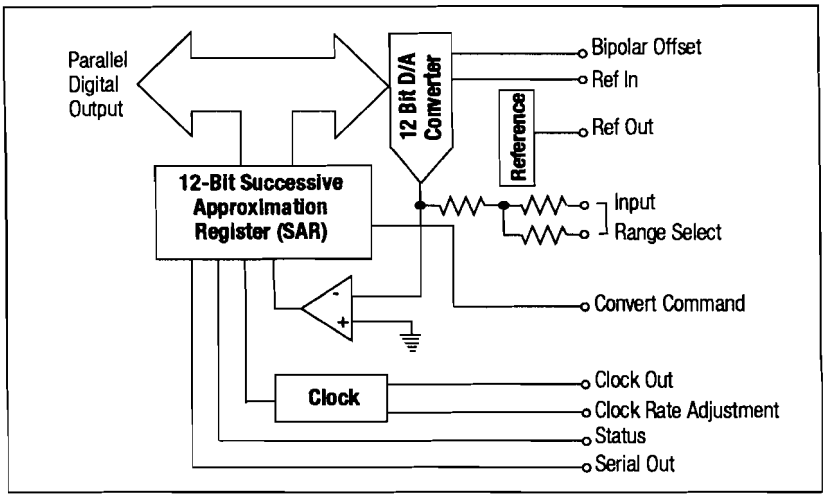
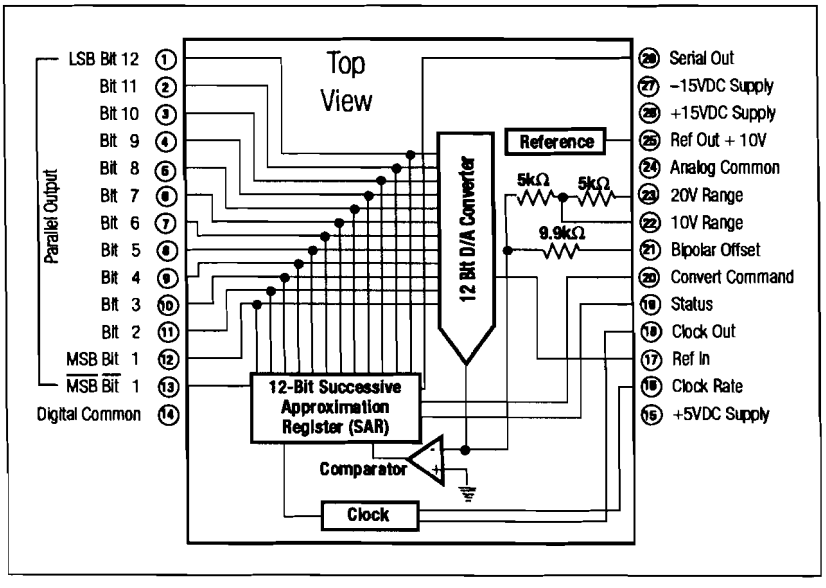
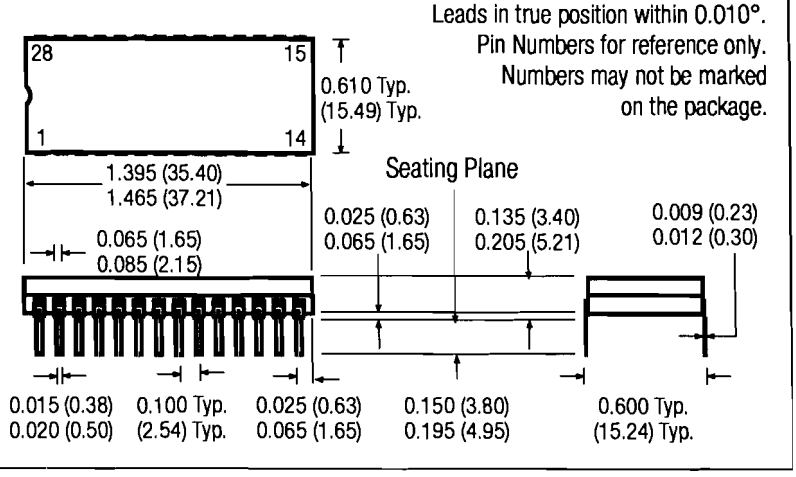
1-6H005 12-Bit A/D Converter

InterFET HYBRID TECHNOLOGY





12-Bit Successive Approximation Register (SAR)



Features

- **– 55°C to + 200°C Specifications**
- **50 µsec Maximum Conversion Time**
- **No Missing Codes Over Full Temperature Range**
- **Complete With Internal Clock and Reference Voltage**
- **Serial Output Data Available**
- **TTL and +5V CMOS Compatible**
- **Hermetic Package**
- **Low Power Operation with External Reference (250mW)**
- **Pin Compatible with Burr Brown ADC10HT**

Description

The I-6H005 general purpose, 12-bit, successive approximation A/D converter is ideally qualified for circuits that must operate over wide temperature ranges. The I-6H005 incorporates state-of-the-art IC and laser-trimmed components. It is complete with an internal clock and reference voltage. Internal scaling resistors allow bipolar input voltage ranges of ±5V and ±10V. A pin is provided for serial output data.

The I-6H005 is contained in a compact, dual-width, 28-pin hermetic DIL package and is fully PIN compatible with the Burr Brown ADC10HT. 100% screened versions available upon request. Refer to Table II on the back page for example.

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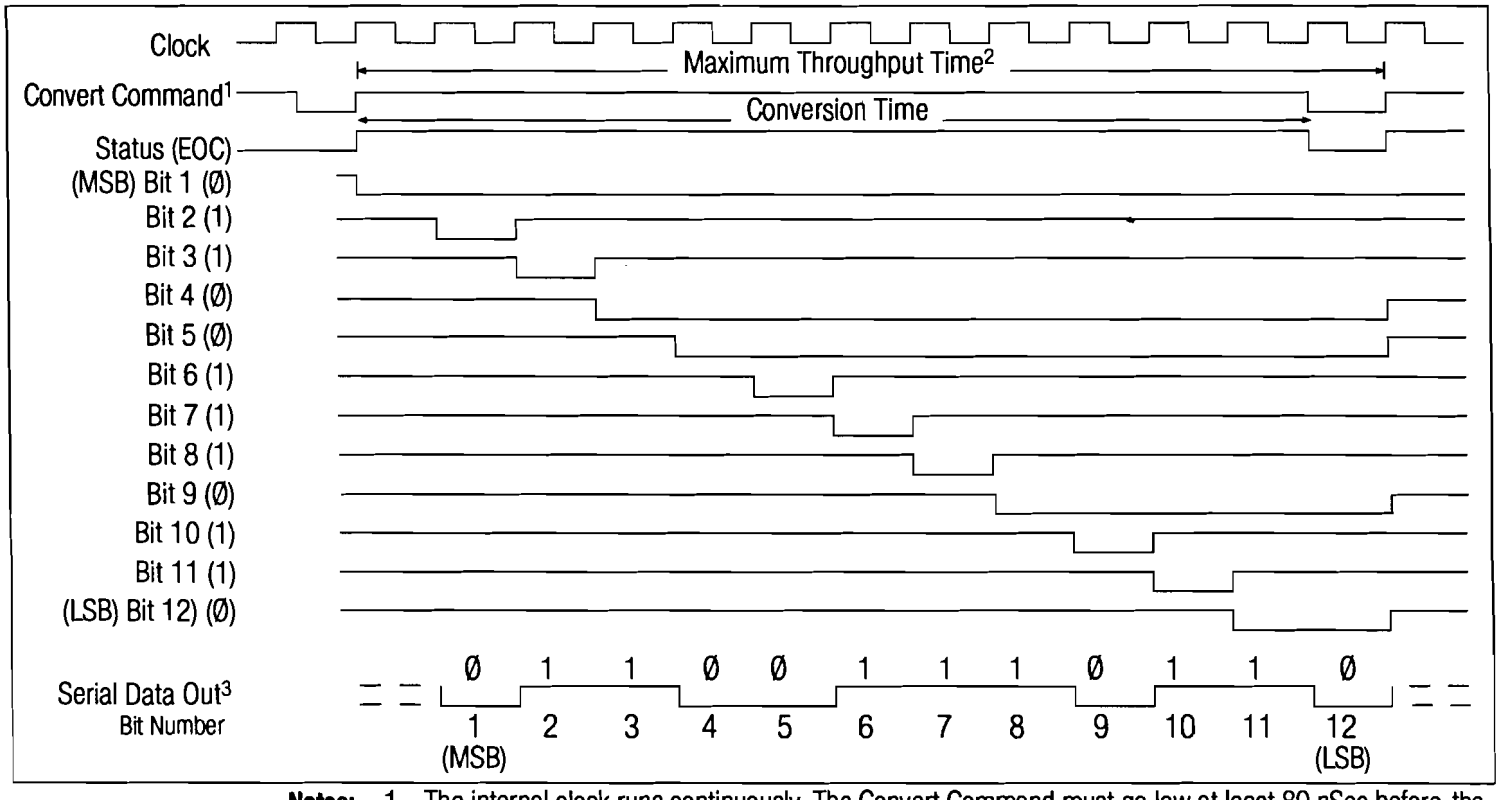
Table II - 100% Device Screening

TEST SCREEN	METHOD*	CONDITIONS
1. Precap Internal Visual	2017	
2. High Temperature Storage	1008	Conditions C, T_A = 150°C. Time = 24 hours minimum
3. Temperature Cycling	1010	Condition C, -65°C to + 150°C, 10 Cycles
4. Constant Acceleration	2001	Condition A, 5KGs, Y, and Y_2 axis only.
5. Fine Leak	1014	Condition A
6. Gross Leak	1014	Condition C
7. Interim Electrical Test	—	Optional
8. Burn-In	1015	Condition B, Time = 160 hours minimum. TA = +5°C, VCC = 5.5V, IF = 20mA, ID = 25mA.
9. Final Electrical Test	—	Group A, Subgroup 1, 10% PDA applies.
		Group A, Subgroup 2, 3, 9.
10. External Visual	2009	

* Refers to screening as defined in MIL-H-38534. InterFET is not certified and does not imply certification by referencing these methods.

Timing Diagram



Notes:
1. The internal clock runs continuously. The Convert Command must go low at least 80 nSec before the rising edge of any clock pulse to initiate a conversion, and must return high at lease 80 nSec before the next low to high clock transition.
2. The maximum throughput time is 54 µSec for 12 bits.
3. If serial data is strobed, use the trailing edge of the clock. During data conversion, the determination as to the proper state of any bit (bit "n") is made on the rising edge of the clock pulse and the parallel output data is considered valid at the negative edge of the clock cycle (actually valid following the clock low to high transition). The serial output then is clocked at the next clock cycle, thus it will require 13 clock steps to obtain the correct serial 12 bit data. Thus valid serial data is provided at clock "n" + 1.

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Electrical Characteristics	**Conditions**	**Min**	**Typ**	**Max**	**Units**

Table 1. Specifications at rated power supply voltages and T_A = +25°C unless otherwise noted.

RESOLUTION		12			Bits
INPUT					
ANALOG	– 55°C to + 200°C				
Voltage Ranges	Unipolar	(972) 238-1287		to + 20	V
	Bipolar	(972) 238-1287			V
Impedance (direct input)	Ø to 10V, ± 5V	(972) 238-1287			kΩ
	Ø to + 20V, ± 10V		10		kΩ
DIGITAL[1]	– 55°C to + 200°C				
Convert Command Logic Loading			1		CMOS Load
TRANSFER CHARACTERISTICS – ACCURACY					
Gain Error[2]			± 0.05	± 0.2	%
Offset Error[3]	Unipolar		± 0.05	± 0.2	% of FSR[3]
	Bipolar		± 0.05	± 0.2	% of FSR
Linearity Error				± 0.012	% of FSR
Inherent Quantization Error			± 1/2		LSB
Differential Linearity Error			± 0.012	± 0.024	% of FSR
Total Unadjusted Error[4]	+ 25°C		± 0.10	± 0.4	% of FSR
	– 55°C to + 200°C		± 0.30	± 1	% of FSR
Total Adjusted Error[5]	+ 25°C		± 0.006	± 0.012	% of FSR
	– 55°C to + 200°C		± 0.2	± 0.6	% of FSR
Total Unadjusted Error[6] Exclusive of Reference	+ 25°C		± 0.1	± 0.4	% of FSR
	– 55°C to + 200°C		± 0.2	± 0.8	% of FSR
Total Adjusted Error[7] Exclusive of Reference	+ 25°C		± 0.006	± 0.012	% of FSR
	– 55°C to + 200°C		± 0.15	± 0.4	% of FSR
CONVERSION TIME			30	50	µ sec
DRIFT (– 55°C ≤ T_A ≤ + 200°C)					
Gain With Internal Reference			± 15	± 35	ppm/°C
Gain Exclusive of Reference			± 5	± 10	ppm/°C
Offset	Unipolar		± 2		ppm of FSR/°C
Offset With Internal Reference	Bipolar		± 10	± 35	ppm of FSR/°C
Offset Exclusive of Reference	Bipolar		± 4	± 1	ppm of FSR/°C
Linearity			± 0.5	± 1	ppm of FSR/°C
No Missing Codes Over Temp. Range	– 55°C to + 200°C	12			Bits

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Electrical Characteristics

Table 1. (Continued) Specifications at rated power supply voltages and T_A = +25°C unless otherwise noted.

	Conditions	Min	Typ	Max	Units
OUTPUT – DIGITAL DATA					
Parallel Output Codes [8]	Unipolar		SB		
	Bipolar[9]		OB,TC		
Parallel Output Drive		1			LSTTL Loads
Serial Data Code	(NZR) – SB, OB				
Serial Output Drive		1			LSTTL Loads
Status		Logic "1" during conversion			
Status Output Drive		1			LSTTL Loads
Internal Clock - Output Drive		1			LSTTL Loads
Internal Clock - Frequency			400		kHz
POWER SUPPLY & REFERENCE					
Rated Voltage	VCC	± 14.5	± 15		VDC
	VDD	± 4.75	± 5		VDC
Supply Drain	+ VCC		+ 15		mA
	– VCC		– 30		mA
	VDD		+ 16		mA
Power Supply Sensitivity	± VCC		0.01	0.10	% of FRS/% VCC
	VDD		0.01	0.10	% of FRS/% VDD
Internal Reference Voltage		9.990	10	10.010	V
Max External Current with no degradaton of specs			2		mA
Temperature Coefficient			± 10		ppm/°C
TEMPERATURE RANGE					
Operating		– 55		+ 200	°C
Storage		– 55		+ 200	°C

Notes

1. + 5V CMOS compatible. Input current (low to high) = 1 µA max. Use pull-up resistor when driving convert command from TTL.
2. Adjustrable to zero.
3. FSR means Full Scale Range. For example, connected for a ±10V has a 20V FSR.
4. Includes Gain, Offset, and Linearity Errors (Bipolar Mode).
5. Gain, Offset, Errors removed at + 25°C (Bipolar Mode).
4. Includes Gain, Offset, and Linearity Errors with external + 10V ± 1mV reference; does not include Reference Drift (Bipolar Mode).
5. Gain, Offset, Errors removed at + 25°C with external + 10V ± 1mV reference; does not include Reference Drift (Bipolar Mode).
8. SB - Straight Binary; OB - Offset Binary; TC - Two's Complement.
9. TC coding obtained by useing MSB - pin 13 - instead of MSB - pin 12.

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