Quad Parametric Measurement Unit with Integrated 16-Bit Level Setting DACs

AD5522

FEATURES

- Quad parametric measurement unit (PMU)
  - FV, FI, FN (high-Z), MV, MI functions
- 4 programmable current ranges (internal R_{SENSE})
  - ±5 µA, ±20 µA, ±200 µA, and ±2 mA
- 1 programmable current range up to ±80 mA (external R_{SENSE})
- 22.5 V FV range with asymmetrical operation
- Integrated 16-bit DACs provide programmable levels
- Gain and offset correction on chip
- Low capacitance outputs suited to relayless systems
- On-chip comparators per channel
- FI voltage clamps and FV current clamps
- Guard drive amplifier
- System PMU connections
- Programmable temperature shutdown
- SPI- and LVDS-compatible interfaces
- Compact 80-lead TQFP with exposed pad (top or bottom)

APPLICATIONS

- Automated test equipment (ATE)
  - Per-pin parametric measurement unit
  - Continuity and leakage testing
  - Device power supply
- Instrumentation
  - Source measure unit (SMU)
  - Precision measurement

FUNCTIONAL BLOCK DIAGRAM

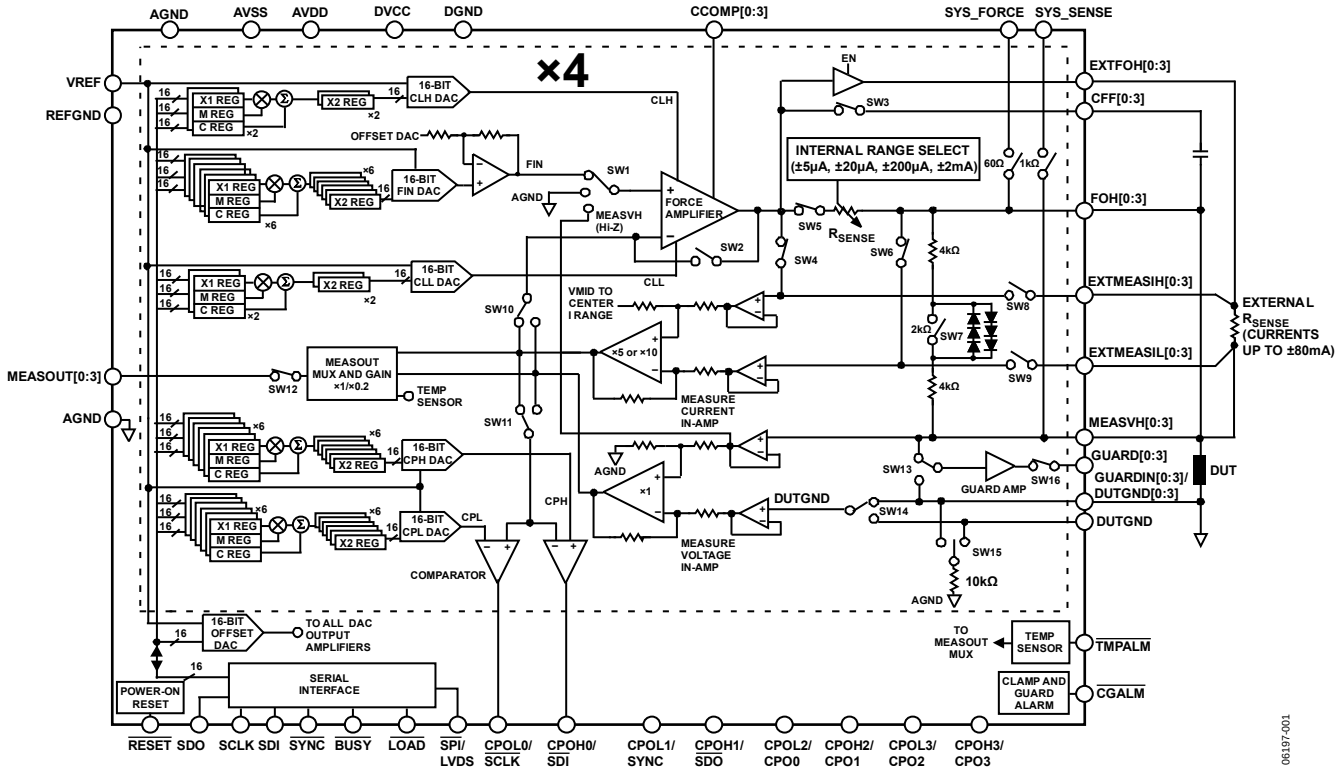

Figure 1.

Rev. D

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GENERAL DESCRIPTION

The AD5522 is a high performance, highly integrated parametric measurement unit consisting of four independent channels. Each per-pin parametric measurement unit (PPMU) channel includes five 16-bit, voltage output DACs that set the programmable input levels for the force voltage inputs, clamp inputs, and comparator inputs (high and low). Five programmable force and measure current ranges are available, ranging from ±5 μA to ±80 mA. Four of these ranges use on-chip sense resistors; one high current range up to ±80 mA is available per channel using off-chip sense resistors. Currents in excess of ±80 mA require an external amplifier. Low capacitance DUT connections (FOHx and EXTFOHx) ensure that the device is suited to relayless test systems.

The PMU functions are controlled via a simple 3-wire serial interface compatible with SPI, QSPI™, MICROWIRE™, and DSP interface standards. Interface clocks of 50 MHz allow fast updating of modes. The low voltage differential signaling (LVDS) interface protocol at 83 MHz is also supported. Comparator outputs are provided per channel for device go-no-go testing and characterization. Control registers allow the user to easily change force or measure conditions, DAC levels, and selected current ranges. The SDO (serial data output) pin allows the user to read back information for diagnostic purposes.

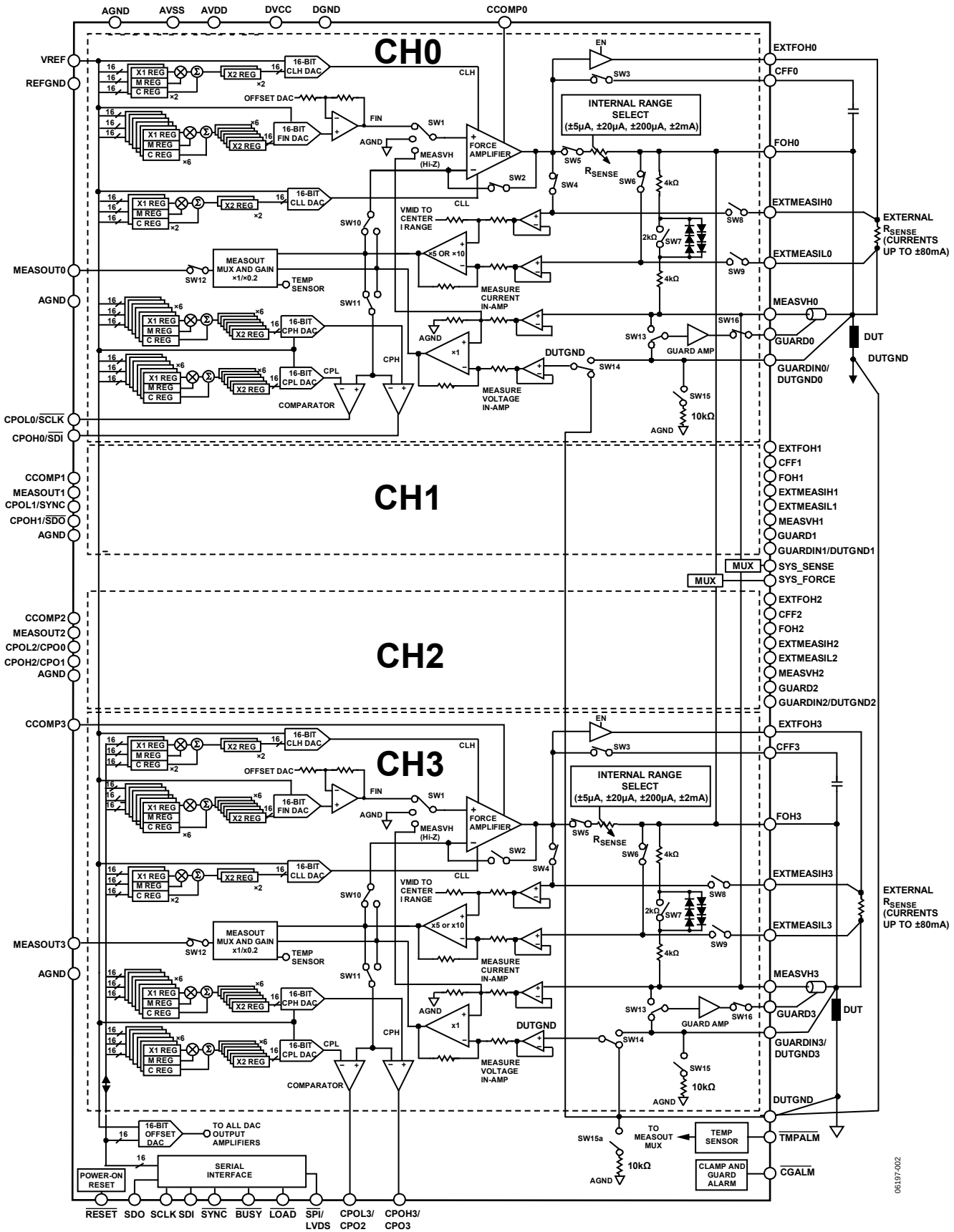


Figure 2. Detailed Block Diagram

SPECIFICATIONS

AVDD ≥ 10 V; AVSS ≤ −5 V; |AVDD − AVSS| ≥ 20 V and ≤ 33 V; DVCC = 2.3 V to 5.25 V; VREF = 5 V; REFGND = DUTGND = AGND = 0 V; gain (M), offset (C), and DAC offset registers at default values; T_J = 25°C to 90°C, unless otherwise noted. (FV = force voltage, FI = force current, MV = measure voltage, MI = measure current, FS = full scale, FSR = full-scale range, FSVR = full-scale voltage range, FSCR = full-scale current range.)

Table 1.

Parameter	Min	Typ [1]	Max	Unit	Test Conditions/Comments
FORCE VOLTAGE					
FOHx Output Voltage Range [2]	AVSS + 4		AVDD − 4	V	All current ranges from FOHx at full-scale current; includes ±1 V dropped across sense resistor
EXTFOHx Output Voltage Range [2]	AVSS + 3		AVDD − 3	V	External high current range at full-scale current; does not include ±1 V dropped across sense resistor
Output Voltage Span		22.5		V	
Offset Error	−50		+50	mV	Measured at midscale code; prior to calibration
Offset Error Tempco [2]		−10		µV/°C	Standard deviation = 20 µV/°C
Gain Error	−0.5		+0.5	% FSR	Prior to calibration
Gain Error Tempco [2]		0.5		ppm/°C	Standard deviation = 0.5 ppm/°C
Linearity Error	−0.01		+0.01	% FSR	FSR = full-scale range (±10 V), gain and offset errors calibrated out
Short-Circuit Current Limit [2]	−150		+150	mA	±80 mA range
	−10		+10	mA	All other ranges
Noise Spectral Density (NSD) [2]		320		nV/√Hz	1 kHz, at FOHx in FV mode
MEASURE CURRENT					Measure current = (I_{DUT} × R_{SENSE} × gain); amplifier gain = 5 or 10, unless otherwise noted
Differential Input Voltage Range [2]	−1.125		+1.125	V	Voltage across R_{SENSE}; gain = 5 or 10
Output Voltage Span		22.5		V	Measure current block with VREF = 5 V, MEASOUT scaling happens after
Offset Error	−0.5		+0.5	% FSCR	V(R_{SENSE}) = ±1 V, measured with zero current flowing
Offset Error Tempco [2]		1		µV/°C	Referred to MI input; standard deviation = 4 µV/°C
Gain Error	−1		+1	% FSCR	Using internal current ranges
	−0.5		+0.5	% FSCR	Measure current amplifier alone
Gain Error Tempco [2]		−2		ppm/°C	Standard deviation = 2 ppm/°C Measure current amplifier alone; internal sense resistor 25 ppm/°C
Linearity Error (MEASOUTx Gain = 1)	−0.015		+0.015	% FSR	MI gain = 10
	−0.01		+0.01	% FSR	MI gain = 5
Linearity Error (MEASOUTx Gain = 0.2)	−0.06		+0.06	% FSR	MI gain = 10, AVDD = 28 V, AVSS = −5 V, offset DAC = 0x0
	−0.11		+0.11	% FSR	MI gain = 10, AVDD = 10 V, AVSS = −23 V, offset DAC = 0x0EDB7
	−0.015		+0.015	% FSR	MI gain = 10, AVDD = 15.25 V, AVSS = −15.25 V, offset DAC = 0xA492
	−0.06		+0.06	% FSR	MI gain = 5, AVDD = 28 V, AVSS = −5 V, offset DAC = 0x0
	−0.01		+0.01	% FSR	MI gain = 5, AVDD = 10 V, AVSS = −23 V, offset DAC = 0xEDB7
	−0.01		+0.01	% FSR	MI gain = 5, AVDD = 15.25 V, AVSS = −15.25 V, offset DAC = 0xA492
Common-Mode Voltage Range [2]	AVSS + 4		AVDD − 4	V	
Common-Mode Error (Gain = 5)	−0.01		+0.01	% FSCR/V	% of full-scale change at force output per V change in DUT voltage
Common-Mode Error (Gain = 10)	−0.005		+0.005	% FSCR/V	% of full-scale change at force output per V change in DUT voltage
Sense Resistors					Sense resistors are trimmed to within 1%
		200		kΩ	±5 µA range
		50		kΩ	±20 µA range
		5		kΩ	±200 µA range
		0.5		kΩ	±2 mA range

Parameter	Min	Typ [1]	Max	Unit	Test Conditions/Comments
Measure Current Ranges[2]					Specified current ranges are achieved with VREF = 5 V and MI gain = 10, or with VREF = 2.5 V and MI gain = 5
		±5		µA	Set using internal sense resistor
		±20		µA	Set using internal sense resistor
		±200		µA	Set using internal sense resistor
		±2		mA	Set using internal sense resistor
			±80	mA	Set using external sense resistor; internal amplifier can drive up to ±80 mA
Noise Spectral Density (NSD)[2]		400		nV/√Hz	1 kHz, MI amplifier only, inputs grounded
FORCE CURRENT					
Voltage Compliance, FOHx[2]	AVSS + 4		AVDD − 4	V	
Voltage Compliance, EXTFOHx[2]	AVSS + 3		AVDD − 3	V	
Offset Error	−0.5		+0.5	% FSCR	Measured at midscale code, 0 V, prior to calibration
Offset Error Tempco[2]		5		ppm FS/°C	Standard deviation = 5 ppm/°C
Gain Error	−1.5		+1.5	% FSCR	Prior to calibration
Gain Error Tempco[2]		−6		ppm/°C	Standard deviation = 5 ppm/°C
Linearity Error	−0.02		+0.02	% FSCR	
Common-Mode Error (Gain = 5)	−0.01		+0.01	% FSCR/V	% of full-scale change per V change in DUT voltage
Common-Mode Error (Gain = 10)	−0.006		+0.006	% FSCR/V	% of full-scale change per V change in DUT voltage
Force Current Ranges					Specified current ranges achieved with VREF = 5 V and MI gain = 10, or with VREF = 2.5 V and MI gain = 5 V
		±5		µA	Set using internal sense resistor, 200 kΩ
		±20		µA	Set using internal sense resistor, 50 kΩ
		±200		µA	Set using internal sense resistor, 5 kΩ
		±2		mA	Set using internal sense resistor, 500 Ω
			±80	mA	Set using external sense resistor; internal amplifier can drive up to ±80 mA
MEASURE VOLTAGE					
Measure Voltage Range[2]	AVSS + 4		AVDD − 4	V	
Offset Error	−10		+10	mV	Gain = 1, measured at 0 V
	−25		+25	mV	Gain = 0.2, measured at 0 V
Offset Error Tempco[2]		−1		µV/°C	Standard deviation = 6 µV/°C
Gain Error	−0.25		+0.25	% FSR	MEASOUTx gain = 1
	−0.5		+0.5	% FSR	MEASOUTx gain = 0.2
Gain Error Tempco[2]		1		ppm/°C	Standard deviation = 4 ppm/°C
Linearity Error (MEASOUTx Gain = 1)	−0.01		+0.01	% FSR	
Linearity Error (MEASOUTx Gain = 0.2)	−0.01		+0.01	% FSR	AVDD = 15.25 V, AVSS = −15.25 V, offset DAC = 0xA492
	−0.06		+0.06	% FSR	AVDD = 28 V, AVSS = −5 V, offset DAC = 0x0
	−0.1		+0.1	% FSR	AVDD = −10 V, AVSS = −23 V, offset DAC = 0x3640
Noise Spectral Density (NSD)[2]		100		nV/√Hz	1 kHz; measure voltage amplifier only, inputs grounded
OFFSET DAC					
Span Error		±30		mV	
COMPARATOR					
Comparator Span		22.5		V	
Offset Error	−2	+1	+2	mV	Measured directly at comparator; does not include measure block errors
Offset Error Tempco[2]		1		µV/°C	Standard deviation = 2 µV/°C
Propagation Delay[2]		0.25		µs	
VOLTAGE CLAMPS					
Clamp Span		22.5		V	
Positive Clamp Accuracy			155	mV	
Negative Clamp Accuracy	−155			mV	
CLL to CLH[2]	500			mV	CLL < CLH and minimum voltage apart
Recovery Time[2]		0.5	1.5	µs	
Activation Time[2]		1.5	3	µs	

Parameter	Min	Typ [1]	Max	Unit	Test Conditions/Comments
CURRENT CLAMPS					
Clamp Accuracy	Programmed clamp value		Programmed clamp value ± 10	% FSC	MI gain = 10, clamp current scales with selected range
	Programmed clamp value		Programmed clamp value ± 20	% FSC	MI gain = 5, clamp current scales with selected range
CLL to CLH[2]	5			% of I_{RANGE}	CLL < CLH and minimum setting apart, MI gain = 10
	10			% of I_{RANGE}	CLL < CLH and minimum setting apart, MI gain = 5
Recovery Time[2]		0.5	1.5	µs	
Activation Time[2]		1.5	3	µs	
FOHx, EXTFOHx, EXTMEASILx, EXTMEASIHx, CFFx PINS					
Pin Capacitance[2]		10		pF	
Leakage Current	−3		+3	nA	Individual pin on or off switch leakage, measured with ±11 V stress applied to pin, channel enabled, but tristate
Leakage Current Tempco[2]		±0.01		nA/°C	
MEASVHx PIN					
Pin Capacitance[2]		3		pF	
Leakage Current	−3		+3	nA	Measured with ±11 V stress applied to pin, channel enabled, but tristate
Leakage Current Tempco[2]		±0.01		nA/°C	
SYS_SENSE PIN					SYS_SENSE connected, force amplifier inhibited
Pin Capacitance[2]		3		pF	
Switch Impedance		1	1.3	kΩ	
Leakage Current	−3		+3	nA	Measured with ±11 V stress applied to pin, switch off
Leakage Current Tempco[2]		±0.01		nA/°C	
SYS_FORCE PIN					SYS_FORCE connected, force amplifier inhibited
Pin Capacitance[2]		6		pF	
Switch Impedance		60	80	Ω	
Leakage Current	−3		+3	nA	Measured with ±11 V stress applied to pin, switch off
Leakage Current Tempco[2]		±0.01		nA/°C	
COMBINED LEAKAGE AT DUT					Includes FOHx, MEASVHx, SYS_SENSE, SYS_FORCE, EXTMEASILx, EXTMEASIHx, EXTFOHx, and CFFx; calculation of all the individual leakage contributors
Leakage Current	−15		+15	nA	T_J = 25°C to 70°C
	−25		+25	nA	T_J = 25°C to 90°C
Leakage Current Tempco[2]		±0.1		nA/°C	
DUTGNDx PIN					
Voltage Range	−500		+500	mV	
Leakage Current	−30		+30	nA	
MEASOUTx PIN					With respect to AGND
Output Voltage Span		22.5		V	Software programmable output range
Output Impedance		60	80	Ω	
Output Leakage Current	−3		+3	nA	With SW12 off
Output Capacitance[2]			15	pF	
Maximum Load Capacitance[2]			0.5	µF	
Output Current Drive[2]		2		mA	
Short-Circuit Current	−10		+10	mA	
Slew Rate[2]		2		V/µs	
Enable Time[2]		150	320	ns	Closing SW12, measured from $\overline{BUSY}$ rising edge
Disable Time[2]		400	1100	ns	Opening SW12, measured from $\overline{BUSY}$ rising edge
MI to MV Switching Time[2]		200		ns	Measured from $\overline{BUSY}$ rising edge; does not include slewing or settling

Parameter	Min	Typ [1]	Max	Unit	Test Conditions/Comments
GUARDx PIN					
Output Voltage Span		22.5		V	
Output Offset	−10		+10	mV	
Short-Circuit Current	−15		+15	mA	
Maximum Load Capacitance[2]			100	nF	
Output Impedance		85		Ω	
Tristate Leakage Current[2]	−30		+30	nA	When guard amplifier is disabled
Slew Rate[2]		5		V/µs	C_{LOAD} = 10 pF
Alarm Activation Time[2]		200		µs	Alarm delayed to eliminate false alarms
FORCE AMPLIFIER[2]					
Slew Rate		0.4		V/µs	CCOMPx = 100 pF, CFFx = 220 pF, C_{LOAD} = 200 pF
Gain Bandwidth		1.3		MHz	CCOMPx = 100 pF, CFFx = 220 pF, C_{LOAD} = 200 pF
Max Stable Load Capacitance			10,000	pF	CCOMPx = 100 pF, larger C_{LOAD} requires larger CCOMP capacitor
			100	nF	CCOMPx = 1 nF, larger C_{LOAD} requires larger CCOMP capacitor
FV SETTLING TIME TO 0.05% OF FS[2]					Midscale to full-scale change; measured from $\overline{SYNC}$ rising edge, clamps on
±80 mA Range		22	40	µs	CCOMPx = 100 pF, CFFx = 220 pF, C_{LOAD} = 200 pF
±2 mA Range		24	40	µs	CCOMPx = 100 pF, CFFx = 220 pF, C_{LOAD} = 200 pF
±200 µA Range		40	80	µs	CCOMPx = 100 pF, CFFx = 220 pF, C_{LOAD} = 200 pF
±20 µA Range		300		µs	CCOMPx = 100 pF, CFFx = 220 pF, C_{LOAD} = 200 pF
±5 µA Range		1400		µs	CCOMPx = 100 pF, CFFx = 220 pF, C_{LOAD} = 200 pF
MI SETTLING TIME TO 0.05% OF FS[2]					Midscale to full-scale change; driven from force amplifier in FV mode, so includes FV settling time; measured from $\overline{SYNC}$ rising edge, clamps on
±80 mA Range		22	40	µs	CCOMPx = 100 pF, CFFx = 220 pF, C_{LOAD} = 200 pF
±2 mA Range		24	40	µs	CCOMPx = 100 pF, CFFx = 220 pF, C_{LOAD} = 200 pF
±200 µA Range		60	100	µs	CCOMPx = 100 pF, CFFx = 220 pF, C_{LOAD} = 200 pF
±20 µA Range		462		µs	CCOMPx = 100 pF, CFFx = 220 pF, C_{LOAD} = 200 pF
±5 µA Range		1902		µs	CCOMPx = 100 pF, CFFx = 220 pF, C_{LOAD} = 200 pF
FI SETTLING TIME TO 0.05% OF FS[2]					Midscale to full-scale change; measured from $\overline{SYNC}$ rising edge, clamps on
±80 mA Range		24	55	µs	CCOMPx = 100 pF, C_{LOAD} = 200 pF
±2 mA Range		24	60	µs	CCOMPx = 100 pF, C_{LOAD} = 200 pF
±200 µA Range		50	120	µs	CCOMPx = 100 pF, C_{LOAD} = 200 pF
±20 µA Range		450		µs	CCOMPx = 100 pF, C_{LOAD} = 200 pF
±5 µA Range		2700		µs	CCOMPx = 100 pF, C_{LOAD} = 200 pF
MV SETTLING TIME TO 0.05% OF FS[2]					Midscale to full-scale change; driven from force amplifier in FV mode, so includes FV settling time; measured from $\overline{SYNC}$ rising edge, clamps on
±80 mA Range		24	55	µs	CCOMPx = 100 pF, C_{LOAD} = 200 pF
±2 mA Range		24	60	µs	CCOMPx = 100 pF, C_{LOAD} = 200 pF
±200 µA Range		50	120	µs	CCOMPx = 100 pF, C_{LOAD} = 200 pF
±20 µA Range		450		µs	CCOMPx = 100 pF, C_{LOAD} = 200 pF
±5 µA Range		2700		µs	CCOMPx = 100 pF, C_{LOAD} = 200 pF
DAC SPECIFICATIONS					
Resolution			16	Bits	
Output Voltage Span[2]		22.5		V	VREF = 5 V, within a range of −16.25 V to +22.5 V
Differential Nonlinearity[2]	−1		+1	LSB	Guaranteed monotonic by design over temperature
COMPARATOR DAC DYNAMIC SPECIFICATIONS[2]					
Output Voltage Settling Time		1		µs	500 mV change to ±½ LSB
Slew Rate		5.5		V/µs	
Digital-to-Analog Glitch Energy		20		nV-sec	
Glitch Impulse Peak Amplitude		10		mV	
REFERENCE INPUT					
VREF DC Input Impedance	1	100		MΩ	
VREF Input Current	−10	+0.03	+10	µA	
VREF Range[2]	2		5	V	

Parameter	Min	Typ [1]	Max	Unit	Test Conditions/Comments
DIE TEMPERATURE SENSOR					
Accuracy[2]		±7		°C	
Output Voltage at 25°C		1.5		V	
Output Scale Factor[2]		4.6		mV/°C	
Output Voltage Range[2]	0		3	V	
INTERACTION AND CROSSTALK[2]					
DC Crosstalk (FOHx)		0.05	0.65	mV	DC change resulting from a dc change in any DAC in the device, FV and FI modes, ±2 mA range, C_{LOAD} = 200 pF, R_{LOAD} = 5.6 kΩ
DC Crosstalk (MEASOUTx)		0.05	0.65	mV	DC change resulting from a dc change in any DAC in the device, MV and MI modes, ±2 mA range, C_{LOAD} = 200 pF, R_{LOAD} = 5.6 kΩ
DC Crosstalk Within a Channel		0.05		mV	All channels in FVMI mode, one channel at midscale; measure the current for one channel in the lowest current range for a change in comparator or clamp DAC levels for that PMU
SPI INTERFACE LOGIC INPUTS					
Input High Voltage, V_{IH}	1.7/2.0			V	(2.3 V to 2.7 V)/(2.7 V to 5.25 V), JEDEC-compliant input levels
Input Low Voltage, V_{IL}			0.7/0.8	V	(2.3 V to 2.7 V)/(2.7 V to 5.25 V), JEDEC-compliant input levels
Input Current, I_{INH}, I_{INL}	−1		+1	µA	
Input Capacitance, C_{IN}[2]			10	pF	
CMOS LOGIC OUTPUTS					SDO, CPOx
Output High Voltage, V_{OH}	DVCC − 0.4			V	
Output Low Voltage, V_{OL}			0.4	V	I_{OL} = 500 µA
Tristate Leakage Current	−2		+2	µA	SDO, CPOH1/$\overline{SDO}$
	−1		+1	µA	All other output pins
Output Capacitance[2]			10	pF	
OPEN-DRAIN LOGIC OUTPUTS					$\overline{BUSY}$, $\overline{TMPALM}$, $\overline{CGALM}$
Output Low Voltage, V_{OL}			0.4	V	I_{OL} = 500 µA, C_{LOAD} = 50 pF, R_{PULLUP} = 1 kΩ
Output Capacitance[2]			10	pF	
LVDS INTERFACE LOGIC INPUTS REDUCED RANGE LINK[2]					
Input Voltage Range	875		1575	mV	
Input Differential Threshold	−100		+100	mV	
External Termination Resistance	80	100	120	Ω	
Differential Input Voltage	100			mV	
LVDS INTERFACE LOGIC OUTPUTS REDUCED RANGE LINK					
Output Offset Voltage		1200		mV	
Output Differential Voltage		400		mV	
POWER SUPPLIES					
AVDD	10		28	V	|AVDD − AVSS| ≤ 33 V
AVSS	−23		−5	V	
DVCC	2.3		5.25	V	
AI_{DD}			26	mA	Internal ranges (±5 µA to ±2 mA), excluding load conditions; comparators and guard disabled
AI_{SS}	−26			mA	Internal ranges (±5 µA to ±2 mA), excluding load conditions; comparators and guard disabled
AI_{DD}			28	mA	Internal ranges (±5 µA to ±2 mA), excluding load conditions; comparators and guard enabled
AI_{SS}	−28			mA	Internal ranges (±5 µA to ±2 mA), excluding load conditions; comparators and guard enabled
AI_{DD}			36	mA	External range, excluding load conditions
AI_{SS}	−36			mA	External range, excluding load conditions
DI_{CC}			1.5	mA	
Maximum Power Dissipation[2]			7	W	Maximum power that should be dissipated in this package under worst-case load conditions; careful consideration should be given to supply selection and thermal design

Parameter	Min	Typ [1]	Max	Unit	Test Conditions/Comments
Power Supply Sensitivity[2]					From dc to 1 kHz
ΔForced Voltage/ΔAVDD		−80		dB	
ΔForced Voltage/ΔAVSS		−80		dB	
ΔMeasured Current/ΔAVDD		−85		dB	
ΔMeasured Current/ΔAVSS		−75		dB	
ΔForced Current/ΔAVDD		−75		dB	
ΔForced Current/ΔAVSS		−75		dB	
ΔMeasured Voltage/ΔAVDD		−85		dB	
ΔMeasured Voltage/ΔAVSS		−80		dB	
ΔForced Voltage/ΔDVCC		−90		dB	
ΔMeasured Current/ΔDVCC		−90		dB	
ΔForced Current/ΔDVCC		−90		dB	
ΔMeasured Voltage/ΔDVCC		−90		dB	

[1] Typical specifications are at 25°C and nominal supply, ±15.25 V, unless otherwise noted.
[2] Guaranteed by design and characterization; not production tested. Tempco values are mean and standard deviation, unless otherwise noted.

TIMING CHARACTERISTICS

AVDD ≥ 10 V, AVSS ≤ −5 V, |AVDD − AVSS| ≥ 20 V and ≤ 33 V, DVCC = 2.3 V to 5.25 V, VREF = 5 V, T_J = 25°C to 90°C, unless otherwise noted.

Table 2. SPI Interface

	DVCC, Limit at T_{MIN}, T_{MAX}				
Parameter [1, 2, 3]	**2.3 V to 2.7 V**	**2.7 V to 3.6 V**	**4.5 V to 5.25 V**	**Unit**	**Description**
t_{WRITE}[4]	1030	735	735	ns min	Single channel update cycle time (X1 register write)
	950	655	655	ns min	Single channel update cycle time (any other register write)
t_1	30	20	20	ns min	SCLK cycle time
t_2	8	8	8	ns min	SCLK high time
t_3	8	8	8	ns min	SCLK low time
t_4	10	10	10	ns min	$\overline{SYNC}$ falling edge to SCLK falling edge setup time
t_5[4]	150	150	150	ns min	Minimum $\overline{SYNC}$ high time in write mode after X1 register write (one channel)
	70	70	70	ns min	Minimum $\overline{SYNC}$ high time in write mode after any other register write
t_6	10	5	5	ns min	29th SCLK falling edge to $\overline{SYNC}$ rising edge
t_7	5	5	5	ns min	Data setup time
t_8	9	7	4.5	ns min	Data hold time
t_9	120	75	55	ns max	$\overline{SYNC}$ rising edge to $\overline{BUSY}$ falling edge
t_{10}					$\overline{BUSY}$ pulse width low for X1 and some PMU register writes; see Table 17 and Table 18
1 DAC X1	1.65	1.65	1.65	µs max	
2 DAC X1	2.3	2.3	2.3	µs max	
3 DAC X1	2.95	2.95	2.95	µs max	
4 DAC X1	3.6	3.6	3.6	µs max	
Other Registers	270	270	270	ns max	System control register/PMU registers
t_{11}	20	20	20	ns min	29th SCLK falling edge to $\overline{LOAD}$ falling edge
t_{12}	20	20	20	ns min	$\overline{LOAD}$ pulse width low
t_{13}	150	150	150	ns min	$\overline{BUSY}$ rising edge to FOHx output response time
t_{14}	0	0	0	ns min	$\overline{BUSY}$ rising edge to $\overline{LOAD}$ falling edge
t_{15}	100	100	100	ns max	$\overline{LOAD}$ falling edge to FOHx output response time

Parameter [1, 2, 3]	DVCC, Limit at T_{MIN}, T_{MAX}			Unit	Description
	2.3 V to 2.7 V	2.7 V to 3.6 V	4.5 V to 5.25 V		
t_{16}	1.8	1.2	0.9	µs min	$\overline{\text{RESET}}$ pulse width low
t_{17}	670	700	750	µs max	$\overline{\text{RESET}}$ time indicated by $\overline{\text{BUSY}}$ low
t_{18}	400	400	400	ns min	Minimum $\overline{\text{SYNC}}$ high time in readback mode
t_{19} [5, 6]	60	45	25	ns max	SCLK rising edge to SDO valid; DVCC = 5 V to 5.25 V

[1] Guaranteed by design and characterization; not production tested.
[2] All input signals are specified with $t_R = t_F = 2$ ns (10% to 90% of DVCC) and timed from a voltage level of 1.2 V.
[3] See Figure 5 and Figure 6.
[4] Writes to more than one X1 register engages the calibration engine for longer times, shown by the $\overline{\text{BUSY}}$ low time, t_{10}. Subsequent writes to one or more X1 registers should either be timed or should wait until $\overline{\text{BUSY}}$ returns high (see Figure 56). This is required to ensure that data is not lost or overwritten.
[5] t_{19} is measured with the load circuit shown in Figure 4.
[6] SDO output slows with lower DVCC supply and may require use of a slower SCLK.

Table 3. LVDS Interface

Parameter [1, 2, 3]	DVCC, Limit at T_{MIN}, T_{MAX}		Unit	Description
	2.7 V to 3.6 V	4.5 V to 5.25 V		
t_1	20	12	ns min	SCLK cycle time
t_2	8	5	ns min	SCLK pulse width high and low time
t_3	3	3	ns min	$\overline{\text{SYNC}}$ to SCLK setup time
t_4	3	3	ns min	Data setup time
t_5	5	3	ns min	Data hold time
t_6	3	3	ns min	SCLK to $\overline{\text{SYNC}}$ hold time
t_7 [4]	45	25	ns min	SCLK rising edge to SDO valid
t_8	150	150	ns min	Minimum $\overline{\text{SYNC}}$ high time in write mode after X1 register write
	70	70	ns min	Minimum $\overline{\text{SYNC}}$ high time in write mode after any other register write
	400	400	ns min	Minimum $\overline{\text{SYNC}}$ high time in readback mode

[1] Guaranteed by design and characterization; not production tested.
[2] All input signals are specified with $t_R = t_F = 2$ ns (10% to 90% of DVCC) and timed from a voltage level of 1.2 V.
[3] See Figure 7.
[4] SDO output slows with lower DVCC supply and may require use of slower SCLK.

Circuit and Timing Diagrams

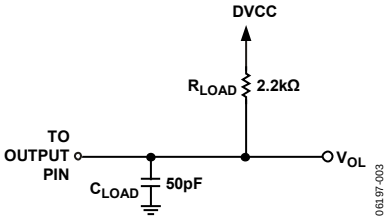


Figure 3. Load Circuit for $\overline{CGALM}$, $\overline{TMPALM}$

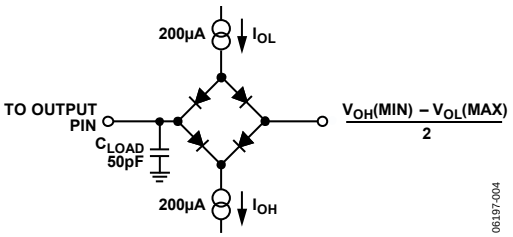


Figure 4. Load Circuit for SDO, $\overline{BUSY}$ Timing Diagram

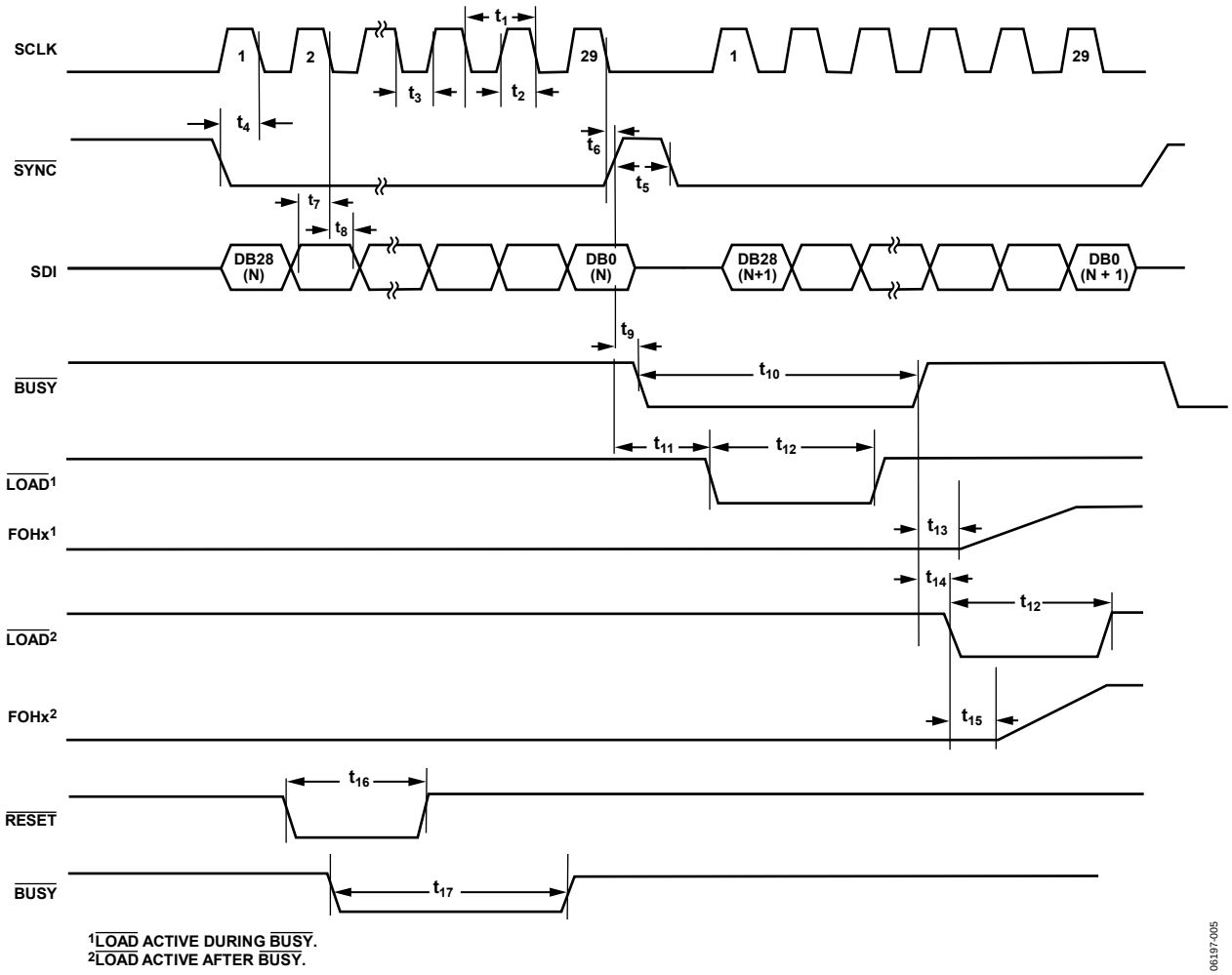


Figure 5. SPI Write Timing (Write Word Contains 29 Bits)

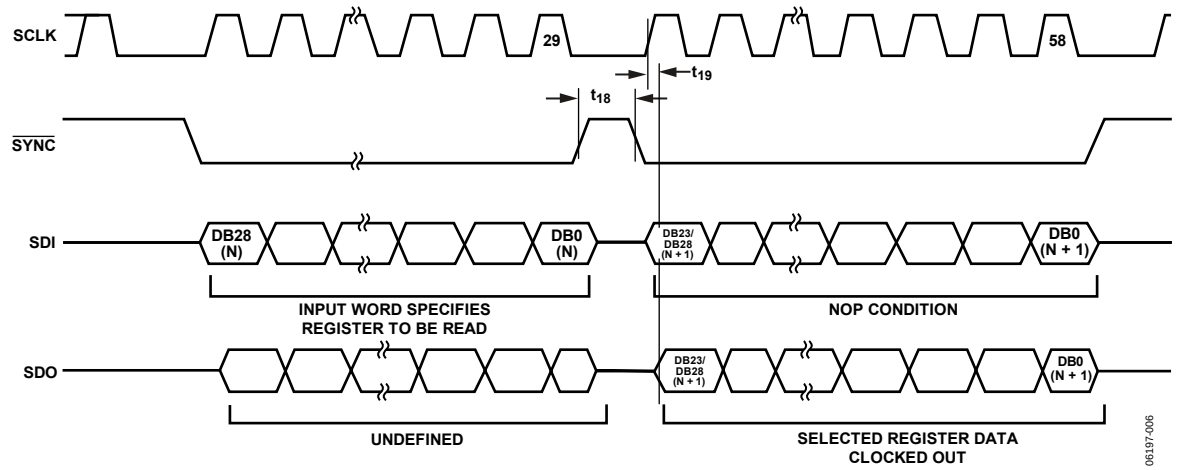


Figure 6. SPI Read Timing (Readback Word Contains 24 Bits and Can Be Clocked Out with a Minimum of 24 Clock Edges)

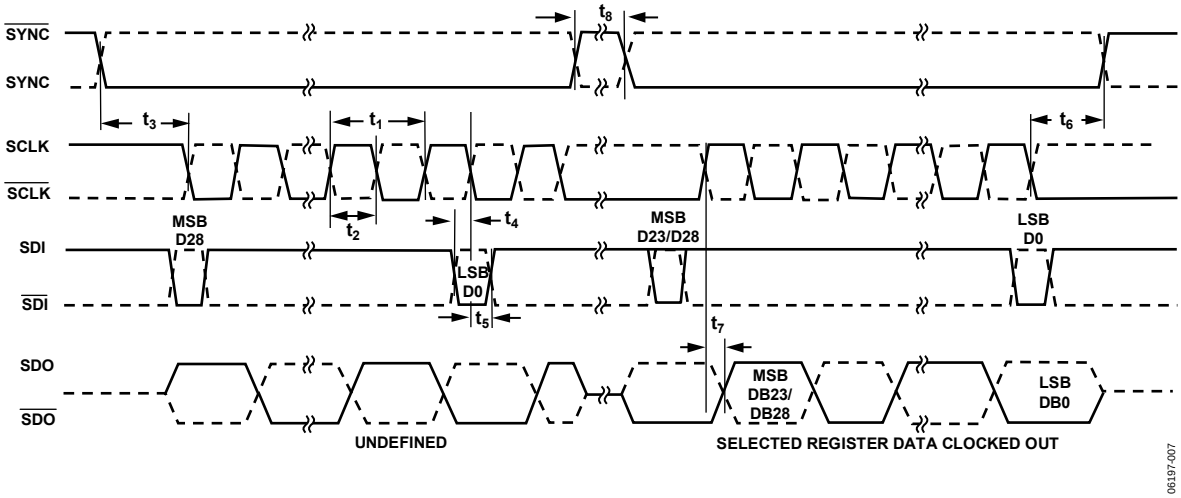


Figure 7. LVDS Read and Write Timing (Readback Word Contains 24 Bits and Can Be Clocked Out with a Minimum of 24 Clock Edges)

ABSOLUTE MAXIMUM RATINGS

Table 4.

Parameter	Rating
Supply Voltage, AVDD to AVSS	34 V
AVDD to AGND	−0.3 V to +34 V
AVSS to AGND	+0.3 V to −34 V
VREF to AGND	−0.3 V to +7 V
DUTGND to AGND	AVDD + 0.3 V to AVSS − 0.3 V
REFGND to AGND	AVDD + 0.3 V to AVSS − 0.3 V
DVCC to DGND	−0.3 V to +7 V
AGND to DGND	−0.3 V to +0.3 V
Digital Inputs to DGND	−0.3 V to DVCC + 0.3 V
Analog Inputs to AGND	AVSS − 0.3 V to AVDD + 0.3 V
Storage Temperature Range	−65°C to +125°C
Operating Junction Temperature Range (J Version)	25°C to 90°C
Reflow Soldering	JEDEC Standard (J-STD-020)
Junction Temperature	150°C max

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

Thermal resistance values are specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 5. Thermal Resistance[1] (JEDEC 4-Layer (1S2P) Board)

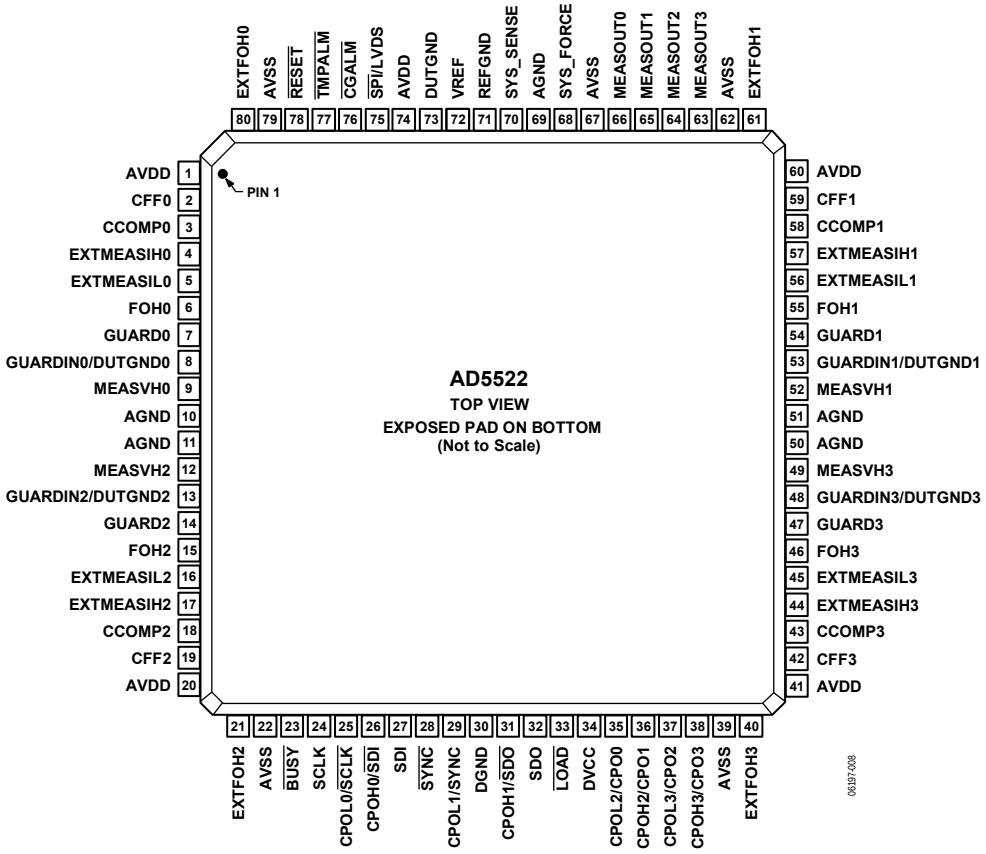
Package Type	Airflow (LFPM)	θ_{JA}	θ_{JC}	Unit
TQFP Exposed Pad on Bottom			4.8	°C/W
No Heat Sink[2]	0	22.3		°C/W
	200	17.2		°C/W
	500	15.1		°C/W
With Cooling Plate at 45°C[3]	N/A[4]	5.4	4.8	°C/W
TQFP Exposed Pad on Top			2	°C/W
No Heat Sink[2]	0	42.4		°C/W
	200	37.2		°C/W
	500	35.7		°C/W
With Cooling Plate at 45°C[3]	N/A[4]	3.0	2	°C/W

[1] The information in this section is based on simulated thermal information.
[2] These values apply to the package with no heat sink attached. The actual thermal performance of the package depends on the attached heat sink and environmental conditions.
[3] Natural convection at 55°C ambient. Assumes perfect thermal contact between the cooling plate and the exposed paddle.
[4] N/A means not applicable.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS



NOTES
1. THE EXPOSED PAD IS INTERNALLY ELECTRICALLY CONNECTED TO AVSS. FOR ENHANCED THERMAL, ELECTRICAL, AND BOARD LEVEL PERFORMANCE, THE EXPOSED PADDLE ON THE BOTTOM OF THE PACKAGE SHOULD BE SOLDERED TO A CORRESPONDING THERMAL LAND PADDLE ON THE PCB.

Figure 8. Pin Configuration, Exposed Pad on Bottom

Table 6. Pin Function Descriptions

Pin No.	Mnemonic	Description
	Exposed pad	The exposed pad is internally electrically connected to AVSS. For enhanced thermal, electrical, and board level performance, the exposed paddle on the bottom of the package should be soldered to a corresponding thermal land paddle on the PCB.
1, 20, 41, 60, 74	AVDD	Positive Analog Supply Voltage.
2	CFF0	External Capacitor for Channel 0. This pin optimizes the stability and settling time performance of the force amplifier when in force voltage mode. See the Compensation Capacitors section.
3	CCOMP0	Compensation Capacitor Input for Channel 0. See the Compensation Capacitors section.
4	EXTMEASIH0	Sense Input (High Sense) for High Current Range (Channel 0).
5	EXTMEASIL0	Sense Input (Low Sense) for High Current Range (Channel 0).
6	FOH0	Force Output for Internal Current Ranges (Channel 0).
7	GUARD0	Guard Output Drive for Channel 0.
8	GUARDIN0/ DUTGND0	Guard Amplifier Input for Channel 0/DUTGND Input for Channel 0. This dual function pin is configured via the serial interface. The default function at power-on is GUARDIN0. If this pin is configured as a DUTGND input for the channel, the input to the guard amplifier is internally connected to MEASVH0. For more information, see the Device Under Test Ground (DUTGND) section and the Guard Amplifier section.
9	MEASVH0	DUT Voltage Sense Input (High Sense) for Channel 0.
10, 11, 50, 51, 69	AGND	Analog Ground. These pins are the reference points for the analog supplies and the measure circuitry.
12	MEASVH2	DUT Voltage Sense Input (High Sense) for Channel 2.

Pin No.	Mnemonic	Description
13	GUARDIN2/ DUTGND2	Guard Amplifier Input for Channel 2/DUTGND Input for Channel 2. This dual function pin is configured via the serial interface. The default function at power-on is GUARDIN2. If this pin is configured as a DUTGND input for the channel, the input to the guard amplifier is internally connected to MEASVH2. For more information, see the Device Under Test Ground (DUTGND) section and the Guard Amplifier section.
14	GUARD2	Guard Output Drive for Channel 2.
15	FOH2	Force Output for Internal Current Ranges (Channel 2).
16	EXTMEASIL2	Sense Input (Low Sense) for High Current Range (Channel 2).
17	EXTMEASIH2	Sense Input (High Sense) for High Current Range (Channel 2).
18	CCOMP2	Compensation Capacitor Input for Channel 2. See the Compensation Capacitors section.
19	CFF2	External Capacitor for Channel 2. This pin optimizes the stability and settling time performance of the force amplifier when in force voltage mode. See the Compensation Capacitors section.
21	EXTFOH2	Force Output for High Current Range (Channel 2). Use an external resistor at this pin for current ranges up to ±80 mA. For more information, see the Current Range Selection section.
22, 39, 62, 67, 79	AVSS	Negative Analog Supply Voltage.
23	$\overline{\text{BUSY}}$	Digital Input/Open-Drain Output. This pin indicates the status of the interface. See the $\overline{\text{BUSY}}$ and $\overline{\text{LOAD}}$ Functions section for more information.
24	SCLK	Serial Clock Input, Active Falling Edge. Data is clocked into the shift register on the falling edge of SCLK. This pin operates at clock speeds up to 50 MHz.
25	CPOL0/$\overline{\text{SCLK}}$	Comparator Output Low (Channel 0) for SPI Interface/Differential Serial Clock Input (Complement) for LVDS Interface.
26	CPOH0/$\overline{\text{SDI}}$	Comparator Output High (Channel 0) for SPI Interface/Differential Serial Data Input (Complement) for LVDS Interface.
27	SDI	Serial Data Input for SPI or LVDS Interface.
28	$\overline{\text{SYNC}}$	Active Low Frame Synchronization Input for SPI or LVDS Interface.
29	CPOL1/SYNC	Comparator Output Low (Channel 1) for SPI Interface/Differential SYNC Input for LVDS Interface.
30	DGND	Digital Ground Reference Point.
31	CPOH1/$\overline{\text{SDO}}$	Comparator Output High (Channel 1) for SPI Interface/Differential Serial Data Output (Complement) for LVDS Interface.
32	SDO	Serial Data Output for SPI or LVDS Interface. This pin can be used for data readback and diagnostic purposes.
33	$\overline{\text{LOAD}}$	Logic Input (Active Low). This pin synchronizes updates within one device or across a group of devices. If synchronization is not required, $\overline{\text{LOAD}}$ can be tied low; in this case, DAC channels and PMU modes are updated immediately after $\overline{\text{BUSY}}$ goes high. See the $\overline{\text{BUSY}}$ and $\overline{\text{LOAD}}$ Functions section for more information.
34	DVCC	Digital Supply Voltage.
35	CPOL2/CPO0	Comparator Output Low (Channel 2) for SPI Interface/Comparator Output Window (Channel 0) for LVDS Interface.
36	CPOH2/CPO1	Comparator Output High (Channel 2) for SPI Interface/Comparator Output Window (Channel 1) for LVDS Interface.
37	CPOL3/CPO2	Comparator Output Low (Channel 3) for SPI Interface/Comparator Output Window (Channel 2) for LVDS Interface.
38	CPOH3/CPO3	Comparator Output High (Channel 3) for SPI Interface/Comparator Output Window (Channel 3) for LVDS Interface.
40	EXTFOH3	Force Output for High Current Range (Channel 3). Use an external resistor at this pin for current ranges up to ±80 mA. For more information, see the Current Range Selection section.
42	CFF3	External Capacitor for Channel 3. This pin optimizes the stability and settling time performance of the force amplifier when in force voltage mode. See the Compensation Capacitors section.
43	CCOMP3	Compensation Capacitor Input for Channel 3. See the Compensation Capacitors section.
44	EXTMEASIH3	Sense Input (High Sense) for High Current Range (Channel 3).
45	EXTMEASIL3	Sense Input (Low Sense) for High Current Range (Channel 3).
46	FOH3	Force Output for Internal Current Ranges (Channel 3).
47	GUARD3	Guard Output Drive for Channel 3.
48	GUARDIN3/ DUTGND3	Guard Amplifier Input for Channel 3/DUTGND Input for Channel 3. This dual function pin is configured via the serial interface. The default function at power-on is GUARDIN3. If this pin is configured as a DUTGND input for the channel, the input to the guard amplifier is internally connected to MEASVH3. For more information, see the Device Under Test Ground (DUTGND) section and the Guard Amplifier section.

Pin No.	Mnemonic	Description
49	MEASVH3	DUT Voltage Sense Input (High Sense) for Channel 3.
52	MEASVH1	DUT Voltage Sense Input (High Sense) for Channel 1.
53	GUARDIN1/ DUTGND1	Guard Amplifier Input for Channel 1/DUTGND Input for Channel 1. This dual function pin is configured via the serial interface. The default function at power-on is GUARDIN1. If this pin is configured as a DUTGND input for the channel, the input to the guard amplifier is internally connected to MEASVH1. For more information, see the Device Under Test Ground (DUTGND) section and the Guard Amplifier section.
54	GUARD1	Guard Output Drive for Channel 1.
55	FOH1	Force Output for Internal Current Ranges (Channel 1).
56	EXTMEASIL1	Sense Input (Low Sense) for High Current Range (Channel 1).
57	EXTMEASIH1	Sense Input (High Sense) for High Current Range (Channel 1).
58	CCOMP1	Compensation Capacitor Input for Channel 1. See the Compensation Capacitors section.
59	CFF1	External Capacitor for Channel 1. This pin optimizes the stability and settling time performance of the force amplifier when in force voltage mode. See the Compensation Capacitors section.
61	EXTFOH1	Force Output for High Current Range (Channel 1). Use an external resistor at this pin for current ranges up to ±80 mA. For more information, see the Current Range Selection section.
63	MEASOUT3	Multiplexed DUT Voltage, Current Sense Output, Temperature Sensor Voltage for Channel 3. This pin is referenced to AGND.
64	MEASOUT2	Multiplexed DUT Voltage, Current Sense Output, Temperature Sensor Voltage for Channel 2. This pin is referenced to AGND.
65	MEASOUT1	Multiplexed DUT Voltage, Current Sense Output, Temperature Sensor Voltage for Channel 1. This pin is referenced to AGND.
66	MEASOUT0	Multiplexed DUT Voltage, Current Sense Output, Temperature Sensor Voltage for Channel 0. This pin is referenced to AGND.
68	SYS_FORCE	External Force Signal Input. This pin enables the connection of the system PMU.
70	SYS_SENSE	External Sense Signal Output. This pin enables the connection of the system PMU.
71	REFGND	Accurate Analog Reference Input Ground.
72	VREF	Reference Input for DAC Channels (5 V for specified performance).
73	DUTGND	DUT Voltage Sense Input (Low Sense). By default, this input is shared among all four PMU channels. If a DUTGND input is required for each channel, the user can configure the GUARDINx/DUTGNDx pins as DUTGND inputs for each PMU channel.
75	$\overline{\text{SPI}}$/LVDS	Interface Select Pin. Logic low selects SPI-compatible interface mode; logic high selects LVDS interface mode. This pin has a pull-down current source (~350 µA). In LVDS interface mode, the CPOHx and CPOLx pins default to differential interface pins.
76	$\overline{\text{CGALM}}$	Open-Drain Output for Guard and Clamp Alarms. This open-drain pin provides shared alarm information about the guard amplifier and clamp circuitry. By default, this output pin is disabled. The system control register allows the user to enable this function and to set the open-drain output as a latched output. The user can also choose to enable alarms for the guard amplifier, the clamp circuitry, or both. When this pin flags an alarm, the origins of the alarm can be determined by reading back the alarm status register. Two flags per channel in this word (one latched, one unlatched) indicate which function caused the alarm and whether the alarm is still present.
77	$\overline{\text{TMPALM}}$	Open-Drain Output for Temperature Alarm. This latched, active low, open-drain output flags a temperature alarm to indicate that the junction temperature has exceeded the default temperature setting (130°C) or the user programmed temperature setting. Two flags in the alarm status register (one latched, one unlatched) indicate whether the temperature has dropped below 130°C or remains above 130°C. User action is required to clear this latched alarm flag by writing to the clear bit (Bit 6) in any of the PMU registers.
78	$\overline{\text{RESET}}$	Digital Reset Input. This active low, level sensitive input resets all internal nodes on the device to their power-on reset values.
80	EXTFOH0	Force Output for High Current Range (Channel 0). Use an external resistor at this pin for current ranges up to ±80 mA. For more information, see the Current Range Selection section.

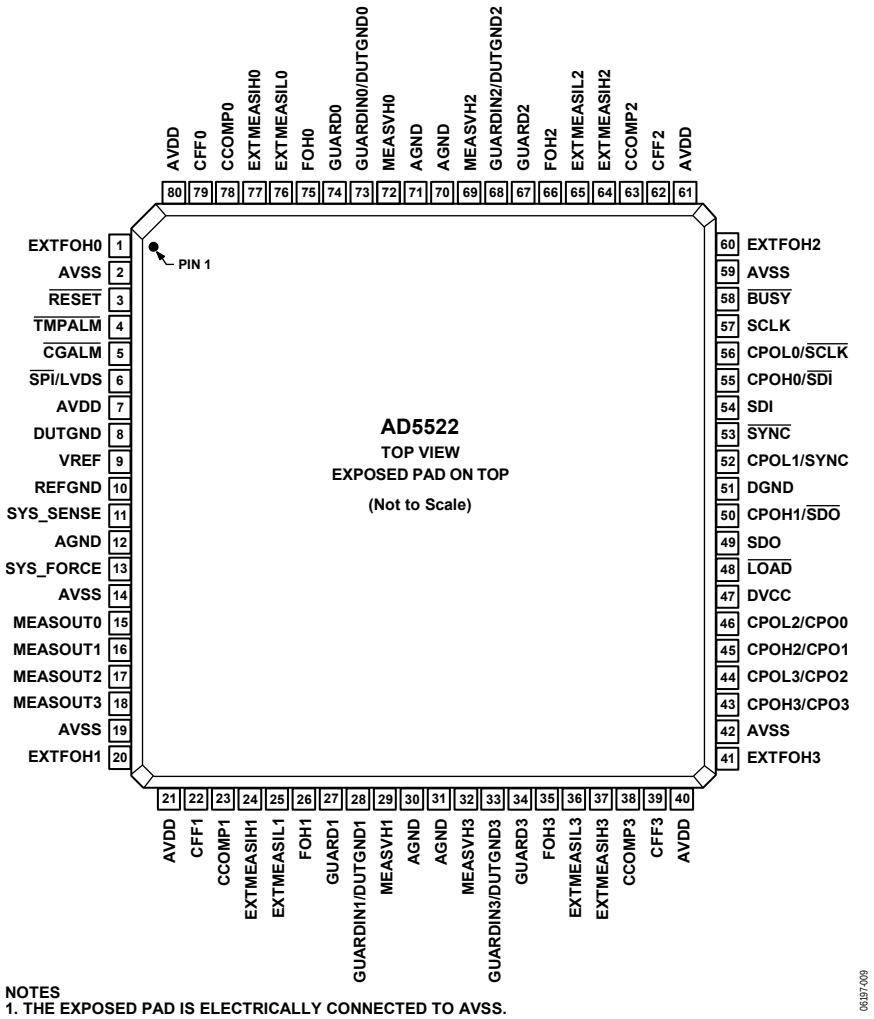


Figure 9. Pin Configuration, Exposed Pad on Top

Table 7. Pin Function Descriptions

Pin No.	Mnemonic	Description
	Exposed pad	The exposed pad is electrically connected to AVSS.
1	EXTFOH0	Force Output for High Current Range (Channel 0). Use an external resistor at this pin for current ranges up to ±80 mA. For more information, see the Current Range Selection section.
2, 14, 19, 42, 59	AVSS	Negative Analog Supply Voltage.
3	$\overline{\text{RESET}}$	Digital Reset Input. This active low, level sensitive input resets all internal nodes on the device to their power-on reset values.
4	$\overline{\text{TMPALM}}$	Open-Drain Output for Temperature Alarm. This latched, active low, open-drain output flags a temperature alarm to indicate that the junction temperature has exceeded the default temperature setting (130°C) or the user programmed temperature setting. Two flags in the alarm status register (one latched, one unlatched) indicate whether the temperature has dropped below 130°C or remains above 130°C. User action is required to clear this latched alarm flag by writing to the clear bit (Bit 6) in any of the PMU registers.
5	$\overline{\text{CGALM}}$	Open-Drain Output for Guard and Clamp Alarms. This open-drain pin provides shared alarm information about the guard amplifier and clamp circuitry. By default, this output pin is disabled. The system control register allows the user to enable this function and to set the open-drain output as a latched output. The user can also choose to enable alarms for the guard amplifier, the clamp circuitry, or both. When this pin flags an alarm, the origins of the alarm can be determined by reading back the alarm status register. Two flags per channel in this word (one latched, one unlatched) indicate which function caused the alarm and whether the alarm is still present.

Pin No.	Mnemonic	Description
6	$\overline{\text{SPI}}$/LVDS	Interface Select Pin. Logic low selects SPI-compatible interface mode; logic high selects LVDS interface mode. This pin has a pull-down current source (~350 μA). In LVDS interface mode, the CPOHx and CPOLx pins default to differential interface pins.
7, 21, 40, 61, 80	AVDD	Positive Analog Supply Voltage.
8	DUTGND	DUT Voltage Sense Input (Low Sense). By default, this input is shared among all four PMU channels. If a DUTGND input is required for each channel, the user can configure the GUARDINx/DUTGNDx pins as DUTGND inputs for each PMU channel.
9	VREF	Reference Input for DAC Channels. 5 V for specified performance.
10	REFGND	Accurate Analog Reference Input Ground.
11	SYS_SENSE	External Sense Signal Output. This pin enables the connection of the system PMU.
12, 30, 31, 70, 71	AGND	Analog Ground. These pins are the reference points for the analog supplies and the measure circuitry.
13	SYS_FORCE	External Force Signal Input. This pin enables the connection of the system PMU.
15	MEASOUT0	Multiplexed DUT Voltage, Current Sense Output, Temperature Sensor Voltage for Channel 0. This pin is referenced to AGND.
16	MEASOUT1	Multiplexed DUT Voltage, Current Sense Output, Temperature Sensor Voltage for Channel 1. This pin is referenced to AGND.
17	MEASOUT2	Multiplexed DUT Voltage, Current Sense Output, Temperature Sensor Voltage for Channel 2. This pin is referenced to AGND.
18	MEASOUT3	Multiplexed DUT Voltage, Current Sense Output, Temperature Sensor Voltage for Channel 3. This pin is referenced to AGND.
20	EXTFOH1	Force Output for High Current Range (Channel 1). Use an external resistor at this pin for current ranges up to ±80 mA. For more information, see the Current Range Selection section.
22	CFF1	External Capacitor for Channel 1. This pin optimizes the stability and settling time performance of the force amplifier when in force voltage mode. See the Compensation Capacitors section.
23	CCOMP1	Compensation Capacitor Input for Channel 1. See the Compensation Capacitors section.
24	EXTMEASIH1	Sense Input (High Sense) for High Current Range (Channel 1).
25	EXTMEASIL1	Sense Input (Low Sense) for High Current Range (Channel 1).
26	FOH1	Force Output for Internal Current Ranges (Channel 1).
27	GUARD1	Guard Output Drive for Channel 1.
28	GUARDIN1/ DUTGND1	Guard Amplifier Input for Channel 1/DUTGND Input for Channel 1. This dual function pin is configured via the serial interface. The default function at power-on is GUARDIN1. If this pin is configured as a DUTGND input for the channel, the input to the guard amplifier is internally connected to MEASVH1. For more information, see the Device Under Test Ground (DUTGND) section and the Guard Amplifier section.
29	MEASVH1	DUT Voltage Sense Input (High Sense) for Channel 1.
32	MEASVH3	DUT Voltage Sense Input (High Sense) for Channel 3.
33	GUARDIN3/ DUTGND3	Guard Amplifier Input for Channel 3/DUTGND Input for Channel 3. This dual function pin is configured via the serial interface. The default function at power-on is GUARDIN3. If this pin is configured as a DUTGND input for the channel, the input to the guard amplifier is internally connected to MEASVH3. For more information, see the Device Under Test Ground (DUTGND) section and the Guard Amplifier section.
34	GUARD3	Guard Output Drive for Channel 3.
35	FOH3	Force Output for Internal Current Ranges (Channel 3).
36	EXTMEASIL3	Sense Input (Low Sense) for High Current Range (Channel 3).
37	EXTMEASIH3	Sense Input (High Sense) for High Current Range (Channel 3).
38	CCOMP3	Compensation Capacitor Input for Channel 3. See the Compensation Capacitors section.
39	CFF3	External Capacitor for Channel 3. This pin optimizes the stability and settling time performance of the force amplifier when in force voltage mode. See the Compensation Capacitors section.
41	EXTFOH3	Force Output for High Current Range (Channel 3). Use an external resistor at this pin for current ranges up to ±80 mA. For more information, see the Current Range Selection section.
43	CPOH3/CPO3	Comparator Output High (Channel 3) for SPI Interface/Comparator Output Window (Channel 3) for LVDS Interface.
44	CPOL3/CPO2	Comparator Output Low (Channel 3) for SPI Interface/Comparator Output Window (Channel 2) for LVDS Interface.
45	CPOH2/CPO1	Comparator Output High (Channel 2) for SPI Interface/Comparator Output Window (Channel 1) for LVDS Interface.

Pin No.	Mnemonic	Description
46	CPOL2/CPO0	Comparator Output Low (Channel 2) for SPI Interface/Comparator Output Window (Channel 0) for LVDS Interface.
47	DVCC	Digital Supply Voltage.
48	$\overline{\text{LOAD}}$	Logic Input (Active Low). This pin synchronizes updates within one device or across a group of devices. If synchronization is not required, $\overline{\text{LOAD}}$ can be tied low; in this case, DAC channels and PMU modes are updated immediately after $\overline{\text{BUSY}}$ goes high. See the $\overline{\text{BUSY}}$ and $\overline{\text{LOAD}}$ Functions section for more information.
49	SDO	Serial Data Output for SPI or LVDS Interface. This pin can be used for data readback and diagnostic purposes.
50	CPOH1/$\overline{\text{SDO}}$	Comparator Output High (Channel 1) for SPI Interface/Differential Serial Data Output (Complement) for LVDS Interface.
51	DGND	Digital Ground Reference Point.
52	CPOL1/SYNC	Comparator Output Low (Channel 1) for SPI Interface/Differential SYNC Input for LVDS Interface.
53	$\overline{\text{SYNC}}$	Active Low Frame Synchronization Input for SPI or LVDS Interface.
54	SDI	Serial Data Input for SPI or LVDS Interface.
55	CPOH0/$\overline{\text{SDI}}$	Comparator Output High (Channel 0) for SPI Interface/Differential Serial Data Input (Complement) for LVDS Interface.
56	CPOL0/$\overline{\text{SCLK}}$	Comparator Output Low (Channel 0) for SPI Interface/Differential Serial Clock Input (Complement) for LVDS Interface.
57	SCLK	Serial Clock Input, Active Falling Edge. Data is clocked into the shift register on the falling edge of SCLK. This pin operates at clock speeds up to 50 MHz.
58	$\overline{\text{BUSY}}$	Digital Input/Open-Drain Output. This pin indicates the status of the interface. See the $\overline{\text{BUSY}}$ and $\overline{\text{LOAD}}$ Functions section for more information.
60	EXTFOH2	Force Output for High Current Range (Channel 2). Use an external resistor at this pin for current ranges up to ±80 mA. For more information, see the Current Range Selection section.
62	CFF2	External Capacitor for Channel 2. This pin optimizes the stability and settling time performance of the force amplifier when in force voltage mode. See the Compensation Capacitors section.
63	CCOMP2	Compensation Capacitor Input for Channel 2. See the Compensation Capacitors section.
64	EXTMEASIH2	Sense Input (High Sense) for High Current Range (Channel 2).
65	EXTMEASIL2	Sense Input (Low Sense) for High Current Range (Channel 2).
66	FOH2	Force Output for Internal Current Ranges (Channel 2).
67	GUARD2	Guard Output Drive for Channel 2.
68	GUARDIN2/ DUTGND2	Guard Amplifier Input for Channel 2/DUTGND Input for Channel 2. This dual function pin is configured via the serial interface. The default function at power-on is GUARDIN2. If this pin is configured as a DUTGND input for the channel, the input to the guard amplifier is internally connected to MEASVH2. For more information, see the Device Under Test Ground (DUTGND) section and the Guard Amplifier section.
69	MEASVH2	DUT Voltage Sense Input (High Sense) for Channel 2.
72	MEASVH0	DUT Voltage Sense Input (High Sense) for Channel 0.
73	GUARDIN0/ DUTGND0	Guard Amplifier Input for Channel 0/DUTGND Input for Channel 0. This dual function pin is configured via the serial interface. The default function at power-on is GUARDIN0. If this pin is configured as a DUTGND input for the channel, the input to the guard amplifier is internally connected to MEASVH0. For more information, see the Device Under Test Ground (DUTGND) section and the Guard Amplifier section.
74	GUARD0	Guard Output Drive for Channel 0.
75	FOH0	Force Output for Internal Current Ranges (Channel 0).
76	EXTMEASIL0	Sense Input (Low Sense) for High Current Range (Channel 0).
77	EXTMEASIH0	Sense Input (High Sense) for High Current Range (Channel 0).
78	CCOMP0	Compensation Capacitor Input for Channel 0. See the Compensation Capacitors section.
79	CFF0	External Capacitor for Channel 0. This pin optimizes the stability and settling time performance of the force amplifier when in force voltage mode. See the Compensation Capacitors section.

TYPICAL PERFORMANCE CHARACTERISTICS

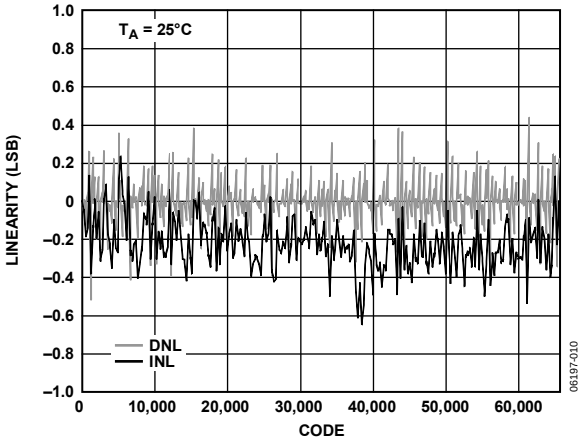


Figure 10. Force Voltage Linearity vs. Code, All Ranges, 1 LSB = 0.0015% FSR (20 V FSR)

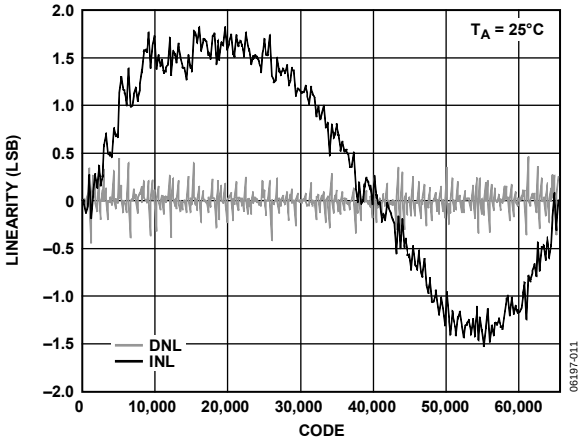


Figure 11. Force Current Linearity vs. Code, All Ranges, 1 LSB = 0.0015% FSR (20 V FSR)

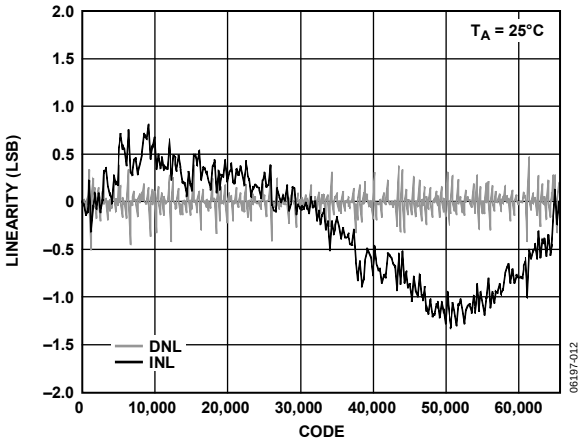


Figure 12. Measure Voltage Linearity vs. Code, All Ranges, 1 LSB = 0.0015% FSR (20 V FSR), MEASOUTx Gain = 1

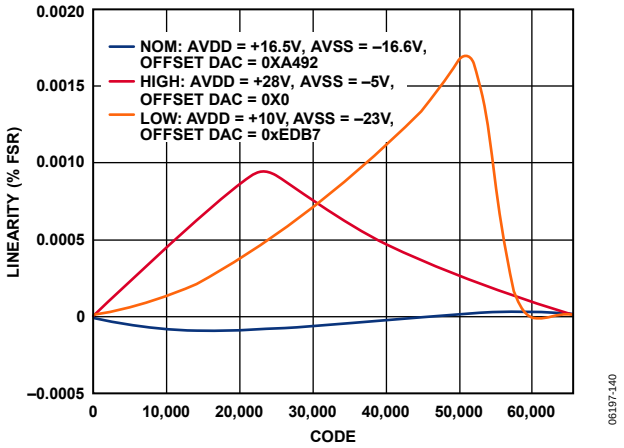


Figure 13. Measure Voltage Linearity vs. Code, All Ranges, MEASOUTx Gain = 0.2

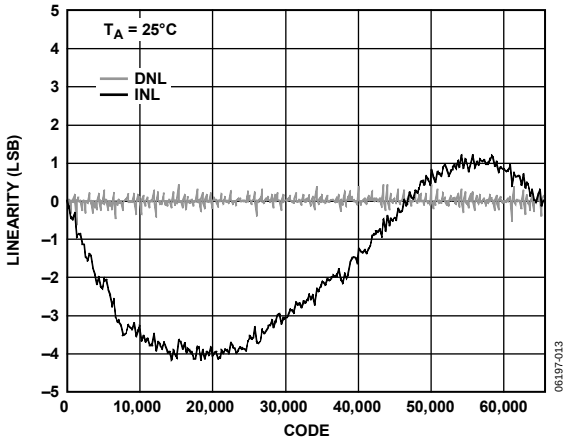


Figure 14. Measure Current Linearity vs. Code, All Ranges, 1 LSB = 0.0015% FSR (20 V FSR), MI Gain = 10, MEASOUTx Gain = 1

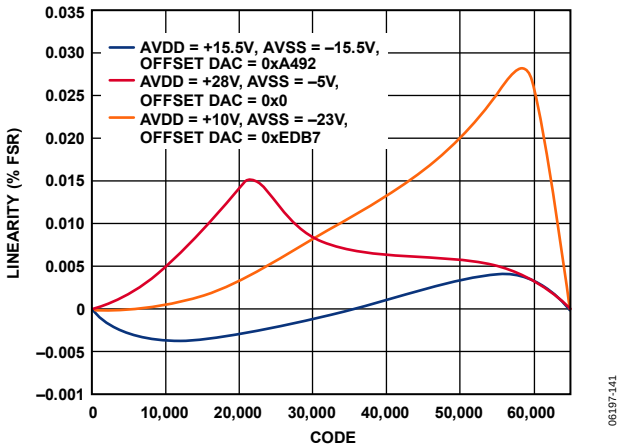


Figure 15. Measure Current Linearity vs. Code, All Ranges, MEASOUTx Gain = 0.2, MI Gain = 10

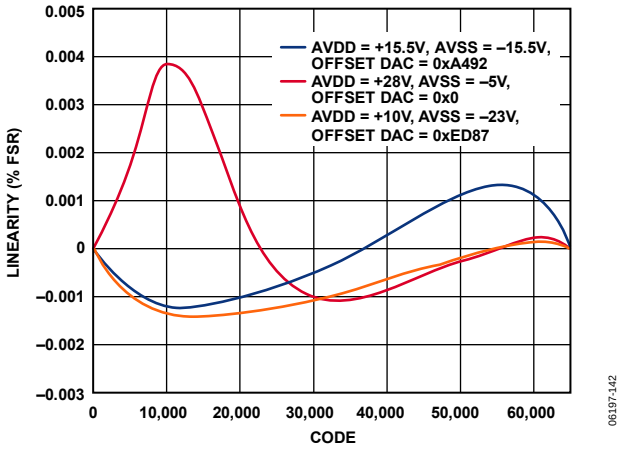


Figure 16. Measure Current Linearity vs. Code, All Ranges, MEASOUTx Gain = 0.2, MI Gain = 5

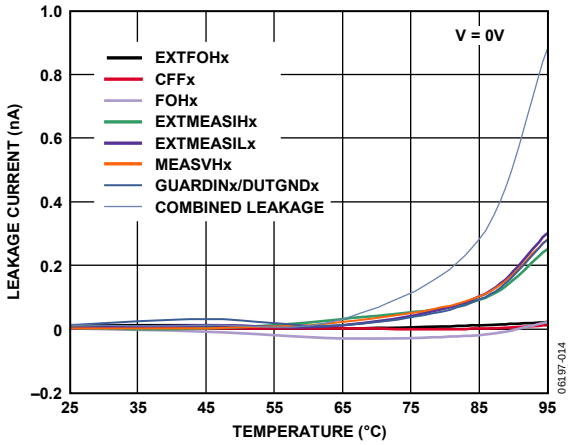


Figure 17. Leakage Current vs. Temperature (Stress Voltage = 0 V)

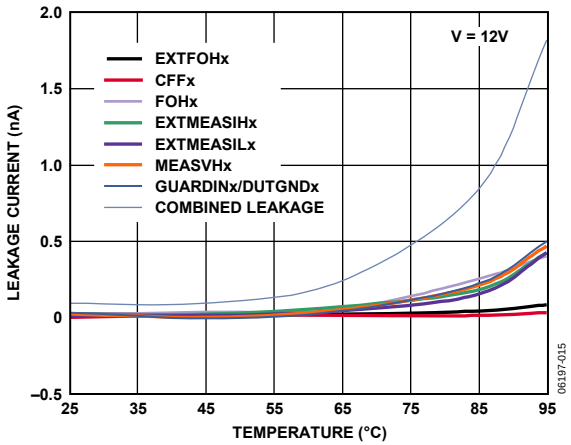


Figure 18. Leakage Current vs. Temperature (Stress Voltage = 12 V)

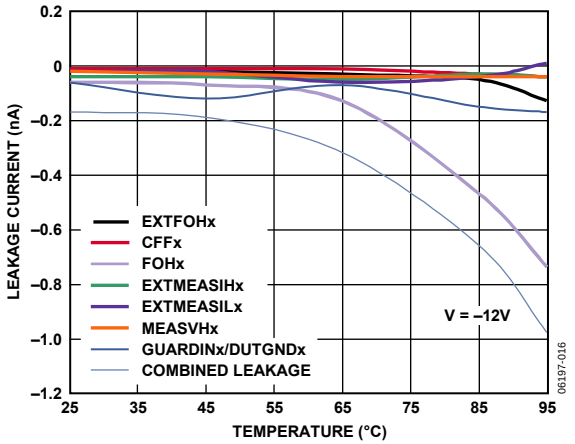


Figure 19. Leakage Current vs. Temperature (Stress Voltage = –12 V)

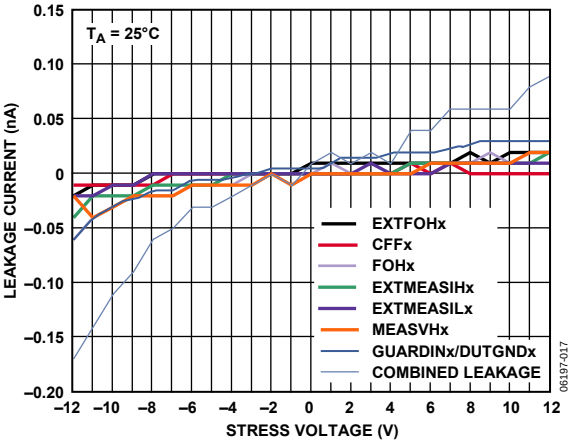


Figure 20. Leakage Current vs. Stress Voltage

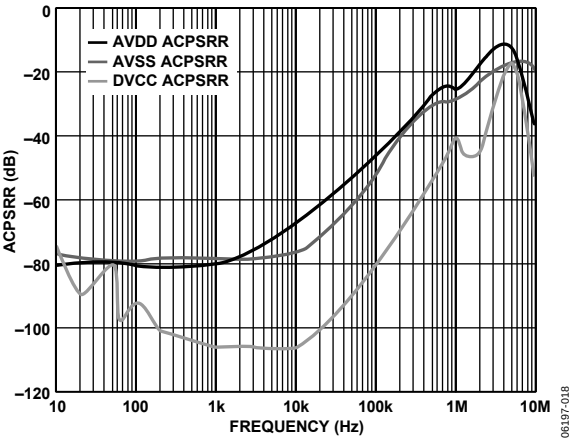


Figure 21. ACPSRR at FOHx in Force Voltage Mode vs. Frequency

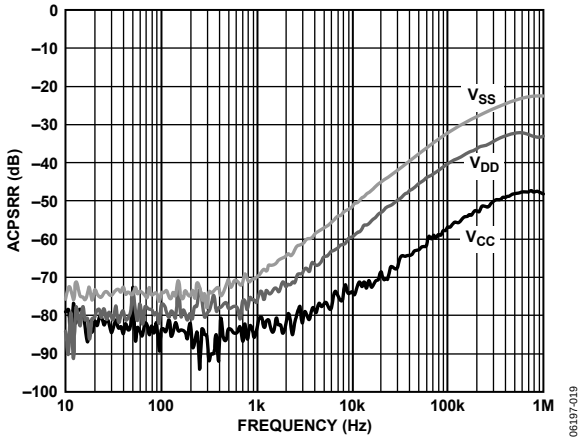


Figure 22. ACPSRR at FOHx in Force Current Mode vs. Frequency (MI Gain = 10)

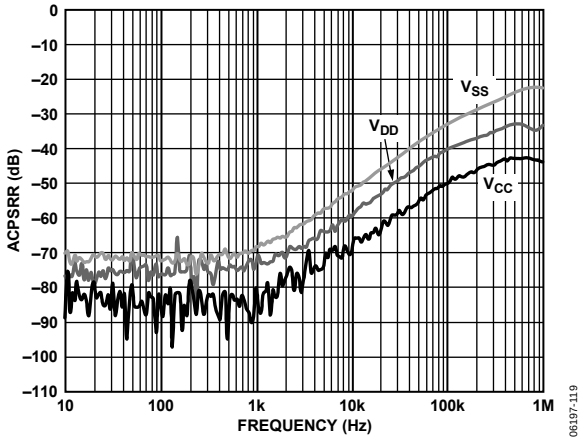


Figure 23. ACPSRR at FOHx in Force Current Mode vs. Frequency (MI Gain = 5)

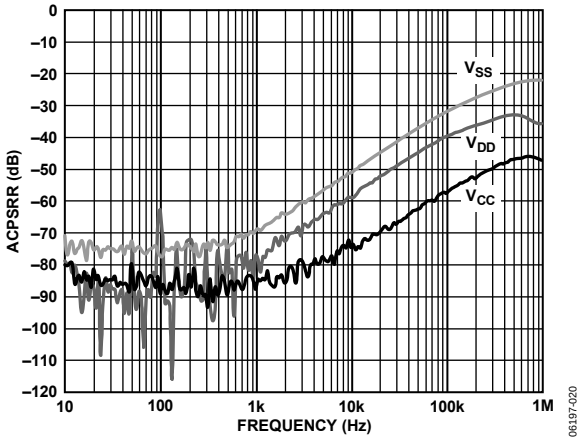


Figure 24. ACPSRR at MEASOUTx in Measure Voltage Mode vs. Frequency (MEASOUT Gain = 1)

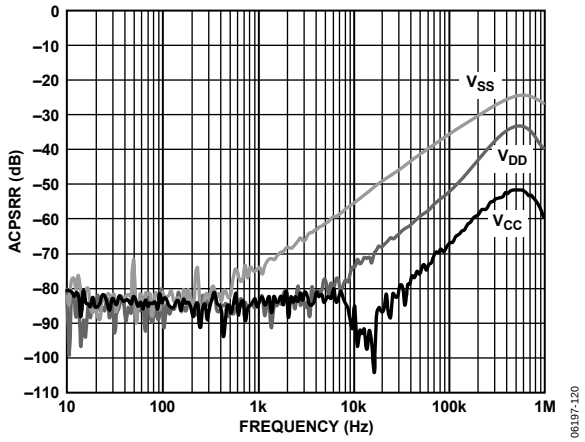


Figure 25. ACPSRR at MEASOUTx in Measure Voltage Mode vs. Frequency (MEASOUT Gain = 0.2)

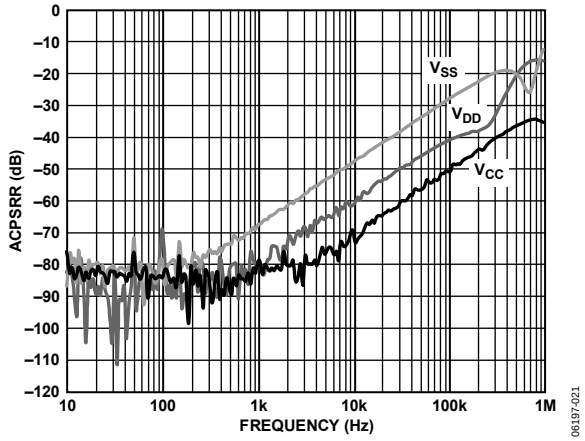


Figure 26. ACPSRR at MEASOUTx in Measure Current Mode vs. Frequency (MI Gain = 10, MEASOUT Gain = 1)

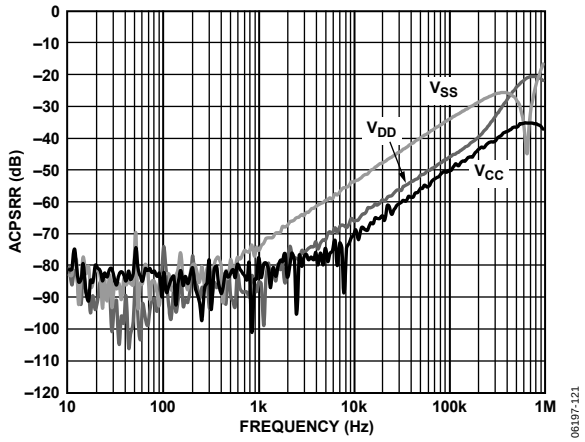


Figure 27. ACPSRR at MEASOUTx in Measure Current Mode vs. Frequency (MI Gain = 5, MEASOUT Gain = 1)

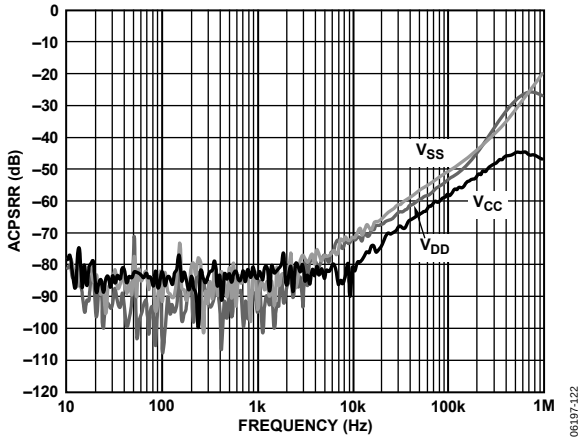


Figure 28. APCSRR at MEASOUTx in Measure Current Mode vs. Frequency (MI Gain = 10, MEASOUT Gain = 0.2)

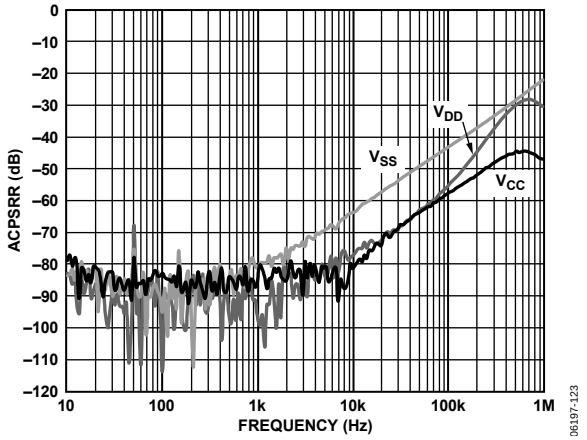


Figure 29. APCSRR at MEASOUTx in Measure Current Mode vs. Frequency (MI Gain = 5, MEASOUT Gain = 0.2)

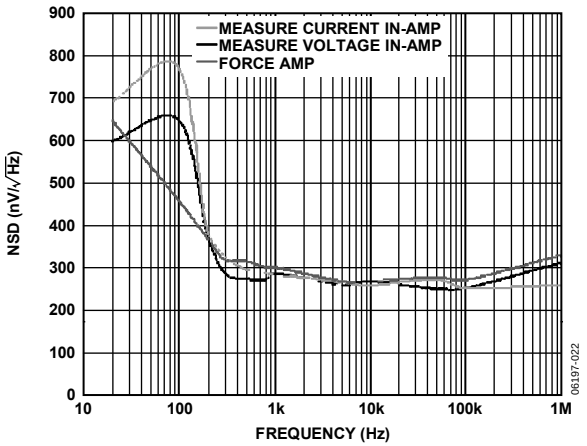


Figure 30. NSD vs. Frequency (Measured in FVMV and FVMI Mode)

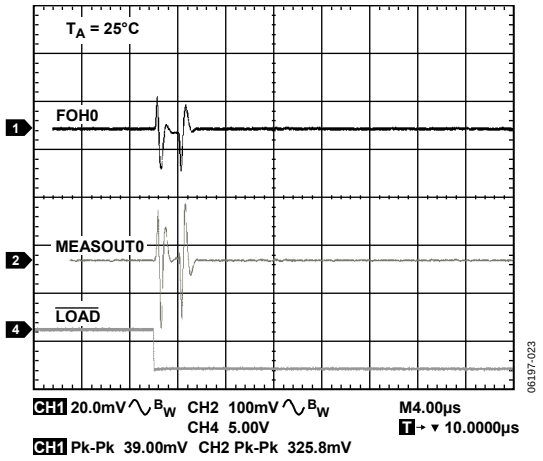


Figure 31. AC Crosstalk, FVMI Mode, PMU 0, Full-Scale Transition on One CPH DAC, MI Gain = 10, MEASOUT Gain = 1, ±2 mA Range, C_{LOAD} = 200 pF

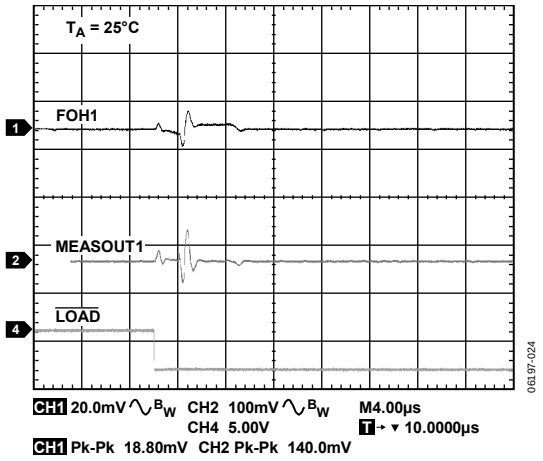


Figure 32. AC Crosstalk, FVMI Mode, PMU 1, Full-Scale Transition on One CPH DAC, MI Gain = 10, MEASOUT Gain = 1, ±2 mA Range, C_{LOAD} = 200 pF

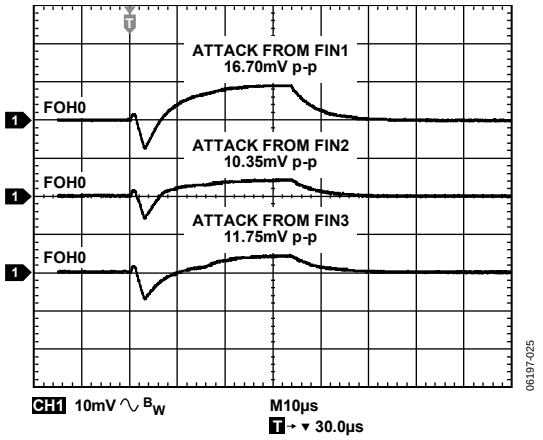


Figure 33. AC Crosstalk at FOH0 in FI Mode from FIN DAC of Each Other PMU (Full-Scale Transition), MI Gain = 10, MEASOUT Gain = 1, ±2 mA Range, C_{LOAD} = 200 pF

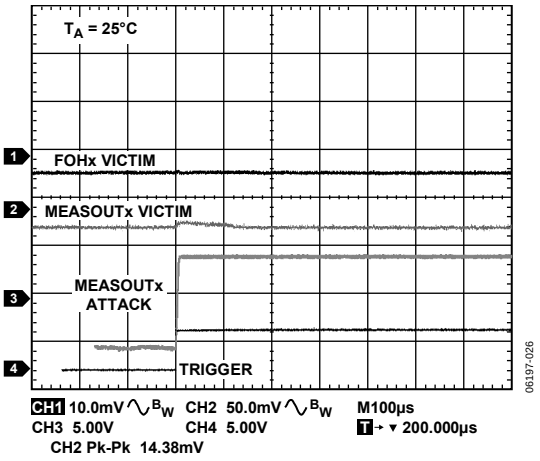


Figure 34. Shorted DUT AC Crosstalk, Victim PMU in FVMI Mode (±200 µA Range)

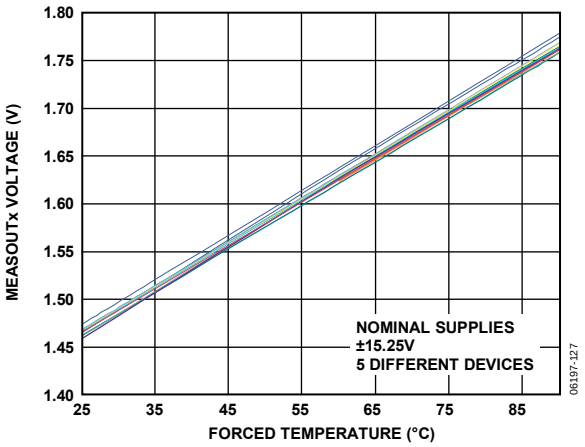


Figure 35. Temperature Sensor Voltage on MEASOUTx vs. Forced Temperature

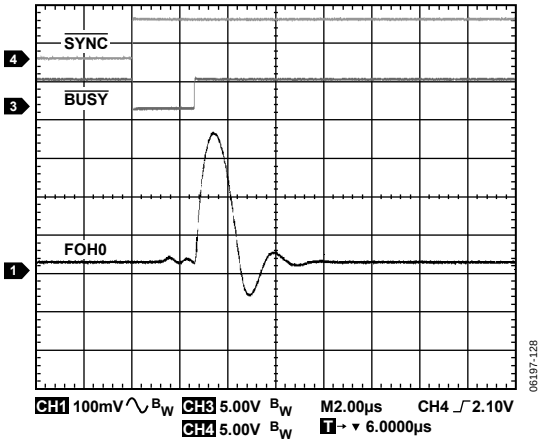


Figure 36. Range Change, PMU0, ±5 µA to ±2 mA, C_{LOAD} = 1 nF, R_{LOAD} = 620 kΩ, FV = 3 V

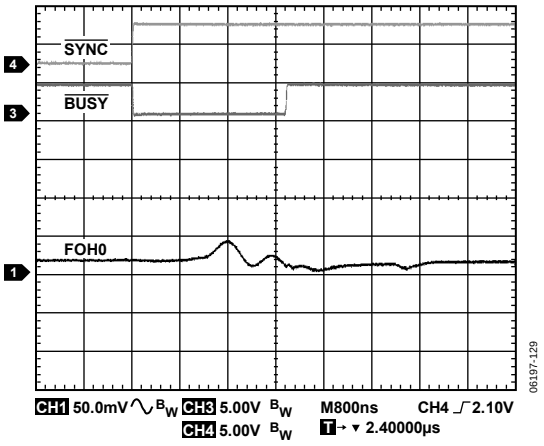


Figure 37. Range Change, PMU0, ±2 mA to ±5 µA, C_{LOAD} = 1 nF, R_{LOAD} = 620 kΩ, FV = 3 V

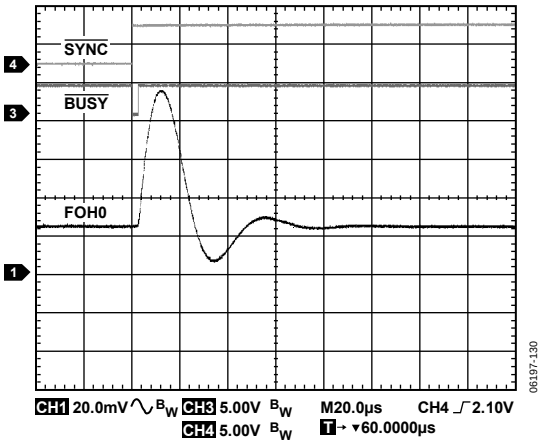


Figure 38. Range Change, PMU0, ±5 µA to ±2 mA, C_{LOAD} = 100 nF, R_{LOAD} = 620 kΩ, FV = 3 V

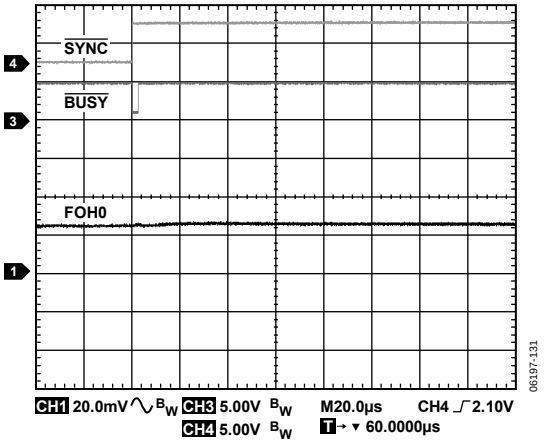


Figure 39. Range Change, PMU0, ±2 mA to ±5 µA, C_{LOAD} = 100 nF, R_{LOAD} = 620 kΩ, FV = 3 V

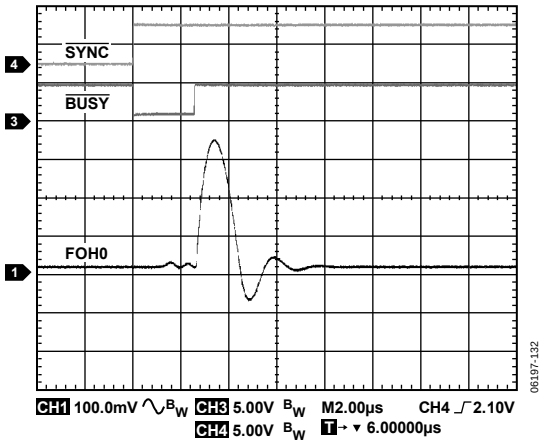


Figure 40. Range Change, PMU0, ±20 µA to ±2 mA, C_{LOAD} = 1 nF, R_{LOAD} = 150 kΩ, FV = 3 V

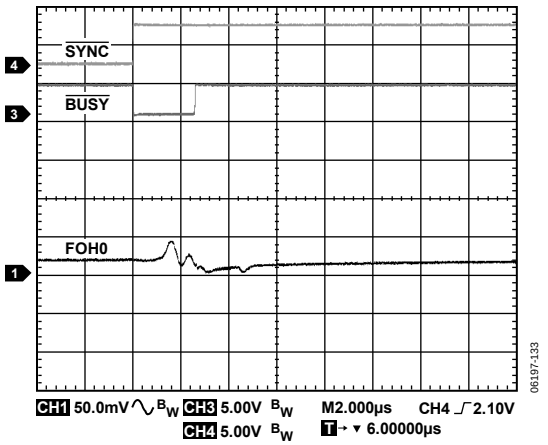


Figure 41. Range Change, PMU0, ±2 mA to ±20 µA, C_{LOAD} = 1 nF, R_{LOAD} = 150 kΩ, FV = 3 V

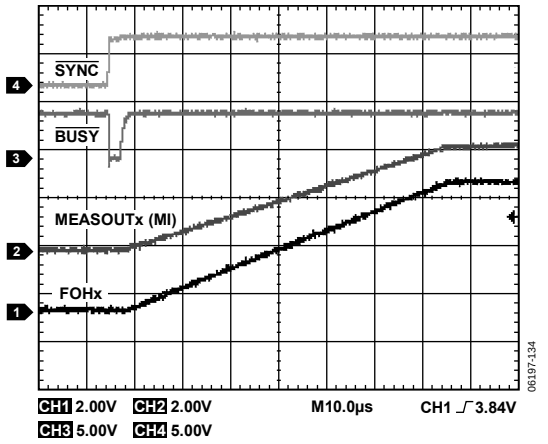


Figure 42. FV Settling, 0 V to 5 V, ±2 mA Range, C_{LOAD} = 220 pF, CCOMPx = 1 nF, R_{LOAD} = 5.6 kΩ

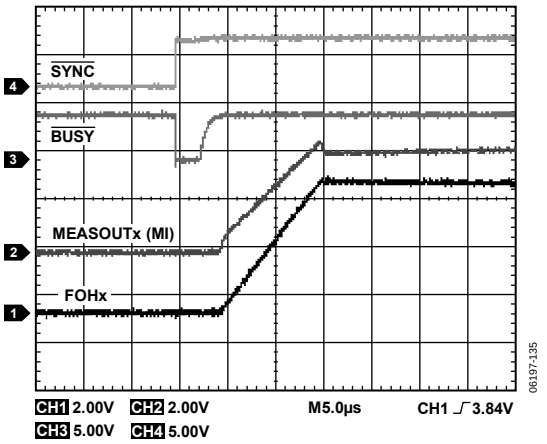


Figure 43. FV Settling, 0 V to 5 V, ±2 mA Range, C_{LOAD} = 220 pF, CCOMPx = 100 pF, R_{LOAD} = 5.6 kΩ

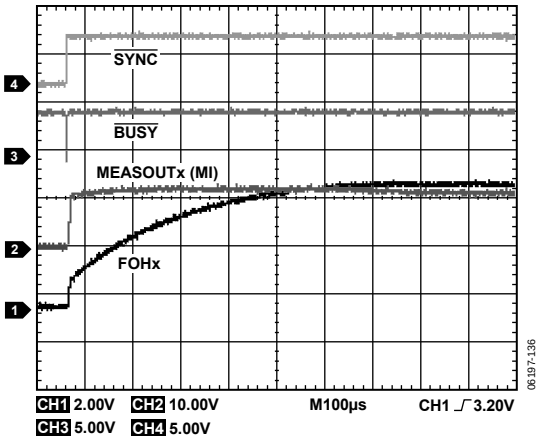


Figure 44. FV Settling, 0 V to 5 V, ±5 µA Range, C_{LOAD} = 220 pF, CCOMPx = 100 pF, R_{LOAD} = 1 MΩ

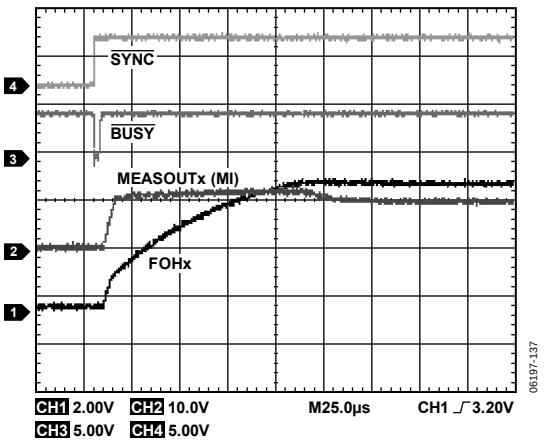


Figure 45. FV Settling, 0 V to 5 V, ±20 µA Range, C_{LOAD} = 220 pF, CCOMPx = 100 pF, R_{LOAD} = 270 kΩ

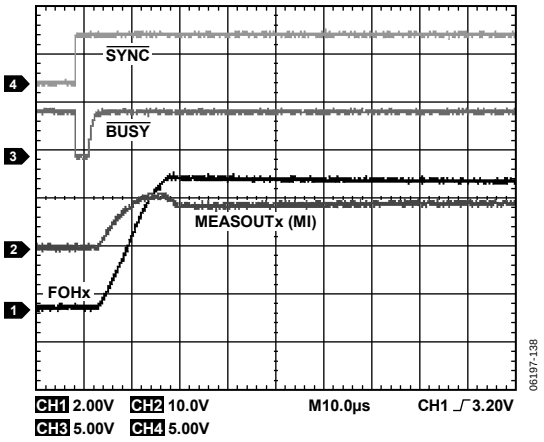


Figure 46. FV Settling, 0 V to 5 V, ±200 µA Range, C_{LOAD} = 220 pF, CCOMPx = 100 pF, R_{LOAD} = 27 kΩ

TERMINOLOGY

Offset Error
Offset error is a measure of the difference between the actual voltage and the ideal voltage at midscale or at zero current expressed in mV or % FSR.

Gain Error
Gain error is the difference between full-scale error and zero-scale error. It is expressed in % FSR.

Gain Error = Full-Scale Error − Zero-Scale Error

where:
Full-Scale Error is the difference between the actual voltage and the ideal voltage at full scale.
Zero-Scale Error is the difference between the actual voltage and the ideal voltage at zero scale.

Linearity Error
Linearity error, or relative accuracy, is a measure of the maximum deviation from a straight line passing through the endpoints of the full-scale range. It is measured after adjusting for gain error and offset error and is expressed in % FSR.

Differential Nonlinearity (DNL)
Differential nonlinearity is the difference between the measured change and the ideal 1 LSB change between any two adjacent codes. A specified differential nonlinearity of ±1 LSB maximum ensures monotonicity.

Common-Mode (CM) Error
Common-mode (CM) error is the error at the output of the amplifier due to the common-mode input voltage. It is expressed in % of FSVR/V.

Leakage Current
Leakage current is the current measured at an output pin when that function is off or high impedance.

Pin Capacitance
Pin capacitance is the capacitance measured at a pin when that function is off or high impedance.

Slew Rate
The slew rate is the rate of change of the output voltage expressed in V/µs.

Output Voltage Settling Time
Output voltage settling time is the amount of time it takes for the output of a DAC to settle to a specified level for a full-scale input change.

Digital-to-Analog Glitch Energy
Digital-to-analog glitch energy is the amount of energy that is injected into the analog output at the major code transition. It is specified as the area of the glitch in nV-sec. It is measured by toggling the DAC register data between 0x7FFF and 0x8000.

Digital Crosstalk
Digital crosstalk is defined as the glitch impulse transferred to the output of one converter due to a change in the DAC register code of another converter. It is specified in nV-sec.

AC Crosstalk
AC crosstalk is defined as the glitch impulse transferred to the output of one PMU due to a change in any of the DAC registers in the package.

ACPSRR

ACPSRR is a measure of the ability of the device to avoid coupling noise and spurious signals that appear on the supply voltage pin to the output of the switch. The dc voltage on the device is modulated by a sine wave of 0.2 V p-p. The ratio of the amplitude of the signal on the output to the amplitude of the modulation is the ACPSRR.

THEORY OF OPERATION

The AD5522 is a highly integrated, quad per-pin parametric measurement unit (PPMU) for use in semiconductor automated test equipment. It provides programmable modes to force a pin voltage and measure the corresponding current (FVMI) and to force a pin current and measure the corresponding voltage (FIMV). The device is also capable of all other combinations, including force high-Z and measure high-Z. The PPMU can force or measure a voltage range of 22.5 V. It can force or measure currents up to ±80 mA per channel using the internal amplifier; the addition of an external amplifier enables higher current ranges. All the DAC levels required for each PMU channel are on chip.

FORCE AMPLIFIER

The force amplifier drives the analog output, FOHx, which drives a programmed current or voltage to the device under test (DUT). Headroom and footroom requirements for this amplifier are 3 V on either end. An additional ±1 V is dropped across the sense resistor when maximum (rated) current is flowing through it.

The force amplifier is designed to drive DUT capacitances up to 10 nF, with a compensation value of 100 pF. Larger DUT capacitive loads require larger compensation capacitances.

Local feedback ensures that the amplifiers are stable when disabled. A disabled channel reduces power consumption by 2.5 mA per channel.

COMPARATORS

Per channel, the DUT measured voltage or current is monitored by two comparators configured as window comparators. Internal DAC levels set the CPL (comparator low) and CPH (comparator high) threshold values. There are no restrictions on the voltage settings of the comparator highs and lows. CPL going higher than CPH is not a useful operation; however, it does not cause any problems with the device. CPOLx (comparator output low) and CPOHx (comparator output high) are continuous time comparator outputs.

Table 8. Comparator Output Function Using SPI Interface

Test Condition	CPOLx	CPOHx
V_{DUT} or I_{DUT} > CPH		0
V_{DUT} or I_{DUT} < CPH		1
V_{DUT} or I_{DUT} > CPL	1	
V_{DUT} or I_{DUT} < CPL	0	
CPH > V_{DUT} or I_{DUT} > CPL	1	1

When using the SPI interface, full comparator functionality is available. When using the LVDS interface, the comparator function is limited to one output per comparator, due to the large pin count requirement of the LVDS interface.

When using the LVDS interface, the comparator output available pins, CPO0 to CPO3, provide information on whether the measured voltage or current is inside or outside the set CPH and CPL window. Information on whether the measurement was high or low is available via the serial interface (comparator status register).

Table 9. Comparator Output Function Using LVDS Interface

Test Condition	CPOx Output
(CPL < (V_{DUT} or I_{DUT})) and ((V_{DUT} or I_{DUT}) < CPH)	1
(CPL > (V_{DUT} or I_{DUT})) or ((V_{DUT} or I_{DUT}) > CPH)	0

CLAMPS

Current and voltage clamps are included on chip, one clamp for each PMU channel. The clamps protect the DUT in the event of an open-circuit or short-circuit condition. Internal DAC levels set the CLL (clamp low) and CLH (clamp high) levels. The clamps work to limit the force amplifier if a voltage or current at the DUT exceeds the set levels. The clamps also protect the DUT if a transient voltage or current spike occurs when changing to a different operating mode or when programming the device to a different current range.

The voltage clamps are available while forcing current, and the current clamps are available while forcing voltage. The user can set up the voltage or current clamp status (enabled or disabled) using the serial interface (system control register or PMU register).

Each clamp has a smooth, finite transition region between normal (unclamped) operation and the final clamped level, and an internal flag is activated within this transition zone. The open-drain $\overline{\text{CGALM}}$ pin indicates whether one or more PMU channels has clamped. The clamp status of an individual PMU can be determined by polling the alarm status register using the SPI or LVDS interface.

CLL should never be greater than CLH. For the voltage clamps, there should be 500 mV between the CLL and CLH levels to ensure that a region exists in the middle of the clamps where both are off. Similarly, set current clamps ±250 mV away from 0 A.

The transfer function for voltage clamping in FI mode is

$$VCLL \text{ or } VCLH = 4.5 \times VREF \times (DAC\_CODE/2^{16}) - (3.5 \times VREF \times (OFFSET\_DAC\_CODE/2^{16})) + DUTGND$$

See the DAC Levels section for more information.

The transfer function for current clamping in FV mode is

$$ICLL \text{ or } ICLH = 4.5 \times VREF \times ((DAC\_CODE - 32{,}768)/2^{16})/(R_{SENSE} \times MI\_Amplifier\_Gain)$$

where:
R_{SENSE} is the sense resistor of the selected current range.
MI_Amplifier_Gain is the gain of the measure current instrumentation amplifier, either 5 or 10.

Do not change clamp levels while the channel is in force mode because this can affect the forced voltage or current applied to the DUT. Similarly, the clamps should not be enabled or disabled during a force operation.

When the AD5522 is placed in high-Z mode, the clamp circuit is always configured to monitor the measure current signal (irrespective of which high-Z mode is selected, high-Z V or high-Z I). At this time, the clamp circuit is also comparing to the voltage clamp levels. Because the device is in high-Z mode, the measure current signal is at zero, but zero for the measure current is always the VMID voltage set by the offset DAC. For default offset DAC conditions, this causes no concern. For other settings of the offset DAC, the zero point follows the VMID, and as the clamp circuit is comparing the voltage clamp levels to the measure current signal, there may be instances where the voltage clamp levels cause the alarm to flag during high-Z mode. To avoid this, the clamps can be disabled when going into high-Z mode.

CURRENT RANGE SELECTION

Integrated thin film resistors minimize the need for external components and allow easy selection of any of these current ranges: ±5 μA (200 kΩ), ±20 μA (50 kΩ), ±200 μA (5 kΩ), and ±2 mA (500 Ω). One current range up to ±80 mA can be accommodated per channel by connecting an external sense resistor. For current ranges in excess of ±80 mA, it is necessary that an external amplifier be used.

For the suggested current ranges, the maximum voltage drop across the sense resistors is ±1 V. However, to allow for error correction, there is some overrange available in the current ranges (±12.5% or ±0.125 V across R_{SENSE}). The full-scale voltage range that can be loaded to the FIN DAC is ±11.5 V; the forced current can be calculated as follows:

$$FI = 4.5 \times VREF \times ((DAC\_CODE - 32{,}768)/2^{16})/(R_{SENSE} \times MI\_Amplifier\_Gain)$$

where:
FI is the forced current.
R_{SENSE} is the selected sense resistor.
MI_Amplifier_Gain is the gain of the measure current instrumentation amplifier. This gain can be set to 5 or 10 via the serial interface.

In the ±200 μA range with the 5 kΩ sense resistor and an I_{SENSE} gain of 10, the maximum current range possible is ±225 μA. Similarly, for the other current ranges, there is an overrange of 12.5% to allow for error correction.

Also, the forced current range is the quoted full-scale range only with an applied reference of 5 V or 2.5 V (with I_{SENSE} amplifier gain = 5). The I_{SENSE} amplifier is biased by the VMID DAC voltage in such a way as to center the measure current output irrespective of the voltage span used.

When using the EXTFOHx outputs for current ranges up to ±80 mA, there is no switch in series with the EXTFOHx line, ensuring minimum capacitance present at the output of the force amplifier. This feature is important when using a pin electronics driver to provide high current ranges.

HIGH CURRENT RANGES

With the use of an external high current amplifier, one high current range in excess of ±80 mA is possible. The high current amplifier buffers the force output and provides the drive for the required current.

To eliminate any timing concerns when switching between the internal ranges and the external high current range, there is a mode where the internal ±80 mA stage can be enabled at all times. See Table 26 for more information.

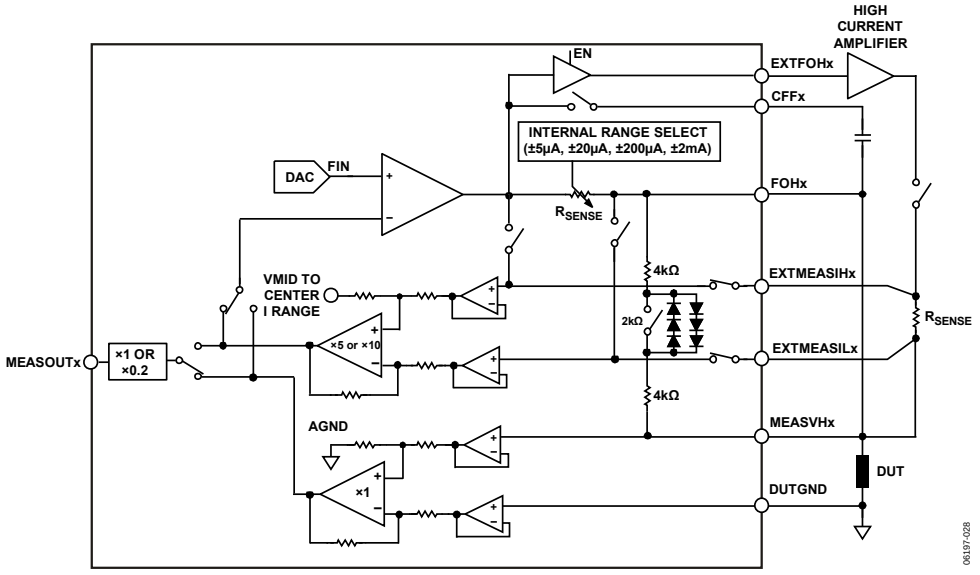


Figure 47. Addition of High Current Amplifier for Wider Current Range (>±80 mA)

MEASURE CURRENT GAINS

The measure current amplifier has two gain settings, 5 and 10. The two gain settings allow users to achieve the quoted/specified current ranges with large or small voltage swing. Use the 10 gain setting with a 5 V reference, and use the 5 gain setting with a 2.5 V reference. Both combinations ensure the specified current ranges. Using other VREF/gain setting combinations should achieve smaller current ranges only. Achieving greater current ranges than the specified ranges is outside the intended operation of the AD5522. The maximum guaranteed voltage across R_{SENSE} = ±1.125 V.

Following are examples of VREF/gain setting combinations. In these examples, the offset DAC is at its default value of 0xA492.

- VREF = 5 V results in a ±11.25 V range. Using a gain setting of 10, there is ±1.125 V maximum across R_{SENSE}, resulting in current ranges of ±5.625 μA, ±22.5 μA, and so on (including overrange of ±12.5% to allow for error correction).
- VREF = 2.5 V results in a ±5.625 V range. Using a gain setting of 5 results in current ranges of ±5.625 μA, ±22.5 μA, and so on (including overrange of ±12.5% to allow for error correction).

VREF = 3.5 V results in a ±7.87 V range. Using a gain setting of 10, there is ±0.785 V maximum across R_{SENSE}, resulting in current ranges of ±3.92 μA, ±15.74 μA, and so on (including overrange of ±12.5% to allow for error correction).

VMID VOLTAGE

The midcode voltage (VMID) is used in the measure current amplifier block to center the current ranges about 0 A. This is required to ensure that the quoted current ranges can be achieved when using offset DAC settings other than the default. VMID corresponds to 0x8000 or the DAC midcode value, that is, the middle of the voltage range set by the offset DAC setting (see Table 13). See the block diagram in Figure 48.

$$VMID = 4.5 \times VREF \times (32{,}768/2^{16}) - (3.5 \times VREF \times (OFFSET\_DAC\_CODE/2^{16}))$$

or

$$VMID = 3.5 \times VREF \times ((42{,}130 - OFFSET\_DAC\_CODE)/2^{16})$$

$$VMIN = -3.5 \times VREF \times (OFFSET\_DAC\_CODE/2^{16})$$

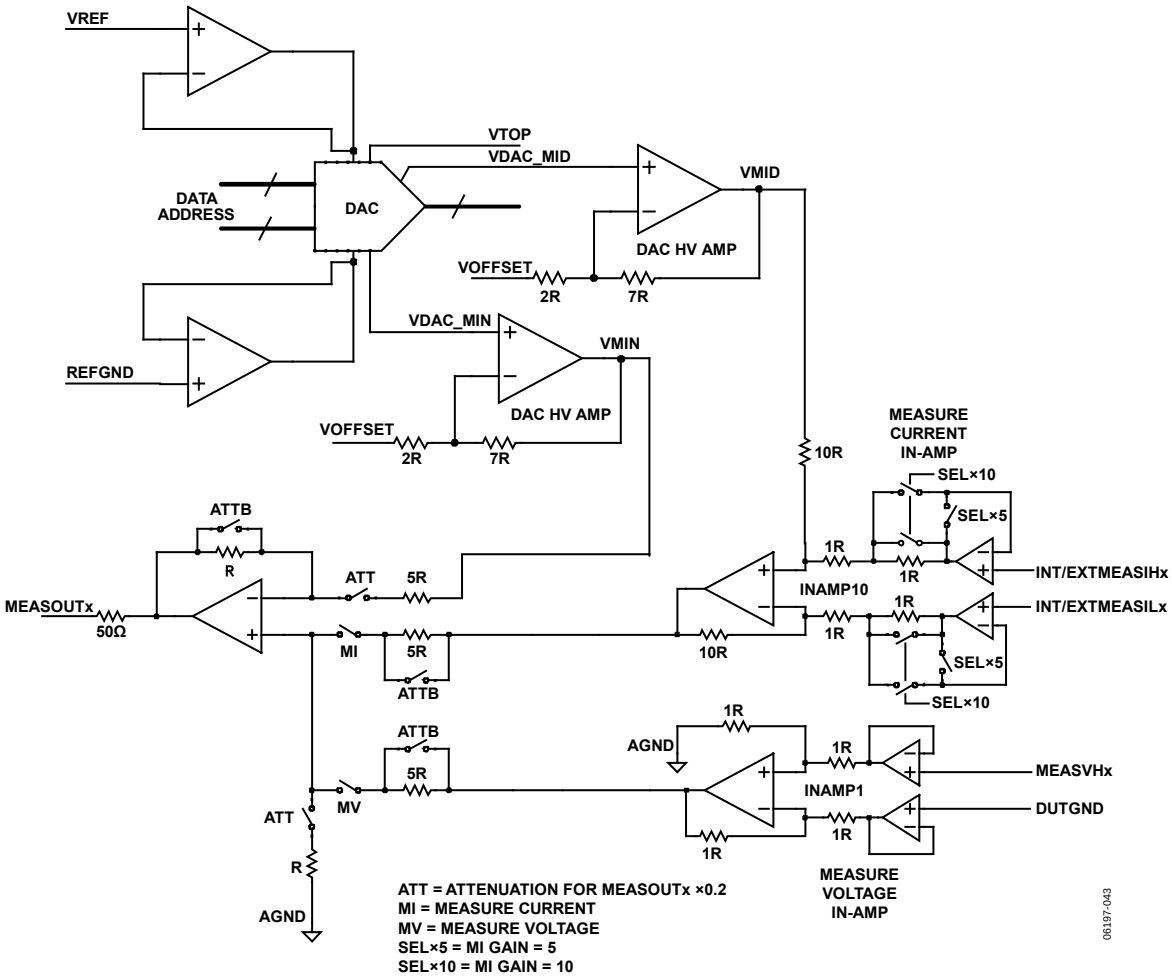


Figure 48. Measure Block and VMID Influence

CHOOSING POWER SUPPLY RAILS

As noted in the Specifications section, the minimum supply variation across the part |AVDD − AVSS| ≥ 20 V. For the AD5522 circuits to operate correctly, the supply rails must take into account not only the force voltage range, but also the internal DAC minimum voltage level, as well as headroom and so on. The DAC amplifier gains VREF by 4.5, and the offset DAC centers that range about some chosen point.

The supplies need to cater to the DAC output voltage range to avoid impinging on other parts of the circuit (for example, if the measure current block for rated current ranges has a gain of 10/5, the supplies need to provide sufficient headroom and footroom to not clip the measure current circuit when full current range is required).

Also, the MEASOUT gain = 0.2 setting uses the VMIN level for scaling purposes; if there is not enough footroom for this VMIN level, then the MV and MI output voltage range is affected.

For the MEASOUT gain = 0.2 setting, it is important to choose AVSS based on the following:

$$AVSS \leq -3.5 \times (VREF \times (OFFSET\_DAC\_CODE/2^{16})) - AVSS\_footroom - V_{DUTGND} - (R_{CABLE} \times I_{LOAD})$$

where:
AVSS_footroom = 4 V.
V_{DUTGND} is the voltage range anticipated at DUTGND.
R_{CABLE} is the cable/path resistance.
I_{LOAD} is the maximum load current.

MEASURE OUTPUT (MEASOUTx PINS)

The measured DUT voltage or current (voltage representation of DUT current) is available on the MEASOUTx pin with respect to AGND. The default MEASOUTx range is the forced voltage range for voltage measure and current measure (nominally ±11.25 V, depending on the reference voltage and offset DAC) and includes some overrange to allow for offset correction.

The serial interface allows the user to select another MEASOUTx range of 0.9 × VREF to AGND, allowing an ADC with a 5 V input range to be used. The MEASOUTx line for each PMU channel can be made high impedance via the serial interface.

The offset DAC directly offsets the measured output voltage level, but only when GAIN1 = 0. When the MEASOUT gain is 0.2, the minimum code from the DAC is used to center the MEASOUTx voltage and to ensure that the voltage is within the range of 0 to 0.9 × VREF (see Figure 48).

When using low supply voltages, ensure that there is sufficient headroom and footroom for the DAC output range (set by the VREF and offset DAC setting).

DEVICE UNDER TEST GROUND (DUTGND)

By default, there is one DUTGND input available for all four PMU channels. However, in some PMU applications, it is necessary that each channel operate from its own DUTGND level. The dual function pin, GUARDINx/DUTGNDx, can be configured as an input to the guard amplifier (GUARDIN) or as a DUTGND input for each channel.

The pin function can be configured through the serial interface on power-on for the required operation. The default connection is SW13b (GUARDIN) and SW14b (shared DUTGND).

Table 10. MEASOUTx Output Ranges for GAIN1 = 0, MEASOUT Gain = 1

MEASOUT Function	Measure Current Gain	Transfer Function	Output Voltage Range for VREF = 5 V[1]		
			Offset DAC = 0x0	Offset DAC = 0xA492	Offset DAC = 0xED67
MV	5 or 10	$\pm V_{DUT}$	0 V to 22.5 V	±11.25 V	−16.26 V to +6.25 V
MI					
GAIN0 = 0	10	$(I_{DUT} \times R_{SENSE} \times 10) + VMID$	0 V to 22.5 V	±11.25 V	−16.26 V to +6.25 V
GAIN0 = 1	5	$(I_{DUT} \times R_{SENSE} \times 5) + VMID$	0 V to 11.25 V (VREF = 2.5 V)	±5.625 V (VREF = 2.5 V)	−8.13 V to +3.12 V (VREF = 2.5 V)

[1] VREF = 5 V unless otherwise noted.

Table 11. MEASOUTx Output Ranges for GAIN1 = 1, MEASOUT Gain = 0.2

MEASOUT Function	Measure Current Gain	Transfer Function	Output Voltage Range for VREF = 5 V[1, 2]
MV	5 or 10	$V_{DUT} \times 0.2 + (0.45 \times VREF)$	0 V to 4.5 V (±2.25 V centered around 2.25 V)
MI			
GAIN0 = 0	10	$(I_{DUT} \times R_{SENSE} \times 10 \times 0.2) + (0.45 \times VREF)$	0 V to 4.5 V (±2.25 V centered around 2.25 V)
GAIN0 = 1	5	$(I_{DUT} \times R_{SENSE} \times 5 \times 0.2) + (0.45 \times VREF)$	1.125 V to 3.375 V (±1.125 V, centered around 2.25 V) 0 V to 2.25 V (±1.125 V, centered around 1.125 V) (VREF = 2.5 V)

[1] VREF = 5 V unless otherwise noted.
[2] The offset DAC setting has no effect on the output voltage range.

When configured as DUTGND per channel, this dual function pin is no longer connected to the input of the guard amplifier. Instead, it is connected to the low end of the instrumentation amplifier (SW14a), and the input of the guard amplifier is connected internally to MEASVHx (SW13a).

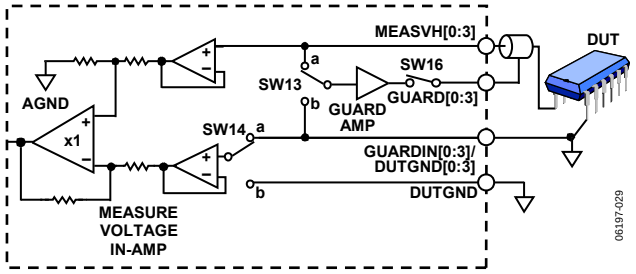


Figure 49. Using the DUTGND per Channel Feature

GUARD AMPLIFIER

A guard amplifier allows the user to bootstrap the shield of the cable to the voltage applied to the DUT, ensuring minimal drops across the cable. This is particularly important for measurements requiring a high degree of accuracy and in leakage current testing.

If not required, all four guard amplifiers can be disabled via the serial interface (system control register). Disabling the guard amplifiers decreases power consumption by 400 µA per channel.

As described in the Device Under Test Ground (DUTGND) section, GUARDINx/DUTGNDx are dual function pins. Each pin can function either as a guard amplifier input for one channel or as a DUTGND input for one channel, depending on the requirements of the end application (see Figure 49).

A guard alarm event occurs when the guard output moves more than 100 mV away from the guard input voltage for more than 200 µs. In this case, the event is flagged via the open-drain output $\overline{\text{CGALM}}$. Because the guard and clamp alarm functions share the same alarm output, $\overline{\text{CGALM}}$, the alarm information (alarm trigger and alarm channel) is available via the serial interface in the alarm status register.

Alternatively, the serial interface allows the user to set up the $\overline{\text{CGALM}}$ output to flag either the clamp status or the guard status. By default, this open-drain alarm pin is an unlatched output, but it can be configured as a latched output via the serial interface (system control register).

COMPENSATION CAPACITORS

Each channel requires an external compensation capacitor (CCOMP) to ensure stability into the maximum load capacitance while ensuring that settling time is optimized. In addition, one CFF pin per channel is provided to further optimize stability and settling time performance when in force voltage (FV) mode. When changing from force current (FI) mode to FV mode, the internal switch connecting the CFF capacitor is automatically closed.

Although the force amplifier is designed to drive load capacitances up to 10 nF (with CCOMP capacitor = 100 pF), it is possible to use larger compensation capacitor values to drive larger loads, at the expense of an increase in settling time. If a wide range of load capacitances must be driven, an external multiplexer connected to the CCOMPx pin allows optimization of settling time vs. stability. The series resistance of a switch placed on CCOMPx should typically be <50 Ω.

Suitable multiplexers for use are the ADG1404, ADG1408, or one of the multiplexers in the ADG4xx family, which typically have on resistances of less than 50 Ω.

Similarly, connecting the CFF node to an external multiplexer accommodates a wide range of C_{DUT} in FV mode. The ADG1204 or ADG1209 family of multiplexers meet these requirements. The series resistance of the multiplexer used should be such that

$$1/(2\pi \times R_{ON} \times C_{DUT}) > 100 \text{ kHz}$$

The voltage range of the CFFx and CCOMPx pins is the same as the voltage range expected on the FOHx pin; therefore, choice of capacitor must take this into account.

Table 12. Suggested Compensation Capacitor Selection

C_{LOAD}	CCOMP Capacitor	CFF Capacitor
≤1 nF	100 pF	220 pF
≤10 nF	100 pF	1 nF
≤100 nF	C_{LOAD}/100	C_{LOAD}/10

SYSTEM FORCE AND SENSE SWITCHES

Each channel has switches to allow connection of the force (FOHx) and sense (MEASVHx) lines to a central PMU for calibration purposes. There is one set of SYS_FORCE and SYS_SENSE pins per device. It is recommended that these connections be made individually to each PMU channel.

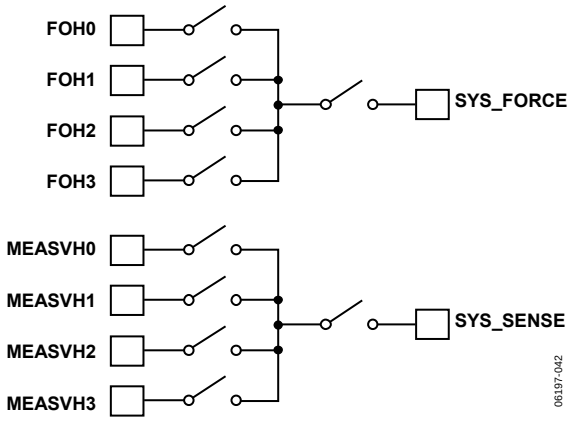


Figure 50. SYS_FORCE and SYS_SENSE Connections to FOHx and MEASVHx Pins

TEMPERATURE SENSOR

An on-board temperature sensor monitors die temperature. The temperature sensor is located at the center of the die. If the temperature exceeds the factory specified value (130°C) or a user programmable value, the device protects itself by shutting down all channels and flagging an alarm through the latched, open-drain $\overline{\text{TMPALM}}$ pin. Alarm status can be read back from the alarm status register or the PMU register, where latched and unlatched bits indicate whether an alarm has occurred and whether the temperature has dropped below the set alarm temperature. The shutdown temperature is set using the system control register.

DAC LEVELS

Each channel contains five dedicated DAC levels: one for the force amplifier, one each for the clamp high and clamp low levels, and one each for the comparator high and comparator low levels.

The architecture of a single DAC channel consists of a 16-bit resistor-string DAC followed by an output buffer amplifier. This resistor-string architecture guarantees DAC monotonicity. The 16-bit binary digital code loaded to the DAC register determines at which node on the string the voltage is tapped off before being fed into the output amplifier.

The transfer function for DAC outputs is as follows:

$$VOUT = 4.5 \times VREF \times (X2/2^{16}) - (3.5 \times VREF \times (OFFSET\_DAC\_CODE/2^{16})) + DUTGND$$

where:
VREF is the reference voltage and is in the range of 2 V to 5 V.
X2 is the calculated DAC code value and is in the range of 0 to 65,535 (see the Gain and Offset Registers section). *OFFSET_DAC_CODE* is the code loaded to the offset DAC. It is multiplied by 3.5 in the transfer function. On power-up, the default code loaded to the offset DAC is 0xA492; with a 5 V reference, this gives a span of ±11.25 V.

OFFSET DAC

The AD5522 is capable of forcing a 22.5 V (4.5 × VREF) voltage span. Included on chip is one 16-bit offset DAC (one for all four channels) that allows for adjustment of the voltage range.

The usable range is −16.25 V to +22.5 V. Zero scale loaded to the offset DAC gives a full-scale range of 0 V to 22.5 V, midscale gives ±11.25 V, and the most useful negative range is −16.25 V to +6.25 V. Full scale loaded to the offset DAC does not give a useful output voltage range, because the output amplifiers are limited by the available footroom. Table 13 shows the effect of the offset DAC on the other DACs in the device.

Table 13. Relationship of Offset DAC to Other DACs (VREF = 5 V)

Offset DAC Code	DAC Code	DAC Output Voltage (V)
0	0	0
	32,768	+11.25
	65,535	+22.50
32,768	0	−8.75
	32,768	+2.50
	65,535	+13.75
42,130	0	−11.25
	32,768	0
	65,535	+11.25
60,855	0	−16.25
	32,768	−5.00
	65,535	+6.25
65,535		Footroom limitations

The power supplies should be selected to support the required range and should take into account amplifier headroom and footroom and sense resistor voltage drop (±4 V).

Therefore, depending on the headroom available, the input to the force amplifier can be unipolar positive or bipolar, either symmetrical or asymmetrical about DUTGND, but always within a voltage span of 22.5 V.

The offset DAC offsets all DAC functions. It also centers the current range so that zero current always flows at midscale code, regardless of the offset DAC setting.

Rearranging the transfer function for the DAC output gives the following equation to determine which offset DAC code is required for a given reference and output voltage range.

$$OFFSET\_DAC\_CODE = (2^{16} \times (VOUT - DUTGND))/(3.5 \times VREF) - ((4.5 \times DAC\_CODE)/3.5)$$

When the output range is adjusted by changing the default value of the offset DAC, an extra offset is introduced due to the gain error of the offset DAC channel. The amount of offset is dependent on the magnitude of the reference and how much the offset DAC channel deviates from its default value. See the Specifications section for this offset. The worst-case offset occurs when the offset DAC channel is at positive or negative full scale. This value can be added to the offset present in the main DAC channel to give an indication of the overall offset for that channel. In most cases, the offset can be removed by programming the C register of the channel with an appropriate value. The extra offset caused by the offset DAC needs to be taken into account only when the offset DAC is changed from its default value.

GAIN AND OFFSET REGISTERS

Each DAC level has an independent gain (M) register and an independent offset (C) register, which allow trimming out of the gain and offset errors of the entire signal chain, including the DAC. All registers in the AD5522 are volatile, so they must be loaded on power-on during a calibration cycle. Data from the X1 register is operated on by a digital multiplier and adder controlled by the contents of the M and C registers. The calibrated DAC data is then stored in the X2 register.

The digital input transfer function for each DAC can be represented as follows:

$$X2 = [(M + 1)/2^n \times X1] + (C - 2^{n-1})$$

where:
X2 is the data-word loaded to the resistor-string DAC.
X1 is the 16-bit data-word written to the DAC input register.
M is the code in the gain register (default code = $2^{16} - 1$). The M register is 15 bits (D15 to D1, the LSB is a don't care).
C is the code in the offset register (default code = 2^{15}).
n is the DAC resolution (*n* = 16).

The calibration engine is engaged only when data is written to the X1 register and for some PMU writes (see Table 18). The calibration engine is not engaged when data is written to the M or C register. This has the advantage of minimizing the initial setup time of the device. To calculate a result that includes new M or C data, a write to X1 is required.

CACHED X2 REGISTERS

Each DAC has a number of cached X2 registers. These registers store the result of a gain and offset calibration in advance of a mode change. This enables the user to preload registers, allowing the calibration engine to calculate the appropriate X2 value and store it until a change in mode occurs. Because the data is ready and held in the appropriate register, mode changing is as time efficient as possible. If an update occurs to a DAC register set that is currently part of the operating PMU mode, the DAC output is updated immediately (depending on the $\overline{\text{LOAD}}$ condition).

Gain and Offset Registers for the FIN DAC

The force amplifier input (FIN) DAC level contains independent gain and offset control registers that allow the user to digitally trim gain and offset. There are six sets of X1, M, and C registers: one set for the force voltage range and one set for each force current range (four internal current ranges and one external current range). Six X2 registers store the calculated DAC values, ready to load to the DAC register upon a PMU mode change.

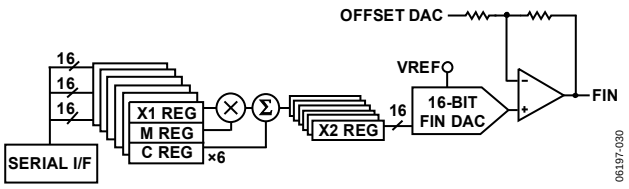


Figure 51. FIN DAC Registers

Gain and Offset Registers for the Comparator DACs

The comparator DAC levels contain independent gain and offset control registers that allow the user to digitally trim gain and offset. There are six sets of X1, M, and C registers: one set for the force voltage mode and one set for each force current range (four internal current ranges and one external current range). In this way, X2 can be preprogrammed, which allows for efficient switching into the required compare mode. Six X2 registers store the calculated DAC values, ready to load to the DAC register upon a PMU mode change.

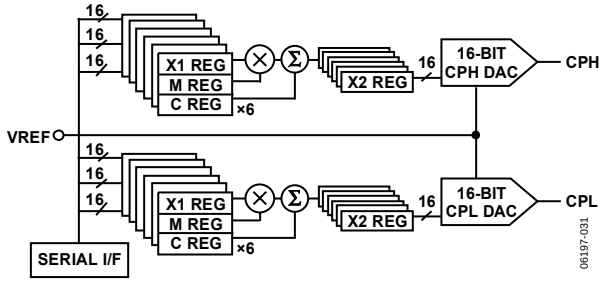


Figure 52. Comparator Registers

Gain and Offset Registers for the Clamp DACs

The clamp DAC levels contain independent gain and offset control registers that allow the user to digitally trim gain and offset. There are two sets of X1, M, and C registers: one set for the force voltage mode and one set for all five current ranges. Two X2 registers store the calculated DAC values, ready to load to the DAC register upon a PMU mode change.

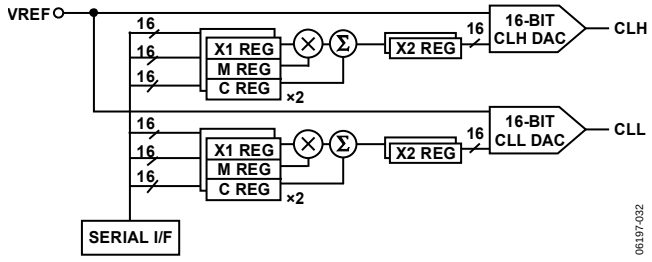


Figure 53. Clamp Registers

REFERENCE VOLTAGE (VREF)

One buffered analog input, VREF, supplies all 21 DACs with the necessary reference voltage to generate the required dc levels.

REFERENCE SELECTION

The voltage applied to the VREF pin determines the output voltage range and span applied to the force amplifier, clamp, and comparator inputs. The AD5522 can be used with a reference input ranging from 2 V to 5 V; however, for most applications, a reference input of 5 V or 2.5 V is sufficient to meet all voltage range requirements. The DAC amplifier gain is 4.5, which gives a DAC output span of 22.5 V. The DACs have gain and offset registers that can be used to trim out system errors.

In addition, the gain register can be used to reduce the DAC output range to the desired force voltage range. The FIN DAC retains 16-bit resolution even with a gain register setting of quarter scale (0x4000). Therefore, from a single 5 V reference, it is possible to obtain a voltage span as high as 22.5 V or as low as 5.625 V.

When using the gain and offset registers, the selected output range should take into account the system gain and offset errors that need to be trimmed out. Therefore, the selected output range should be larger than the actual required range.

When using low supply voltages, ensure that there is sufficient headroom and footroom for the required force voltage range.

Also, the forced current range is the quoted full-scale range only with an applied reference of 5 V (I_{SENSE} amplifier gain = 10) or 2.5 V (I_{SENSE} amplifier gain = 5).

Table 14. References Suggested For Use with AD5522[1]

Part No.	Voltage (V)	Initial Accuracy %	Ref Out TC (ppm/°C)	Ref Output Current (mA)	Supply Voltage Range (V)	Package
ADR435	5	±0.04	1	30	+7 to +18	MSOP, SOIC
ADR445	5	±0.04	1	10	+5.5 to +18	MSOP, SOIC
ADR431	2.5	±0.04	1	30	+4.5 to +18	MSOP, SOIC
ADR441	2.5	±0.04	1	10	+3 to +18	MSOP, SOIC

[1] Subset of the possible references suitable for use with the AD5522. Visit www.analog.com for more options.

For other voltage and current ranges, the required reference level can be calculated as follows:

1. Identify the nominal range required.
2. Identify the maximum offset span and the maximum gain required on the full output signal range.
3. Calculate the new maximum output range, including the expected maximum gain and offset errors.
4. Choose the new required $VOUT_{MAX}$ and $VOUT_{MIN}$, keeping the VOUT limits centered on the nominal values. Note that AVDD and AVSS must provide sufficient headroom.
5. Calculate the value of VREF as follows:

$$VREF = (VOUT_{MAX} - VOUT_{MIN})/4.5$$

Reference Selection Example

If, given the following conditions:

Nominal output range = 10 V (−2 V to +8 V)
Offset error = ±100 mV
Gain error = ±0.5%
REFGND = AGND = 0 V

Then, with gain error = ±0.5%, the maximum positive gain error = +0.5%, and the output range including gain error = 10 V + 0.005(10 V) = 10.05 V.

With offset error = ±100 mV, the maximum offset error span = 2(100 mV) = 0.2 V, and the output range including gain error and offset error = 10.05 V + 0.2 V = 10.25 V.

To calculate VREF with actual output range = 10.25 V, that is, −2.125 V to +8.125 V (centered),

VREF = (8.125 V + 2.125 V)/4.5 = 2.28 V

If the solution yields an inconvenient reference level, the user can adopt one of the following approaches:

- Use a resistor divider to divide down a convenient, higher reference level to the required level.
- Select a convenient reference level above VREF and modify the gain and offset registers to digitally downsize the reference. In this way, the user can use almost any convenient reference level.
- Use a combination of these two approaches.

In this case, the optimum reference is a 2.5 V reference; the user can use the M and C registers and the offset DAC to achieve the required −2 V to +8 V range. Change the I_{SENSE} amplifier gain to 5 to ensure a full-scale current range of the specified values (see the Current Range Selection section). This gain also allows optimization of power supplies and minimizes power consumption within the device.

It is important to bear in mind when choosing a reference value that values other than 5 V (MI gain = 10) and 2.5 V (MI gain = 5) result in current ranges other than those specified. See the Measure Current Gains section for more details.

CALIBRATION

Calibration involves determining the gain and offset of each channel in each mode and overwriting the default values in the M and C registers of the individual DACs. In some cases (for example, FI mode), the calibration constants, particularly those for gains, may be range dependent.

Reducing Zero-Scale Error

Zero-scale error can be reduced as follows:

1. Set the output to the lowest possible value.
2. Measure the actual output voltage and compare it to the required value. This gives the zero-scale error.
3. Calculate the number of LSBs equivalent to the zero-scale error and add/subtract this number to the default value of the C register.

Reducing Gain Error

Gain error can be reduced as follows:

1. Measure the zero-scale error.
2. Set the output to the highest possible value.
3. Measure the actual output voltage and compare it to the required value. This is the gain error.
4. Calculate the number of LSBs equivalent to the gain error and subtract this number from the default value of the M register. Note that only positive gain error can be reduced.

Calibration Example

Nominal offset coefficient = 32,768
Nominal gain coefficient = 65,535

For example, the gain error = 0.5%, and the offset error = 100 mV.

Gain error (0.5%) calibration:

$$65{,}535 \times 0.995 = 65{,}207$$

Therefore, load Code 1111 1110 1011 0111 to the M register.

Offset error (100 mV) calibration:

$$\text{LSB size} = 10.25/65{,}535 = 156\ \mu\text{V}$$

Offset coefficient for 100 mV offset = 100/0.156 = 641 LSBs

Therefore, load Code 0111 1101 0111 1111 to the C register.

ADDITIONAL CALIBRATION

The techniques described in the Calibration section are usually sufficient to reduce the zero-scale and gain errors. However, there are limitations whereby the errors may not be sufficiently reduced. For example, the offset (C) register can only be used to reduce the offset caused by negative zero-scale error. A positive offset cannot be reduced. Likewise, if the maximum voltage is below the ideal value, that is, a negative gain error, the gain (M) register cannot be used to increase the gain to compensate for the error. These limitations can be overcome by increasing the reference value.

SYSTEM LEVEL CALIBRATION

There are many ways to calibrate the device on power-on. Following is an example of how to calibrate the FIN DAC of the device without a DUT or DUT board connected.

The calibration procedure for the force and measure circuitry is as follows:

1. Calibrate the force voltage (2 points).

   In FV mode, write zero scale to the FIN DAC. Connect SYS_FORCE to FOHx and SYS_SENSE to MEASVHx, and close the internal force/sense switch (SW7).

   Using the system PMU, measure the error between the voltage at FOHx/MEASVHx and the desired value.

   Similarly, load full scale to the FIN DAC and measure the error between the voltage at FOHx/MEASVHx and the desired value. Calculate the M and C values. Load these values to the appropriate M and C registers of the FIN DAC.

2. Calibrate the measure voltage (2 points).

   Connect SYS_FORCE to FOHx and SYS_SENSE to MEASVHx, and close the internal force/sense switch (SW7). Force voltage on FOHx via SYS_FORCE and measure the voltage at MEASOUTx. The difference is the error between the actual forced voltage and the voltage at MEASOUTx.

3. Calibrate the force current (2 points).

   In FI mode, write zero scale to the FIN DAC. Connect SYS_FORCE to an external ammeter and to the FOHx pin. Measure the error between the ammeter reading and the MEASOUTx reading. Repeat this step with full scale loaded to the FIN DAC. Calculate the M and C values.

4. Calibrate the measure current (2 points).

   In FI mode, write zero scale to the FIN DAC. Connect SYS_FORCE to an external ammeter and to the FOHx pin. Measure the error between the ammeter reading and the MEASOUTx reading. Repeat this step with full scale loaded to the FIN DAC.

5. Repeat this procedure for all four channels.

Similarly, calibrate the comparator and clamp DACs, and load the appropriate gain and offset registers. Calibrating these DACs requires some successive approximation to find where the comparator trips or the clamps engage.

CIRCUIT OPERATION

FORCE VOLTAGE (FV) MODE

Most PMU measurements are performed in force voltage/measure current (FVMI) mode, for example, when the device is used as a device power supply, or in continuity or leakage testing. In force voltage (FV) mode, the voltage forced is mapped directly to the DUT. The measure voltage amplifier completes the loop, giving negative feedback to the forcing amplifier (see Figure 54).

The forced voltage can be calculated as follows:

Forced Voltage at DUT = VOUT

$$VOUT = 4.5 \times VREF \times (DAC\_CODE/2^{16}) - (3.5 \times VREF \times (OFFSET\_DAC\_CODE/2^{16})) + DUTGND$$

where:
VOUT is the voltage of the FIN DAC (see the DAC Levels section).

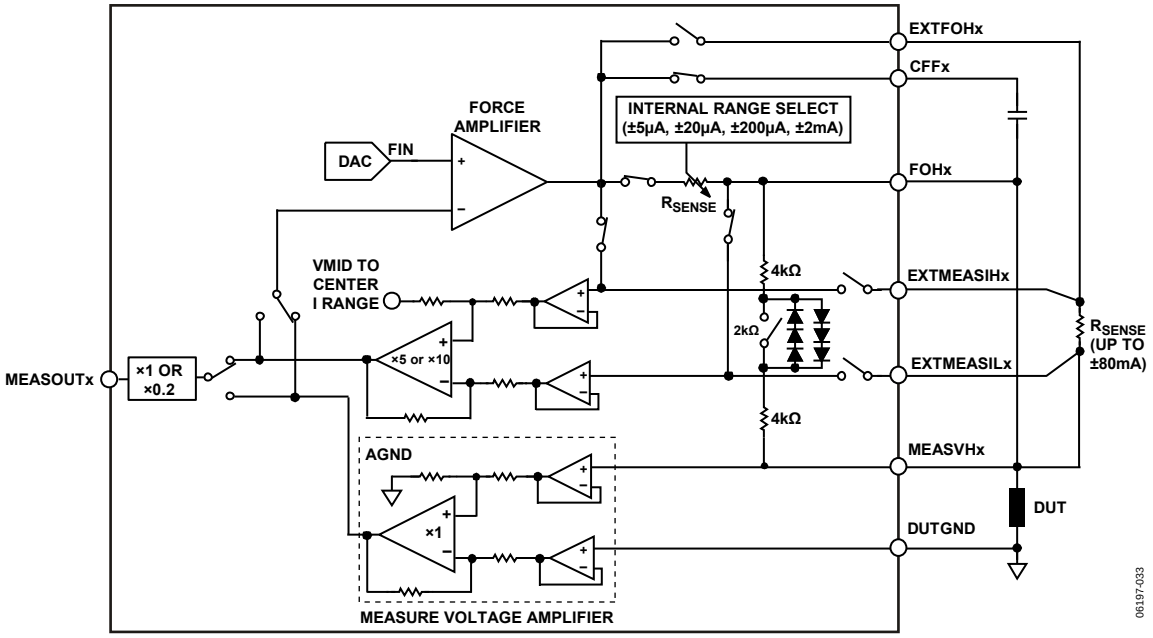


Figure 54. Forcing Voltage, Measuring Current

FORCE CURRENT (FI) MODE

In force current (FI) mode, the voltage at the FIN DAC is converted to a current and is applied to the DUT. The feedback path is the measure current amplifier, feeding back the voltage measured across the sense resistor. MEASOUTx reflects the voltage measured across the DUT (see Figure 55).

For the suggested current ranges, the maximum voltage drop across the sense resistors is ±1 V. However, to allow for error correction, there is some overrange available in the current ranges. The maximum full-scale voltage range that can be loaded to the FIN DAC is ±11.5 V. The forced current can be calculated as follows:

$$FI = 4.5 \times VREF \times ((DAC\_CODE - 32{,}768)/2^{16})/(R_{SENSE} \times MI\_Amplifier\_Gain)$$

where:
FI is the forced current.
R_{SENSE} is the selected sense resistor.
MI_Amplifier_Gain is the gain of the measure current instrumentation amplifier. This gain can be set to 5 or 10 via the serial interface.

The I_{SENSE} amplifier is biased by the offset DAC output voltage in such a way as to center the measure current output regardless of the voltage span used.

In the ±200 µA range with the 5 kΩ sense resistor and an I_{SENSE} gain of 10, the maximum current range possible is ±225 µA. Similarly, for the other current ranges, there is an overrange of 12.5% to allow for error correction.

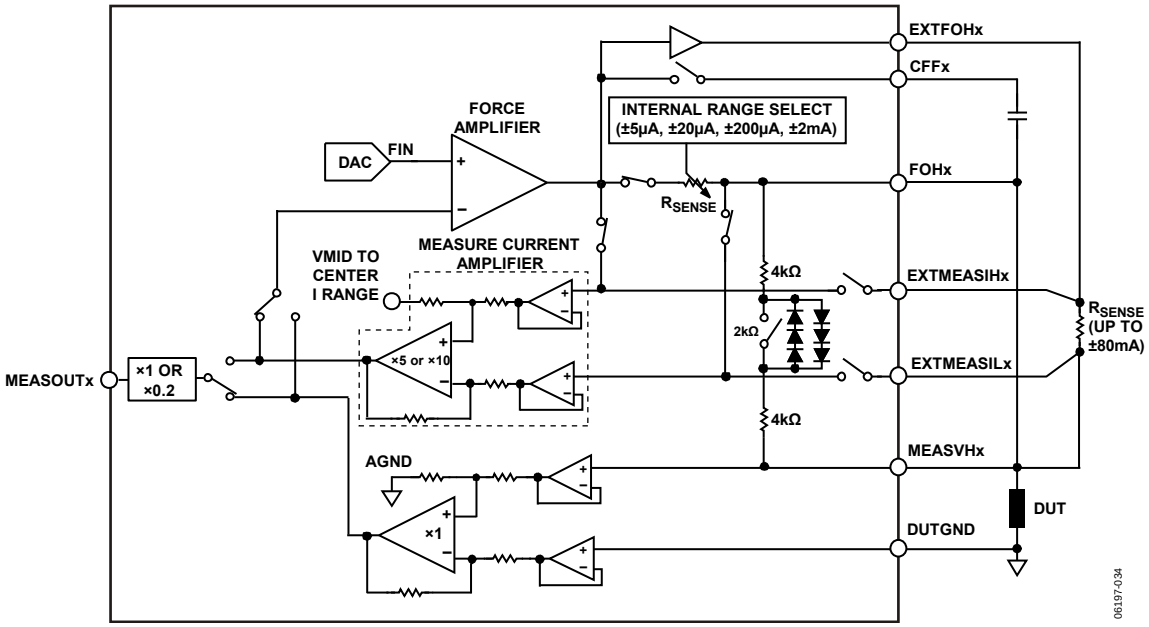


Figure 55. Forcing Current, Measuring Voltage

SERIAL INTERFACE

The AD5522 provides two high speed serial interfaces: an SPI-compatible interface operating at clock frequencies up to 50 MHz and an EIA-644-compliant LVDS interface. To minimize both the power consumption of the device and the on-chip digital noise, the serial interface powers up fully only when the device is being written to, that is, on the falling edge of $\overline{\text{SYNC}}$.

SPI INTERFACE

The serial interface operates from a 2.3 V to 5.25 V DVCC supply range. The SPI interface is selected when the $\overline{\text{SPI}}$/LVDS pin is held low. It is controlled by four pins, as described in Table 15.

Table 15. Pins That Control the SPI Interface

Pin	Description
$\overline{\text{SYNC}}$	Frame synchronization input
SDI	Serial data input pin
SCLK	Clocks data in and out of the device
SDO	Serial data output pin for data readback (weak SDO output driver, may require reduction in SCLK frequency to correctly read back, see Table 2)

LVDS INTERFACE

The LVDS interface uses the same input pins, with the same designations, as the SPI interface. In addition, four other pins are provided for the complementary signals needed for differential operation, as described in Table 16.

Table 16. Pins That Control the LVDS Interface

Pin	Description
SYNC	Differential frame synchronization signal
$\overline{\text{SYNC}}$	Differential frame synchronization signal (complement)
SDI	Differential serial data input
$\overline{\text{SDI}}$	Differential serial data input (complement)
SCLK	Differential serial clock input
$\overline{\text{SCLK}}$	Differential serial clock input (complement)
SDO	Differential serial data output for data readback
$\overline{\text{SDO}}$	Differential serial data output for data readback (complement)

SERIAL INTERFACE WRITE MODE

The AD5522 allows writing of data via the serial interface to every register directly accessible to the serial interface, that is, all registers except the DAC registers.

The serial word is 29 bits long. The serial interface works with both a continuous and a burst (gated) serial clock. Serial data applied to SDI is clocked into the AD5522 by clock pulses applied to SCLK. The first falling edge of $\overline{\text{SYNC}}$ starts the write cycle. At least 29 falling clock edges must be applied to SCLK to clock in 29 bits of data before $\overline{\text{SYNC}}$ is taken high again.

The input register addressed is updated on the rising edge of $\overline{\text{SYNC}}$. For another serial transfer to take place, $\overline{\text{SYNC}}$ must be taken low again.

The shift register can accept longer words (for example, 32-bit words), framed by $\overline{\text{SYNC}}$, but the data should always be in the 29$^{\text{th}}$ LSB positions.

$\overline{\text{RESET}}$ FUNCTION

Bringing the level-sensitive $\overline{\text{RESET}}$ line low resets the contents of all internal registers to their power-on reset state (see the Power-On Default section). This sequence takes approximately 600 µs. $\overline{\text{BUSY}}$ goes low for the duration, returning high when $\overline{\text{RESET}}$ is brought high again and the initialization is complete. While $\overline{\text{BUSY}}$ is low, all interfaces are disabled. When $\overline{\text{BUSY}}$ returns high, normal operation resumes, and the status of the $\overline{\text{RESET}}$ pin is ignored until it goes low again. The SDO output is high impedance during a power-on reset or a $\overline{\text{RESET}}$. A power-on reset functions the same way as $\overline{\text{RESET}}$.

$\overline{\text{BUSY}}$ AND $\overline{\text{LOAD}}$ FUNCTIONS

The $\overline{\text{BUSY}}$ pin is an open-drain output that indicates the status of the AD5522 interface. When writing to any register, $\overline{\text{BUSY}}$ goes low and stays low until the command completes.

A write operation to a DAC X1 register and some PMU register bits (see Table 18) drives the $\overline{\text{BUSY}}$ signal low for longer than a write M, C, or system control register. For DACs, the value of the internal cached (X2) data is calculated and stored each time that the user writes new data to the corresponding X1 register. During the calculation and writing of X2, the $\overline{\text{BUSY}}$ output is driven low. While $\overline{\text{BUSY}}$ is low, the user can continue writing new data to the any register, but this write should not be completed with $\overline{\text{SYNC}}$ going high until $\overline{\text{BUSY}}$ returns high (see Figure 56 and Figure 57).

X2 values are stored and held until a PMU word is written that calls the appropriate cached X2 register. Only then is a DAC output updated.

The DAC outputs and PMU modes are updated by taking the $\overline{\text{LOAD}}$ input low. If $\overline{\text{LOAD}}$ goes low while $\overline{\text{BUSY}}$ is active, the $\overline{\text{LOAD}}$ event is stored and the DAC outputs or PMU modes are updated immediately after $\overline{\text{BUSY}}$ goes high. A user can also hold the $\overline{\text{LOAD}}$ input permanently low. In this case, the DAC outputs or PMU modes are updated immediately after $\overline{\text{BUSY}}$ goes high.

The $\overline{\text{BUSY}}$ pin is bidirectional and has a 50 kΩ internal pull-up resistor. When multiple AD5522 devices are used in one system, the $\overline{\text{BUSY}}$ pins can be tied together. This is useful when it is required that no DAC or PMU in any device be updated until all others are ready to be updated. When each device finishes updating its X2 registers, it releases the $\overline{\text{BUSY}}$ pin. If another device has not finished updating its X2 registers, it holds $\overline{\text{BUSY}}$ low, thus delaying the effect of $\overline{\text{LOAD}}$ going low.

Because there is only one calibration engine shared among four channels, the task of calculating X2 values must be done sequentially, so that the length of the $\overline{\text{BUSY}}$ pulse varies according to the number of channels being updated. Following any register update, including multiple channel updates, subsequent writes should either be timed or should wait until $\overline{\text{BUSY}}$ returns high (see Figure 56). If subsequent writes are presented before the calibration engine completes the first stage of the last Channel X2 calculation, data may be lost.

Table 17. $\overline{\text{BUSY}}$ Pulse Widths

Action	$\overline{\text{BUSY}}$ Pulse Width[1]
Loading Data to System Control Register, or Readback[2]	0.27 µs maximum
Loading X1 to 1 PMU DAC Channel	1.65 µs maximum
Loading X1 to 2 PMU DAC Channels	2.3 µs maximum
Loading X1 to 3 PMU DAC Channels	2.95 µs maximum
Loading X1 to 4 PMU DAC Channels	3.6 µs maximum

[1] $\overline{\text{BUSY}}$ pulse width = ((number of channels + 1) × 650 ns) + 350 ns.
[2] Refer to Table 18 for details of PMU register effect on $\overline{\text{BUSY}}$ pulse width.

$\overline{\text{BUSY}}$ also goes low during a power-on reset and when a falling edge is detected on the $\overline{\text{RESET}}$ pin.

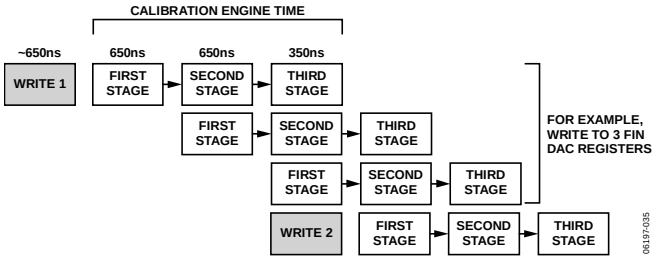


Figure 56. Multiple Writes to DAC X1 Registers

Writing data to the system control register, some PMU control bits (see Table 18), the M register, and the C register do not involve the digital calibration engine, thus speeding up configuration of the device on power-on. However, care should be taken not to issue these commands while $\overline{\text{BUSY}}$ is low, as previously described.

Table 18. $\overline{\text{BUSY}}$ Pulse Widths for PMU Register Updates

PMU Register Update (See Table 26)			Maximum $\overline{\text{BUSY}}$ Low Time per Channel Update			
Bit	**Bit Name**		**One Channel**	**Two Channels**	**Three Channels**	**Four Channels**
21	CH EN		270 ns			
20, 19	FORCE1, FORCE0 (depends on mode change)					
	Transition From	**Transition To**				
	High-Z FOHx current (11)	Force current (01)	270 ns			
	High-Z FOHx current (11)	Force voltage (00)	1.65 µs	2.3 µs	2.95 µs	3.6 µs
	High-Z FOHx current (11)	High-Z FOHx voltage (10)	1.65 µs	2.3 us	2.95 us	3.6 µs
	Force current (01)	High-Z FOHx current (11)	270 ns			
	Force current (01)	High-Z FOHx voltage (10)	1.65 µs	2.3 µs	2.95 µs	3.6 µs
	Force current (01)	Force voltage (00)	1.65 µs	2.3 µs	2.95 µs	3.6 µs
	High-Z FOHx voltage (10)	Force voltage (00)	270 ns			
	High-Z FOHx voltage (10)	Force current (01)	1.65 µs	2.3 µs	2.95 µs	3.6 µs
	High-Z FOHx voltage (10)	High-Z FOHx current (11)	1.65 µs	2.3 µs	2.95 µs	3.6 µs
	Force voltage (00)	High-Z FOHx voltage (10)	270 ns			
	Force voltage (00)	High-Z FOHx current (11)	1.65 µs	2.3 µs	2.95 µs	3.6 µs
	Force voltage (00)	Force current (01)	1.65 µs	2.3 µs	2.95 µs	3.6 µs
17, 16, 15	C2 to C0; current range selection (any range change)		1.65 µs	2.3 µs	2.95 µs	3.6 µs
14, 13	MEASx (measure mode selection)		270 ns			
12	FIN		270 ns			
11	SFO		270 ns			
10	SS0		270 ns			
9	CL		270 ns			
8	CPOLH		270 ns			
7	Compare V/I		1.65 µs	2.3 µs	2.95 µs	3.6 µs
6	Clear		270 ns			

REGISTER UPDATE RATES

The value of the X2 register is calculated each time the user writes new data to the corresponding X1 register and for some PMU register updates. The calculation is performed in a three-stage process. The first two stages take approximately 650 ns each, and the third stage takes approximately 350 ns. When the write to the X1 register is complete, the calculation process begins. If the write operation involves the update of a single DAC channel, the user is free to write to another X1 register, provided that the write operation does not finish ($\overline{\text{SYNC}}$ returns high) until after the first-stage calculation is complete, that is, 650 ns after the completion of the first write operation.

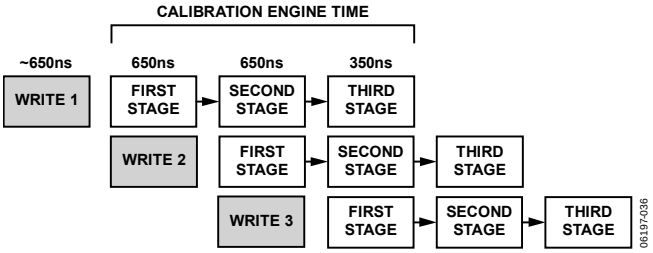


Figure 57. Multiple Single-Channel Writes Engaging the Calibration Engine

REGISTER SELECTION

The serial word assignment consists of 29 bits. Bit 28 to Bit 22 are common to all registers, whether writing to or reading from the device. The PMU3 to PMU0 data bits (Bit 27 to Bit 24) address each PMU channel (or associated DAC register). When the PMU3 to PMU0 bits are all 0s, the system control register is addressed.

The mode bits, MODE0 and MODE1, address the different sets of DAC registers and the PMU register.

Table 19. Mode Bits

B23 MODE1	B22 MODE0	Action
0	0	Write to the system control register or the PMU register
0	1	Write to the DAC gain (M) register
1	0	Write to the DAC offset (C) register
1	1	Write to the DAC input data (X1) register

Readback Control, RD/$\overline{\text{WR}}$

Setting the RD/$\overline{\text{WR}}$ bit (Bit 28) high initiates a readback sequence of the PMU, alarm status, comparator status, system control, or DAC register, as determined by the address bits.

PMU Address Bits: PMU3, PMU2, PMU1, PMU0

The PMU3 to PMU0 data bits (Bit 27 to Bit 24) address each PMU channel on chip. These bits allow individual control of each PMU channel or any combination of channels, in addition to multichannel programming. PMU bits also allow access to write registers such as the system control register and the DAC registers, in addition to reading from all the registers (see Table 20).

NOP (No Operation)

If an NOP (no operation) command is loaded, no change is made to the DAC or PMU registers. This code is useful when performing a readback of a register within the device (via the SDO pin) where a change of DAC code or PMU function may not be required.

Reserved Commands

Any bit combination that is not described in the register address tables for the PMU, DAC, and system control registers indicates a reserved command. These commands are unassigned and are reserved for factory use. To ensure correct operation of the device, do not use reserved commands.

All codes not explicitly referenced in this table are reserved and should not be used (see Table 29).

Table 20. Read and Write Functions of the AD5522

B28	B27	B26	B25	B24	B23	B22	B21 to B0	Selected Channel			
RD/$\overline{WR}$	PMU3	PMU2	PMU1	PMU0	MODE1	MODE0	Data bits	CH3	CH2	CH1	CH0
Write Functions											
0	0	0	0	0	0	0	Data bits	Write to system control register (see Table 23)			
0	0	0	0	0	0	1	Data bits	Reserved			
0	0	0	0	0	1	0	Data bits	Reserved			
0	0	0	0	0	1	1	All 1s	NOP (no operation)			
0	0	0	0	0	1	1	Data bits other than all 1s	Reserved			
Write Addressed DAC or PMU Register											
0	0	0	0	1	Select DAC or PMU register (see Table 19)		Address and data bits				CH0
0	0	0	1	0						CH1	
0	0	0	1	1						CH1	CH0
0	0	1	0	0					CH2		
0	0	1	0	1					CH2		CH0
0	0	1	1	0					CH2	CH1	
0	0	1	1	1					CH2	CH1	CH0
0	1	0	0	0				CH3			
0	1	0	0	1				CH3			CH0
0	1	0	1	0				CH3		CH1	
0	1	0	1	1				CH3		CH1	CH0
0	1	1	0	0				CH3	CH2		
0	1	1	0	1				CH3	CH2		CH0
0	1	1	1	0				CH3	CH2	CH1	
0	1	1	1	1				CH3	CH2	CH1	CH0
Read Functions											
1	0	0	0	0	0	0	All 0s	Read from system control register			
1	0	0	0	0	0	1	All 0s	Read from comparator status register			
1	0	0	0	0	1	0	X (don't care)	Reserved			
1	0	0	0	0	1	1	All 0s	Read from alarm status register			
Read Addressed DAC or PMU Register (Only One PMU or DAC Register Can Be Read at One Time)											
1	0	0	0	1	Select PMU or DAC register (see Table 19)		All 0s if reading PMU registers; DAC address plus all 0s if reading a DAC register DAC address (see Table 29)				CH0
1	0	0	1	0						CH1	
1	0	1	0	0					CH2		
1	1	0	0	0				CH3			

WRITE SYSTEM CONTROL REGISTER

The system control register is accessed when the PMU channel address bits (PMU3 to PMU0) and the mode bits (MODE1 and MODE0) are all 0s. This register allows quick setup of various functions in the device. The system control register operates on a per-device basis.

Table 21. System Control Register Bits—Bit B28 to Bit B15

B28	B27	B26	B25	B24	B23	B22	B21	B20	B19	B18	B17	B16	B15
RD/$\overline{WR}$	PMU3	PMU2	PMU1	PMU0	MODE1	MODE0	CL3	CL2	CL1	CL0	CPOLH3	CPOLH2	CPOLH1

Table 22. System Control Register Bits—Bit B14 to Bit B0

B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1[1]	B0[1]
CPOLH0	CPBIASEN	DUTGND/CH	Guard ALM	Clamp ALM	INT10K	Guard EN	GAIN1	GAIN0	TMP enable	TMP1	TMP0	Latched	0	0

[1] Bit B1 and Bit B0 are unused data bits.

Table 23. System Control Register Functions

Bit	Bit Name	Description
28 (MSB)	RD/$\overline{WR}$	When low, a write function takes place to the selected register; setting the RD/$\overline{WR}$ bit high initiates a readback sequence of the PMU, alarm status, comparator status, system control, or DAC register, as determined by the address bits.
27 26 25 24	PMU3 PMU2 PMU1 PMU0	Set Bit PMU3 to Bit PMU0 to 0 to address the system control register.
23 22	MODE1 MODE0	Set the MODE1 and MODE0 bits to 0 to address the system control register.
System Control Register-Specific Bits		
21 20 19 18	CL3 CL2 CL1 CL0	Current or voltage clamp enable. Bit CL3 to Bit CL0 enable and disable the current or voltage clamp function per channel (0 = disable; 1 = enable). The clamp enable function is also available in the PMU register on a per-channel basis. This dual functionality allows flexible enabling or disabling of this function. When reading back information about the status of the clamp enable function, the data that was most recently written to the clamp register is available in the readback word from either the PMU register or the system control register.
17 16 15 14	CPOLH3 CPOLH2 CPOLH1 CPOLH0	Comparator output enable. By default, the comparator outputs are high-Z on power-on. A 1 in each bit position enables the comparator output for the selected channel. Bit 13 (CPBIASEN) must be enabled to power on the comparator functions. The comparator enable function is also available in the PMU register on a per-channel basis. This dual functionality allows flexible enabling or disabling of this function. When reading back information about the status of the comparator enable function, the data that was most recently written to the comparator status register is available in the readback word from either the PMU register or the system control register.
13	CPBIASEN	Comparator enable. By default, the comparators are powered down when the device is powered on. To enable the comparator function for all channels, write a 1 to this bit. A 0 disables the comparators and shuts them down. The comparator output enable bits (CPOLHx, Bit 17 to Bit 14) allow the user to turn on each comparator output individually, enabling busing of comparator outputs.
12	DUTGND/CH	DUTGND per channel enable. The GUARDINx/DUTGNDx pins are shared pins that can be configured to enable a DUTGND per PMU channel or a guard input per PMU channel. Setting this bit to 1 enables DUTGND per channel. In this mode, the pin functions as a DUTGND pin on a per-channel basis. The guard inputs are disconnected from this pin and instead are connected directly to the MEASVHx line by an internal connection. The default power-on condition is GUARDINx.
11 10	GUARD ALM CLAMP ALM	Clamp and guard alarm functions share one open-drain alarm pin ($\overline{CGALM}$). By default, the $\overline{CGALM}$ pin is disabled. The guard ALM and clamp ALM bits allow the user to choose whether clamp alarm information, guard alarm information, or both sets of alarm information are flagged by the $\overline{CGALM}$ pin. Set high to enable either alarm function.
9	INT10K	Internal sense short. Setting this bit high allows the user to connect an internal sense short resistor of 10 kΩ (4 kΩ + 2 kΩ switch + 4 kΩ) between the FOHx and the MEASVHx lines (SW7 is closed). Setting this bit high also closes SW15, allowing the user to connect another 10 kΩ resistor between DUTGNDx and AGND.
8	Guard EN	Guard enable. The guard amplifier is disabled on power-on; to enable the guard amplifier, set this bit to 1. If the guard function is not in use, disabling it saves power (typically 400 µA per channel).

<table>
<tr><th>Bit</th><th>Bit Name</th><th>Description</th></tr>
<tr><td>7
6</td><td>GAIN1
GAIN0</td><td>MEASOUTx output range. The MEASOUTx range defaults to the force voltage span for voltage and current measurements, which includes some overrange to allow for offset correction. The nominal output voltage range is ±11.25 V with the default offset DAC setting, but changes for other offset DAC settings when GAIN1 = 0. Therefore, the MEASOUTx range can be an asymmetrical bipolar voltage range. GAIN1 = 1 enables a unipolar output voltage range, which allows the use of asymmetrical supplies or a smaller input range ADC. See Table 10 and Table 11 for more details.
<table>
<tr><th rowspan="2">MEASOUT Function</th><th rowspan="2">Measure Current Gain</th><th colspan="2">Output Voltage Range for VREF = 5 V, Offset DAC = 0xA492</th></tr>
<tr><th>GAIN1 = 0, MEASOUT Gain = 1</th><th>GAIN1 = 1, MEASOUT Gain = 0.2</th></tr>
<tr><td>MV</td><td>5 or 10</td><td>$\pm V_{DUT}$ (up to ±11.25 V)</td><td>0 V to 4.5 V</td></tr>
<tr><td>MI (GAIN0 = 0)</td><td>10</td><td>$\pm I_{DUT} \times R_{RSENSE} \times 10$ + VMID (up to ±11.25 V)</td><td>0 V to 4.5 V</td></tr>
<tr><td>MI (GAIN0 = 1)</td><td>5</td><td>$\pm I_{DUT} \times R_{RSENSE} \times 5$ + VMID (up to ±5.625 V)</td><td>0 V to 2.25 V</td></tr>
</table></td></tr>
<tr><td>5</td><td>TMP ENABLE</td><td>Thermal shutdown feature. To disable the thermal shutdown feature, set the TMP ENABLE bit to 0 (thermal shutdown is enabled by default).</td></tr>
<tr><td>4
3</td><td>TMP1
TMP0</td><td>The TMP1 and TMP0 bits allow the user to program the temperature that triggers thermal shutdown.
<table>
<tr><th>TMP ENABLE</th><th>TMP1</th><th>TMP0</th><th>Action</th></tr>
<tr><td>0</td><td>X</td><td>X</td><td>Thermal shutdown disabled.</td></tr>
<tr><td>1</td><td>X</td><td>X</td><td>Thermal shutdown enabled.</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>Shutdown at junction temperature of 130°C (power-on default).</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>Shutdown at junction temperature of 120°C.</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>Shutdown at junction temperature of 110°C.</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>Shutdown at junction temperature of 100°C.</td></tr>
</table></td></tr>
<tr><td>2</td><td>Latched</td><td>Configure the open-drain pin ($\overline{\text{CGALM}}$) as a latched or unlatched output pin. When high, this bit configures the $\overline{\text{CGALM}}$ alarm output as a latched output, allowing it to drive a controller I/O without needing to poll the line constantly. The power-on default for this pin is unlatched.</td></tr>
<tr><td>1
0 (LSB)</td><td>0
0</td><td>Unused bits. Set to 0.</td></tr>
</table>

WRITE PMU REGISTER

To address PMU functions, set the MODE1 and MODE0 bits to 0. This setting selects the PMU register (see Table 19 and Table 20). The AD5522 has very flexible addressing, which allows writing of data to a single PMU channel, any combination of PMU channels, or all PMU channels. This functionality enables multipin broadcasting to similar pins on a DUT. Bit 27 to Bit 24 select the PMU or group of PMUs that is addressed.

Table 24. PMU Register Bits—Bit B28 to Bit B15

B28	B27	B26	B25	B24	B23	B22	B21	B20	B19	B18[1]	B17	B16	B15
RD/$\overline{WR}$	PMU3	PMU2	PMU1	PMU0	MODE1	MODE0	CH EN	FORCE1	FORCE0	0	C2	C1	C0

[1] Bit B18 is reserved.

Table 25. PMU Register Bits—Bit B14 to Bit B0

B14	B13	B12	B11	B10	B9	B8	B7	B6	B5[1]	B4[1]	B3[1]	B2[1]	B1[1]	B0[1]
MEAS1	MEAS0	FIN	SF0	SS0	CL	CPOLH	Compare V/I	Clear	0	0	0	0	0	0

[1] Bit B5 to Bit B0 are unused data bits.

Table 26. PMU Register Functions

Bit	Bit Name	Description
28 (MSB)	RD/$\overline{WR}$	When low, a write to the selected register takes place; setting the RD/$\overline{WR}$ bit high initiates a readback sequence of the PMU, alarm status, comparator status, system control, or DAC register, as determined by the address bits.
27	PMU3	Bit PMU3 to Bit PMU0 address each PMU channel in the device. These bits allow control of an individual PMU channel or any combination of channels, in addition to multichannel programming (see Table 20).
26	PMU2	
25	PMU1	
24	PMU0	
23	MODE1	Set the MODE1 and MODE0 bits to 0 to access the PMU register selected by the PMU3 to PMU0 bits (Bit 27 to Bit 24).
22	MODE0	
PMU Register-Specific Bits		
21	CH EN	Channel enable. Set high to enable the selected channel or group of channels; set low to disable the selected channel or channels. When disabled, SW2 is closed and SW5 is open (outputs are high-Z). The measure mode is determined by the MEAS1 and MEAS0 bits at all times and is not affected by the CH EN bit. The guard amplifier and the comparators are not affected by this bit.
20	FORCE1	The FORCE1 and FORCE0 bits set the force function for each PMU channel (in association with the PMUx bits). All combinations of forcing and measuring (using the MEAS1 and MEAS0 bits) are available. The high-Z (voltage and current) modes allow the user to optimize glitch response during mode changes. While in high-Z voltage or current mode, with the PMU high-Z, new X1 codes loaded to the FIN DAC register and to the clamp DAC register are calibrated, stored in the X2 register, and loaded directly to the DAC outputs.
19	FORCE0	

FORCE1	FORCE0	Action
0	0	FV and current clamp (if clamp is enabled).
0	1	FI and voltage clamp (if clamp is enabled).
1	0	High-Z FOHx voltage (preload FIN DAC and clamp DAC).
1	1	High-Z FOHx current (preload FIN DAC and clamp DAC).

18	Reserved	0
17	C2	Bit C2 to Bit C0 specify the required current range. High-Z FV/FI commands ignore the current range address bits (C2, C1, and C0); therefore, these bit combinations cannot be used to enable or disable the force function for a PMU channel.
16	C1	
15	C0	

C2	C1	C0	Selected Current Range
0	0	0	±5 µA current range.
0	0	1	±20 µA current range.
0	1	0	±200 µA current range.
0	1	1	±2 mA current range (default).
1	0	0	±external current range.
1	0	1	Disable the always on mode for the external current range buffer[1].
1	1	0	Enable the always on mode for the external current range buffer[2].
1	1	1	Reserved.

<table>
<tr><th>Bit</th><th>Bit Name</th><th colspan="4">Description</th></tr>
<tr><td>14
13</td><td>MEAS1
MEAS0</td><td colspan="4">The MEAS1 and MEAS0 bits specify the required measure mode, allowing the MEASOUTx line to be disabled, connected to the temperature sensor, or enabled for measurement of current or voltage.
MEAS1 | MEAS0 | Action
0 | 0 | MEASOUTx is connected to I_{SENSE}
0 | 1 | MEASOUTx is connected to V_{SENSE}
1 | 0 | MEASOUTx is connected to the temperature sensor
1 | 1 | MEASOUTx is high-Z (SW12 open)</td></tr>
<tr><td>12</td><td>FIN</td><td colspan="4">This bit sets the status of the force input (FIN) amplifier.
0 = input of the force amplifier switched to GND.
1 = input of the force amplifier connected to the FIN DAC output.</td></tr>
<tr><td>11
10</td><td>SF0
SS0</td><td colspan="4">The SF0 and SS0 bits specify the switching of system force and sense lines to the force and sense paths at the DUT. The channel to which the system force and system sense lines are connected is set by the PMU3 to PMU0 bits. For correct operation, only one PMU channel should be connected to the SYS_FORCE and SYS_SENSE paths at any one time.
SF0 | SS0 | Action
0 | 0 | SYS_FORCE and SYS_SENSE are high-Z for the selected channel
0 | 1 | SYS_FORCE is high-Z and SYS_SENSE is connected to MEASVHx for the selected channels
1 | 0 | SYS_FORCE is connected to FOHx and SYS_SENSE is high-Z for the selected channel
1 | 1 | SYS_FORCE is connected to FOHx and SYS_SENSE is connected to MEASVHx for the selected channel</td></tr>
<tr><td>9</td><td>CL</td><td colspan="4">Per-PMU current or voltage clamp enable bit. A logic high enables the clamp function for the selected PMU. The clamp enable function is also available in the system control register. This dual functionality allows flexible enabling or disabling of this function. When reading back information about the status of the clamp enable function on a per-channel basis, the data that was most recently written to the clamp register is available in the readback word from either the PMU register or the system control register.</td></tr>
<tr><td>8</td><td>CPOLH</td><td colspan="4">Comparator output enable bit. By default, the comparator outputs are high-Z on power-on. A logic high enables the comparator output for the selected PMU. The comparator function CPBIASEN (Bit 13 in the system control register), must be enabled. The comparator output enable function is also available in the system control register. This dual functionality allows flexible enabling or disabling of this function. When reading back information about the status of the comparator enable function, the data that was most recently written to the comparator status register is available in the readback word from either the PMU register or the system control register.</td></tr>
<tr><td>7</td><td>Compare V/I</td><td colspan="4">A logic high selects the compare voltage function; a logic low selects the compare current function.</td></tr>
<tr><td>6</td><td>Clear</td><td colspan="4">To clear or reset a latched alarm bit and pin (temperature, guard, or clamp), write a 1 to this bit. This bit applies to latched alarm conditions (clamp and guard) on all four PMU channels.</td></tr>
<tr><td>5
4
3
2
1
0 (LSB)</td><td>Unused</td><td colspan="4">Unused bits. Set to 0.</td></tr>
</table>

[1] Writing 101 in Bit 17 to Bit 15 disables the always on mode for the external current range buffer. Use with FV mode (FORCE1 = FORCE0 = 0) only. To complete the disabling of the always on mode, the PMU channel is placed into high-Z mode and the external current range buffer is returned to its default operation (off).

[2] Writing 110 in Bit 17 to Bit 15 places the external current range buffer into always on mode. In this mode, the buffer is always active with no regard to the selected current range. The always on mode is intended for use where an external high current stage is being used for a current drive in excess of ±80 mA; having the internal stage always on should help to eliminate timing concerns when transitioning between this current range and other ranges. When first enabling the always on mode, use it in conjunction with FV mode (FORCE1 = FORCE0 = 0); the device now enables the external current range buffer. The 110 code also places the device into high-Z mode (necessary to complete the enabling function). To return to an FV or FI operating mode, select the appropriate mode and current range. The external range sense resistor is connected to an MI circuit only when the external current range address is selected (C2 to C0 are set to 100). The default operation at power-on is disabled (or off).

WRITE DAC REGISTER

The DAC input, gain, and offset registers are addressed through a combination of PMU bits (Bit 27 to Bit 24) and mode bits (Bit 23 and Bit 22). Bit A5 to Bit A0 address each DAC level on chip. Bit D15 to Bit D0 are the DAC data bits used when writing to these registers. The PMU address bits allow addressing of a particular DAC for any combination of PMU channels.

Table 27. DAC Register Bits

B28	B27	B26	B25	B24	B23	B22	B21	B20	B19	B18	B17	B16	B15 to B0
RD/$\overline{WR}$	PMU3	PMU2	PMU1	PMU0	MODE1	MODE0	A5	A4	A3	A2	A1	A0	Data Bits[D15 (MSB):D0 (LSB)]

Table 28. DAC Register Functions

Bit	Bit Name	Description		
28 (MSB)	RD/$\overline{WR}$	When this bit is low, a write function takes place to the selected register; setting the RD/$\overline{WR}$ bit high initiates a readback sequence of the PMU, alarm status, comparator status, system control, or DAC register, as determined by the address bits.		
27	PMU3	Bit PMU3 to Bit PMU0 address each PMU and DAC channel in the device. These bits allow control of each individual DAC channel or any combination of channels, in addition to multichannel programming.		
26	PMU2			
25	PMU1			
24	PMU0			
23	MODE1	The MODE1 and MODE0 bits allow addressing of the DAC gain (M), offset (C), or input (X1) register.		
22	MODE0	**MODE1**	**MODE0**	**Action**
		0	0	Write to the system control register or the PMU register
		0	1	Write to the DAC gain (M) register
		1	0	Write to the DAC offset (C) register
		1	1	Write to the DAC input data (X1) register
DAC Register-Specific Bits				
21	A5	DAC address bits. The A5 to A3 bits select the register set that is addressed. See the DAC Addressing section.		
20	A4			
19	A3			
18	A2	DAC address bits. The A2 to A0 bits select the DAC that is addressed. See the DAC Addressing section.		
17	A1			
16	A0			
15 to 0	D15 (MSB) to D0 (LSB)	16 DAC data bits for X1 and C registers. M register is 15 bits wide, D15 to D1.		

DAC Addressing

For the FIN and comparator (CPH and CPL) DACs, there is a set of X1, M, and C registers for each current range, and one set for the voltage range; for the clamp DACs (CLL and CLH), there are only two sets of X1, M, and C registers.

When calibrating the device, the M and C registers allow volatile storage of gain and offset coefficients. Calculation of the corresponding DAC X2 register occurs only when the X1 data is loaded (no internal calculation occurs on M or C updates).

There is one offset DAC for all four channels in the device that is addressed using the PMUx bits. The offset DAC has only an input register associated with it; no M or C registers are associated with this DAC. When writing to the offset DAC, set the MODE1 and MODE0 bits high to address the DAC input register (X1).

The same address table is also used for readback of a particular DAC address.

Note that CLL is clamp level low and CLH is clamp level high.

- When forcing a voltage, the current clamps are engaged; therefore, both the CLL current ranges register set and the CLH current ranges register set are loaded to the clamp DACs.
- When forcing a current, the voltage clamps are engaged; therefore, both the CLL voltage range register set and the CLH voltage range register set are loaded to the clamp DACs.

All codes not explicitly referenced Table 29 are reserved and should not be used.

Table 29. DAC Register Addressing

A5	A4	A3	A2	A1	A0	MODE1	MODE0	Register Set	Addressed Register
0	0	0	0	0	0	1	1	N/A	Offset DAC X
0	0	1	0	0	0	0	1	±5 µA current range	FIN M
						1	0		FIN C
						1	1		FIN X1
0	0	1	0	0	1	0	1	±20 µA current range	FIN M
						1	0		FIN C
						1	1		FIN X1
0	0	1	0	1	0	0	1	±200 µA current range	FIN M
						1	0		FIN C
						1	1		FIN X1
0	0	1	0	1	1	0	1	±2 mA current range	FIN M
						1	0		FIN C
						1	1		FIN X1
0	0	1	1	0	0	0	1	±external current range	FIN M
						1	0		FIN C
						1	1		FIN X1
0	0	1	1	0	1	0	1	Voltage range	FIN M
						1	0		FIN C
						1	1		FIN X1
0	1	0	1	0	0	0	1	Current ranges	CLL M
						1	0		CLL C
						1	1		CLL X1[1]
0	1	0	1	0	1	0	1	Voltage range	CLL M
						1	0		CLL C
						1	1		CLL X1
0	1	1	1	0	0	0	1	Current ranges	CLH M
						1	0		CLH C
						1	1		CLH X1[2]
0	1	1	1	0	1	0	1	Voltage range	CLH M
						1	0		CLH C
						1	1		CLH X1
1	0	0	0	0	0	0	1	±5 µA current range	CPL M
						1	0		CPL C
						1	1		CPL X1

A5	A4	A3	A2	A1	A0	MODE1	MODE0	Register Set	Addressed Register
1	0	0	0	0	1	0	1	±20 µA current range	CPL M
						1	0		CPL C
						1	1		CPL X1
1	0	0	0	1	0	0	1	±200 µA current range	CPL M
						1	0		CPL C
						1	1		CPL X1
1	0	0	0	1	1	0	1	±2 mA current range	CPL M
						1	0		CPL C
						1	1		CPL X1
1	0	0	1	0	0	0	1	±external current range	CPL M
						1	0		CPL C
						1	1		CPL X1
1	0	0	1	0	1	0	1	Voltage range	CPL M
						1	0		CPL C
						1	1		CPL X1
1	0	1	0	0	0	0	1	±5 µA current range	CPH M
						1	0		CPH C
						1	1		CPH X1
1	0	1	0	0	1	0	1	±20 µA current range	CPH M
						1	0		CPH C
						1	1		CPH X1
1	0	1	0	1	0	0	1	±200 µA current range	CPH M
						1	0		CPH C
						1	1		CPH X1
1	0	1	0	1	1	0	1	±2 mA current range	CPH M
						1	0		CPH C
						1	1		CPH X1
1	0	1	1	0	0	0	1	±external current range	CPH M
						1	0		CPH C
						1	1		CPH X1
1	0	1	1	0	1	0	1	Voltage range	CPH M
						1	0		CPH C
						1	1		CPH X1

[1] CLL should be within the range of 0x0000 to 0x7FFF.
[2] CLH should be within the range of 0x8000 to 0xFFFF.

READ REGISTERS

Readback of all the registers in the device is possible via the SPI and the LVDS interfaces. To read data from a register, it is first necessary to write a readback command to tell the device which register is required for readback. See Table 30 to address the appropriate channel.

When the required channel is addressed, the device loads the 24-bit readback data into the MSB positions of the 29-bit serial shift register (the five LSBs are filled with 0s). SCLK rising edges clock this readback data out on SDO (framed by the $\overline{\text{SYNC}}$ signal).

A minimum of 24 clock rising edges is required to shift the readback data out of the shift register. If writing a 24-bit word to shift data out of the device, the user must ensure that the 24-bit write is effectively an NOP (no operation) command. The last five bits in the shift register are always 00000: these five bits become the MSBs of the shift register when the 24-bit write is loaded. To ensure that the device receives an NOP command as described in Table 20, the recommended flush command is 0xFFFFFF; thus, no change is made to any register in the device.

Readback data can also be shifted out by writing another 29-bit write or read command. If writing a 29-bit command, the readback data is MSB data available on SDO, followed by 00000.

Table 30. Read Functions of the AD5522

B28	B27	B26	B25	B24	B23	B22	B21 to B0	Selected Channel			
RD/$\overline{\text{WR}}$	PMU3	PMU2	PMU1	PMU0	MODE1	MODE0	Data bits	CH3	CH2	CH1	CH0
Read Functions											
1	0	0	0	0	0	0	All 0s	Read from system control register			
1	0	0	0	0	0	1	All 0s	Read from comparator status register			
1	0	0	0	0	1	0	X (don't care)	Reserved			
1	0	0	0	0	1	1	All 0s	Read from alarm status register			
Read Addressed PMU Register (Only One PMU Register Can Be Read at One Time)											
1	0	0	0	1	0	0	All 0s				CH0
1	0	0	1	0	0	0				CH1	
1	0	1	0	0	0	0			CH2		
1	1	0	0	0	0	0		CH3			
Read Addressed DAC M Register (Only One DAC Register Can Be Read at One Time)											
1	0	0	0	1	0	1	DAC address (see Table 29)				CH0
1	0	0	1	0	0	1				CH1	
1	0	1	0	0	0	1			CH2		
1	1	0	0	0	0	1		CH3			
Read Addressed DAC C Register (Only One DAC Register Can Be Read at One Time)											
1	0	0	0	1	1	0	DAC address (see Table 29)				CH0
1	0	0	1	0	1	0				CH1	
1	0	1	0	0	1	0			CH2		
1	1	0	0	0	1	0		CH3			
Read Addressed DAC X1 Register (Only One DAC Register Can Be Read at One Time)											
1	0	0	0	1	1	1	DAC address (see Table 29)				CH0
1	0	0	1	0	1	1				CH1	
1	0	1	0	0	1	1			CH2		
1	1	0	0	0	1	1		CH3			

READBACK OF SYSTEM CONTROL REGISTER

The system control register readback function is a 24-bit word. Mode and system control register data bits are shown in Table 31.

Table 31. System Control Register Readback

Bit	Bit Name	Description
23 (MSB)	MODE1	Set the MODE1 and MODE0 bits to 0 to address the system control register.
22	MODE0	
System Control Register-Specific Readback Bits		
21 20 19 18	CL3 CL2 CL1 CL0	Read back the status of the individual current clamp enable bits. 0 = clamp is disabled. 1 = clamp is enabled. When reading back information about the status of the clamp enable function, the data that was most recently written to the current clamp register from either the system control register or the PMU register is available in the readback word.
17 16 15 14	CPOLH3 CPOLH2 CPOLH1 CPOLH0	Read back information about the status of the comparator output enable bits. 1 = PMU comparator output is enabled. 0 = PMU comparator output is disabled. When reading back information about the status of the comparator output enable function, the data that was most recently written to the comparator status register from either the system control register or the PMU register is available in the readback word.
13	CPBIASEN	This readback bit indicates the status of the comparator enable function. 1 = comparator function is enabled. 0 = comparator function is disabled.
12	DUTGND/CH	DUTGND per channel enable. 1 = DUTGND per channel is enabled. 0 = individual guard inputs are available per channel.
11 10	GUARD ALM CLAMP ALM	These bits provide information about which of these alarm bits trigger the $\overline{\text{CGALM}}$ pin. 1 = guard/clamp alarm is enabled. 0 = guard/clamp alarm is disabled.
9	INT10K	If this bit is high, the internal 10 kΩ resistor (SW7) is connected between FOHx and MEASVHx, and between DUTGND and AGND. If this bit is low, SW7 is open.
8	Guard EN	Read back the status of the guard amplifiers. If this bit is high, the amplifiers are enabled.
7 6	GAIN1 GAIN0	Status of the selected MEASOUTx output range. See Table 10 and Table 11.
5 4 3	TMP ENABLE TMP1 TMP0	Read back the status of the thermal shutdown function. **Bits[5:3]** / **Action** 0XX — Thermal shutdown disabled. 100 — Thermal shutdown enabled at junction temperature of 130°C (power-on default). 101 — Thermal shutdown enabled at junction temperature of 120°C. 110 — Thermal shutdown enabled at junction temperature of 110°C. 111 — Thermal shutdown enabled at junction temperature of 100°C. 1XX — Thermal shutdown enabled.
2	Latched	This bit indicates the status of the open-drain alarm outputs, $\overline{\text{TMPALM}}$ and $\overline{\text{CGALM}}$. 1 = open-drain alarm outputs are latched. 0 = open-drain alarm outputs are unlatched.
1 0 (LSB)	Unused readback bits	Loads with 0s.

READBACK OF PMU REGISTER

The PMU register readback function is a 24-bit word that includes the mode and PMU data bits. Only one PMU register can be read back at any one time.

Table 32. PMU Register Readback

Bit	Bit Name	Description
23 (MSB) 22	MODE1 MODE0	Set the MODE1 and MODE0 bits to 0 to access the selected PMU register.
PMU Register-Specific Bits		
21	CH EN	Channel enable. If this bit is high, the selected channel is enabled; if this bit is low, the channel is disabled.
20 19	FORCE1 FORCE0	These bits indicate which force mode the selected channel is in. 00 = FV and current clamp (if clamp is enabled). 01 = FI and voltage clamp (if clamp is enabled). 10 = high-Z FOHx voltage. 11 = high-Z FOHx current.
18	Reserved	0.
17 16 15	C2 C1 C0	These three bits indicate which forced or measured current range is set for the selected channel (see Table 26).
14 13	MEAS1 MEAS0	These bits indicate which measure mode is selected: voltage, current, temperature sensor, or high-Z. 00 = MEASOUTx is connected to I_{SENSE}. 01 = MEASOUTx is connected to V_{SENSE}. 10 = MEASOUTx is connected to the temperature sensor. 11 = MEASOUTx is high-Z (SW12 open).
12	FIN	This bit shows the status of the force input (FIN) amplifier. 0 = input of the force amplifier switched to GND. 1 = input of the force amplifier connected to the FIN DAC output.
11 10	SF0 SS0	The system force and sense lines can be connected to any of the four PMU channels. These bits indicate whether the system force and sense lines are switched in (see Table 26).
9	CL	Read back the status of the individual current clamp enable bits. 1 = clamp is enabled on this channel. 0 = clamp is disabled on this channel. When reading back information about the status of the current clamp enable function, the data that was most recently written to the current clamp register from either the system control register or the PMU register is available in the readback word.
8	CPOLH	Read back the status of the comparator output enable bit. 1 = PMU comparator output is enabled. 0 = PMU comparator output is disabled. When reading back information about the status of the comparator output enable function, the data that was most recently written to the comparator register from either the system control register or the PMU register is available in the readback word.
7	Compare V/I	1 = compare voltage function is enabled on the selected channel. 0 = compare current function is enabled on the selected channel.
6 5	$\overline{\text{LTMPALM}}$ $\overline{\text{TMPALM}}$	$\overline{\text{TMPALM}}$ corresponds to the open-drain $\overline{\text{TMPALM}}$ output pin that flags a temperature event exceeding the default or user programmed level. The temperature alarm is a per-device alarm; the latched ($\overline{\text{LTMPALM}}$) and unlatched ($\overline{\text{TMPALM}}$) bits indicate whether a temperature event occurred and whether the alarm still exists (that is, whether the junction temperature still exceeds the programmed alarm level). To reset an alarm event, the user must write a 1 to the clear bit (Bit 6) in the PMU register.
4 to 0 (LSB)	Unused readback bits	Loads with 0s.

READBACK OF COMPARATOR STATUS REGISTER

The comparator status register is a read-only register that provides access to the output status of each comparator pin on the chip. Table 33 shows the format of the comparator register readback word.

READBACK OF ALARM STATUS REGISTER

The alarm status register is a read-only register that provides information about temperature, clamp, and guard alarm events (see Table 34). Temperature alarm status is also available in any of the four PMU readback registers.

Table 33. Comparator Status Register (Read-Only)

Bit	Bit Name	Description
23 (MSB)	MODE1	0
22	MODE0	1
Comparator Status Register-Specific Bits		
21	CPOL0	Comparator output conditions per channel corresponding to the comparator output pins. 1 = PMU comparator output is high. 0 = PMU comparator output is low.
20	CPOH0	
19	CPOL1	
18	CPOH1	
17	CPOL2	
16	CPOH2	
15	CPOL3	
14	CPOH3	
13 to 0 (LSB)	Unused readback bits	Loads with zeros.

Table 34. Alarm Status Register Readback

Bit	Bit Name	Description
23 (MSB)	MODE1	1
22	MODE0	1
Alarm Status Register-Specific Bits		
21	$\overline{\text{LTMPALM}}$	$\overline{\text{TMPALM}}$ corresponds to the open-drain $\overline{\text{TMPALM}}$ output pin that flags a temperature event exceeding the default or user programmed level. The temperature alarm is a per-device alarm; the latched ($\overline{\text{LTMPALM}}$) and unlatched ($\overline{\text{TMPALM}}$) bits indicate whether a temperature event occurred and whether the alarm still exists (that is, whether the junction temperature still exceeds the programmed alarm level). To reset an alarm event, the user must write a 1 to the clear bit (Bit 6) in the PMU register.
20	$\overline{\text{TMPALM}}$	
19	$\overline{\text{LG0}}$	$\overline{\text{LGx}}$ is the per-channel latched guard alarm bit, and $\overline{\text{Gx}}$ is the unlatched guard alarm bit. These bits indicate which channel flagged the alarm on the open-drain alarm pin, $\overline{\text{CGALM}}$, and whether the alarm condition still exists.
18	$\overline{\text{G0}}$	
17	$\overline{\text{LG1}}$	
16	$\overline{\text{G1}}$	
15	$\overline{\text{LG2}}$	
14	$\overline{\text{G2}}$	
13	$\overline{\text{LG3}}$	
12	$\overline{\text{G3}}$	
11	$\overline{\text{LC0}}$	$\overline{\text{LCx}}$ is the per-channel latched clamp alarm bit, and $\overline{\text{Cx}}$ is the unlatched clamp alarm bit. These bits indicate which channel flagged the alarm on the open-drain alarm pin $\overline{\text{CGALM}}$ and whether the alarm condition still exists.
10	$\overline{\text{C0}}$	
9	$\overline{\text{LC1}}$	
8	$\overline{\text{C1}}$	
7	$\overline{\text{LC2}}$	
6	$\overline{\text{C2}}$	
5	$\overline{\text{LC3}}$	
4	$\overline{\text{C3}}$	
3 to 0 (LSB)	Unused readback bits	Loads with 0s.

READBACK OF DAC REGISTER

The DAC register readback function is a 24-bit word that includes the mode, address, and DAC data bits.

Table 35. DAC Register Readback

Bit	Bit Name	Description
23 (MSB) 22	MODE1 MODE0	The MODE1 and MODE0 bits indicate the type of DAC register (X1, M, or C) that is read. 01 = DAC gain (M) register. 10 = DAC offset (C) register. 11 = DAC input data (X1) register.
DAC Register-Specific Bits		
21 to 16	A5 to A0	Address bits indicating the DAC register that is read (see Table 29).
15 to 0 (LSB)	D15 to D0	Contents of the addressed DAC register (X1, M, or C).

APPLICATIONS INFORMATION

POWER-ON DEFAULT

The power-on default for all DAC channels is that the contents of each M register are set to full scale (0xFFFF), and the contents of each C register are set to midscale (0x8000). The contents of the DAC X1 registers at power-on are listed in Table 36.

The power-on default for the alarm status register is 0xFFFFF0, and the power-on default for the comparator status register is 0x400000. The power-on default values of the PMU register and the system control register are shown in Table 37 and Table 38.

SETTING UP THE DEVICE ON POWER-ON

On power-on, default conditions are recalled from the power-on reset register to ensure that each PMU and DAC channel is powered up in a known condition. To operate the device, the user must follow these steps:

1. Configure the device by writing to the system control register to set up different functions as required.
2. Calibrate the device to trim out errors, and load the required calibration values to the gain (M) and offset (C) registers. Load codes to each DAC input (X1) register. When X1 values are loaded to the individual DACs, the calibration engine calculates the appropriate X2 value and stores it, ready for the PMU address to call it.
3. Load the required PMU channel with the required force mode, current range, and so on. Loading the PMU channel configures the switches around the force amplifier, measure function, clamps, and comparators, and also acts as a load signal for the DACs, loading the DAC register with the appropriate stored X2 value.
4. Because the voltage and current ranges have individual DAC registers associated with them, each PMU register mode of operation calls a particular X2 register. Therefore, only updates (that is, changes to the X1 register) to DACs associated with the selected mode of operation are reflected in the output of the PMU. If there is a change to the X1 value associated with a different PMU mode of operation, this X1 value and its M and C coefficients are used to calculate a corresponding X2 value, which is stored in the correct X2 register, but this value is not loaded to the DAC.

Table 36. Default Contents of DAC Registers at Power-On

DAC Register	Default Value
Offset DAC	0xA492
FIN DAC	0x8000
CLL DAC	0x0000
CLH DAC	0xFFFF
CPL DAC	0x0000
CPH DAC	0xFFFF

Table 37. Power-On Default for System Control Register

Bit	Bit Name	Default Value
21 (MSB)	CL3	0
20	CL2	0
19	CL1	0
18	CL0	0
17	CPOLH3	0
16	CPOLH2	0
15	CPOLH1	0
14	CPOLH0	0
13	CPBIASEN	0
12	DUTGND/CH	0
11	Guard ALM	0
10	Clamp ALM	0
9	INT10K	0
8	Guard EN	0
7	GAIN1	0
6	GAIN0	0
5	TMP enable	1
4	TMP1	0
3	TMP0	0
2	Latched	0
1	Unused data bit	0
0 (LSB)	Unused data bit	0

Table 38. Power-On Default for PMU Register

Bit	Bit Name	Default Value
21 (MSB)	CH EN	0
20	FORCE1	0
19	FORCE0	0
18	Reserved	0
17	C2	0
16	C1	1
15	C0	1
14	MEAS1	1
13	MEAS0	1
12	FIN	0
11	SF0	0
10	SS0	0
9	CL	0
8	CPOLH	0
7	Compare V/I	0
6	$\overline{\text{LTMPALM}}$	1
5	$\overline{\text{TMPALM}}$	1
4	Unused data bit	0
3	Unused data bit	0
2	Unused data bit	0
1	Unused data bit	0
0 (LSB)	Unused data bit	0

CHANGING MODES

There are different ways of handling a mode change.

1. Load any DAC X1 values that require changes. Remember that for force amplifier and comparator DACs, X1 registers are available per voltage and current range, so the user can preload new DAC values to make DAC updates ahead of time; the calibration engine calculates the X2 values and stores them.
2. Change to the new PMU mode (FI or FV). This action loads the new switch conditions to the PMU circuitry and loads the DAC register with the stored X2 data.

The following steps describe another method for changing modes:

1. In the PMU register (Bit 20 and Bit 19), enable the high-Z voltage or high-Z current mode to make the amplifier high impedance (SW5 open).
2. Load any DAC X1 values that require changes. Remember that for force amplifier and comparator DACs, X1 registers are available per voltage and current range, so the user can preload new DAC values to make DAC updates ahead of time; the calibration engine calculates the X2 values and stores them.
3. When the high-Z (voltage or current) mode is used, the relevant DAC outputs are automatically updated (FIN, CLL, and CLH DACs). For example, in high-Z voltage mode, when new X1 writes occur, the FIN voltage X2 result is calculated, cached, and loaded to the FIN DAC. When forcing a voltage, current clamps are engaged, so the CLL current register can be loaded, and the gain and offset corrected and loaded to the DAC register. (The CLH current register works the same way.)
4. Change to the new PMU mode (FI or FV). This action loads the new switch conditions to the PMU circuitry. Because the DAC outputs are already loaded, transients are minimized when changing current or voltage mode.

REQUIRED EXTERNAL COMPONENTS

The minimum required external components for use with the AD5522 are shown in Figure 58. Decoupling is greatly dependent on the type of supplies used, other decoupling on the board, and the noise in the system. It is possible that more or less decoupling may be required.

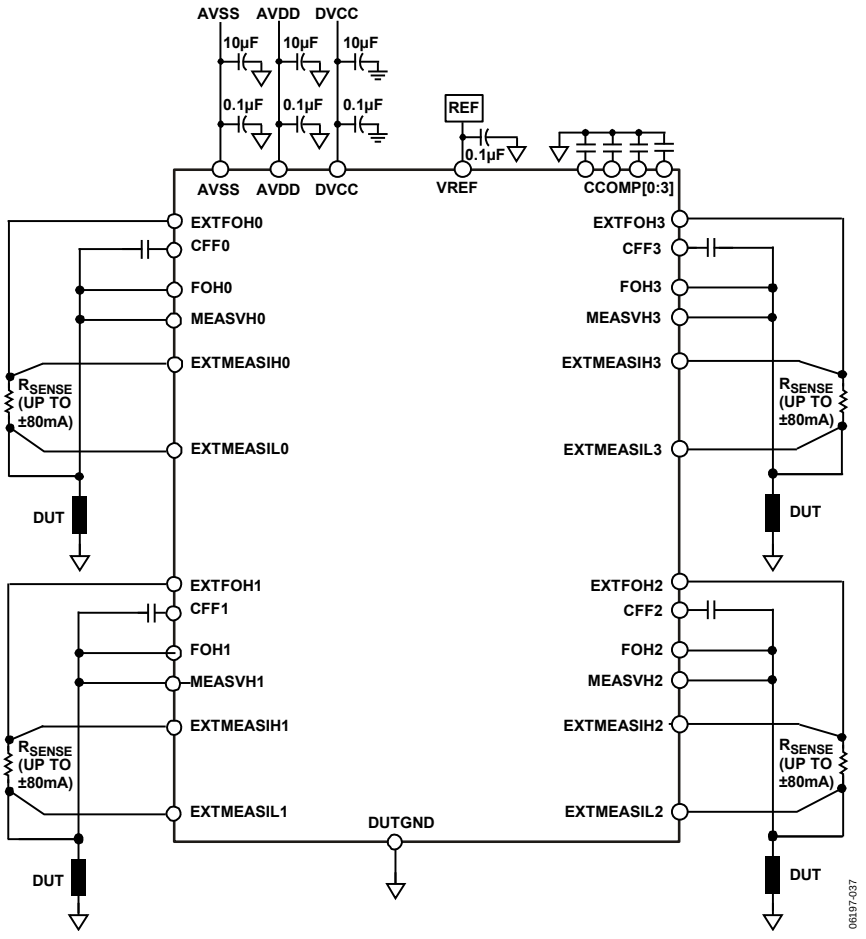


Figure 58. External Components Required for Use with the AD5522

Table 39. ADCs and ADC Drivers Suggested For Use with AD5522[1]

Part No.	Resolution	Sample Rate	Ch. No.	AIN Range	Interface	ADC Driver	Multiplexer[2]	Package
AD7685	16	250 kSPS	1	0 V to VREF	Serial, SPI	ADA4841-x	ADG704, ADG708	MSOP, LFCSP
AD7686	16	500 kSPS	1	0 V to VREF	Serial, SPI	ADA4841-x	ADG704, ADG708	MSOP, LFCSP
AD7693[3]	16	500 kSPS	1	−VREF to +VREF	Serial, SPI	ADA4841-x, ADA4941-1	ADG1404, ADG1408, ADG1204	MSOP, LFCSP
AD7610	16	250 kSPS	1	Bipolar 10 V, Bipolar 5 V, Unipolar 10 V, Unipolar 5 V	Serial/Parallel	AD8021	ADG1404, ADG1408, ADG1204	LFCSP, LQFP
AD7655	16	1 MSPS	4	0 V to 5 V	Serial/Parallel	ADA4841-x/ AD8021		

[1] Subset of the possible ADCs suitable for use with the AD5522. Visit www.analog.com for more options.
[2] For purposes of sharing an ADC among multiple PMU channels. Note that the multiplexer is not absolutely necessary because the AD5522 MEASOUTx path has a tri-state mode per channel.
[3] Do not allow the MEASOUTx output range to exceed the analog input (AIN) range of the ADC.

POWER SUPPLY DECOUPLING

Careful consideration of the power supply and ground return layout helps to ensure the rated performance. Design the printed circuit board (PCB) on which the AD5522 is mounted so that the analog and digital sections are separated and confined to certain areas of the board. If the AD5522 is in a system where multiple devices require an AGND-to-DGND connection, the connection should be made at one point only. Establish the star ground point as close as possible to the device.

For supplies with multiple pins (AVSS and AVDD), it is recommended that these pins be tied together and that each supply be decoupled only once.

The AD5522 should have ample supply decoupling of 10 µF in parallel with 0.1 µF on each supply located as close to the package as possible, ideally right up against the device. The 10 µF capacitors are the tantalum bead type. The 0.1 µF capacitors should have low effective series resistance (ESR) and low effective series inductance (ESL)—typical of the common ceramic types that provide a low impedance path to ground at high frequencies—to handle transient currents due to internal logic switching.

Avoid running digital lines under the device because they can couple noise onto the device. However, allow the analog ground plane to run under the AD5522 to avoid noise coupling (applies only to the package with paddle up). The power supply lines of the AD5522 should use as large a trace as possible to provide low impedance paths and reduce the effects of glitches on the power supply line. Fast switching digital signals should be shielded with digital ground to avoid radiating noise to other parts of the board, and they should never be run near the reference inputs. It is essential to minimize noise on all VREF lines.

Avoid crossover of digital and analog signals. Traces on opposite sides of the board should run at right angles to each other to reduce the effects of feedthrough through the board. As is the case for all thin packages, care must be taken to avoid flexing the package and to avoid a point load on the surface of this package during the assembly process.

Also, note that the exposed paddle of the AD5522 is connected to the negative supply, AVSS.

POWER SUPPLY SEQUENCING

When the supplies are connected to the AD5522, it is important that the AGND and DGND pins be connected to the relevant ground planes before the positive or negative supplies are applied. This is the only power sequencing requirement for this device.

TYPICAL APPLICATION FOR THE AD5522

Figure 59 shows the AD5522 used in an ATE system. The device can be used as a per-pin parametric unit to speed up the rate at which testing can be done.

The central PMU (shown in the block diagram) is usually a highly accurate PMU and is shared among a number of pins in the tester. In general, many discrete levels are required in an ATE system for the pin drivers, comparators, clamps, and active loads. DAC devices such as the AD537x family offer a highly integrated solution for a number of these levels.

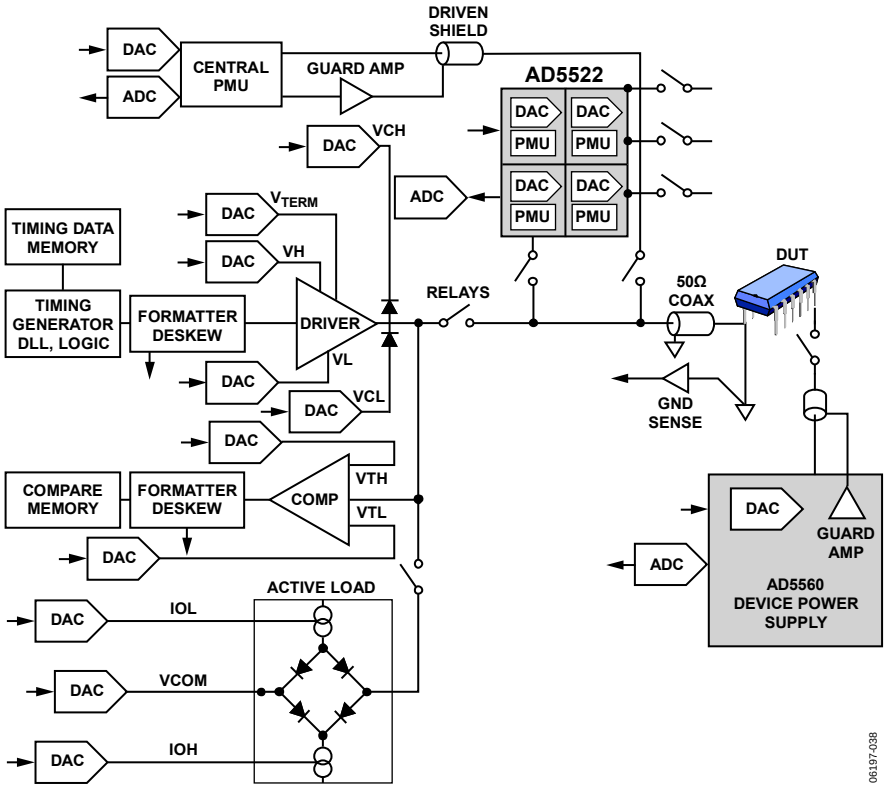
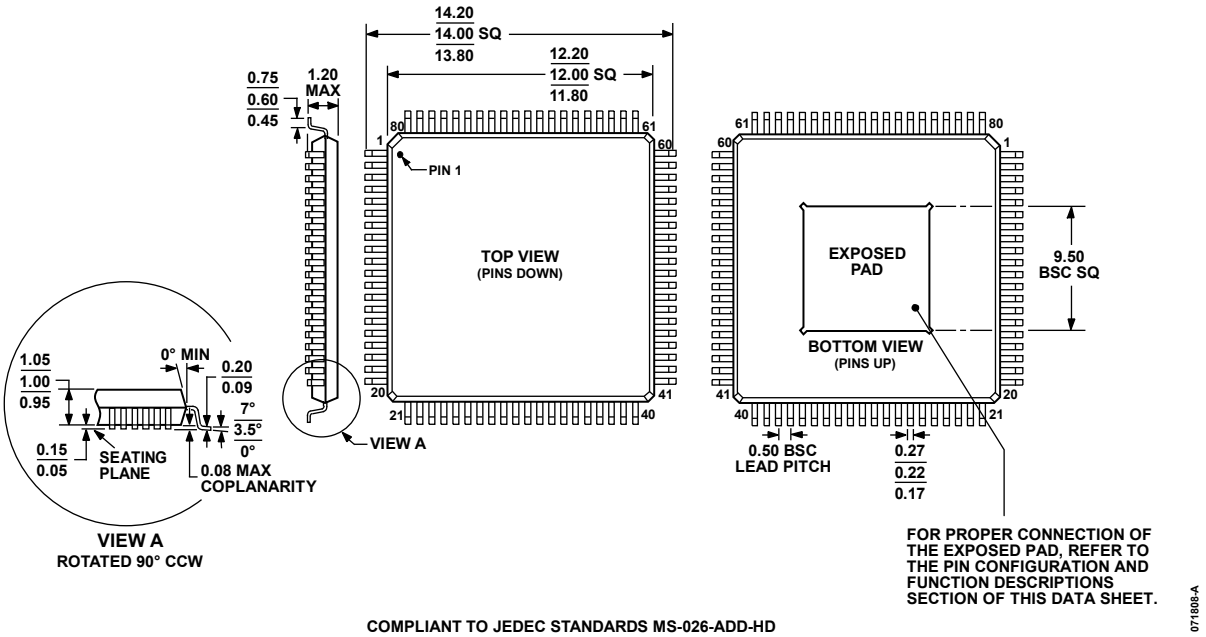


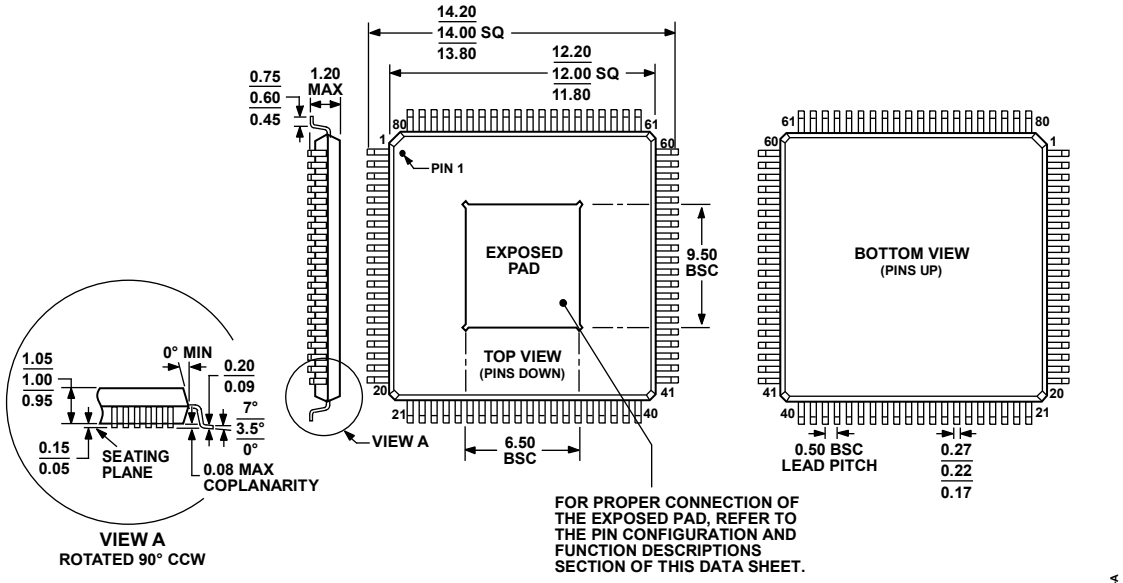
Figure 59. Typical Applications Circuit Using the AD5522 as a Per-Pin Parametric Unit

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-026-ADD-HD

Figure 60. 80-Lead Thin Quad Flat Package, Exposed Pad [TQFP_EP]
SV-80-3
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MS-026-ADD-HU

Figure 61. 80-Lead Thin Quad Flat Package, Exposed Pad [TQFP_EP]
SV-80-2
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range (T_J)	Package Description	Package Option
AD5522JSVDZ	25°C to 90°C	80-Lead TQFP_EP with Exposed Pad on Bottom	SV-80-3
AD5522JSVUZ	25°C to 90°C	80-Lead TQFP_EP with Exposed Pad on Top	SV-80-2
EVAL-AD5522EBDZ		Evaluation Board with Exposed Pad on Bottom	
EVAL-AD5522EBUZ		Evaluation Board with Exposed Pad on Top	

[1] Z = RoHS Compliant Part.

NOTES

D06197-0-2/11(D)