# F16267

## 8-bit Microcontroller with CIR Receiver

**Release Date: Feb, 2009**
**Version: 0.20P**

# F16267 Datasheet Revision History

| Version | Date | Page | Revision History |
|---|---|---|---|
| 0.10P | Dec, 2007 | | Preliminary version |
| 0.11P | Mar, 2008 | 7 | Add the lost description of pin 15 |
| | | 10 | Add current consumption description |
| | | 13 | Add all the register descriptions |
| 0.12P | Apr, 2008 | 11 | Add internal 12Mhz clock description |
| | | 13-23 | Revise register address |
| 0.13P | Jul, 2008 | 13-15 | Revise register description |
| 0.14P | Oct, 2008 | 20-24 | Register address: 7.38-7.53 |
| 0.15P | Oct, 2008 | 21-24 | Correct descriptions of Alarm Register 0x0087-0x008B |
| | | 24 | Remove the redundant register 0x8F |
| | | | RAM Data Register –Index 00B090h~00EFCFh (Total 64 Bytes) |
| | | 26 | Package Dimensions (~~28~~16-SSOP) |
| 0.16P | Oct, 2008 | 25 | Correct the typo F16167R as F16267R |
| 0.17P | Oct, 2008 | 6 | Revise pin configuration, swap pin 9 and 10 |
| 0.18P | Nov, 2008 | 19 | Add Register 0x002F description |
| 0.19P | Nov, 2008 | 11 | Add 6.5 Watchdog timer function description |
| | | 13 | Add table 3 INT0, INT1 behavior |
| | | | Add 6.6.3 power saving mode description |
| | | 15 | Remove Register 0x0000~0x0007 description |
| | | 23 | Description of bit7 in Register 0x008E: ~~FP~~PF*PIE = “1” |
| | | 24 | Name of Register 0x00FD: Time_~~Middle~~Low_Byte |
| 0.20P | Feb, 2009 | 17 | Register 0x0012, bit0: RX Delay → Ready |
| | | 18 | Register 0x0015, 0x0017 default: 04h →80h |
| | | 19-20 | Register 0x0030, exchange the descriptions of bit 1 and 0 |
| | | 20 | Register 0x0032, 0x0033 typo revised |

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# Table of Contents

# 1 General Description

The F16267 is an 80C31 instruction compatible microcontroller for general purpose system management. With external I2C serial EEPROM(2K bytes), The F16267 provides the best extendable flexibility by different customized features and memory size, loading program through two wires I2C serial port will be easily to implement. Furthermore, the F16267 supports one I2C slave serial ports to connect system chipset. The F16267 also supports 8 suits general purpose input / output pins and a low current consumption RTC.

These functions of F16267 are implemented for different kinds of applications. Major application fields are small home appliances or computer peripheral applications. The F16267 is in SSOP-16 package and powered by 3.3VCC.

# 2 Feature

- Compatible with 80C31 instructions
- Supports CIR for receive
- 2K bytes RAM for loading the program from external EEPROM
- 64 bytes RAM of uC
- Supports RTC with 64 bytes SRAM by 32.768KHz
- Supports 8 suits general purpose input / output
- Hardware I2C Slave Functions
- Used extend I2C EEPROM storage code
- Supports firmware power down /idle mode
- Powered by 3.3VCC and packaged in SSOP-16

# 3 Pin Configuration

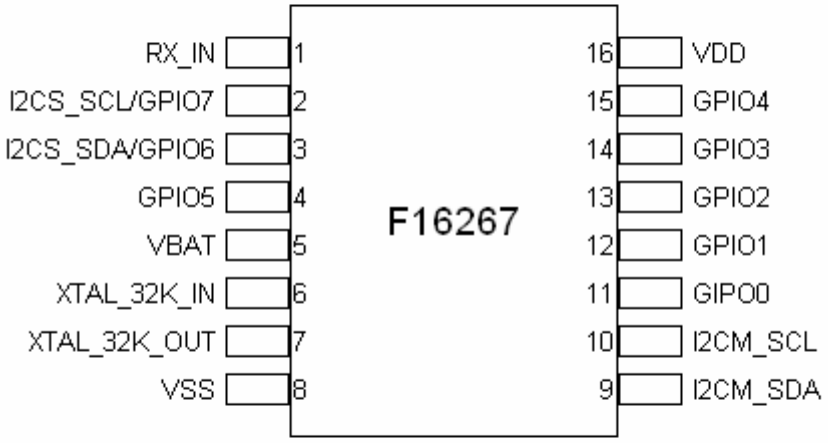



Figure1. F16267 pin configuration

# 4 Pin Description

P - Power pins

$IN_{st5V}$ - TTL level input pin with schmitt trigger

$I/OD_{12st5V}$ - TTL level bi-directional pin with schmitt trigger, Open-drain output with 12 mA sink capability, 5V tolerance

$I/O_{12st5v}$ - Output pin with 12mA sink/driving capability.5V tolerance

AIN - Input pin (Analog).

AOUT - Output pin (Analog).

## 4.1. Power Pin

| Pin No. | Pin Name | Type | Description |
|---|---|---|---|
| 5 | VBAT | P | Power source of RTC supplied from 3.3V battery |
| 8 | VSS | | Ground |
| 16 | VCC | | Power supply input 3.3V |

## 4.2. GPIO Pin

| Pin No. | Pin Name | Type | PWR | Description |
|---|---|---|---|---|
| 4 | GPIO5 | $I/O_{12st5v}$ | VDD | General purpose input/output bit 5 |
| 11 | GPIO0 | $I/O_{12st5v}$ | VDD | General purpose input/output bit 0 |
| 12 | GPIO1 | $I/O_{12st5v}$ | VDD | General purpose input/output bit 1 |
| 13 | GPIO2 | $I/O_{12st5v}$ | VDD | General purpose input/output bit 2 |
| 14 | GPIO3 | $I/O_{12st5v}$ | VDD | General purpose input/output bit 3 |
| 15 | GPIO4 | $I/O_{12st5v}$ | VDD | General purpose input/output bit 4 |

## 4.3. RTC Pin

| Pin No. | Pin Name | Type | PWR | Description |
|---|---|---|---|---|
| 6 | XTAL_32K_IN | AIN | VBAT | 32.768KHz clock input |
| 7 | XTAL_32K_IN | AIN | VBAT | 32.768KHz clock output |

### 4.4. I2C Interface Pin

| Pin No. | Pin Name | Type | PWR | Description |
|---|---|---|---|---|
| 2 | I2CS_SCL/GPIO7 | $I/OD_{12st5v}$ | VDD | I2C serial clock for slave function/ General purpose input output bit 7 |
| 3 | I2CS_SDA/GPIO6 | $I/OD_{12st5V}$ | VDD | I2C serial data for slave function/ General purpose input output bit 6 |
| 9 | I2CM_SDA | $I/OD_{12st5V}$ | VDD | I2C serial data for load external ROM function or other I2C salve device |
| 10 | I2CM_SCL | $I/OD_{12st5V}$ | VDD | I2C serial clock for load external ROM function or other I2C salve device |

### 4.5. IR Pin

| Pin No. | Pin Name | Type | PWR | Description |
|---|---|---|---|---|
| 1 | RX_IN | $IN_{st5V}$ | VDD | IR receiver input |

# 5 Electrical Characteristic

## 5.1 Absolute Maximum Ratings

| PARAMETER | RATING | UNIT |
|---|---|---|
| Power Supply Voltage | -0.5 to 5.5 | V |
| Input Voltage | -0.5 to VDD+0.5 | V |
| Operating Temperature | 0 to +70 | ° C |
| Storage Temperature | -55 to 150 | ° C |

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device

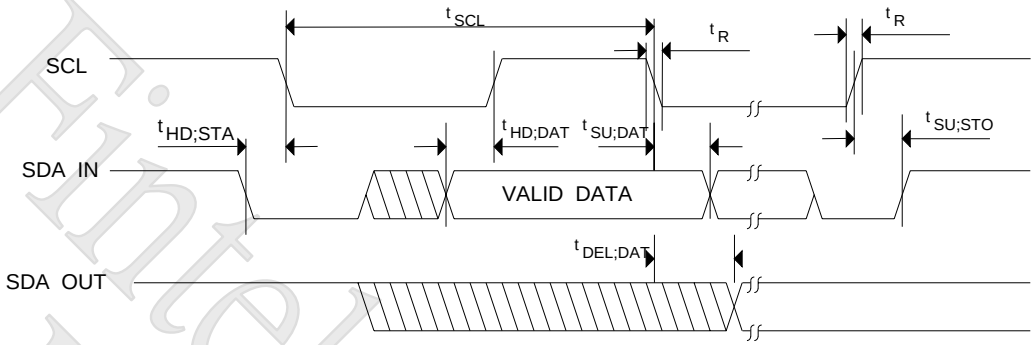
## 5.2 DC Characteristics

(Ta = 0° C to 70° C, VCC = 3.3V ± 10%, VSS = 0V)

| PARAMETER | SYM. | MIN. | TYP. | MAX. | UNIT | CONDITIONS |
|---|---|---|---|---|---|---|
| Operating Voltage | VDD | 3.0 | 3.3 | 3.6 | V | |
| Battery Voltage | VBAT | 2.4 | 3.3 | 3.6 | V | |
| Operating Current | ICC | | 35 | | mA | VCC=3.3V VBAT=3.3V |
| Idle State Current | ISTY | | 5 | | uA | VCC=3.3V VBAT=3.3V |
| Battery Current | IBAT | | 4 | | uA | VCC=3.3V VBAT=3.3V |
| **$I/OD_{12st5v}$ - TTL level and schmitt trigger bi-directional pin with 12 mA source-sink capability 5V tolerance** | | | | | | |
| Input Low Voltage | VIL | | | 0.8 | V | |
| Input High Voltage | VIH | 2.0 | | | V | |
| Hysteresis | | | 0.5 | | V | |
| Output Low Current | IOL | | +12 | | mA | VOL = 0.4V |
| Input High Leakage | ILIH | -1 | | +1 | μA | |
| Input Low Leakage | ILIL | -1 | | +1 | μA | |
| **$I/O_{12}$ – Output pin with12mA source-sink capability ,5V tolerance** | | | | | | |
| Input Low Voltage | VIL | | | 0.8 | V | VDD = 3.3 V |
| Input High Voltage | VIH | 2.0 | | | V | VDD = 3.3 V |
| Hysteresis | | | 0.5 | | V | |
| Output High Current | IOH | | 12 | | mA | VOH = 2.0 V |
| Input High Leakage | ILIH | -1 | | +1 | μA | |
| Input Low Leakage | ILIL | -1 | | +1 | μA | |
| **$IN_{ts\_5v}$ – TTL level input pin and schmitt trigger, 5V tolerance** | | | | | | |
| Input Low Voltage | VIL | | | 0.8 | V | |
| Input High Voltage | VIH | 2.0 | | | V | |
| Hysteresis | | | 0.5 | | V | |
| Input High Leakage | ILIH | | | +1 | μA | |

| | | | | | | |
|---|---|---|---|---|---|---|
| Input Low Leakage | ILIL | -1 | | | μA | |

### 5.3 AC Characteristics




Serial Bus Timing Diagram

Figure 2 SMBus timing diagram

**Serial Bus Timing**

| PARAMETER | SYMBOL | MIN | MAX | UNIT |
|---|---|---|---|---|
| SCL clock period | $t_{SCL}$ | 3 | | uS |
| Start condition hold time | $t_{HD;SDA}$ | 50 | | nS |
| Stop condition setup-up time | $t_{SU;STO}$ | 50 | | nS |
| DATA to SCL setup time | $t_{SU;DAT}$ | 50 | | nS |
| DATA to SCL hold time | $t_{HD;DAT}$ | 5 | | nS |
| DATA OUT to SCL delay time | $t_{DEL:DATA}$ | 200 | | ns |
| SCL and SDA rise time | $t_R$ | | 200 | nS |
| SCL and SDA fall time | $t_F$ | | 200 | nS |

# 6 Functional Description

## 6.1 CIR Function

The CIR is used in Consumer Remote Control equipment. It is programmable amplitude shift keyed (ASK) serial communication protocol. By adjusting frequency, baud rate divisors, and sensitivity ranges, the CIR register are able to support the popular protocols such as ITT, NEC, NOKIA, SHARP, SONY and PHILIPS RC5./RC6 Software driver programming can support new protocol. The CIR builds 8 bytes FIFO for data reception.

## 6.2 RTC Function

The F16267 provides a Real-Time-Clock with 64 bytes of RAM. The RTC provides a time-of-day clock in two data formats (Binary or BCD) and two hour formats (24 HR or AM/PM). The clock/calendar provides seconds, minutes, hours, day, date, month, year, and century information. It also provides a special time update and corrections for leap years. It has one alarm and three programmable interrupts.

The F16267 is designed with either a crystal oscillator or external clock. The F16267 incorporates a built-in crystal oscillator. To make the oscillator work, a crystal must be connected across XTAL_32K_IN pin and XTAL_32K_OUT pin. In addition, an external clock should be connected to XTAL_32K_IN pin and XTAL_32K_OUT pin should be unconnected. Recommend to be connected with 32.768KHz input.

## 6.3 I2C Function

The F16267 provides two I2C serial ports for transmission. The pins, I2C_SDA_M and I2C_SDA_M, are connected to external serial EEPROM for different customized requirement to transmit or receive I2C salve device data. The pins, I2C_SDA_S and I2C_SDA_S, are for I2C slave function. The I2C slave function support byte read, byte write, continuous read (256 bytes), and continuous write (256 bytes) mode and it defaults to address at 8'h9C and its address can be programmed by the register. The I2C slave function supports real-time read or write internal data of RTC/CIR/GPIO.

## 6.4 GPIO Function

The F16267 provides 8 suits general purpose input/output. This function provides drives or sinks and input detects capability. The GPIO6 and GPIO7 are the multi-function pins with I2C_SDA_S and I2C_SCL_S. They can be switched by the register.

### 6.5 Watchdog Timer Function

The F16267 contains a watchdog timer which will reset the IC when it counts down the set value in Register 0x00FB ~ 0x00FD (20 bits) to zero. The watchdog timer is based on 12MHz clock.

### 6.6 MCU Function

The F16267 is an 8031 based micro processor for general purpose system management. The instruction set of the F16267 is fully compatible with the standard 8031, but not provides timer1/UART function and multiplication/division operation. The F16267 utilizes the external 32.768KHz crystal to oscillate 12Mhz internally instead of the external 12MHz crystal. The rest of the functions are as below description.

The F16267 separates the memory into two separate sections, the Program Memory and the Data Memory. The Program Memory is used to store the instruction op-codes, while the Data Memory is used to store data or for memory mapped devices.

#### 6.6.1 Program Memory

The Program Memory on the F16267 can be up to 2Kbytes long. All instructions are fetched for execution from this memory area. The MOVC instruction can also access this memory region.

#### 6.6.2 Data Memory

The F16267 can access internal device function (RTC/CIR/GPO) of external Data Memory mapping. This memory region is accessed by the MOVX instructions. And internal device is mapping in data memory region. In addition, the F16267 has the 128 bytes of on-chip Scratchpad RAM. This can be accessed either by direct addressing or by indirect addressing. There are also some Special Function Registers (SFRs), which can only be accessed by direct addressing. Since the Scratchpad RAM is only 128 bytes.

Table 1 3 source interrupt information

| INTERRUPT SOURCE | VECTOR ADDRESS | ENABLE REQUIRED SETTINGS | INTERRUPT TYPE EDGE/LEVEL |
|---|---|---|---|
| External Interrupt 0 | 03H | IE.0 | TCON.0 |
| Timer 0 Interrupt | 0bH | IE.1 | TCON.5 |
| External Interrupt 1 | 13H | IE.2 | TCON.2 |

Table 2 2 source interrupt information

| INTERRUPT SOURCE | VECTOR ADDRESS | Function |
|---|---|---|
| External Interrupt 0 | 03H | CIR |
| External Interrupt 1 | 13H | RTC/I2C Master/GPIO |

### 6.6.3 Power Saving Mode

**Normal State:**

All internal devices are working, and the internal clock is on

**Idle Mode:**

When set SFR index 8'h87 bit 0=1, the F16267 goes into idle mode, and the clock will stop. If the internal devices like GPIO, RTC, and CIR are asserted interrupt, the micro processor will resume the normal mode.

**Power Down Mode:**

When set SFR index 8'h87 bit 1=1, the F16267 goes into power down mode, and the clock will stop. If the micro processor wants to be resumed the normal mode, power off or software reset (Register 16'h0005 bit 0) is necessary.

# 7 Register Description (I2C Address = 0x9C)

## 7.1 Data Memory Structure and Special Function Register (SFR) Structure

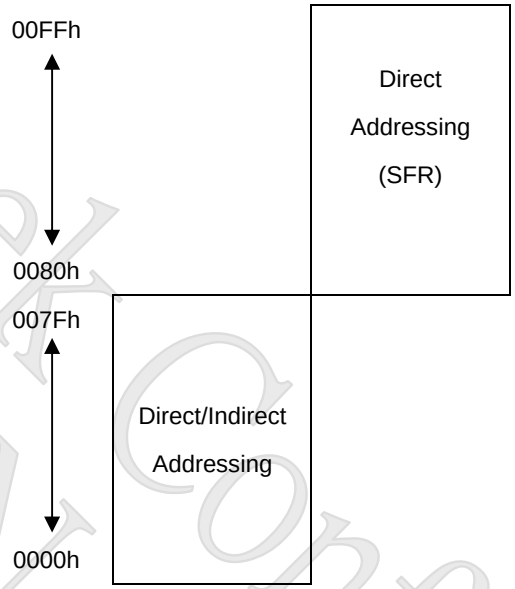



Figure 3 Data memory structure

Table 3 F16267 SFR memory allocation

| SFR | | | | | | | | | Address |
|---|---|---|---|---|---|---|---|---|---|
| WDT CLB | CLB7 | CLB6 | CLB5 | CLB4 | CLB3 | CLB2 | CLB1 | CLB0 | FDh |
| WDT MLB | MLB7 | MLB6 | MLB5 | MLB4 | MLB3 | MLB2 | MLB1 | MLB0 | FCh |
| WDTHLB | HLB7 | HLB6 | HLB5 | HLB4 | HLB3 | HLB2 | HLB1 | HLB0 | FBh |
| WDT EN | EN | | | | | | | STATUS | FAh |
| ACC | ACC7 | ACC6 | ACC5 | ACC4 | ACC3 | ACC2 | ACC1 | ACC0 | E0h |
| PSW | CY | AC | F0 | RS1 | RS0 | OV | | P | D0h |
| IP | | | | | | | PT0 | PX0 | B8h |
| P3 | P37 | P36 | P35 | P34 | P33 | P32 | P31 | P30 | B0h |
| IE | EA | | | | | | ET0 | EX0 | A8h |
| P2 | P27 | P26 | P25 | P24 | P23 | P22 | P21 | P20 | A0h |
| P1 | P17 | P16 | P15 | P14 | P13 | P12 | P11 | P10 | 90h |
| TH0 | | | | | | | | | 8Bh |
| TL0 | | | | | | | | | 8Ah |
| TMOD | GATE | C/T | M1 | M0 | GATE | C/T | M1 | M0 | 89h |
| TCON | | | TF0 | TR0 | IE1 | IT1 | IE0 | IT0 | 88h |
| PCON | SMOD | | | | GF1 | GF0 | PD | IDL | 87h |
| DPH | | | | | | | | | 83h |
| DPL | | | | | | | | | 82h |
| SP | | | | | | | | | 81h |
| P0 | P07 | P06 | P05 | P04 | P03 | P02 | P01 | P00 | 80h |

### 7.2 Reserved – Index 0000h~0007h

| Bit | Name | R/W | Default | Description |
|---|---|---|---|---|
| 7-0 | Reserved | - | 0 | Reserved |

### 7.3 Reserved – Index 0008h

| Bit | Name | R/W | Default | Description |
|---|---|---|---|---|
| 7-0 | Reserved | R | - | Reserved |

### 7.4 Reserved – Index 0009h

| Bit | Name | R/W | Default | Description |
|---|---|---|---|---|
| 7-0 | Reserved | R | - | Reserved |

### 7.5 Reserved – Index 000Ah

| Bit | Name | R/W | Default | Description |
|---|---|---|---|---|

| | | | | |
|---|---|---|---|---|
| 7-0 | Reserved | R | 34h | Reserved |

### 7.6 Reserved – Index 000Bh

| Bit | Name | R/W | Default | Description |
|---|---|---|---|---|
| 7-0 | Reserved | R | 19h | Reserved |

### 7.7 Reserved – Index 000Ch

| Bit | Name | R/W | Default | Description |
|---|---|---|---|---|
| 7-0 | Reserved | R | 20h | Reserved |

### 7.8 Reserved – Index 000Dh

| Bit | Name | R/W | Default | Description |
|---|---|---|---|---|
| 7-0 | Reserved | R | 07h | Reserved |

### 7.9 CIR – CIR FIFO Register – Index 0010h

| Bit | Name | R/W | Default | Description |
|---|---|---|---|---|
| 7-0 | CIR_FIFO | R | 00h | Receiver Buffer Register is read only. When the CIR pulse train has been detected and passed by the internal signal filter, the data sampled and shifted into shifter register will be written into Receiver Buffer Register |

### 7.10 CIR – Interrupt Enable Register – Index 0011h

| Bit | Name | R/W | Default | Description |
|---|---|---|---|---|
| 7 | Interrupt_EN | R/W | 0 | Write 1 to enable CIR interrupt. |
| 6-0 | Reserved | - | 0 | Reserved |

### 7.11 CIR – Interrupt Status Register – Index 0012h

| Bit | Name | R/W | Default | Description |
|---|---|---|---|---|
| 7-4 | FIFO_CNT | R | 0 | This nibble indicates that how many byte RX data will be read. |
| 3 | FIFO_RST | R/W | 0 | Write 1 to reset CIR FIFO |
| 2 | Reserved | R/W | 0 | Reserved |
| 1 | Data_Lost | R | 0 | This bit indicates FIFO data lost, and write 1 to clear |
| 0 | Ready | R | 0 | This bit indicates RX data ready, and write 1 to clear |

### 7.12 CIR – Baud Rate Low Byte Register – Index 0013h

| Bit | Name | R/W | Default | Description |
|---|---|---|---|---|
| 7-0 | Baud_Lo | R/W | A5h | The registers of BLL are baud rate divisor latch. |

### 7.13 CIR – Baud Rate High Byte Register – Index 0014h

| Bit | Name | R/W | Default | Description |
|---|---|---|---|---|
| 7-0 | Baud_Hi | R/W | 01h | The registers of BHL are baud rate divisor latch. |

### 7.14 CIR – Waveform Logic 1 Data Register – Index 0015h

| Bit | Name | R/W | Default | Description |
|---|---|---|---|---|
| 7-0 | WaveH | R/W | 80h | The registers of WaveH indicate RX logic 1 waveform |

### 7.15 CIR – Waveform Logic 0 Data Register – Index 0016h

| Bit | Name | R/W | Default | Description |
|---|---|---|---|---|
| 7-0 | WaveL | R/W | 02h | The registers of WaveL indicate RX logic 0 count number |

### 7.16 CIR – Waveform Logic 1 Count Register – Index 0017h

| Bit | Name | R/W | Default | Description |
|---|---|---|---|---|
| 7-0 | WaveH_Count | R/W | 80h | The registers of WaveH_Count indicate RX logic 1 count number |

### 7.17 CIR – Waveform Logic 0 Count Register – Index 0018h

| Bit | Name | R/W | Default | Description |
|---|---|---|---|---|
| 7-0 | WaveL_Count | R/W | 02h | The registers of WaveL_Count indicate RX logic 0 count number |

### 7.18 CIR – Rx Protocol Register – Index 0019h

| Bit | Name | R/W | Default | Description |
|---|---|---|---|---|
| 7 | Low_Frequency | R/W | 1 | Write 1 to indicate RX carry frequency from 20k to 100k, and write 0 to indicate RX carry frequency from 400k to 500k. |
| 6-5 | Reserved | - | 00 | Reserved |
| 4 | RXINV | R/W | 1 | Write 1 to indicate invert RX input, or to indicate by pass RX. |
| 3 | Bypass | R/W | 1 | Write 1 to indicate RX input is demodulation , or to indicate RX is un-demodulation |
| 2-0 | Protocol | R/W | 001 | 000 : ITT<br>001 : NEC<br>010 : NOKIA<br>011 : Sharp<br>100 : SONY<br>101 : Philips RC5 |

### 7.19 GPIO – GPIO Control Register – Index 0020h

| Bit | Name | R/W | Default | Description |
|---|---|---|---|---|

| | | | | |
|---|---|---|---|---|
| 7-0 | GPIO_CNTL | R/W | 00h | Every bit indicates the corresponding pad of GPIO capability<br>0 : Open drain, 1: Drive/sink capability |

### 7.20 GPIO – GPIO CAP Register – Index 0021h

| Bit | Name | R/W | Default | Description |
|---|---|---|---|---|
| 7-0 | GPO_CAP | R/W | 00h | Every bit indicates the corresponding pad of GPIO direction<br>0 : Input ,1: Output |

### 7.21 GPIO – GPIO Multi-function Register – Index 0022h

| Bit | Name | R/W | Default | Description |
|---|---|---|---|---|
| 7 | Int_Global_EN | R/W | 0 | Set to 1 to enable GPIO global interrupt enable ,or to disable interrupt. |
| 6-1 | Reserved | - | - | Reserved |
| 0 | GPIO/I2C | R/W | 00h | 0 : I2C function 1 : GPIO function |

### 7.22 GPIO – GPIO Data Output Register – Index 0023h

| Bit | Name | R/W | Default | Description |
|---|---|---|---|---|
| 7-0 | GPIO_PDOUT | R/W | FFh | GPIO data output for PAD. |

### 7.23 GPIO – GPIO Input Interrupt Register – Index 0024h

| Bit | Name | R/W | Default | Description |
|---|---|---|---|---|
| 7-0 | GPIO_INT_EN | R/W | 00h | Every bit indicates the corresponding input pad of GPIO interrupt enable.<br>0: Disable, 1: Enable |

### 7.24 GPIO – GPIO Status Register – Index 0025h

| Bit | Name | R/W | Default | Description |
|---|---|---|---|---|
| 7-0 | GPIO_Status | R/W | 00h | Every bit indicates the corresponding input pad of GPIO status Write 1 to clear. |

### 7.25 GPIO – GPIO Level Register – Index 002Fh

| Bit | Name | R/W | Default | Description |
|---|---|---|---|---|
| 7-0 | GPIO_Level | R/W | 00h | Every bit indicates the corresponding input GPIO pad level. |

### 7.26 I2C Master – I2C Interrupt Enable Register – Index 0030h

| Bit | Name | R/W | Default | Description |
|---|---|---|---|---|
| 7 | I2C_Global_INT_EN | R/W | 0 | This bit indicates global interrupt enable |
| 6-2 | Reserved | - | - | Reserved |
| 1 | I2C_Read_INT_EN | R/W | 0 | This bit indicates I2C read finish interrupt enable |

| | | | | |
|---|---|---|---|---|
| 0 | I2C_Write_INT_EN | R/W | 0 | This bit indicates I2C write finish interrupt enable. |

### 7.27 I2C Master – I2C Status Register – Index 0031h

| Bit | Name | R/W | Default | Description |
|---|---|---|---|---|
| 7 | I2C_NAK | R/W | 0 | This bit indicates NAK response from I2C device, and be written 1 to clear. |
| 6-4 | Reserved | - | - | Reserved |
| 3 | Read_Start | R/W | 0 | Write 1 to start I2C read function and be cleared to 0 when I2C read function finish. |
| 2 | Read_Status | R/W | 0 | This bit indicates I2C read finish status, and writes 1 to clear |
| 1 | Write_Start | R/W | 0 | Write 1 to start I2C write function and be cleared to 0 when I2C write function finish. |
| 0 | Write_Status | R/W | 0 | This bit indicates I2C write finish status, and writes 1 to clear |

### 7.28 I2C Master – I2C Device Register – Index 0032h

| Bit | Name | R/W | Default | Description |
|---|---|---|---|---|
| 7-0 | Device_Data | R/W | 00h | Write this byte to indicate I2C start transmit this byte data to device. |

### 7.29 I2C Master – I2C Read Register – Index 0033h

| Bit | Name | R/W | Default | Description |
|---|---|---|---|---|
| 7-0 | Read_Data | R | 00h | This byte indicates receive data from I2C device. |

### 7.30 I2C Master – I2C Index ID Register – Index 0034h

| Bit | Name | R/W | Default | Description |
|---|---|---|---|---|
| 7 | Reserved | - | - | Reserved |
| 6-4 | Device_New_ID | | 0 | This nibble indicates slave address the A0A1A2 of protocol. |
| 3-0 | Device_ID | R/W | 0 | This nibble indicates slave address the highest nibble of protocol. |

### 7.31 I2C Master – I2C Address – Index 0035h

| Bit | Name | R/W | Default | Description |
|---|---|---|---|---|
| 7 | I2C_Address | R | 00h | This byte indicates address of I2C protocol |

### 7.32 RTC – Second Register – Index 0080h

| Bit | Name | R/W | Default | Description |
|---|---|---|---|---|
| 7 | Reserved | - | 0 | Reserved |
| 6-0 | Second | R/W | 0 | To write this bit, “SET” bit (CR8C[7]) must be set to 1. |

### 7.33 RTC – Minute Register – Index 0081h

| Bit | Name | R/W | Default | Description |
|---|---|---|---|---|
| 7 | Reserved | - | 0 | Reserved |
| 6-0 | Minute | R/W | 0 | To write this MIN, “SET” bit (CR8C[7]) must be set to 1. |

### 7.34 RTC – Hour Register – Index 0082h

| Bit | Name | R/W | Default | Description |
|---|---|---|---|---|
| 7 | PM_Flag | R/W | 0 | This bit is used to indicate that hour is at AM or PM. It only makes sense when “M24” bit (CR8C[1]) is set to 0. To write this bit, “SET” bit (CR8C[7]) must be set to 1. 0: AM, 1: PM |
| 6 | Reserved | - | 0 | Reserved |
| 6-0 | Hour | R/W | 12h | To write this bit, “SET” bit (CR8C[7]) must be set to 1. |

### 7.35 RTC – Day of Week Register – Index 0083h

| Bit | Name | R/W | Default | Description |
|---|---|---|---|---|
| 7-3 | Reserved | - | 0 | Reserved |
| 2-0 | Week | R/W | 1 | To write this bit, “SET” bit (CR8C[7]) must be set to 1.<br>001: Sunday<br>010: Monday<br>011: Tuesday<br>101: Thursday<br>110: Friday<br>111: Saturday |

### 7.36 RTC – Date of Month Register – Index 0084h

| Bit | Name | R/W | Default | Description |
|---|---|---|---|---|
| 6-4 | Reserved | - | 0 | Reserved |
| 5-0 | Date | R/W | 1 | To write this bit, “SET” bit (CR8C[7]) must be set to 1. |

### 7.37 RTC – Month Register – Index 0085h

| Bit | Name | R/W | Default | Description |
|---|---|---|---|---|
| 6-4 | Reserved | - | 0 | Reserved |
| 5-0 | Month | R/W | 1 | To write this bit, “SET” bit (CR8C[7]) must be set to 1. |

### 7.38 RTC – Year Register – Index 0086h

| Bit | Name | R/W | Default | Description |
|---|---|---|---|---|
| 6-4 | Reserved | - | 0 | Reserved |

| | | | | |
|---|---|---|---|---|
| 5-0 | Year | R/W | 07h | To write this bit, “SET” bit (CR8C[7]) must be set to 1. |

### 7.39 Alarm – Second Alarm Register – Index 0087h

| Bit | Name | R/W | Default | Description |
|---|---|---|---|---|
| 7 | SEC_ALARM_EN | R/W | 0 | Seconds Alarm Enable. To enable second alarm function to compare SEC_ALARM data set in [6:0] with second, this bit must be set to 1. If this bit is not set to 1, it means that second alarm is not concerned. |
| 6-0 | SEC_ALARM | R/W | 00h | Seconds Alarm data. |

### 7.40 Alarm – Minute Alarm Register – Index 0088h

| Bit | Name | R/W | Default | Description |
|---|---|---|---|---|
| 7 | MIN_ALARM_EN | R/W | 0 | Minutes Alarm Enable. To enable minute alarm function to compare MIN_ALARM data set in [6:0] with Minute, this bit must be set to 1. If this bit is not set to 1, it means that minute alarm is not concerned. |
| 6-0 | MIN_ALARM | R/W | 00h | Minutes Alarm data. |

### 7.41 Alarm – Hour Alarm Register – Index 0089h

| Bit | Name | R/W | Default | Description |
|---|---|---|---|---|
| 7 | HRS_ALARM_EN | R/W | 0 | Hour Alarm Enable. To enable hour alarm function to compare PM_ALARM data set in bit 6 and HRS_ALARM data set in [5:0] with PM/HRS_FLAG, this bit must be set to 1. If this bit is not set to 1, it means that hour alarm is not concerned. |
| 6 | PM_ALARM | R/W | 0 | PM Flag Alarm data |
| 5-0 | HRS_ALARM | R/W | 00h | Hours Alarm data |

### 7.42 Alarm – Date of Month Alarm Register – Index 008Ah

| Bit | Name | R/W | Default | Description |
|---|---|---|---|---|
| 7 | DATE_ALARM_EN | R/W | 0 | Date Alarm Enable. To enable date alarm function to compare DATE_ALARM data set in [5:0], this bit must be set to 1. If this bit is not set to 1, it means that date alarm is not concerned. |
| 6 | Reserved | R | 0 | Reserved |
| 5-0 | DATE_ALARM | R/W | 00h | Date of Month Alarm data |

### 7.43 Alarm – Month Alarm Register – Index 008Bh

| Bit | Name | R/W | Default | Description |
|---|---|---|---|---|
| 7 | MTH_ALARM_EN | R/W | 0 | Month Alarm Enable. To enable month alarm function to compare MTH_ALARM data set in [4:0], this bit must be set to 1. If this bit is not set to 1, it means that month alarm is not concerned. |
| 6-5 | Reserved | R | 0 | Reserved |

| | | | | |
|---|---|---|---|---|
| 4-0 | MTH_ALARM | R/W | 00h | Month Alarm data |

### 7.44 Control Register– Control Register 1 – Index 008Ch

| Bit | Name | R/W | Default | Description |
|---|---|---|---|---|
| 7 | SET | R/W | 0 | Set Calendar Registers (SET)<br>This bit must be set to 1 to while writing calendar registers. When this bit is set, the calendar update process will be stop. |
| 6 | PIE | R/W | 0 | Periodic Interrupt Enable (PIE)<br>The bit is set to 1 to enable the generation of interrupt by PF (CR8E[6]). |
| 5 | AIE | R/W | 0 | Alarm Interrupt Enable (AIE)<br>This bit is set to 1 to enable the generation of interrupt by UF (CR8E[5]). |
| 4 | UIE | R/W | 0 | Update-Ended Interrupt Enable (UIE)<br>This bit is set to 1 to enable the generation of interrupt by UF (CR8E[4]) |
| 3 | Reserved | R | 0 | Reserved |
| 2 | DM | R/W | 0 | Data Mode (DM)<br>0: Binary Coded Decimal Mode (BCD mode)<br>1: Binary Mode |
| 1 | M24 | R/W | 0 | 24/12 Hours Mode (M24)<br>0: AM/PM 12 Hours Mode<br>1: 24 Hours Mode |
| 0 | DSE | R/W | 0 | Daylight Saving Enable (DSE)<br>0: Disable Special Updates<br>1: Enable Special Updates:<br>(a) The first Sunday of April, the time increases from AM 01:59:59 to AM 03:00:00.<br>(b) The last Sunday of October, the time decreases from AM 01:59:59 to AM 01:00:00 |

### 7.45 Control Register– Control Register 1 – Index 008Dh

| Bit | Name | R/W | Default | Description |
|---|---|---|---|---|
| 7 | UIP | R | 0 | Update Cycle In Progress (UIP). UIP is cleared in the end of an update cycle or when “SET” (CR8C[7]) is 1. |
| 6-4 | Reserved | R/W | 010b | Reserved |

| | | | | |
|---|---|---|---|---|
| 3-0 | PIR | R/W | 0000b | Periodic Interrupt Rate (PIR)<br>0000: NONE<br>0001: 16 kHz<br>0010: 8 kHz<br>0011: 4 kHz<br>0100: 2 kHz<br>0101: 1 kHz<br>0110: 512 Hz<br>0111: 256 Hz<br>1000: 128 Hz<br>1001: 64 Hz<br>1010: 32 Hz<br>1011: 16 Hz<br>1100: 8 Hz<br>1101: 4 Hz<br>1110: 2 Hz<br>1111: 1 Hz |

### 7.46 Control Register– Status Register – Index 008Eh

| Bit | Name | R/W | Default | Description |
|---|---|---|---|---|
| 7 | RTC_INT_N | R | 1 | RTC Interrupt Request Flag (RTC_INT_N). The interrupt request flag is set to 0 if one of the following cases are true:<br>PF*PIE = “1”<br>AF*AIE = “1”<br>UF*UIE = “1” |
| 6 | PF | R | 0 | Periodic Interrupt Flag (PF)<br>This bit is set to 1 when a rising edge is detected on the selected PIR clock. PF is set to 1 regardless of the state of PIE bit. This bit is cleared after CR8E is read. |
| 5 | AF | R | 0 | Alarm Interrupt Flag (AF)<br>This bit is set to 1 when the current time has reached the alarm time. AF is set to 1 regardless of the state of AIE bit. This bit is cleared after CR8E is read. |
| 4 | UF | R | 0 | Update-Ended Interrupt Flag (UF)<br>This bit is set to 1 after the end of each update cycle. UF is set to 1 regardless of the state of UIE bit. This bit is cleared after CR8E is read. |
| 3-0 | Reserved | R | 0 | Reserved |

### 7.47 Reserved – Index 008Fh

| Bit | Name | R/W | Default | Description |
|---|---|---|---|---|
| 7-0 | Reserved | R | 80 | Reserved |

### 7.48 RAM Data Register –Index 0090h~00CFh (Total 64 Bytes)

### 7.49 Watchdog Timer Enable Register – Index 00FAh

| Bit | Name | R/W | Default | Description |
|---|---|---|---|---|
| 7 | Watchdog_EN | R/W | 0 | Set to 1 to enable watch dog timer and start count down. |
| | Reserved | R | 0 | |
| 4-0 | Watchdog_Status | R/W | 0 | Set to 1, when watch dog timer count down to 0. Write 1 to clear. |

### 7.50 Watchdog Timer High Nibble Register – Index 00FBh

| Bit | Name | R/W | Default | Description |
|---|---|---|---|---|
| 7-4 | Reserved | - | 0 | Reserved |
| 3-0 | Time_High_Nibble | R/W | 0 | This register sets watch dog time[19:16] |

### 7.51 Watchdog Timer Middle Byte Register – Index 00FCh

| Bit | Name | R/W | Default | Description |
|---|---|---|---|---|
| 7-0 | Time_Middle_Byte | R/W | 0 | This register sets watch dog time[15:8] |

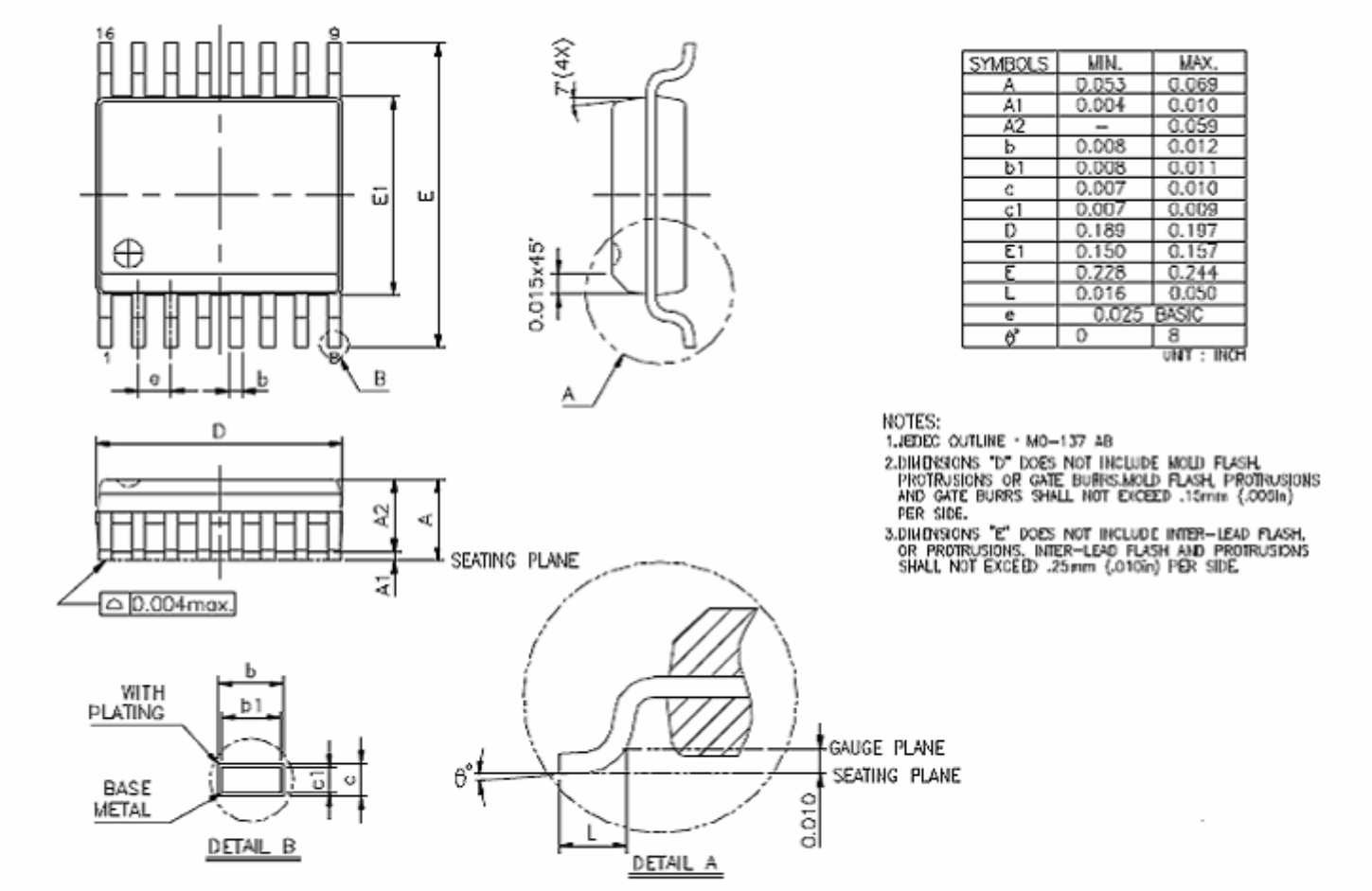
### 7.52 Watchdog Timer Low Byte Register – Index 00FDh

| Bit | Name | R/W | Default | Description |
|---|---|---|---|---|
| 7-0 | Time_Low_Byte | R/W | 0 | This register sets watch dog time[7:0] |

# 8 Ordering Information

| Part Number | Package Type | Production Flow |
|---|---|---|
| F16267R | 16-SSOP (Green Package) | Commercial, 0°C to +70°C |

# 9 Package Dimensions (16-SSOP)




| SYMBOLS | MIN. | MAX. |
|---|---|---|
| A | 0.053 | 0.069 |
| A1 | 0.004 | 0.010 |
| A2 | – | 0.059 |
| b | 0.008 | 0.012 |
| b1 | 0.008 | 0.011 |
| c | 0.007 | 0.010 |
| c1 | 0.007 | 0.009 |
| D | 0.189 | 0.197 |
| E1 | 0.150 | 0.157 |
| E | 0.228 | 0.244 |
| L | 0.016 | 0.050 |
| e | 0.025 BASIC | |
| θ° | 0 | 8 |

UNIT : INCH

NOTES:
1. JEDEC OUTLINE : MO-137 AB
2. DIMENSIONS "D" DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.MOLD FLASH, PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED .15mm (.006in) PER SIDE.
3. DIMENSIONS "E" DOES NOT INCLUDE INTER-LEAD FLASH, OR PROTRUSIONS. INTER-LEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED .25mm (.010in) PER SIDE.

Figure 4. 16 Pin SSOP Package Diagram

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# 10 Application Circuit

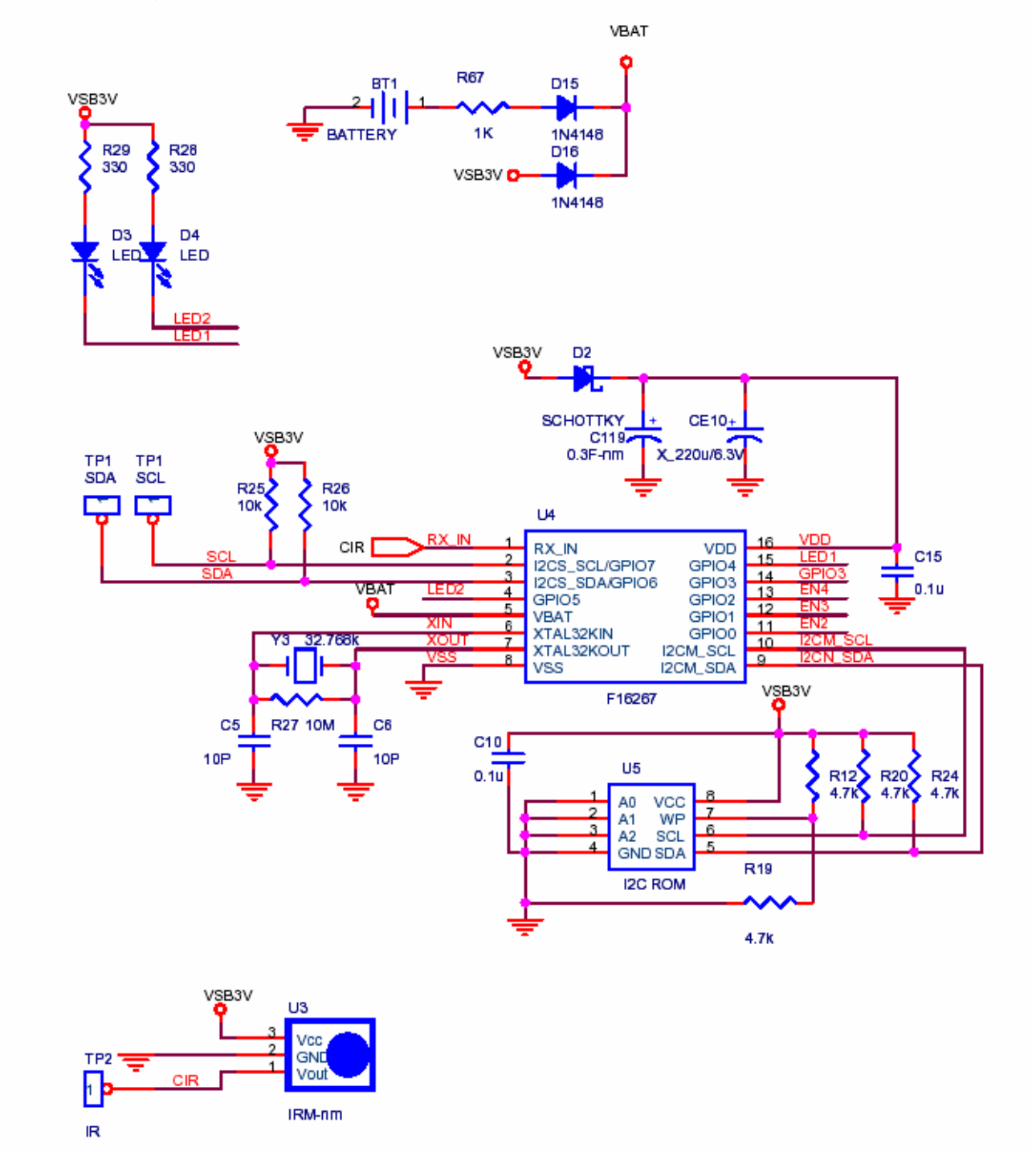


Figure 5. F16267R Application Circuit