

## IR11672AS ADVANCED SMART RECTIFIER™ CONTROL IC

### Features

- Secondary side high speed SR controller
- DCM, CrCM flyback and Resonant half-bridge topologies
- 200V proprietary IC technology
- Max 500KHz switching frequency
- Anti-bounce logic and UVLO protection
- 7A peak turn off drive current
- Micropower start-up & ultra low quiescent current
- 10.7V gate drive clamp
- 50ns turn-off propagation delay
- Vcc range from 11.3V to 20V
- Direct sensing of MOSFET drain voltage
- Enable function synchronized with MOSFET VDS transition
- Cycle by Cycle MOT Check Circuit prevents multiple false trigger GATE pulses
- Lead-free
- Compatible with 0.3W Standby, Energy Star, CECP, etc.

### Typical Applications

- LCD & PDP TV, Telecom SMPS, AC-DC adapters, ATX SMPS, Server SMPS

### Product Summary

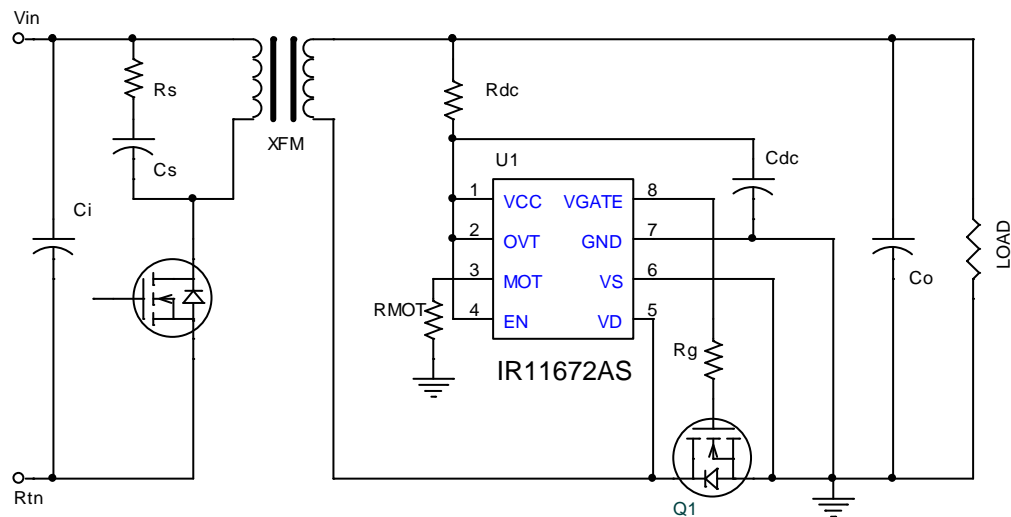
Topology	Flyback, Resonant Half-bridge
VD	200V
V <sub>OUT</sub>	10.7V
I <sub>o+</sub> & I <sub>o-</sub> (typical)	+2A & -7A
Turn on Propagation Delay	60ns (typical)
Turn off Propagation Delay	50ns (typical)

### Package Options



8-Lead SOIC

### Typical Connection Diagram



<b>Table of Contents</b>	<b>Page</b>
Description	3
Qualification Information	4
Absolute Maximum Ratings	5
Electrical Characteristics	6
Functional Block Diagram	8
Input/Output Pin Equivalent Circuit Diagram	9
Lead Definitions	10
Lead Assignments	10
Application Information and Additional Details	12
Package Details	22
Tape and Reel Details	23
Part Marking Information	24
Ordering Information	25

**Description**

IR11672A is a smart secondary-side driver IC designed to drive N-Channel power MOSFETs used as synchronous rectifiers in isolated Flyback and resonant half-bridge converters. The IC can control one or more paralleled N-MOSFETs to emulate the behavior of Schottky diode rectifiers. The drain to source voltage is sensed differentially to determine the polarity of the current and turn the power switch on and off in proximity of the zero current transition. The cycle-by-cycle MOT protection circuit can automatically detect no load condition and turn off gate driver output to avoid negative current flowing through the MOSFETs. Ruggedness and noise immunity are accomplished using an advanced blanking scheme and double-pulse suppression which allow reliable operation in all operating modes.

**Qualification Information<sup>†</sup>**

Qualification Level		Industrial <sup>††</sup>
		Comments: This family of ICs has passed JEDEC's Industrial qualification. IR's Consumer qualification level is granted by extension of the higher Industrial level.
Moisture Sensitivity Level		MSL2 <sup>†††</sup> 260°C (per IPC/JEDEC J-STD-020)
ESD	Machine Model	Class B (per JEDEC standard JESD22-A115)
	Human Body Model	Class 2 (per EIA/JEDEC standard EIA/JESD22-A114)
IC Latch-Up Test		Class I, Level A (per JESD78)
RoHS Compliant		Yes

† Qualification standards can be found at International Rectifier's web site <http://www.irf.com/>

†† Higher qualification ratings may be available should the user have such requirements. Please contact your International Rectifier sales representative for further information.

††† Higher MSL ratings may be available for the specific package types listed here. Please contact your International Rectifier sales representative for further information.

**Absolute Maximum Ratings**

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM, all currents are defined positive into any lead. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

Parameters	Symbol	Min.	Max.	Units	Remarks
Supply Voltage	$V_{CC}$	-0.3	20	V	
Enable Voltage	$V_{EN}$	-0.3	20	V	
Cont. Drain Sense Voltage	$V_D$	-3	200	V	
Pulse Drain Sense Voltage	$V_D$	-5	200	V	
Source Sense Voltage	$V_S$	-3	20	V	
Gate Voltage	$V_{GATE}$	-0.3	20	V	$V_{CC}=20V$ , Gate off
Operating Junction Temperature	$T_J$	-40	150	°C	
Storage Temperature	$T_S$	-55	150	°C	
Thermal Resistance	$R_{\theta JA}$		128	°C/W	SOIC-8
Package Power Dissipation	$P_D$		970	mW	SOIC-8, $T_{AMB}=25^\circ C$
Switching Frequency	fsw		500	kHz	

**Recommended Operating Conditions**

For proper operation the device should be used within the recommended conditions.

Symbol	Definition	Min.	Max.	Units
$V_{CC}$	Supply voltage	11.4	18	V
$V_D$	Drain Sense Voltage	-3	200	
$T_J$	Junction Temperature	-25	125	°C
Fsw	Switching Frequency	---	500	kHz

**Recommended Component Values**

Symbol	Component	Min.	Max.	Units
$R_{MOT}$	MOT pin resistor value	5	75	kΩ

### Electrical Characteristics

V<sub>CC</sub>=15V and T<sub>A</sub> = 25°C unless otherwise specified. The output volt age and current (V<sub>O</sub> and I<sub>O</sub>) parameters are referenced to GND (pin7).

#### Supply Section

Parameters	Symbol	Min.	Typ.	Max.	Units	Remarks
Supply Voltage Operating Range	V <sub>CC</sub>	11.4		18	V	GBD
V <sub>CC</sub> Turn On Threshold	V <sub>CC ON</sub>	9.8	10.55	11.3	V	
V <sub>CC</sub> Turn Off Threshold (Under Voltage Lock Out)	V <sub>CC UVLO</sub>	8.4	9	9.7	V	
V <sub>CC</sub> Turn On/Off Hysteresis	V <sub>CC HYST</sub>		1.55		V	
Operating Current	I <sub>CC</sub>		8.5	10	mA	C <sub>LOAD</sub> =1nF, f <sub>SW</sub> =400kHz
			50	65	mA	C <sub>LOAD</sub> =10nF, f <sub>SW</sub> =400kHz
Quiescent Current	I <sub>QCC</sub>		1.8	2.2	mA	
Start-up Current	I <sub>CC START</sub>		100	200	μA	V <sub>CC</sub> =V <sub>CC ON</sub> - 0.1V
Sleep Current	I <sub>SLEEP</sub>		150	200	μA	V <sub>EN</sub> =0V, V <sub>CC</sub> =15V
Enable Voltage High	V <sub>ENHI</sub>	2.15	2.70	3.2	V	
Enable Voltage Low	V <sub>ENLO</sub>	1.2	1.6	2.0	V	
Enable Pull-up Resistance	R <sub>EN</sub>		1.5		MΩ	GBD

#### Comparator Section

Parameters	Symbol	Min.	Typ.	Max.	Units	Remarks
Turn-off Threshold	V <sub>TH1</sub>	-7	-3.5	0	mV	OVT = 0V, V <sub>S</sub> =0V
		-14	-9.5	-6		OVT floating, V <sub>S</sub> =0V
		-22	-18	-14		OVT = V <sub>CC</sub> , V <sub>S</sub> =0V
Turn-on Threshold	V <sub>TH2</sub>	-150		-50	mV	
Hysteresis	V <sub>HYST</sub>		55		mV	
Input Bias Current	I <sub>BIAS1</sub>		1	7.5	μA	V <sub>D</sub> = -50mV
Input Bias Current	I <sub>BIAS2</sub>		30	100	μA	V <sub>D</sub> = 200V
Comparator Input Offset	V <sub>OFFSET</sub>			2	mV	GBD
Input CM Voltage Range	V <sub>CM</sub>	-0.15		2	V	

#### One-Shot Section

Parameters	Symbol	Min.	Typ.	Max.	Units	Remarks
Blanking pulse duration	t <sub>BLANK</sub>	9	17	25	μs	
Reset Threshold	V <sub>TH3</sub>		2.5		V	V <sub>CC</sub> =10V – GBD
			5.4		V	V <sub>CC</sub> =20V – GBD
Hysteresis	V <sub>HYST3</sub>		40		mV	V <sub>CC</sub> =10V – GBD

**Electrical Characteristics**

V<sub>CC</sub>=15V and T<sub>A</sub> = 25°C unless otherwise specified. The output volt age and current (V<sub>O</sub> and I<sub>O</sub>) parameters are referenced to GND (pin7).

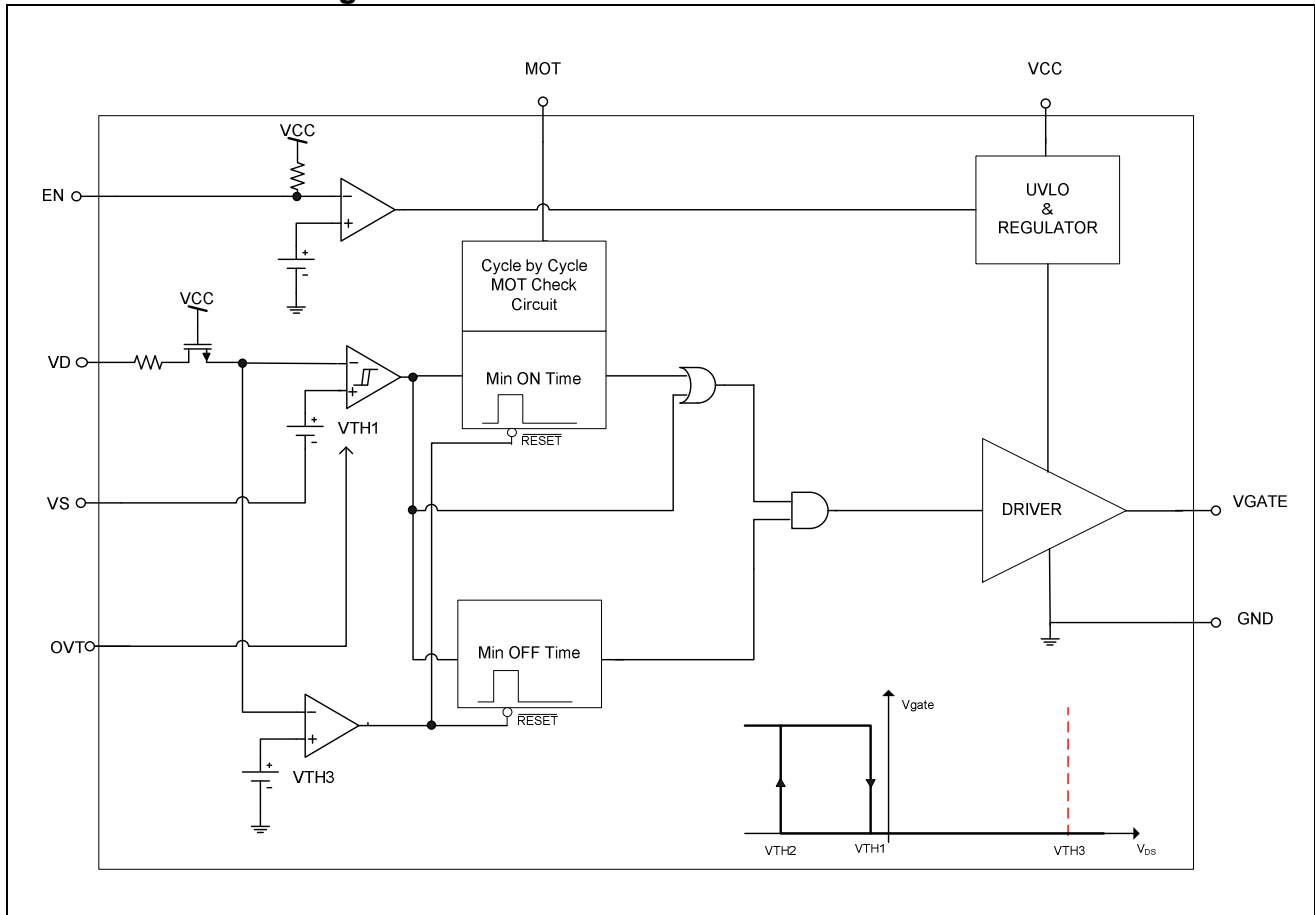
**Minimum On Time Section**

Parameters	Symbol	Min.	Typ.	Max.	Units	Remarks
Minimum on time	T <sub>ONmin</sub>	190	240	290	ns	R <sub>MOT</sub> =5kΩ, V <sub>CC</sub> =12V
		2.48	3.1	3.72	μs	R <sub>MOT</sub> =75kΩ, V <sub>CC</sub> =12V

**Gate Driver Section**

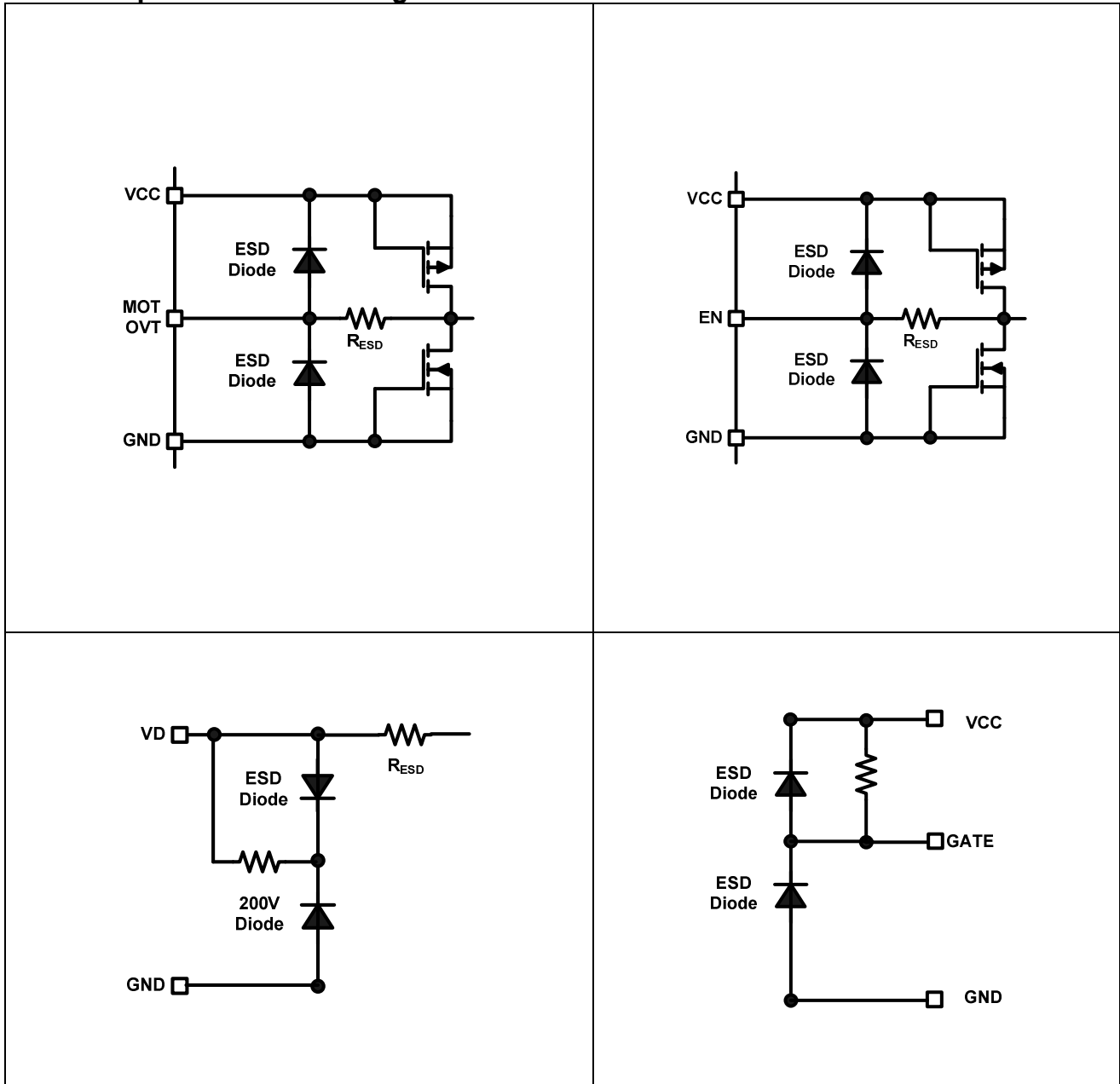
Parameters	Symbol	Min.	Typ.	Max.	Units	Remarks
Gate Low Voltage	V <sub>GLO</sub>		0.3	0.5	V	I <sub>GATE</sub> = 200mA
Gate High Voltage	V <sub>GTH</sub>	9.0	10.7	12.5	V	V <sub>CC</sub> =12V-18V (internally clamped)
Rise Time	t <sub>r1</sub>		18		ns	C <sub>LOAD</sub> = 1nF, V <sub>CC</sub> =12V
	t <sub>r2</sub>		125		ns	C <sub>LOAD</sub> = 10nF, V <sub>CC</sub> =12V
Fall Time	t <sub>f1</sub>		10		ns	C <sub>LOAD</sub> = 1nF, V <sub>CC</sub> =12V
	t <sub>f2</sub>		30		ns	C <sub>LOAD</sub> = 10nF, V <sub>CC</sub> =12V
Turn on Propagation Delay	t <sub>Don</sub>		60	95	ns	V <sub>DS</sub> to V <sub>GATE</sub> -100mV overdrive
Turn off Propagation Delay	t <sub>Doff</sub>		50	75	ns	V <sub>DS</sub> to V <sub>GATE</sub> -100mV overdrive
Pull up Resistance	r <sub>up</sub>		4		Ω	I <sub>GATE</sub> = 1A – GBD
Pull down Resistance	r <sub>down</sub>		0.7		Ω	I <sub>GATE</sub> = -200mA
Output Peak Current(source)	I <sub>O source</sub>		2		A	C <sub>LOAD</sub> = 10nF – GBD
Output Peak Current (sink)	I <sub>O sink</sub>		7		A	C <sub>LOAD</sub> = 10nF – GBD

**Functional Block Diagram**





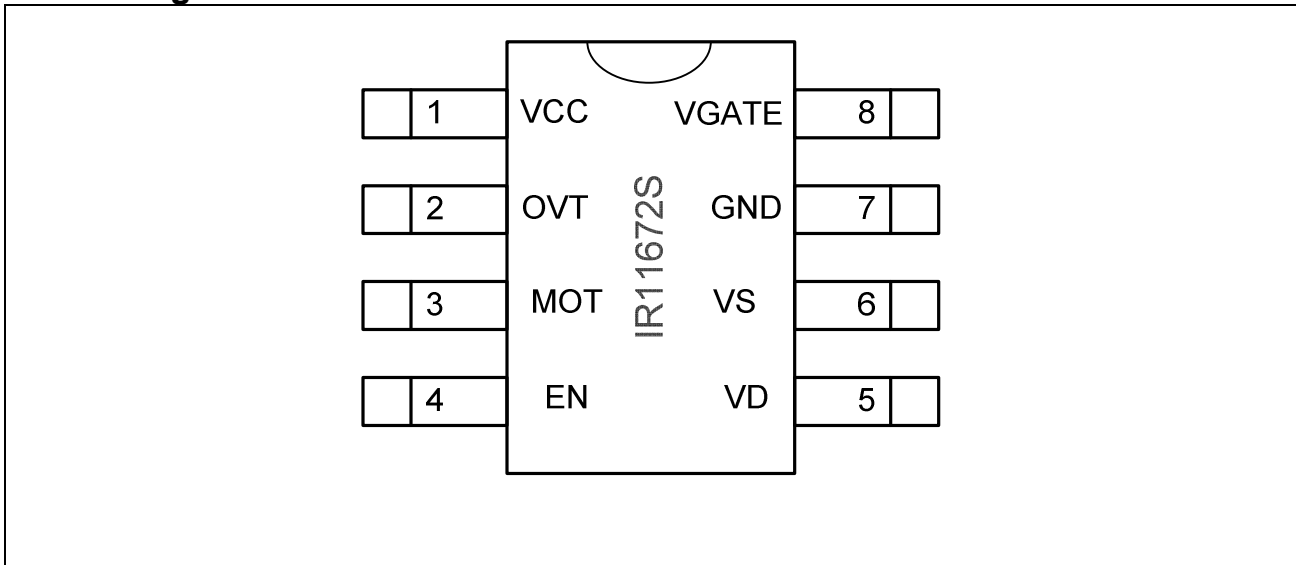
**I/O Pin Equivalent Circuit Diagram**



**Lead Definitions**

PIN#	Symbol	Description
1	VCC	Supply Voltage
2	OVT	Offset Voltage Trimming
3	MOT	Minimum On Time
4	EN	Enable
5	VD	FET Drain Sensing
6	VS	FET Source Sensing
7	GND	Ground
8	VGATE	Gate Drive Output

**Lead Assignments**



## Detailed Pin Description

### VCC: Power Supply

This is the supply voltage pin of the IC and it is monitored by the under voltage lockout circuit. It is possible to turn off the IC by pulling this pin below the minimum turn off threshold voltage, without damage to the IC.

To prevent noise problems, a bypass ceramic capacitor connected to Vcc and COM should be placed as close as possible to the IR11672A. This pin is internally clamped.

### OVT: Offset Voltage Trimming

The OVT pin will program the amount of input offset voltage for the turn-off threshold  $V_{TH1}$ .

The pin can be optionally tied to ground, to VCC or left floating, to select 3 ranges of input offset trimming.

This programming feature allows for accommodating different  $R_{DSon}$  MOSFETs.

### MOT: Minimum On Time

The MOT programming pin controls the amount of minimum on time. Once  $V_{TH2}$  is crossed for the first time, the gate signal will become active and turn on the power FET. Spurious ringings and oscillations can trigger the input comparator off. The MOT blanks the input comparator keeping the FET on for a minimum time.

The MOT is programmed between 200ns and 3us (typ.) by using a resistor referenced to COM.

### EN: Enable

This pin is used to activate the IC "sleep" mode by pulling the voltage level below 1.6V (typ). In sleep mode the IC will consume a minimum amount of current. All switching functions will be disabled and the gate will be inactive.

### VD: Drain Voltage Sense

VD is the voltage sense pin for the power MOSFET Drain. This is a high voltage pin and particular care must be taken in properly routing the connection to the power MOSFET drain.

Additional filtering and or current limiting on this pin are not recommended as it would limit switching performance of the IC.

### VS: Source Voltage Sense

VS is the differential sense pin for the power MOSFET Source. This pin must not be connected directly to the power ground pin (7) but must be used to create a Kelvin contact as close as possible to the power MOSFET source pin.

### GND: Ground

This is ground potential pin of the integrated control circuit. The internal devices and gate driver are referenced to this point.

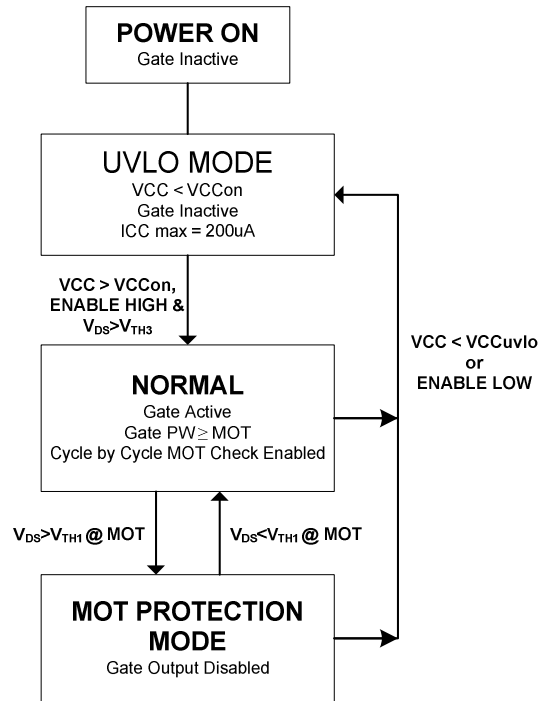
### VGATE: Gate Drive Output

This is the gate drive output of the IC. Drive voltage is internally limited and provides 2A peak source and 7A peak sink capability. Although this pin can be directly connected to the power MOSFET gate, the use of minimal gate resistor is recommended, especially when putting multiple FETs in parallel.

Care must be taken in order to keep the gate loop as short and as small as possible in order to achieve optimal switching performance.

## Application Information and Additional Details

### State Diagram



### UVLO/Sleep Mode

The IC remains in the UVLO condition until the voltage on the VCC pin exceeds the VCC turn on threshold voltage,  $V_{CC\ ON}$ . During the time the IC remains in the UVLO state, the gate drive circuit is inactive and the IC draws a quiescent current of  $I_{CC\ START}$ . The UVLO mode is accessible from any other state of operation whenever the IC supply voltage condition of  $V_{CC} < V_{CC\ UVLO}$  occurs.

The sleep mode is initiated by pulling the EN pin below 1.6V (typ). In this mode the IC is essentially shut down and draws a very low quiescent supply current.

### Normal Mode and Synchronized Enable Function

The IC enters in normal operating mode once the UVLO voltage has been exceeded and the EN voltage is above  $V_{ENHI}$  threshold. When the IC enters the Normal Mode from the UVLO Mode, the GATE output is disabled (stays low) until  $V_{DS}$  exceeds  $V_{TH3}$  to activate the gate. This ensures that the GATE output is not enabled in the middle of a switching cycle. This logic prevents any reverse currents across the device due to the minimum on time function in the IC. The gate will continuously drive the SR MOSFET after this one-time activation. The Cycle by Cycle MOT protection circuit is enabled in Normal Mode.

### MOT Protection Mode

If the secondary current conduction time is shorter than the MOT (Minimum On Time) setting, the next driver output is disabled. This function can avoid reverse current that occurs when the system works at very low duty-cycles or at very light/no load conditions and reduce system standby power consumption by disabling GATE outputs. The Cycle by Cycle MOT Check circuit is always activated under Normal Mode and MOT Protection Mode, so that the IC can automatically resume normal operation once the load increases to a level and the secondary current conduction time is longer than MOT.

## General Description

The IR11672A Smart Rectifier IC can emulate the operation of diode rectifier by properly driving a Synchronous Rectifier (SR) MOSFET. The direction of the rectified current is sensed by the input comparator using the power MOSFET  $R_{DS(on)}$  as a shunt resistance and the GATE pin of the MOSFET is driven accordingly. Internal blanking logic is used to prevent spurious transitions and guarantee operation in continuous (CCM), discontinuous (DCM) and critical (CrCM) conduction mode.

IR11672A is suitable for Flyback and Resonant Half-Bridge topologies.

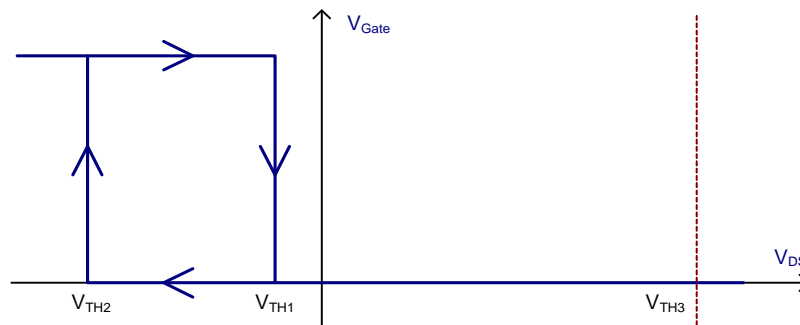


Figure 1: Input comparator thresholds

## Flyback Application

The modes of operation for a Flyback circuit differ mainly for the turn-off phase of the SR switch, while the turn-on phase of the secondary switch (which corresponds to the turn off of the primary side switch) is identical.

### Turn-on phase

When the conduction phase of the SR FET is initiated, current will start flowing through its body diode, generating a negative  $V_{DS}$  voltage across it. The body diode has generally a much higher voltage drop than the one caused by the MOSFET on resistance and therefore will trigger the turn-on threshold  $V_{TH2}$ .

At that point the IR11672A will drive the gate of MOSFET on which will in turn cause the conduction voltage  $V_{DS}$  to drop down. This drop is usually accompanied by some amount of ringing, that can trigger the input comparator to turn off; hence, a Minimum On Time (MOT) blanking period is used that will maintain the power MOSFET on for a minimum amount of time.

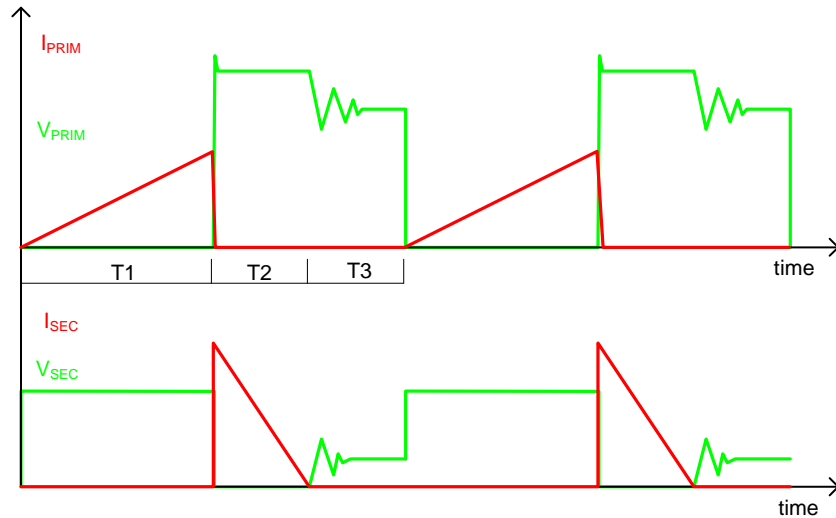
The programmed MOT will limit also the minimum duty cycle of the SR MOSFET and, as a consequence, the max duty cycle of the primary side switch.

### DCM/CrCM Turn-off phase

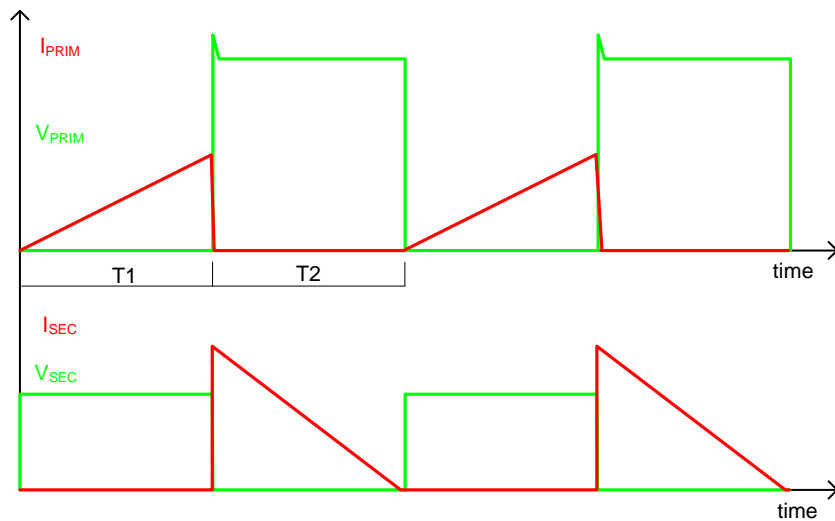
Once the SR MOSFET has been turned on, it will remain on until the rectified current will decay to the level where  $V_{DS}$  will cross the turn-off threshold  $V_{TH1}$ . This will happen differently depending on the mode of operation.

In DCM the current will cross the threshold with a relatively low  $di/dt$ . Once the threshold is crossed, the current will start flowing again thru the body diode, causing the  $V_{DS}$  voltage to jump negative. Depending on the amount of residual current,  $V_{DS}$  may trigger once again the turn on threshold: for this reason  $V_{TH2}$  is blanked for a certain amount of time ( $T_{BLANK}$ ) after  $V_{TH1}$  has been triggered.

The blanking time is internally set. As soon as  $V_{DS}$  crosses the positive threshold  $V_{TH3}$  also the blanking time is terminated and the IC is ready for next conduction cycle.



**Figure 2: Primary and secondary currents and voltages for DCM mode**



**Figure 3: Primary and secondary currents and voltages for CrCM mode**

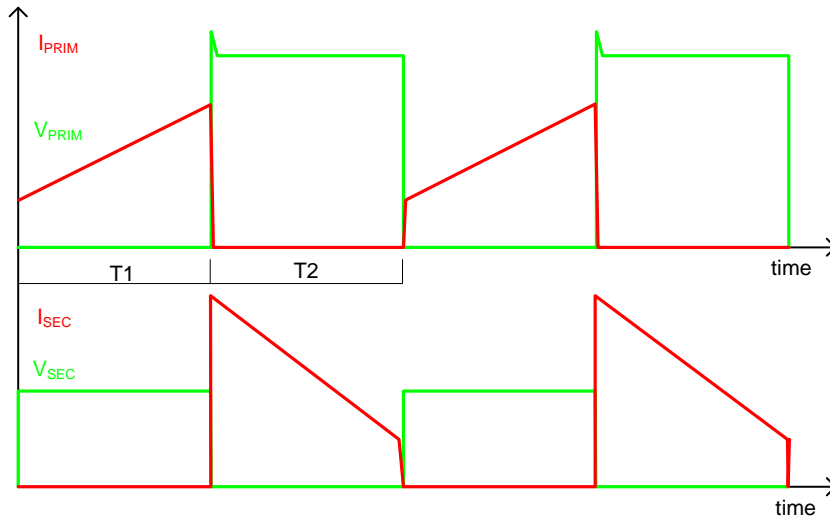
**CCM Turn-off phase**

In CCM mode the turn off transition is much steeper and  $di/dt$  involved is much higher. The turn on phase is identical to DCM or CrCM and therefore won't be repeated here.

During the SR FET conduction phase the current will decay linearly, and so will  $V_{DS}$  on the SR FET.

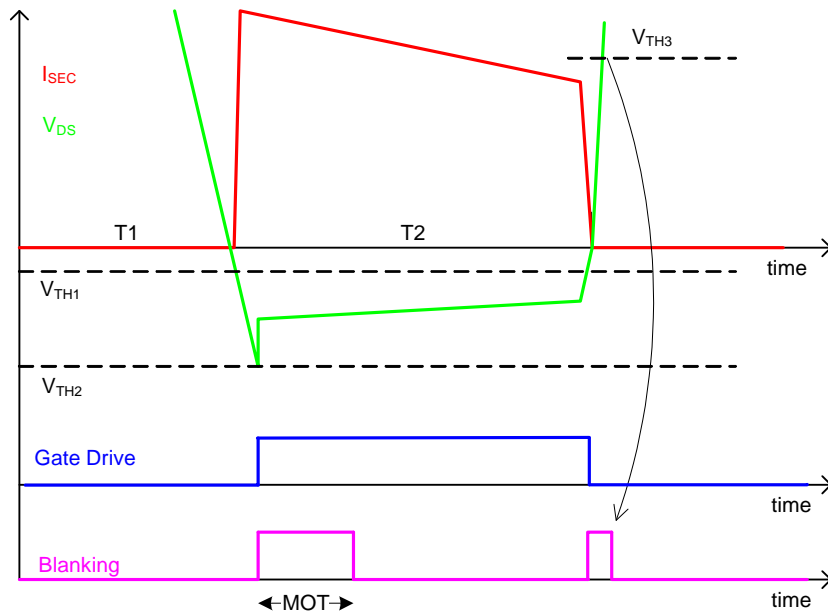
Once the primary switch will start to turn back on, the SR FET current will rapidly decrease crossing  $V_{TH1}$  and turning the gate off. The turn off speed is critical to avoid cross conduction on the primary side and reduce switching losses.

Also in this case a blanking period will be applied, but given the very fast nature of this transition, it will be reset as soon as  $V_{DS}$  crosses  $V_{TH3}$ .

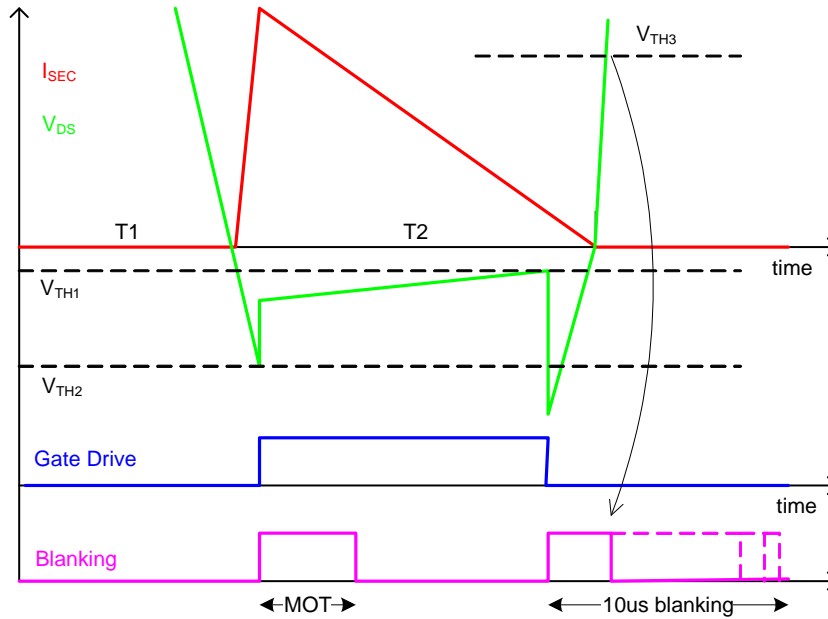


**Figure 4: Primary and secondary currents and voltages for CCM mode**

The operation waveforms of IR11672A in a flyback converter under CCM mode and DCM/CrCM were shown in Figure 5 and Figure 6 respectively.



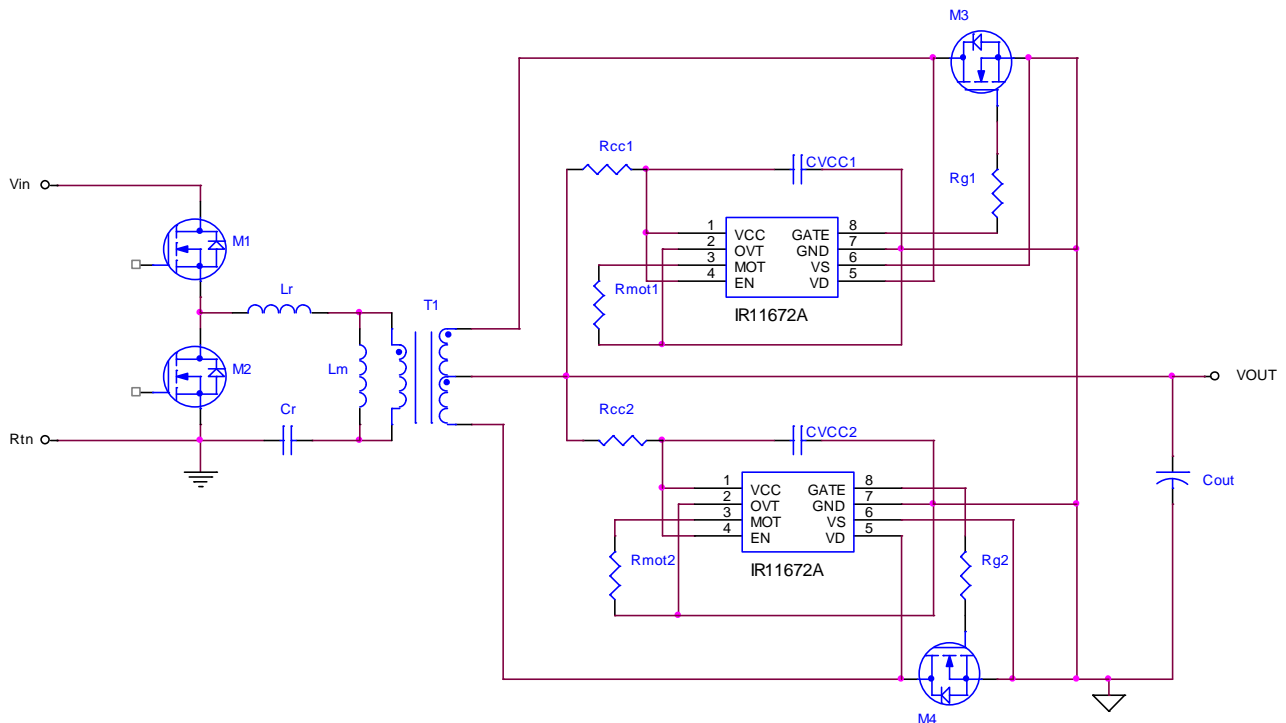
**Figure 5: Secondary side CCM operation**



**Figure 6: Secondary side DCM/CrCM operation**

### Resonant Half-Bridge Application

The typical application circuit of IR11672A in LLC half-bridge is shown in Figure 7.



**Figure 7: Resonant half-bridge application circuit**

In resonant half-bridge converter, the turn-on phase and turn-off phase is similar to flyback except the current shape is sinusoid. The typical operation waveform can be found below.



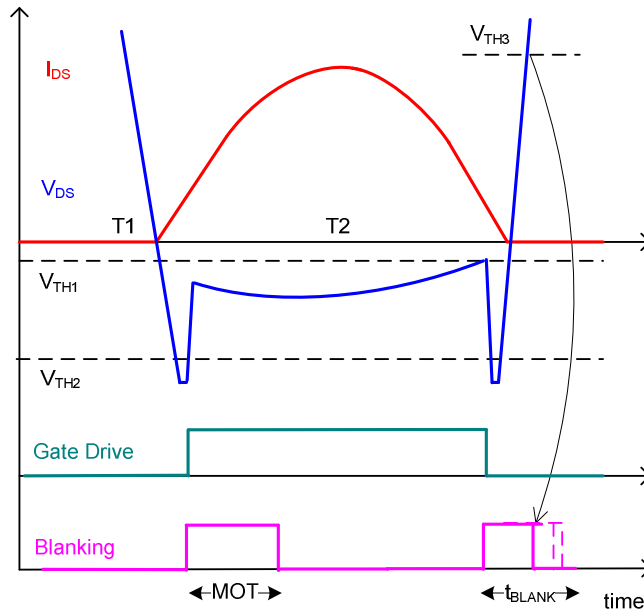


Figure 8: Resonant half-bridge operation waveform

### MOT Protection Mode

The MOT protection prevents reverse current in SR MOSFET which could happen at light load if the MOT time is set very long. The IC disables the gate output in the protection mode and automatically resume to normal operation as the load increasing to a level where the SR current conduction time is longer than MOT.

This function works in both flyback and resonant half-bridge topologies. Figure 9 is an example in Flyback converter.

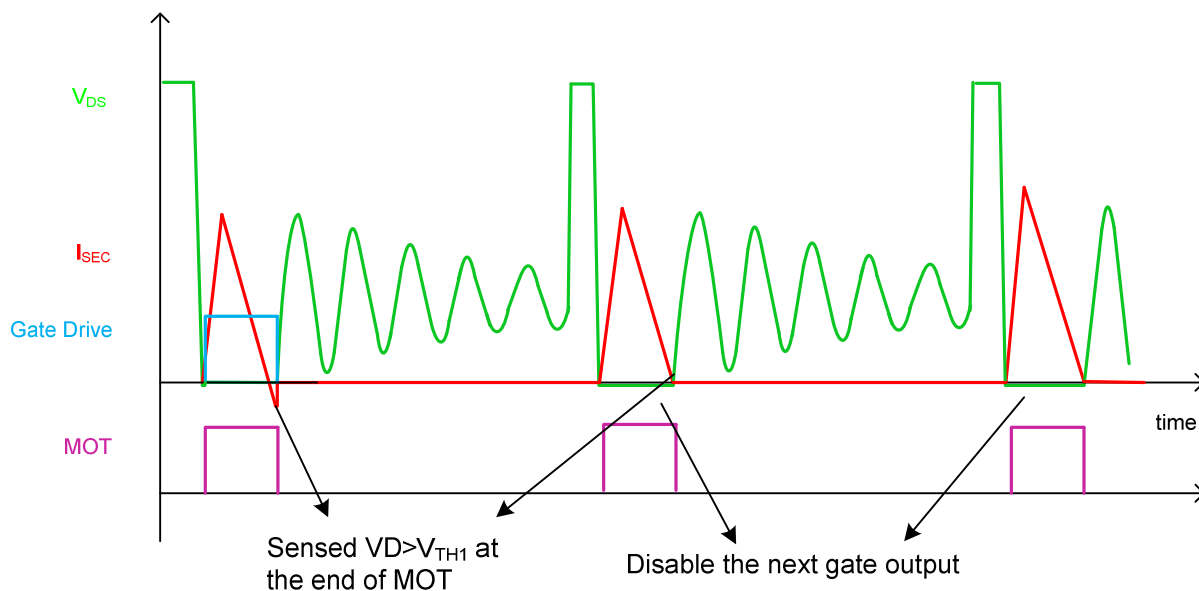


Figure 9: MOT Protection Mode

### Synchronized Enable Function

Sync Enable function guarantees the VGATE always starts switching at the beginning of a switching cycle. This function works in both flyback and resonant half-bridge topologies. Figure 10 is an example in resonant half-bridge converter.

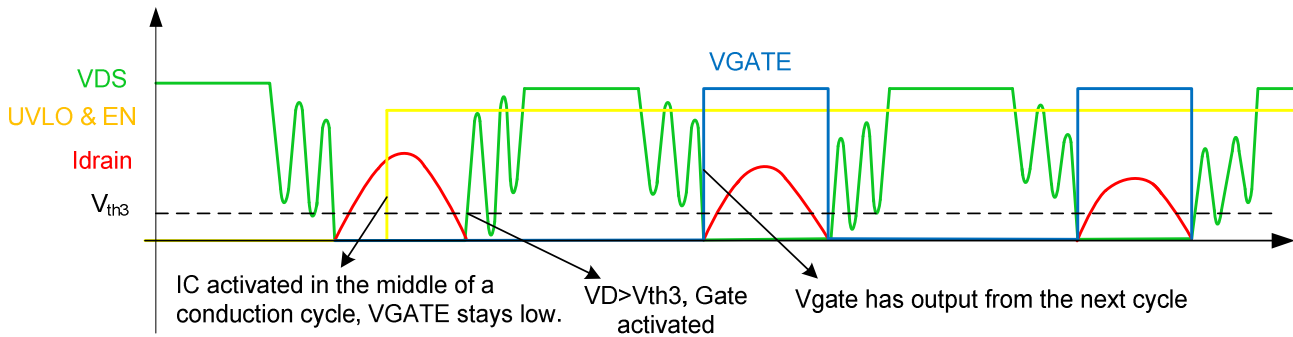


Figure 10: Synchronized Enable Function (resonant half-bridge)

### General Timing Waveform

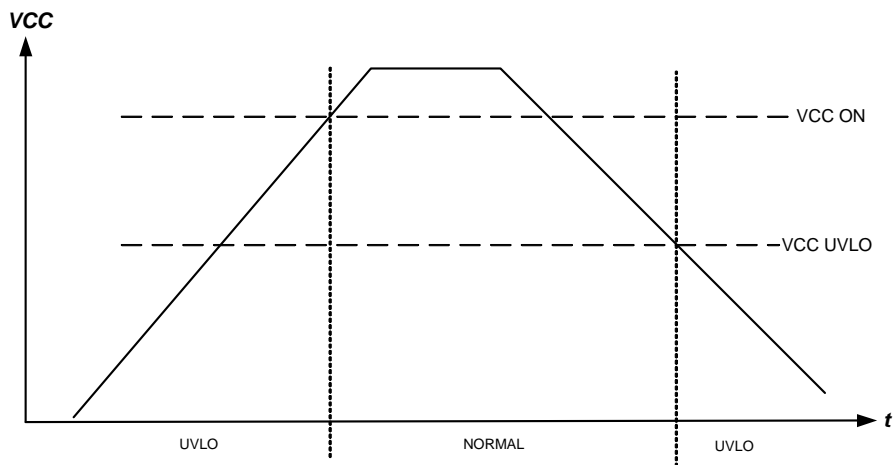


Figure 11: Vcc UVLO

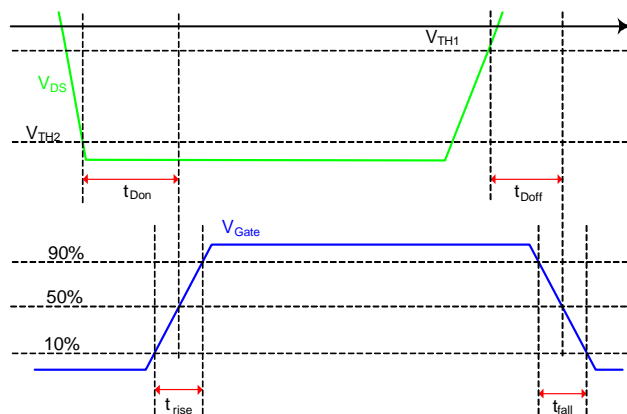
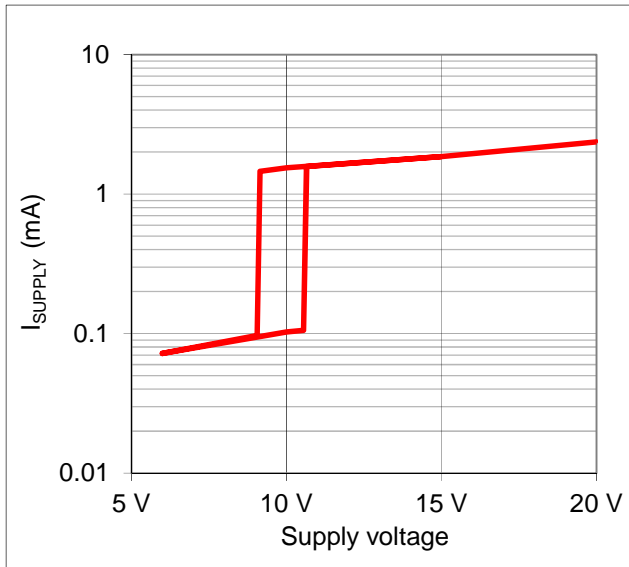
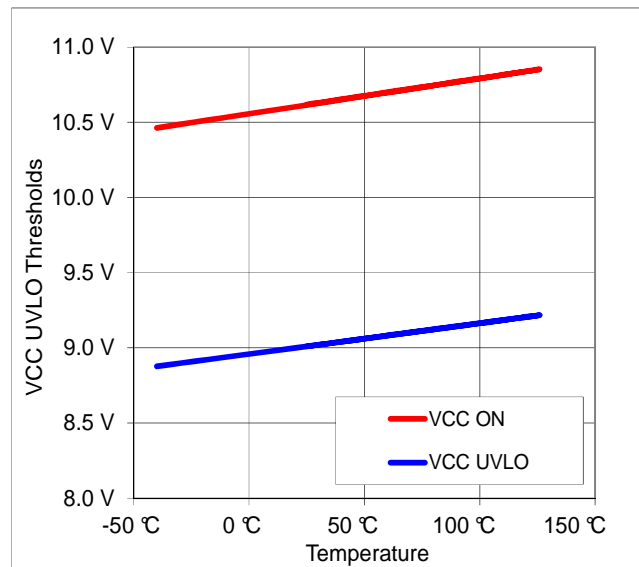


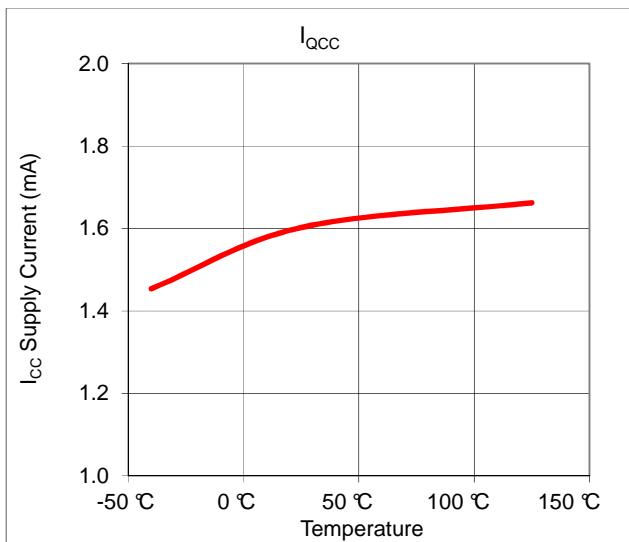
Figure 12: Timing waveform



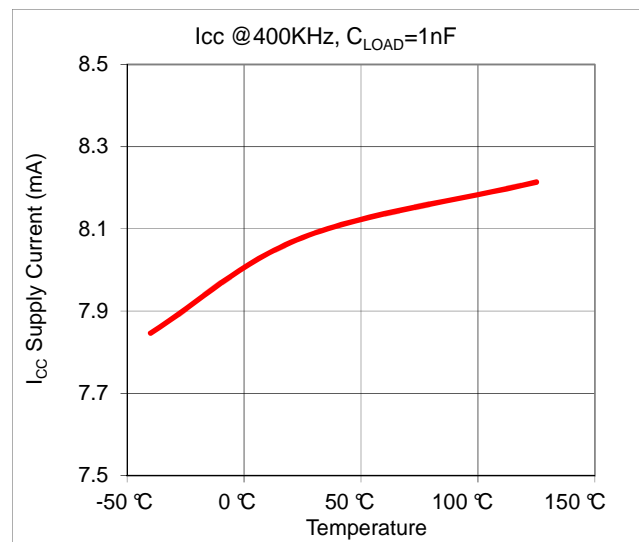
**Figure 13: Supply Current vs. Supply Voltage**



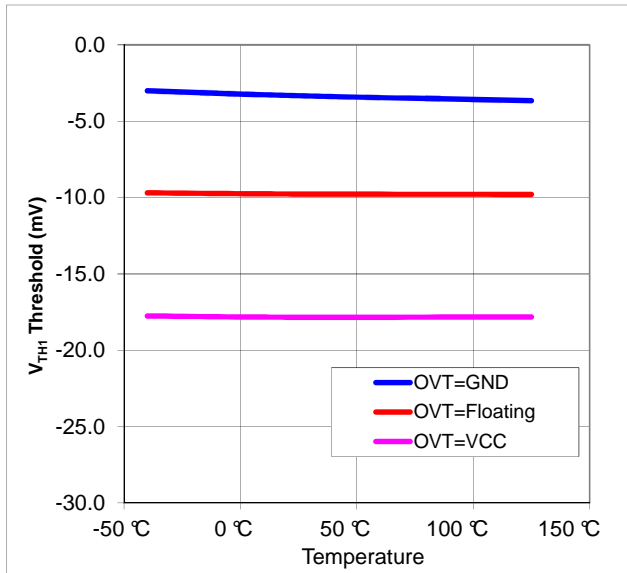
**Figure 14: Undervoltage Lockout vs. Temperature**



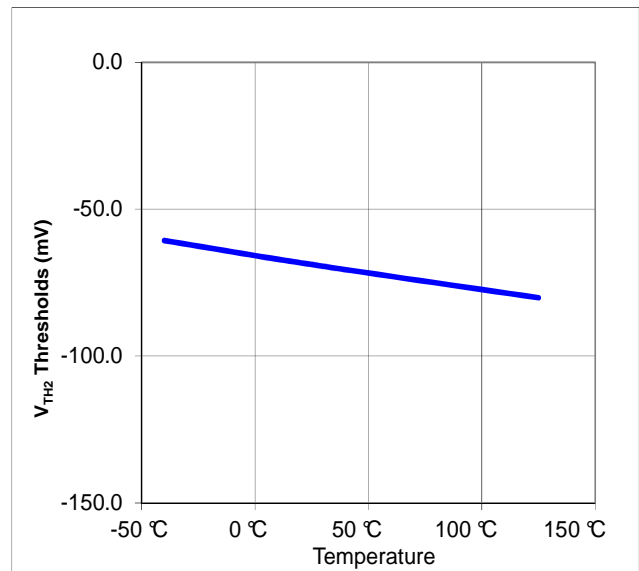
**Figure 15: Icc Quiescent Current vs. Temperature**



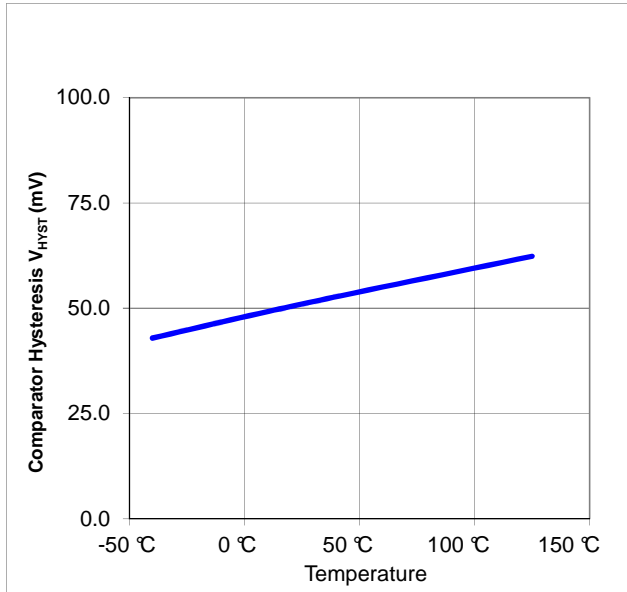
**Figure 16: Icc Supply Current @1nF Load vs. Temperature**



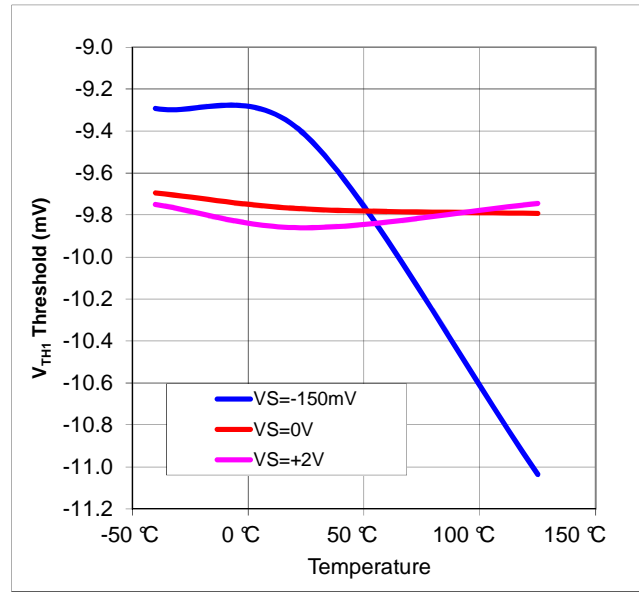
**Figure 17:  $V_{TH1}$  vs. Temperature**



**Figure 18:  $V_{TH2}$  vs. Temperature**



**Figure 19: Comparator Hysteresis vs. Temperature**



**Figure 20:  $V_{TH1}$  vs. Temperature and Common Mode (OVT=Floating)**

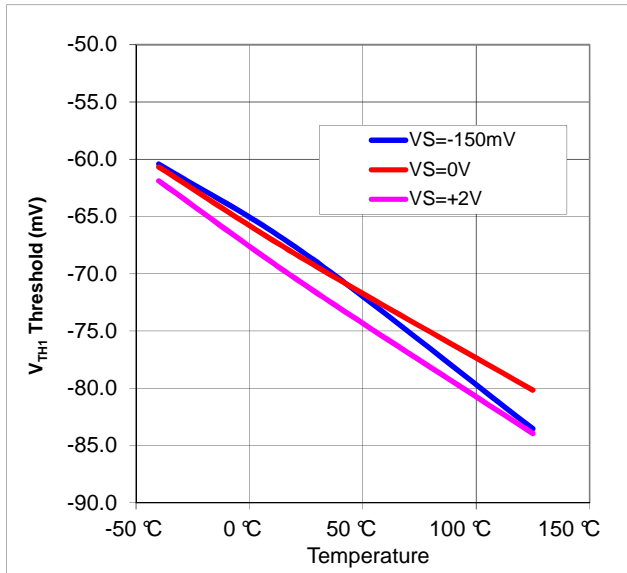


Figure 21:  $V_{TH2}$  vs. Temperature and Common Mode

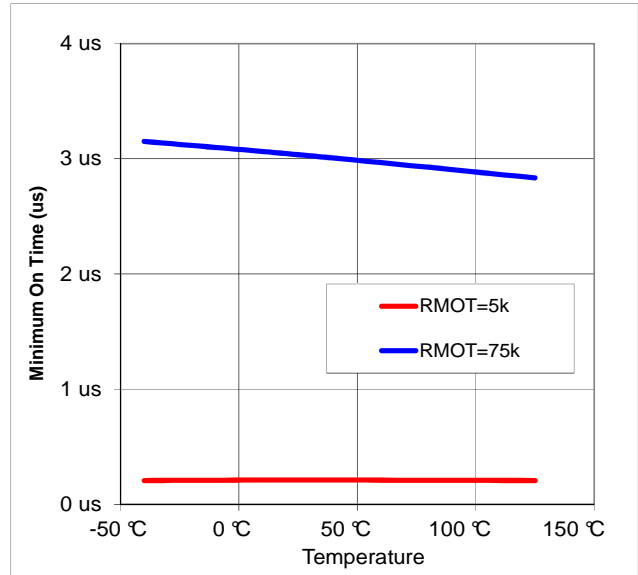


Figure 22: MOT vs Temperature

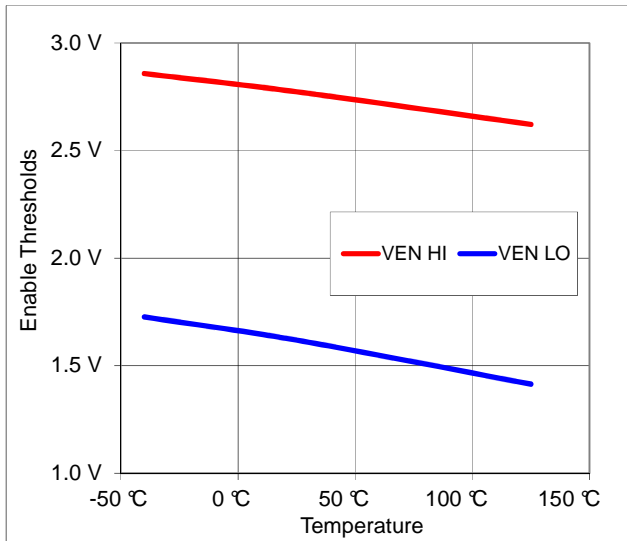


Figure 23: Enable Threshold vs. Temperature

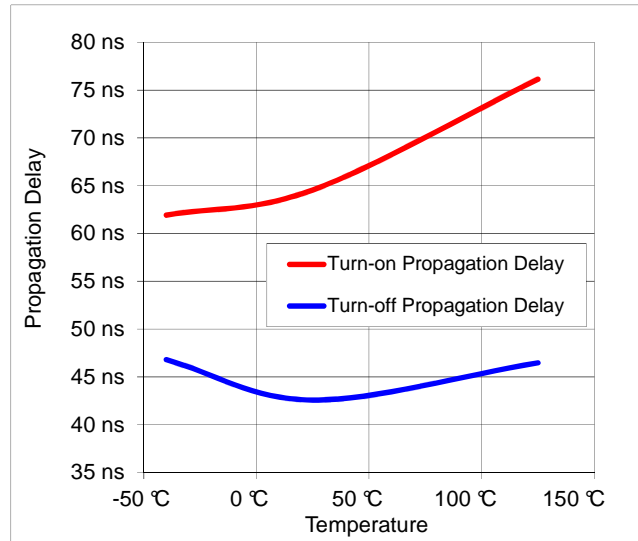
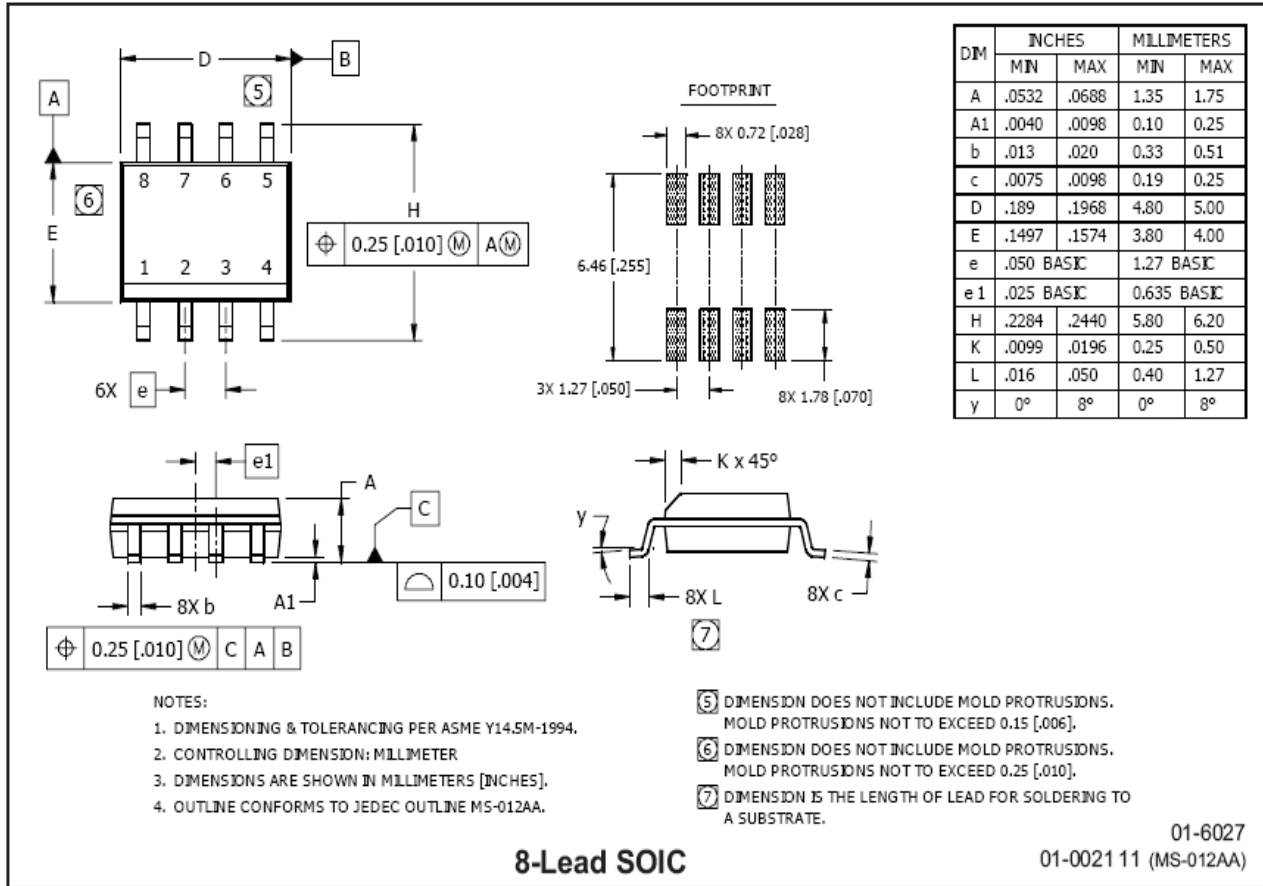
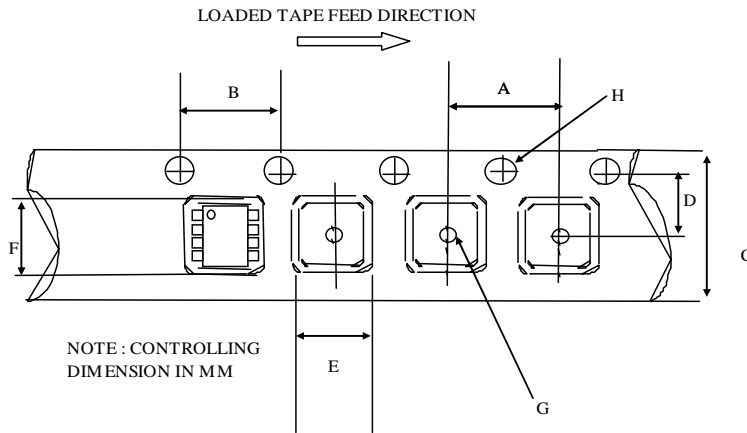


Figure 24: Turn-on and Turn-off Propagation Delay vs. Temperature

**Package Details: SOIC8N**

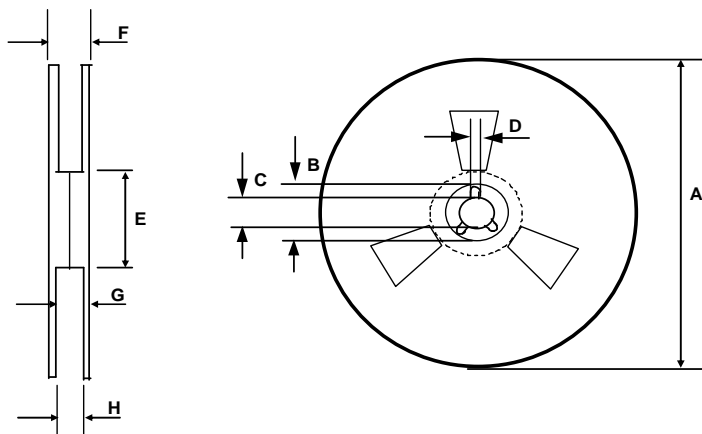


**Tape and Reel Details: SOIC8N**



**CARRIER TAPE DIMENSION FOR 8SOICN**

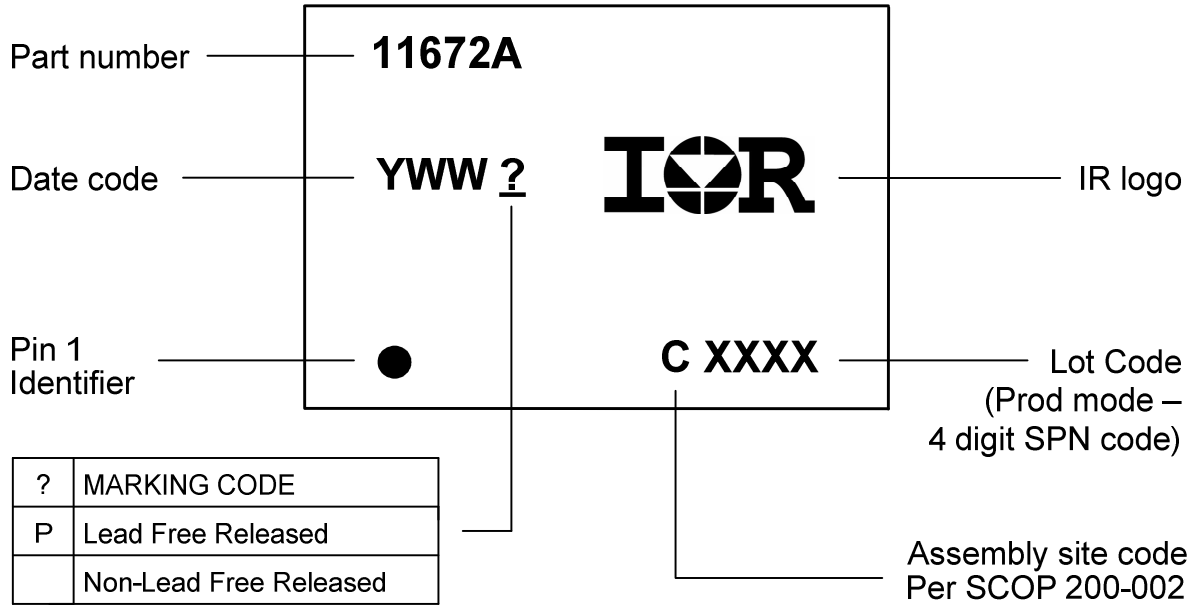
Code	Metric		Imperial	
	Min	Max	Min	Max
A	7.90	8.10	0.311	0.318
B	3.90	4.10	0.153	0.161
C	11.70	12.30	0.46	0.484
D	5.45	5.55	0.214	0.218
E	6.30	6.50	0.248	0.255
F	5.10	5.30	0.200	0.208
G	1.50	n/a	0.059	n/a
H	1.50	1.60	0.059	0.062



**REEL DIMENSIONS FOR 8SOICN**

Code	Metric		Imperial	
	Min	Max	Min	Max
A	329.60	330.25	12.976	13.001
B	20.95	21.45	0.824	0.844
C	12.80	13.20	0.503	0.519
D	1.95	2.45	0.767	0.096
E	98.00	102.00	3.858	4.015
F	n/a	18.40	n/a	0.724
G	14.50	17.10	0.570	0.673
H	12.40	14.40	0.488	0.566

**Part Marking Information**





**Ordering Information**

Base Part Number	Package Type	Standard Pack		Complete Part Number
		Form	Quantity	
IR11672AS	SOIC8N	Tube/Bulk	95	IR11672ASPBF
		Tape and Reel	2500	IR11672ASTRPBF

The information provided in this document is believed to be accurate and reliable. However, International Rectifier assumes no responsibility for the consequences of the use of this information. International Rectifier assumes no responsibility for any infringement of patents or of other rights of third parties which may result from the use of this information. No license is granted by implication or otherwise under any patent or patent rights of International Rectifier. The specifications mentioned in this document are subject to change without notice. This document supersedes and replaces all information previously supplied.

For technical support, please contact IR's Technical Assistance Center  
<http://www.irf.com/technical-info/>

**WORLD HEADQUARTERS:**  
 233 Kansas St., El Segundo, California 90245  
 Tel: (310) 252-7105