19-3507; Rev 1; 3/06

EVALUATION KIT AVAILABLE

Low-Voltage, Internal Switch, Step-Down/DDR Regulator

General Description

The MAX1515 constant-off-time, pulse-width-modulated (PWM) source/sink step-down DC-DC converter is optimized for use in low-voltage active-termination power rails or chipset power supplies in notebook and subnotebook computers. This device features dual internal n-channel MOSFET power switches for high efficiency and reduced component count. External Schottky diodes are not required. An integrated boost switch eliminates the need for an external boost diode. The internal 40mΩ NMOS power switches easily source and sink continuous load currents up to 3A. The MAX1515 produces an adjustable output from +0.5V to +2.7V and achieves efficiencies as high as 95%.

The MAX1515 can be configured as a DDR regulator, producing an output that is exactly half the memory supply rail. The input of the power stage can be taken from the memory supply rail itself, resulting in an efficient power supply that returns the energy to the rail from which it was sourced. The MAX1515 includes a reference buffer that provides ±5mA of drive current.

The MAX1515 uses a unique current-mode, constant-off-time, PWM control scheme. A selectable pulse-skipping mode maintains high efficiency during light-load operation, yet still sources and sinks current on demand. The MAX1515 can also be operated in fixed-PWM mode for low output ripple. The programmable constant-off-time architecture sets switching frequencies up to 1MHz, which allows the user to optimize performance trade-offs between efficiency, output switching noise, component size, and cost. The MAX1515 features an adjustable soft-start to limit surge currents during startup and a low-power shutdown mode to disconnect the input from the output and reduce supply current below 1µA. The MAX1515 is available in a 24-pin thin QFN package with an exposed backside pad.

Applications

Notebook DDR Memory Termination

Active-Termination Buses

Chipset/Graphics Processor Supplies

Pin Configuration appears at end of data sheet.

Features

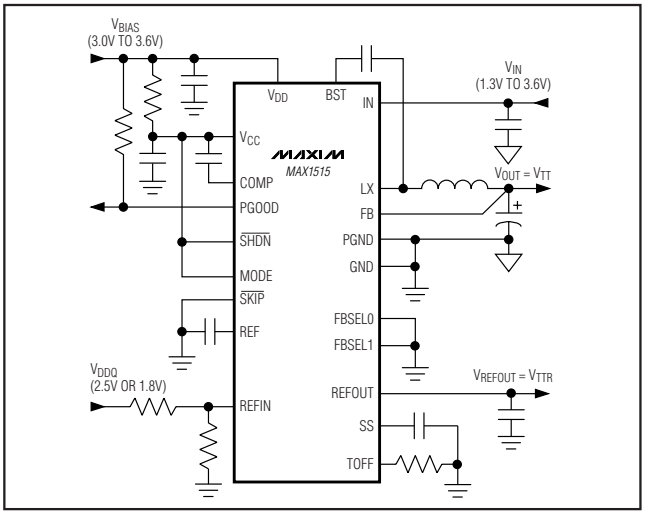
- **Dual 40mΩ Internal n-Channel MOSFETs**
- **Integrated Boost Switch**
- **+1.3V to +3.6V Input Voltage Range**
- **1% VOUT Accuracy Over Line and Load**
- **1MHz Maximum Switching Frequency**
- **DDR Termination Regulator (DDR Mode)**
  - **Tracking Output Voltage**
  - **Source/Sink Pulse Skipping**
  - **±5mA Reference Buffer**
- **Output Voltage (Non-DDR Mode)**
  - **+2.5V, +1.8V, or +1.5V Pin Selectable**
  - **+0.5V to +2.7V Adjustable**
- **1.1V ±0.75% Reference Output**
- **Adjustable Soft-Start Inrush Current Limiting**
- **< 1µA (typ) Shutdown Supply Current**
- **< 800µA (max) Operating Supply Current**
- **Selectable Pulse-Skipping Operation at Light Loads**
- **Positive and Negative Current Limit**
- **Power-Good Window Comparator**
- **Output Short-Circuit Protection**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	PKG CODE
MAX1515ETG	-40°C to +85°C	24 Thin QFN 4mm x 4mm	T2444-4
MAX1515ETG+	-40°C to +85°C	24 Thin QFN 4mm x 4mm	T2444-4

+Denotes lead-free package.

Minimal Operating Circuit



Low-Voltage, Internal Switch, Step-Down/DDR Regulator

ABSOLUTE MAXIMUM RATINGS

V_{CC}, V_{DD}, LX, $\overline{SHDN}$ to GND .....-0.3V to +4V
MODE, IC to GND .....-0.3V to +4V
COMP, FB, REF, REFIN, REFOUT, PGOOD to GND.....-0.3V to (V_{CC} + 0.3V)
FBSEL0, FBSEL1, TOFF, $\overline{SKIP}$, SS to GND....-0.3V to (V_{CC} + 0.3V)
V_{DD} to V_{CC} .....-0.3V to + 0.3V
IN to V_{DD} .....-0.3V to (V_{DD} + 0.3V)
PGND to GND ..... -0.3V to +0.3V
LX to BST..... -4V to +0.3V
BST to GND..... -0.3V to +8.0V
LX Current (Note 1).....±4.7A
REF Short Circuit to GND.....Continuous
REFOUT Short Circuit to GND.....Continuous
Continuous Power Dissipation (T_A = +70°C)
24-Pin Thin QFN (derate 20.8mW/°C above +70°C; part mounted on 1in^2 of 1oz copper).....1667mW
Operating Temperature Range .....-40°C to +85°C
Junction Temperature.....+150°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Note 1: LX has clamp diodes to PGND and IN. If continuous current is applied through these diodes, thermal limits must be observed.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(Circuit of Figure 1, V_{IN} = +3.3V, V_{CC} = V_{DD} = $\overline{SHDN}$ = MODE = +3.3V, V_{REFIN} = V_{REF}, $\overline{SKIP}$ = GND, **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS			MIN	TYP	MAX	UNITS
PWM CONTROLLER								
Input Voltage Range	V_{IN}				1.3		3.6	V
	V_{CC}, V_{DD}				3.0		3.6	
Output Adjust Range		$V_{OUT} \le V_{IN}$			0.5		2.7	V
Feedback Voltage Accuracy	V_{FB} - V_{REFIN}	V_{IN} = +3.3V, I_{LOAD} = 0, MODE = V_{CC}		T_A = +25°C to +85°C	-3	0	+3	mV
				T_A = 0°C to +85°C	-4	0	+4	
	V_{FB}	V_{IN} = +3.3V, I_{LOAD} = 0, MODE = low	FBSEL0 = V_{CC}, FBSEL1 = V_{CC}, REFIN = REF	T_A = +25°C to +85°C	2.463	2.5	2.537	V
				T_A = 0°C to +85°C	2.450	2.5	2.550	
			FBSEL0 = V_{CC}, FBSEL1 = GND, REFIN = REF	T_A = +25°C to +85°C	1.782	1.800	1.827	
				T_A = 0°C to +85°C	1.773	1.800	1.836	
			FBSEL0=GND FBSEL1=V_{CC} REFIN=REF	T_A = +25°C to +85°C	1.477	1.500	1.523	
				T_A = 0°C to +85°C	1.470	1.500	1.530	
			FBSEL0=GND FBSEL1=GND REFIN=0.5V	T_A = +25°C to +85°C	0.492	0.500	0.508	
				T_A = 0°C to +85°C	0.490	0.500	0.510	
Feedback Load-Regulation Error		V_{IN} = +1.3V to +3.6V, I_{LOAD} = 0 to 3A, $\overline{SKIP}$ = V_{CC}				0.1		%

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1, V_{IN} = +3.3V, V_{CC} = V_{DD} = $\overline{SHDN}$ = MODE = +3.3V, V_{REFIN} = V_{REF}, $\overline{SKIP}$ = GND, **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Sink-Mode Detect Threshold	V_{FB} - V_{REFIN}	MODE = V_{CC}, V_{REFIN} = +0.5V to +1.5V		+18		+32	mV
Source-Mode Detect Threshold	V_{FB} - V_{REFIN}	MODE = V_{CC}, V_{REFIN} = +0.5V to +1.5V		-32		-18	mV
MOSFET On-Resistance	R_{NMOS}	V_{CC} = V_{DD} = V_{IN} = +3.3V, I_{LOAD} = 0.5A			0.04	0.10	Ω
Switching Frequency	f_{SW}	(Note 2)				1	MHz
Maximum Output Current	$I_{OUT(RMS)}$	(Note 3)		3.3			A
Current-Limit Threshold	I_{LIMIT_P}	V_{IN} = +3.3V, MODE = GND or V_{CC}, positive or sourcing mode		3.60	4.2	4.85	A
	I_{LIMIT_N}	MODE = V_{CC}, negative or sinking mode			-3.0		
Pulse-Skipping Current Threshold	I_{SKIP_P}	V_{IN} = +3.3V, MODE = GND or V_{CC}, positive or sourcing mode		0.5	0.8	1.1	A
Zero Cross Current Threshold	I_{ZX_P}	V_{IN} = +3.3V, MODE = GND or V_{CC}, positive or sourcing mode			200		mA
	I_{ZX_N}	MODE = V_{CC}, negative or sinking mode			-350		
FB Input Bias Current		FB = 1.01 x V_{TARGET} (Note 4)		-50		+50	nA
Off-Time	t_{OFF}	V_{FB} > 0.3 x V_{TARGET} (Note 4)	R_{TOFF} = 33.2kΩ	0.270	0.34	0.405	µs
			R_{TOFF} = 110kΩ	0.85	1.00	1.15	
			R_{TOFF} = 499kΩ	3.8	4.5	5.2	
Extended Off-Time	$t_{OFF(EXT)}$	V_{FB} < 0.3 x V_{TARGET} (Notes 2, 4)			4 x t_{OFF}		µs
Minimum On-Time	$t_{ON(MIN)}$	(Note 2)			180		ns
Maximum On-Time	$t_{ON(MAX)}$			5	11		µs
SS Source Current	$I_{SS(SRC)}$			3.50	5.25	6.75	µA
SS Sink Current	$I_{SS(SNK)}$			100			µA
No-Load Supply Current	I_{CC} + I_{DD} + I_{IN}	V_{IN} = 3.3V (not switching) (Note 4)	MODE = GND, FBSEL0 = GND, FBSEL1 = GND, V_{FB} = 1.01 x V_{TARGET}		450	800	µA
			MODE = V_{CC}, V_{FB} = V_{TARGET}		700	1200	
Shutdown Supply Currents	I_{CC} + I_{DD} + I_{IN}	$\overline{SHDN}$ = MODE = GND, LX = 0V or 3.3V			0.2	20	µA
	I_{IN}	$\overline{SHDN}$ = MODE = GND, LX = 0V			0.2	20	
	I_{LX}	$\overline{SHDN}$ = MODE = GND, LX = 3.3V			0.1	20	

Low-Voltage, Internal Switch, Step-Down/DDR Regulator

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1, V_{IN} = +3.3V, V_{CC} = V_{DD} = $\overline{SHDN}$ = MODE = +3.3V, V_{REFIN} = V_{REF}, $\overline{SKIP}$ = GND, **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
REFERENCE							
Reference Voltage	V_{REF}	V_{CC} = +3.0V to +3.6V	T_A = +25°C to +85°C	1.0923	1.100	1.1077	V
			T_A = 0°C to +85°C	1.0907	1.100	1.1094	
Reference Load Regulation		I_{REF} = -1µA to +50µA				10	mV
REFIN Input Voltage Range	V_{REFIN}	V_{CC} = +3.0V to +3.6V		0.5		1.5	V
REFOUT Output Accuracy	V_{REFIN} - V_{REFOUT}	V_{REFIN} = +0.5V to +1.5V	I_{REFOUT} = -1mA to +1mA	-10		+10	mV
		V_{REFIN} = +0.5V to +1.5V	I_{REFOUT} = -5mA to +5mA	-20		+20	
REFIN Input Bias Current	I_{REFIN}	V_{REFIN} = 1.1V		-50		+50	nA
FAULT DETECTION							
Thermal Shutdown	T_{SHDN}	Rising, hysteresis = 15°C			+165		°C
Undervoltage-Lockout Threshold	$V_{CC(UVLO)}$	V_{CC} rising, 2% falling-edge hysteresis		2.5	2.7	2.9	V
PGOOD Trip Threshold (Lower)		No load, falling edge, hysteresis = 1%		-13	-10	-7	%
PGOOD Trip Threshold (Upper)		No load, rising edge, hysteresis = 1%		+7	+10	+13	%
PGOOD Propagation Delay	t_{PGOOD}	FB forced 2% beyond PGOOD trip threshold			10		µs
PGOOD Output Low Voltage		I_{SINK} = 1mA				0.1	V
PGOOD Leakage Current Condition		High state, forced to 3.6V; V_{CC} = V_{DD} = 3.6V				1	µA
INPUTS AND OUTPUTS							
Logic Input High Voltage		$\overline{SKIP}$, $\overline{SHDN}$, MODE, FBSEL0, FBSEL1		2.0			V
Logic Input Low Voltage		$\overline{SKIP}$, $\overline{SHDN}$, MODE, FBSEL0, FBSEL1				0.8	V
Logic Input Current		$\overline{SKIP}$, $\overline{SHDN}$, MODE, FBSEL0, FBSEL1		-0.5		+0.5	µA

ELECTRICAL CHARACTERISTICS

(Circuit of Figure 1, V_{IN} = +3.3V, V_{CC} = V_{DD} = $\overline{SHDN}$ = MODE = +3.3V, V_{REFIN} = V_{REF}, $\overline{SKIP}$ = GND, **T_A = -40°C to +85°C**, unless otherwise noted. Note 5)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
PWM CONTROLLER							
Input Voltage Range	V_{IN}			1.3		3.6	V
	V_{CC}, V_{DD}			3.0		3.6	
Output Adjust Range		$V_{OUT} \le V_{IN}$		0.5		V_{CC}	V
Feedback Voltage Accuracy	V_{FB} - V_{REFIN}	V_{IN} = +3.3V, I_{LOAD} = 0, MODE = V_{CC}		-5		+5	mV
	V_{FB}	V_{IN} = +3.3V, I_{LOAD} = 0, MODE = low	FBSEL0 = V_{CC}, FBSEL1 = V_{CC}, REFIN = REF	2.438		2.562	V
			FBSEL0 = V_{CC}, FBSEL1 = GND, REFIN = REF	1.755		1.845	
			FBSEL0 = GND, FBSEL1 = V_{CC}, REFIN = REF	1.463		1.538	
			FBSEL0 = GND, FBSEL1 = GND, REFIN = 0.5V	0.487		0.513	
Sink-Mode Detect Threshold	V_{FB} - V_{REFIN}	MODE = V_{CC}, V_{REFIN} = +0.5V to +1.5V		+15		+35	mV
Source-Mode Detect Threshold	V_{FB} - V_{REFIN}	MODE = V_{CC}, V_{REFIN} = +0.5V to +1.5V		-35		-15	mV
nFET On-Resistance	R_{NMOS}	V_{CC} = V_{DD} = V_{IN} = +3.3V, I_{LOAD} = 0.5A				0.10	Ω
Switching Frequency	f_{SW}	(Note 2)				1	MHz
Current-Limit Threshold	I_{LIMIT_P}	V_{IN} = +3.3V, MODE = GND or V_{CC}, positive or sourcing mode		3.35		5.05	A
Pulse-Skipping Current Threshold	I_{SKIP_P}	V_{IN} = +3.3V, MODE = GND or V_{CC}, positive or sourcing mode		0.4		1.2	A
Off-Time	t_{OFF}	V_{FB} > 0.3 x V_{TARGET} (Note 4)	R_{TOFF} = 33.2kΩ	0.250		0.425	µs
			R_{TOFF} = 110kΩ	0.8		1.2	
			R_{TOFF} = 499kΩ	3.8		5.2	
Maximum On-Time	$t_{ON(MAX)}$			5			µs
SS Source Current	$I_{SS(SRC)}$			3		7	µA
SS Sink Current	$I_{SS(SNK)}$			100			µA

Low-Voltage, Internal Switch, Step-Down/DDR Regulator

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1, V_{IN} = +3.3V, V_{CC} = V_{DD} = $\overline{SHDN}$ = MODE = +3.3V, V_{REFIN} = V_{REF}, $\overline{SKIP}$ = GND, **T_A = -40°C to +85°C**, unless otherwise noted. Note 5)

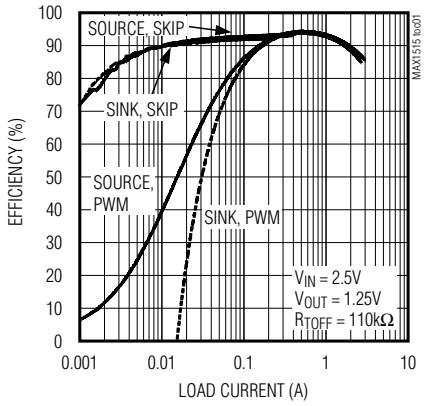
PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
No-Load Supply Current	I_{CC} + I_{DD} + I_{IN}	V_{IN} = 3.3V (Note 4)	MODE = GND, FBSEL0 = FBSEL1 = GND, V_{FB} = 1.01 x V_{TARGET}			900	µA
			MODE = V_{CC} V_{FB} = V_{TARGET}			1300	
Shutdown Supply Currents	I_{CC} + I_{DD} + I_{IN}	$\overline{SHDN}$ = MODE = GND, LX = 0V or 3.3V				20	µA
	I_{IN}	$\overline{SHDN}$ = MODE = GND, LX = 0V				20	
	I_{LX}	$\overline{SHDN}$ = MODE = GND, LX = 3.3V				20	
REFERENCE							
Reference Voltage	V_{REF}	V_{CC} = +3.0V to +3.6V		1.086		1.114	V
Reference Load Regulation		I_{REF} = -1µA to +50µA				12	mV
REFIN Input Voltage Range	V_{REFIN}	V_{CC} = +3.0V to +3.6V, V_{CC} > V_{REFIN} + 1.35V		0.5		1.5	V
REFOUT Output Accuracy	V_{REFIN} - V_{REFOUT}	V_{REFIN} = +0.5V to +1.5V	I_{REFOUT} = -1mA to +1mA	-15		+15	mV
		V_{REFIN} = +0.5V to +1.5V	I_{REFOUT} = -5mA to +5mA	-25		+25	
FAULT DETECTION							
Undervoltage-Lockout Threshold	$V_{CC(UVLO)}$	V_{CC} rising, 2% falling-edge hysteresis		2.40		2.95	V
PGOOD Trip Threshold (Lower)		No load, falling edge, hysteresis = 1%		-13		-7	%
PGOOD Trip Threshold (Upper)		No load, rising edge, hysteresis = 1%		+7		+13	%
INPUTS AND OUTPUTS							
Logic Input High Voltage		$\overline{SKIP}$, $\overline{SHDN}$, MODE, FBSEL0, FBSEL1		2.0			V
Logic Input Low Voltage		$\overline{SKIP}$, $\overline{SHDN}$, MODE, FBSEL0, FBSEL1				0.8	V

Note 2: Guaranteed by design. Not production tested.
Note 3: Not tested; guaranteed by layout. Maximum output current may be limited by thermal capability to a lower value.
Note 4: V_{TARGET} is the set output voltage determined by V_{REFIN}, FBSEL0, and FBSEL1.
Note 5: Specifications to -40°C are guaranteed by design, not production tested.

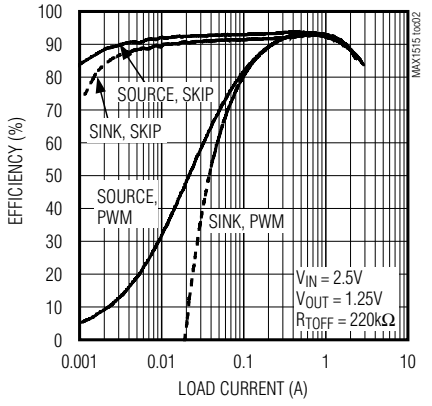
Typical Operating Characteristics

(MAX1515 Circuit of Figure 1, V_{IN} = 2.5V, V_{DD} = V_{CC} = $\overline{SHDN}$ = MODE = 3.3V, T_A = +25°C, unless otherwise noted.)

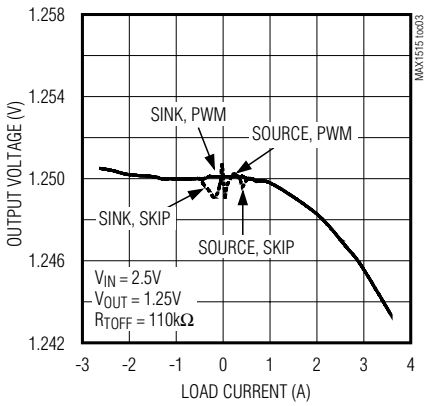
1.25V OUTPUT EFFICIENCY vs. LOAD CURRENT



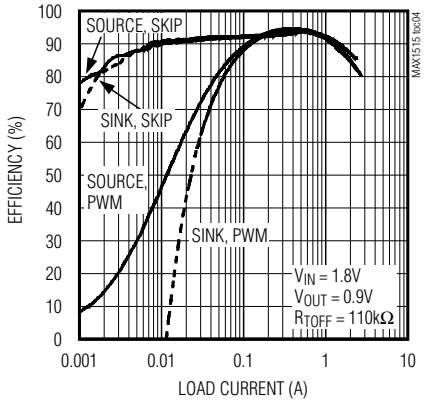
1.25V OUTPUT EFFICIENCY vs. LOAD CURRENT



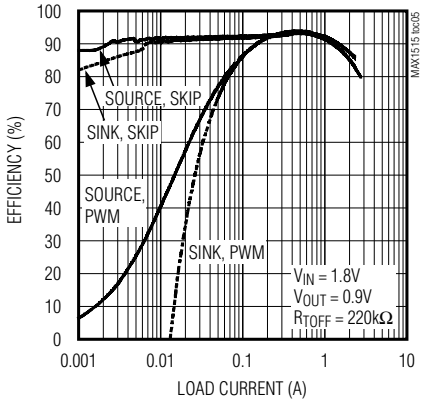
1.25V OUTPUT VOLTAGE vs. LOAD CURRENT



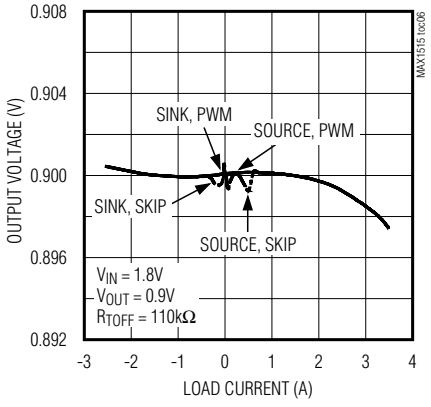
0.9V OUTPUT EFFICIENCY vs. LOAD CURRENT



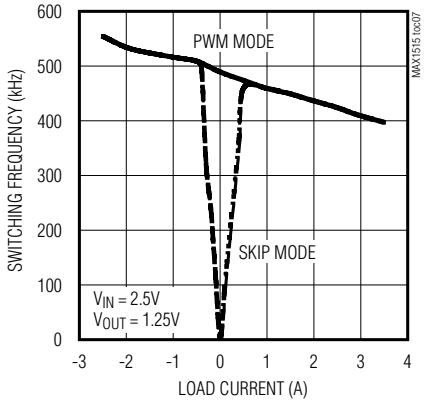
0.9V OUTPUT EFFICIENCY vs. LOAD CURRENT



0.9V OUTPUT VOLTAGE vs. LOAD CURRENT



SWITCHING FREQUENCY vs. LOAD CURRENT

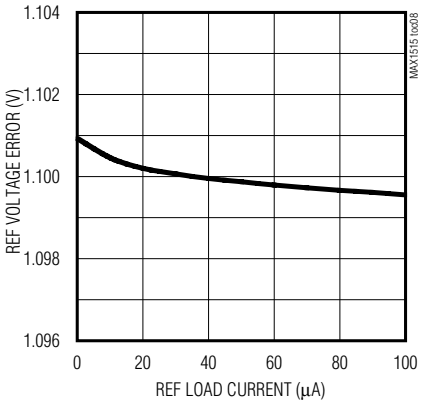


Low-Voltage, Internal Switch, Step-Down/DDR Regulator

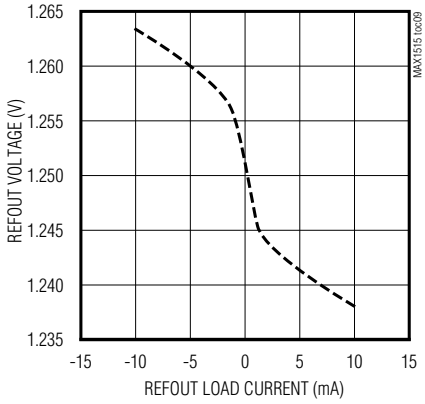
Typical Operating Characteristics (continued)

(MAX1515 Circuit of Figure 1, V_{IN} = 2.5V, V_{DD} = V_{CC} = $\overline{SHDN}$ = MODE = 3.3V, T_A = +25°C, unless otherwise noted.)

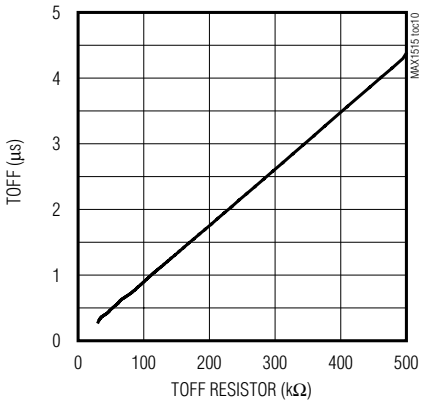
REF VOLTAGE vs. REF LOAD CURRENT



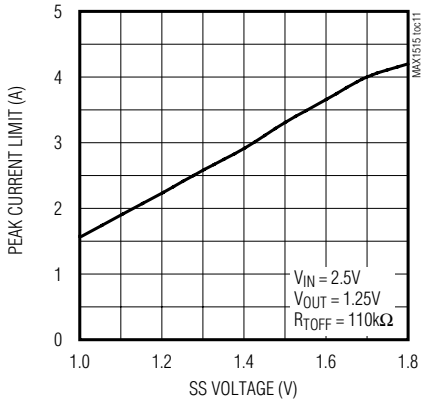
REFOUT VOLTAGE REGULATION vs. LOAD CURRENT



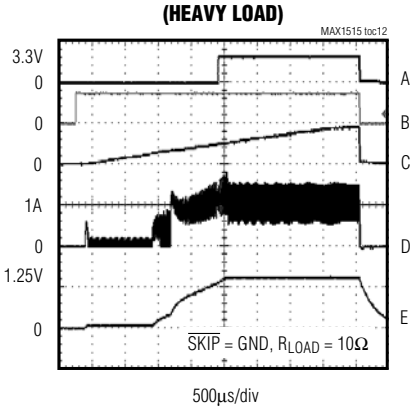
TOFF TIME vs. TOFF RESISTOR



PEAK CURRENT LIMIT vs. SS VOLTAGE



STARTUP AND SHUTDOWN WAVEFORM (HEAVY LOAD)

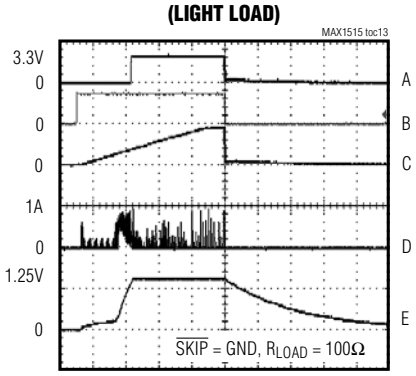


A: PGOOD, 5V/div
B: SS, 2V/div
C: $\overline{SHDN}$, 5V/div
D: INDUCTOR CURRENT, 1A/div
E: OUTPUT VOLTAGE, 1V/div

Typical Operating Characteristics (continued)

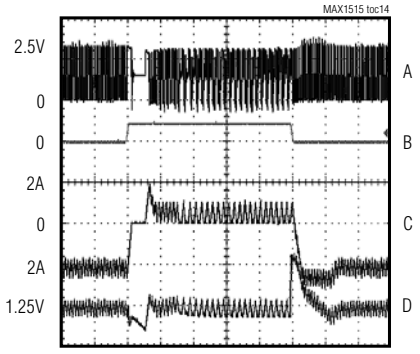
(MAX1515 Circuit of Figure 1, V_{IN} = 2.5V, V_{DD} = V_{CC} = $\overline{SHDN}$ = MODE = 3.3V, T_A = +25°C, unless otherwise noted.)

STARTUP AND SHUTDOWN WAVEFORM (LIGHT LOAD)



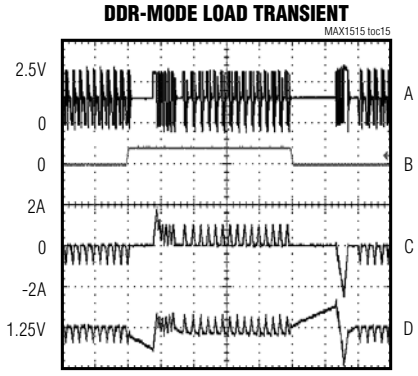
A: PGOOD, 5V/div
B: SS, 2V/div
C: $\overline{SHDN}$, 5V/div
D: INDUCTOR CURRENT, 1A/div
E: OUTPUT VOLTAGE, 1V/div

DDR-MODE LOAD TRANSIENT



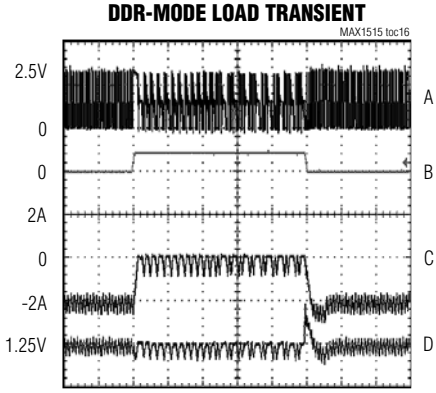
A: LX, 2V/div
B: LOAD CONTROL, 5V/div
$\overline{SKIP}$ = GND
C: INDUCTOR CURRENT, 2A/div
D: OUTPUT VOLTAGE, 50mV/div

DDR-MODE LOAD TRANSIENT



A: LX, 2V/div
B: LOAD CONTROL, 5V/div
$\overline{SKIP}$ = GND
C: INDUCTOR CURRENT, 2A/div
D: OUTPUT VOLTAGE, 50mV/div

DDR-MODE LOAD TRANSIENT



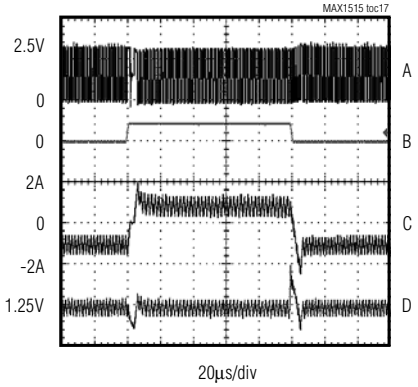
A: LX, 2V/div
B: LOAD CONTROL, 5V/div
$\overline{SKIP}$ = GND
C: INDUCTOR CURRENT, 2A/div
D: OUTPUT VOLTAGE, 50mV/div

Low-Voltage, Internal Switch, Step-Down/DDR Regulator

Typical Operating Characteristics (continued)

(MAX1515 Circuit of Figure 1, V_{IN} = 2.5V, V_{DD} = V_{CC} = $\overline{SHDN}$ = MODE = 3.3V, T_A = +25°C, unless otherwise noted.)

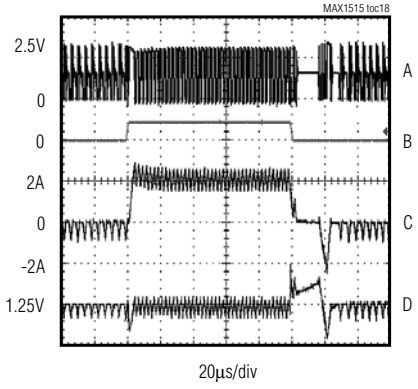
DDR-MODE LOAD TRANSIENT



20µs/div

A: LX, 2V/div
B: LOAD CONTROL, 5V/div
$\overline{SKIP}$ = GND
C: INDUCTOR CURRENT, 2A/div
D: OUTPUT VOLTAGE, 50mV/div

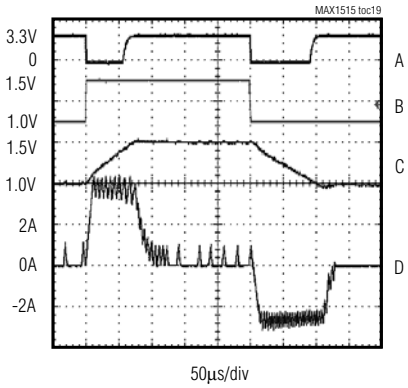
DDR-MODE LOAD TRANSIENT



20µs/div

A: LX, 2V/div
B: LOAD CONTROL, 5V/div
$\overline{SKIP}$ = GND
C: INDUCTOR CURRENT, 2A/div
D: OUTPUT VOLTAGE, 50mV/div

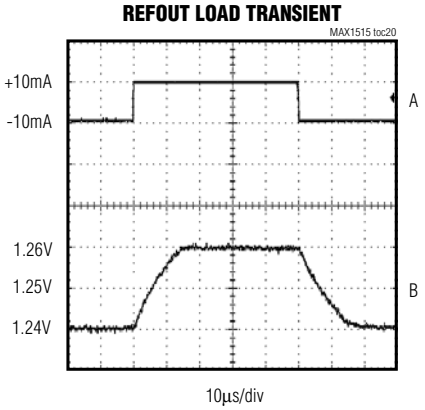
REFIN TRANSITION



50µs/div

A: PGOOD, 5V/div
B: REFIN, 0.5V/div
$\overline{SKIP}$ = GND
C: OUTPUT VOLTAGE, 0.5V/div
D: INDUCTOR CURRENT, 2A/div

REFOUT LOAD TRANSIENT



10µs/div

A: REFOUT LOAD, 20mA/div
B: REFOUT VOLTAGE, 10mV/div

Pin Description

PIN	NAME	FUNCTION
1, 2	PGND	Power Ground. Internal connection to the source of the internal synchronous-rectifier switch. Connect both PGND pins together.
3	IC	Internally Connected Pin. Connect to PGND.
4	V_{DD}	Supply Input for the Low-Side Gate Drive and REFOUT Buffer. Connect to the system supply voltage, +3.0V to +3.6V. Bypass to PGND with a 1µF (min) ceramic capacitor. V_{DD} supplies power to the drivers and the REFOUT buffer.
5	REFOUT	REFIN Buffered Output. REFOUT provides a buffered output voltage of REFIN when MODE = V_{CC}. Bypass to GND with a 0.47µF ceramic capacitor. REFOUT is disabled when MODE = GND.
6	SS	Soft-Start. Connect a capacitor from SS to GND to limit the inrush current during startup.
7	PGOOD	Power-Good Open-Drain Output. PGOOD is low when the output voltage is more than 10% above or below the normal regulation point. PGOOD is high impedance when the output is in regulation. PGOOD is low in shutdown.
8	TOFF	Off-Time Select Input. Connect a resistor from TOFF to GND to adjust the off-time.
9	FB	Feedback Input. In DDR mode (MODE = V_{CC}), FB regulates to the voltage at REFIN. In non-DDR mode (MODE = GND), connect directly to the output for preset voltage operation or to a resistive voltage-divider for adjustable-mode operation.
10	COMP	Integrator Compensation. Connect a 470pF capacitor from COMP to V_{CC} for integrator compensation.
11	V_{CC}	Analog Supply Input. Connect to the system supply voltage, +3.0V to +3.6V, with a series 10Ω resistor. Bypass to GND with a 1µF (min) ceramic capacitor.
12	GND	Analog Ground. Connect exposed backside pad to GND.
13	REF	+1.1V Reference Voltage Output. Bypass to GND with a 1.0µF bypass capacitor. Can supply 50µA for external loads. Reference turns off in shutdown.
14	REFIN	External Reference Input. In DDR mode (MODE = V_{CC}), REFIN sets the voltage that FB regulates to. In non-DDR mode (MODE = GND), connect REFIN to REF.
15	$\overline{SHDN}$	Shutdown Control. Low disables the switching regulator. $\overline{SHDN}$ and MODE select the operational mode of the MAX1515. $\overline{SHDN}$ MODE Description Low Low Step-down regulator and REFOUT OFF Low High Step-down regulator OFF, REFOUT active High Low Step-down regulator ON, non-DDR mode, REFOUT OFF High High Step-down regulator ON, DDR mode, REFOUT active
16	MODE	Mode-Select Pin. Mode sets the regulator into DDR mode or non-DDR operation mode, and controls the REFOUT buffer. When MODE = V_{CC}, MAX1515 is set in DDR mode and REFOUT is active. When MODE = GND, MAX1515 is set in non-DDR mode and REFOUT is disabled. See the *Modes of Operation (MODE)* section.
17	FBSEL0	Used with FBSEL1 to set the output voltage of the step-down regulator when MODE = GND. Connect to GND if MODE = V_{CC}.

Low-Voltage, Internal Switch, Step-Down/DDR Regulator

Pin Description (continued)

PIN	NAME	FUNCTION
18	FBSEL1	Used with FBSEL0 to set the output voltage of the step-down regulator when MODE = GND. Connect to GND if MODE = V_{CC}.
19	$\overline{SKIP}$	Pulse-Skipping Control Input. Connect to V_{CC} for low-noise, forced-PWM mode. Connect to GND to enable automatic pulse-skipping operation.
20	BST	Boost Flying-Capacitor Connection. Connect an external 0.01µF capacitor as shown in the standard application circuit (Figure 1).
21, 22	LX	Inductor Switched Node. LX is the connection for the source of the high-side NMOS power switch and drain of the low-side NMOS synchronous-rectifier switch. Connect both LX pins together.
23, 24	IN	Power Input. Supply voltage input for the switching regulator. Connect to a +1.3V to +3.6V supply voltage. Connect both IN pins together.

Table 1. Component Selection for Standard Applications

COMPONENT	±2A AT 1.25V_{OUT} DDR MODE (MODE = V_{CC})		±2A AT 0.9V_{OUT} DDR MODE (MODE = V_{CC})	
Input Voltage (V_{IN})	2.3V to 2.7V		1.6V to 2.0V	
Output Voltage (V_{OUT})	1.25V		0.9V	
C_{IN}, Input Capacitor	33µF, 6.3V, ceramic TDK C3225XR0J336V		33µF, 6.3V, ceramic TDK C3225XR0J336V	
Switching Frequency (f_{SW})	250kHz	500kHz	250kHz	500kHz
L, Inductor	2.5µH, 4.5A, Sumida CDRH8D28-2R5	1.2µH, 6.8A, Sumida CDR7D28MN-1R2	2.5µH, 4.5A, Sumida CDRH8D28-2R5	1.2µH, 6.8A, Sumida CDR7D28MN-1R2
C_{OUT}, Output Capacitor	330µF, 18mΩ Sanyo 2R5TPE330MI POSCAP	220µF, 18mΩ Sanyo 2R5TPE220MI POSCAP	330µF, 18mΩ Sanyo 2R5TPE330MI POSCAP	220µF, 18mΩ Sanyo 2R5TPE220MI POSCAP
R_{TOFF}	221kΩ, 1%	110kΩ, 1%	221kΩ, 1%	110kΩ, 1%

Table 2. Component Suppliers

SUPPLIER	WEBSITE
Coilcraft	www.coilcraft.com
Coiltronics	www.coiltronics.com
Kemet	www.kemet.com
Panasonic	www.panasonic.com
Sanyo	www.sanyo.com
Sumida	www.sumida.com
Taiyo Yuden	www.t-yuden.com
TDK	www.component.tdk.com
TOKO	www.tokoam.com

Standard Application Circuit

The MAX1515 standard application circuit (Figure 1) generates a tracking output voltage and a reference buffer output required for DDR termination regulators. See Table 1 for component selections. Table 2 lists the component manufacturers.

Detailed Description

The MAX1515 synchronous, current-mode, constant off-time, PWM DC-DC converter steps down an input voltage (V_{IN}) from +1.3V to +3.6V to an output voltage from +0.5V to +2.7V. The MAX1515 output delivers up to 3A of continuous current. Internal 40mΩ NMOS power switches improve efficiency, reduce component count, and eliminate the need for a boost diode or any external Schottky diodes (Figure 2).

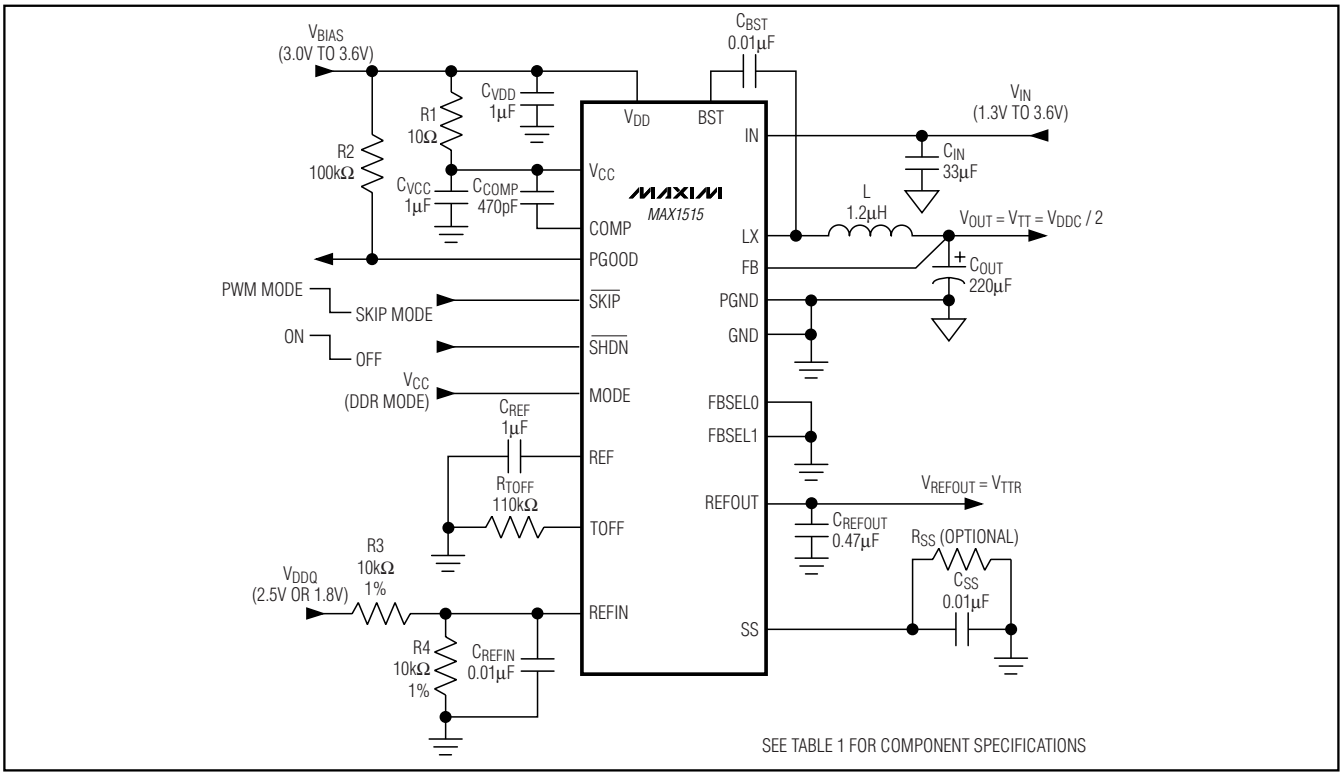


Figure 1. Standard Application Circuit

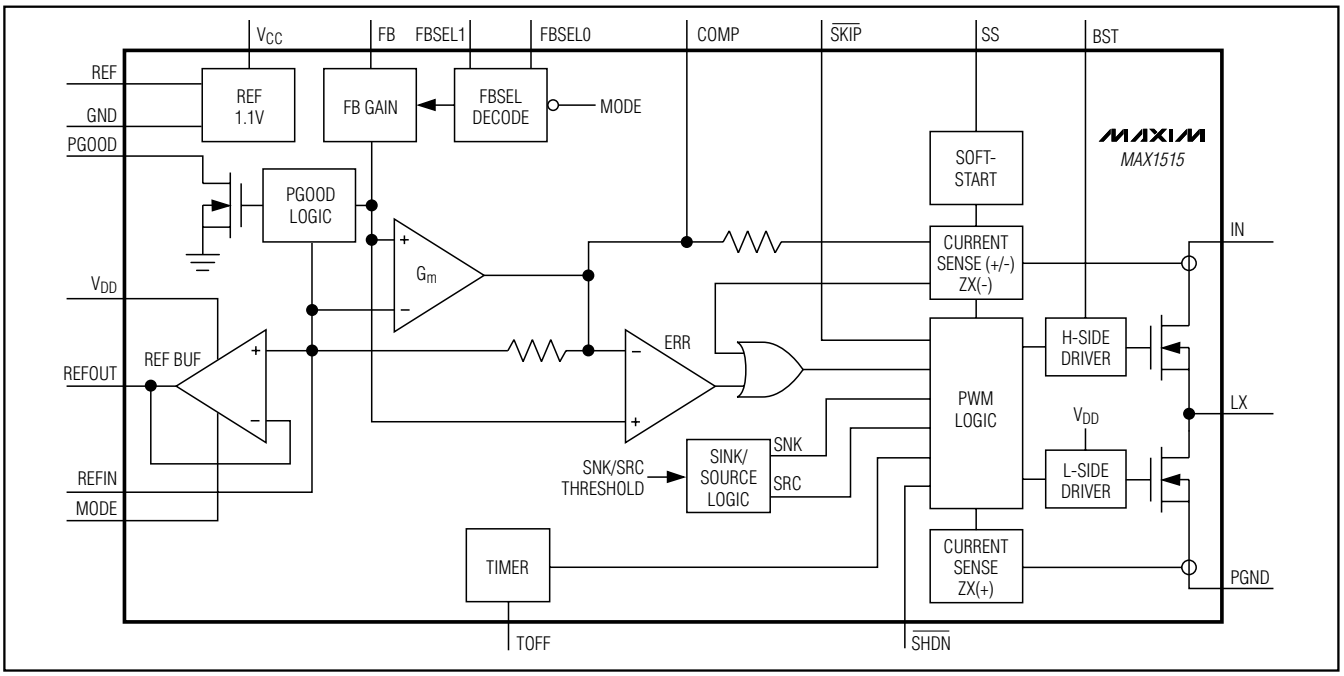


Figure 2. Functional Diagram

Low-Voltage, Internal Switch, Step-Down/DDR Regulator

+3.3V Bias Supply (V_{CC} and V_{DD})

The MAX1515 requires a 3.3V bias supply for its internal circuitry. Typically, this 3.3V bias supply is the notebook's 95%-efficient, 3.3V system supply. The 3.3V bias supply must provide V_{CC} (PWM controller) and V_{DD} (gate-drive and reference buffer power), so the maximum current drawn is:

$$I_{BIAS} = I_{CC} + I_{REFOUT} + f_{SW} (Q_{G(LOW)} + Q_{G(HIGH)})$$

where I_{CC} is 450µA (typ), f_{SW} is the switching frequency, and $Q_{G(LOW)}$ and $Q_{G(HIGH)}$ are the internal MOSFET total gate charge of approximately 1nC.

The input supply (V_{IN}) and 3.3V bias inputs (V_{CC} and V_{DD}) can be connected together if the input source is a fixed 3.0V to 3.6V supply. If the 3.3V bias supply powers up prior to the input supply, the enable signal ($\overline{SHDN}$ going from low to high) must be delayed until the input voltage is present to ensure startup.

Current Limit

The MAX1515 provides peak current limiting to protect the MOSFETs during source/sink overload and short circuit. During source mode the controller switches the high-side MOSFET off when the inductor current exceeds 4.2A. Use the following equation to calculate the maximum source current:

$$I_{SOURCE\_MAX} = I_{LIMIT\_P} - \frac{V_{OUT} \times t_{OFF}}{2 \times L}$$

where I_{SOURCE_MAX} is the maximum source current, I_{LIMIT_P} is the source inductor current limit (4.2A typ), and t_{OFF} is the fixed off-time. For typical operating conditions and component selection, this results in a maximum source current of 3.7A.

In sink mode, the MAX1515 does not issue an off-time until the inductor current is above -3.2A. Use the following equation to calculate the maximum sink current:

$$I_{SINK\_MAX} = I_{LIMIT\_N} + \frac{V_{OUT} t_{OFF} - 2(V_{IN} - V_{OUT})\ t_{DLY}}{2\ L}$$

where I_{SINK_MAX} is the maximum sink current, I_{LIMIT_N} is the sink inductor current limit (-3.0A typ), t_{DLY} is the current-limit propagation delay of approximately 500ns, and t_{OFF} is the fixed off-time. For typical operating conditions and component selection, this results in a maximum sink current of -2.5A.

Soft-Start Current Limit

Soft-start allows a gradual increase of the internal current limit to reduce input surge currents at startup and at exit from shutdown. A timing capacitor, C_{SS}, placed from SS to GND sets the rate at which the internal current limit is changed. Upon power-up, when the device comes out of undervoltage lockout (2.6V typ) or after the $\overline{SHDN}$ pin is pulled high, a 5µA (typ) constant-current source charges the soft-start capacitor and the voltage on SS increases. When the voltage on SS is less than approximately 0.7V, the current limit is set to zero. As the voltage increases from 0.7V to approximately 1.8V, the current limit is adjusted from 0 to the current-limit threshold (see the *Electrical Characteristics*). The voltage across the soft-start capacitor changes with time according to the equation:

$$V_{SS} = \frac{I_{SS(SRC)} \times t}{C_{SS}}$$

where $I_{SS(SRC)}$ is the soft-start source current from the *Electrical Characteristics*.

The time when full current limit is available is given by:

$$t = \frac{C_{SS} \times 1.8V}{I_{SS(SRC)}}$$

The soft-start current limit varies with the voltage on the soft-start pin, SS, according to the equation:

$$SSI_{LIMIT} = \frac{V_{SS} - 0.7V}{V_{REF}} \times I_{LIMIT\_P}$$

where I_{LIMIT_P} is the positive current threshold from the *Electrical Characteristics*. The constant-current source stops charging once the voltage across the soft-start capacitor reaches 1.8V (Figure 3).

Adjustable Positive Current Limit

The MAX1515 has internal current-limit circuitry that limits the maximum current through the NMOS to 4.2A. For applications that require a lower current limit, the maximum current limit can be reduced by placing a resistor (R_{SS}) from SS to GND. The time constant for the soft-start current limit is $R_{SS} \times C_{SS}$.

$$R_{SS} = \left(\frac{V_{REF} \times I_{LIMIT}}{I_{LIMIT\_P}} + 0.7V \right) / I_{SS(SRC)}$$

where I_{LIMIT} is the desired reduced current limit, and I_{LIMIT_P} and $I_{SS(SRC)}$ are taken from the *Electrical Characteristics*.

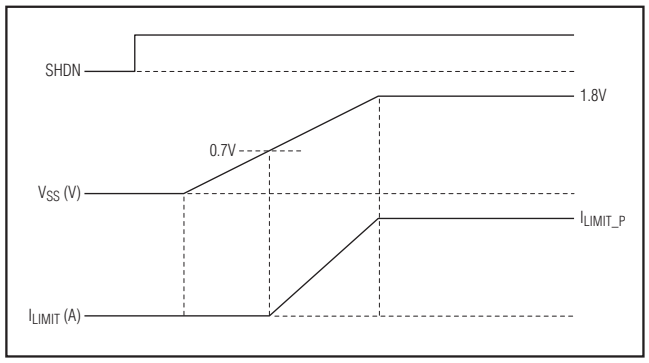


Figure 3. Soft-Start Current Limit

Short-Circuit/Overload Protection

The MAX1515 can sustain a constant short circuit or overload. Under a source-mode short-circuit or overload condition, when $V_{FB} < 0.3 \times V_{TARGET}$, the MAX1515 uses an extended off-time to control the current. Operation during a short circuit or overload is similar to forced-PWM mode except the off-time is 4 x t_{OFF}. At the end of each off-time, the high-side NMOS switch turns on and remains on until the output is in regulation or the current through the switch increases to the maximum current limit. When the high-side NMOS switch turns off, it remains off for four times the programmed off-time (t_{OFF}), and the low-side NMOS synchronous switch turns on. Since either NMOS switch is always on, the inductor current is continuous. The RMS inductor current during a short circuit remains below the maximum current-limit threshold. The MAX1515 operates using the extended off-time until the short circuit or overload is removed and $V_{FB} > 0.3 \times V_{TARGET}$. Prolonged short circuit or overload can result in thermal shutdown.

Summing Comparator

Three signals are added together at the input of the summing comparator (Figure 2): an output-voltage error signal relative to the reference voltage, an integrated output-voltage error-correction signal, and the sensed high-side NMOS switch current. The integrated error signal is provided by a transconductance amplifier with an external capacitor at COMP. This integrator provides high DC accuracy without the need for a high-gain amplifier. Connecting a capacitor at COMP modifies the overall loop response (see the *Integrator Amplifier* section).

Integrator Amplifier

The MAX1515 includes an internal transconductance amplifier that improves the output DC accuracy. A capacitor, C_{COMP}, from COMP to V_{CC} compensates the transconductance amplifier. For stability, choose C_{COMP} = 470pF.

Modes of Operation (MODE)

Use MODE to configure the MAX1515 for DDR mode (MODE = V_{CC}) or non-DDR mode (MODE = GND). In DDR mode, the MAX1515 can sink current even while $\overline{SKIP}$ is low (see the *Pulse Skipping (Source Mode)* and *Pulse Skipping (Sink Mode)* sections). Also, DDR mode enables the REFOUT buffer, providing a buffered output of the REFIN voltage. In non-DDR mode, the MAX1515 can only source current when $\overline{SKIP}$ is low. The REFOUT buffer is also disabled in non-DDR mode.

Light-Load Operation ($\overline{SKIP}$)

The MAX1515 includes a pulse-skipping mode that reduces current consumption during light loads. To configure the MAX1515 for pulse-skipping mode, connect $\overline{SKIP}$ to GND. Forced-PWM mode keeps the switching frequency relatively constant and is desirable in applications that must always keep the frequency of conducted and radiated emissions in a narrow band. Visit Maxim's website (www.maxim-ic.com) for more information on how to control electromagnetic interference (EMI). Pulse-skipping mode has a dynamic switching frequency under light loads and is desirable in applications that require high efficiency at light loads.

Forced-PWM Mode

Connect $\overline{SKIP}$ to V_{CC} to force the MAX1515 to operate in low-noise, constant-off-time PWM mode. Constant off-time PWM architecture provides a relatively constant switching frequency (see the *Frequency Variation with Output Current* section). A single resistor (R_{TOFF}) sets the high-side NMOS power-switch off-time that results in a switching frequency up to 1MHz, allowing performance trade-offs in efficiency, switching noise, component size, and cost.

Forced-PWM mode regulates the output voltage by increasing the high-side NMOS switch on-time to increase the amount of energy transferred to the load per cycle. At the end of each off-time, the high-side NMOS switch turns on and remains on until the output is in regulation or the current through the switch reaches the 4.2A current limit. When the high-side NMOS switch turns off, it remains off for the programmed off-time (t_{OFF}), and the low-side NMOS synchronous switch turns on. The low-side NMOS switch remains on until the end of t_{OFF}. Since either NMOS switch is always on in PWM mode, the inductor current is continuous.

Low-Voltage, Internal Switch, Step-Down/DDR Regulator

Table 3. Modes of Operation

$\overline{SHDN}$	MODE PIN	$\overline{SKIP}$	REFOUT BUFFER	STEP-DOWN REGULATOR MODE	STEP-DOWN REGULATOR CURRENT
Low	Low	X	Off, High-Z	Off	Off
Low	High	X	On	Off	Off
High	Low	Low	Off, High-Z	On, non-DDR mode. FB regulates to preset voltage or 0.5V.	Source only. Pulse-skipping mode.
High	Low	High	Off, High-Z	On, non-DDR mode. FB regulates to preset voltage or 0.5V.	Source/sink. Forced-PWM mode.
High	High	Low	On	On, DDR mode. FB regulates to REFIN.	Source/sink. Pulse-skipping mode.
High	High	High	On	On, DDR mode. FB regulates to REFIN.	Source/sink. Forced-PWM mode.

X = Don't care.

Pulse Skipping (Source Mode)

Connect $\overline{SKIP}$ to GND to allow the MAX1515 to automatically switch between high-efficiency pulse-skipping mode under light loads and PWM mode under heavy loads. The transition from PWM mode to pulse-skipping mode occurs when the load current is half the pulse-skipping mode current threshold (800mA typ).

In pulse-skipping mode, the switching frequency is reduced to increase efficiency. The inductor current is discontinuous in this mode, and the MAX1515 only initiates an LX switching cycle when $V_{FB} < V_{REFIN}$. When V_{FB} falls below V_{REFIN}, the high-side NMOS switch turns on and remains on until output is in regulation and the current through the switch increases to the positive pulse-skipping-mode current threshold (I_{SKIP_P}) of 800mA. When the high-side NMOS switch turns off, the low-side NMOS synchronous switch turns on and remains on until the current through the switch decreases to the zero-cross-current threshold of 200mA.

Pulse Skipping (Sink Mode)

When pulse-skipping operation is selected ($\overline{SKIP}$ = GND) while in DDR mode (MODE = V_{CC}), the MAX1515's source/sink controller switches operating modes when the output voltage crosses either hysteretic sink/source thresholds (V_{REFIN} ±25mV). In pulse-skipping source mode, the MAX1515 regulates the valley of the output ripple voltage (see the *Pulse Skipping (Source Mode)* section). When the output voltage rises above the sink-mode threshold, the MAX1515 enters sink mode. The MAX1515 begins each sink-mode cycle by turning on the low-side NMOS. The low-side NMOS remains on until the off-time (t_{OFF}). After the low-side NMOS turns off, the high-side NMOS turns on and remains on until the current through the switch reaches the zero-cross-current threshold of -350mA. As long as the output voltage remains below the feedback threshold, the controller remains in the high-impedance state. Under light-load conditions, this allows the sink-mode controller to automatically skip pulses. Under heavy-load conditions, the output voltage remains above the feedback threshold, forcing the sink-mode controller to emulate typical forced-PWM operation.

The pulse-skipping current threshold allows the sink-mode control scheme to automatically switch between pulse-skipping PFM and nonskipping PWM operation. This mechanism forces the boundary between continuous and discontinuous inductor-current operation to be half the negative pulse-skipping current threshold.

Table 4. Output-Voltage Programming

FBSEL0	FBSEL1	OUTPUT VOLTAGE
GND	GND	Adjustable $V_{FB} = V_{REFIN}$
GND	V_{CC}	1.5V
V_{CC}	GND	1.8V
V_{CC}	V_{CC}	2.5V

Output Voltage in Non-DDR Mode

In non-DDR mode (MODE = GND and $V_{REFIN} = V_{REF}$), the output of the MAX1515 is selectable between one of three preset output voltages: 2.5V, 1.8V, and 1.5V. For a preset output voltage, connect FB to the output voltage and connect FBSEL0 and FBSEL1 as indicated in Table 4. For an adjustable output voltage, connect FBSEL0 and FBSEL1 to GND and connect REFIN to a

resistive divider between REF and ground (Figure 5). Regulation is maintained for adjustable output voltages when $V_{FB} = V_{REFIN}$. Use 100kΩ for R_B. R_A is given by the equation:

$$V_{FB} = V_{REF}\left(\frac{R_B}{R_A + R_B}\right)$$

where $V_{REF} = 1.1V$.

The preset output voltages use an internally trimmed resistor-divider network that sets the output voltage to the correct level when REFIN is connected to REF. Connecting REFIN to other voltage levels while using the preset voltage modes results in a ratiometrically scaled output voltage.

Output Voltage in DDR Mode

In DDR mode (MODE = V_{CC}), the MAX1515 regulates FB to the voltage set at REFIN. For DDR applications, the termination supply must track to exactly half the memory supply voltage. Figure 1 shows the MAX1515 configured for DDR applications.

Reference Buffer (REFOUT)

A unity-gain amplifier provides a buffered output for the reference input (V_{REFIN}) when MODE = V_{CC}. This transconductance amplifier must be compensated with a 0.47µF or greater ceramic capacitor. Larger capacitor values decrease the amplifier's bandwidth, thereby increasing the response time to dynamic input-voltage changes. The buffer allows this dynamic reference to remain within ±20mV of the input voltage (V_{REFIN}) even when loaded with ±5mA. The input voltage range of the amplifier is 0.5V to 1.5V. The reference buffer shuts down when MODE = GND.

Power-Good Output (PGOOD)

PGOOD is the open-drain output for a window comparator that continuously monitors the output. PGOOD is actively held low in shutdown and during soft-start. After soft-start terminates, PGOOD becomes high impedance as long as the respective output voltage is within ±10% of the nominal regulation voltage. When the output voltage drops 10% below or rises 10% above the nominal regulation voltage, the MAX1515 pulls the power-good output (PGOOD) low by turning on the MOSFET (Figure 2). For logic-level output voltages, connect an external pullup resistor between PGOOD and V_{CC}. A 100kΩ resistor works well in most applications.

Thermal Shutdown

The MAX1515 features a thermal fault-protection circuit. When the junction temperature rises above +165°C, a thermal sensor shuts down the MAX1515 regardless of $V_{\overline{SHDN}}$. The MAX1515 is reactivated after the junction temperature cools to +150°C.

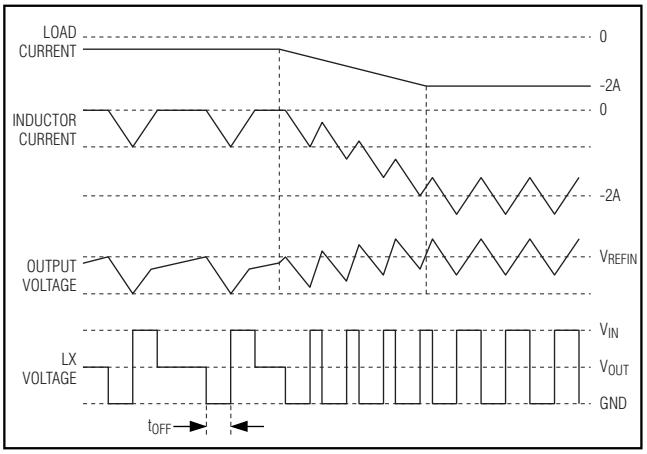


Figure 4. Sink-Mode Waveforms

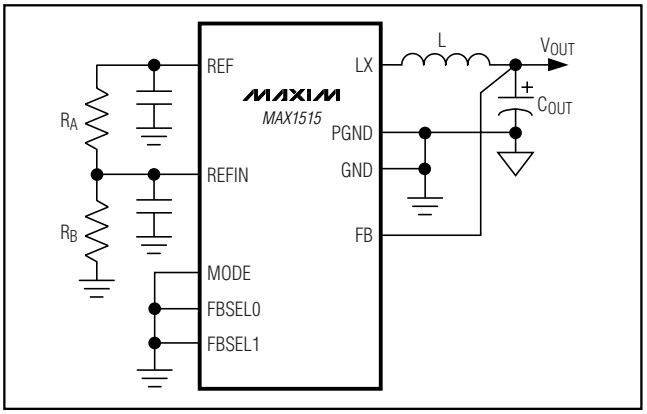


Figure 5. Setting V_{OUT} with a Resistive Voltage-Divider at REFIN

Thermal Resistance

Junction-to-ambient thermal resistance, θ_{JA}, is highly dependent on the amount of copper area connected to the exposed backside pad. Airflow over the board significantly reduces θ_{JA}. For heatsinking purposes, evenly distribute the copper area connected at the IC among the high-current pins. Refer to the Maxim website (www.maxim-ic.com) for QFN thermal considerations.

Power Dissipation

Power dissipation in the MAX1515 is dominated by conduction losses in the two internal power switches. Power dissipation due to supply current in the control section and average current used to charge and discharge the gate capacitance of the internal switches (i.e., switching losses—PSL) is approximately:

$$PSL = C \times V_{IN}^2 \times f_{SW}$$

Low-Voltage, Internal Switch, Step-Down/DDR Regulator

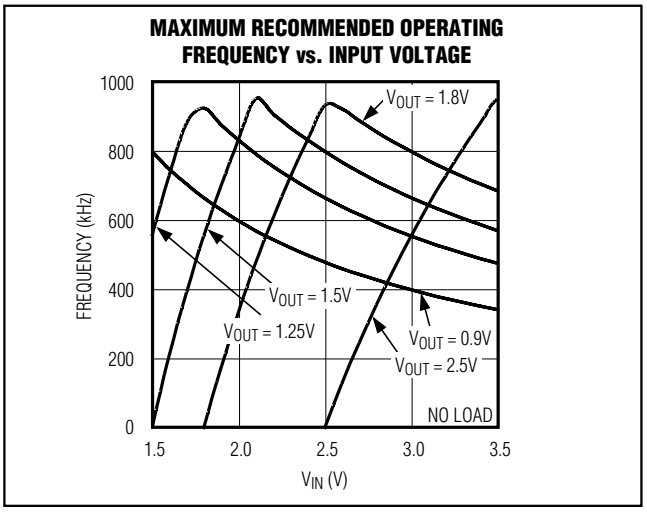


Figure 6. Maximum Operating Frequency vs. Input Voltage

where:

C = 5nF

f_{SW} = switching frequency

The combined conduction losses (PCL) in the two power switches are approximated by:

$$PCL = I_{OUT}^2 \times R_{NMOS}$$

where:

I_{OUT} = load current

R_{NMOS} = NMOS switch on-resistance

Design Procedure

For typical DDR applications, use the recommended component values in Table 1. For other applications, use the recommended component values in Table 5, or take the following steps:

1) Select the desired PWM-mode switching frequency. See Figure 6 for maximum operating frequency.
2) Select the constant off-time as a function of input voltage, output voltage, and switching frequency.
3) Select R_{TOFF} as a function of off-time.
4) Select the inductor as a function of output voltage, off-time, and peak-to-peak inductor current.

Programming the No-Load Switching Frequency and Off-Time

The MAX1515 features a programmable PWM mode switching frequency, which is set by the input and output voltage and the value of R_{TOFF}. R_{TOFF} sets the high-side NMOS power switch off-time in PWM mode.

Table 5. Recommended Component Values (I_{OUT} = 3A)

V_{IN} (V)	V_{OUT} (V)	f_{PWM} (kHz)	L (µH)	C_{OUT} (µF)	R_{TOFF} (kΩ)
3.3	2.5	400	1.5	100	49.9
3.3	1.8	400	2.2	150	110
3.3	1.5	480	2.2	180	110
3.3	1.2	420	2.2	220	150
2.5	1.8	430	1.2	100	49.9
2.5	1.5	320	1.8	150	110
2.5	1.2	440	1.5	180	110

Use the following equation to select the off-time according to the desired no-load switching frequency in PWM mode:

$$t_{OFF} = \frac{V_{IN} - V_{OUT}}{f_{PWM} \times V_{IN}}$$

where:

t_{OFF} = the programmed off-time

V_{IN} = the input voltage

V_{OUT} = the output voltage

f_{PWM} = no-load switching frequency, PWM mode

Select R_{TOFF} according to the formula:

$$R_{TOFF} = \left(t_{OFF} - 0.035\mu s\right)\frac{110k\Omega}{1.00\mu s}$$

V_{RTOFF} is typically 1.1V and the recommended values for R_{TOFF} range from 33.2kΩ to 499kΩ for off-times of 0.35µs to 4.5µs.

Frequency Variation with Output Current

The operating frequency of the MAX1515 in PWM mode is determined primarily by t_{OFF} (set by R_{TOFF}), V_{IN}, and V_{OUT} as shown in the following formula:

$$f_{PWM} = \frac{V_{IN} - V_{OUT} - V_{CHG}}{t_{OFF}\left(V_{IN} - V_{CHG} + V_{DISCHG}\right)}$$

where:

V_{CHG} = the voltage drop in the inductor charge path due to high-side FET R_{NMOS} and inductor DCR

V_{DISCHG} = the voltage drop in the inductor discharge path due to low-side FET R_{NMOS} and inductor DCR

While sourcing current, V_{CHG} and V_{DISCHG} increase with source load current and the voltage across the inductor decreases. This causes the frequency to drop. Conversely, while sinking current, V_{CHG} and V_{DISCHG} decrease with sink load current and the voltage across the inductor increases. Approximate the change in frequency with the following formula:

$$\Delta f_{PWM} = -\frac{I_{OUT} \times R_{DROP}}{V_{IN} \times t_{OFF}}$$

where R_{DROP} is the resistance of the internal MOSFETs (40mΩ typ) and the inductor.

Inductor Selection

The key inductor parameters must be specified: inductor value (L) and peak current (I_{PEAK}). The following equation includes a constant, denoted as LIR, which is the ratio of peak-to-peak inductor AC ripple current to maximum DC load current. A higher value of LIR allows smaller inductance but results in higher losses and ripple. A good compromise between size and losses is found at approximately a 25% ripple-current to load-current ratio (LIR = 0.25), which corresponds to a peak inductor current 1.125 times the DC load current:

$$L = \frac{V_{OUT} \times t_{OFF}}{I_{OUT(MAX)} \times LIR}$$

Additionally, the minimum inductance chosen must be high enough to limit the inductor current during the high-side switch on-time to less than 1A/µs.

$$L_{MIN} \geq \left(V_{IN(MAX)} - V_{OUT}\right) \times \frac{1\mu s}{1A}$$

The peak-inductor current at full load is 1.125 x $I_{OUT(MAX)}$ if the above equation is used; otherwise, the peak current is calculated by:

$$I_{PEAK} = I_{OUT(MAX)} + \frac{V_{OUT} \times t_{OFF}}{2 \times L}$$

Choose an inductor with a saturation current at least as high as the peak-inductor current. The inductor selected should exhibit low losses at the chosen operating frequency.

Input Capacitor Selection

The input-filter capacitors reduce peak currents and noise at the voltage source. Place a low-ESR and low-ESL 0.1µF capacitor for noise filtering no further than 5mm from IN. Select the bulk input capacitor according to the RMS input ripple-current requirements and voltage rating:

$$I_{RMS} = I_{OUT(MAX)}\left(\frac{\sqrt{V_{OUT}(V_{IN} - V_{OUT})}}{V_{IN}}\right)$$

Output Capacitor Selection

The output filter capacitor affects the output-voltage ripple, output load-transient response, and feedback-loop stability. For stable operation, the MAX1515 requires a minimum output ripple voltage of $V_{RIPPLE} \geq 1\% \times V_{OUT}$. The minimum ESR of the output capacitor is calculated by:

$$ESR \geq 1\% \times \frac{L}{t_{OFF}}$$

Stable operation for source-only applications requires the correct output filter capacitor. When choosing the output capacitor, ensure that:

$$C_{OUT} \geq \frac{V_{REFIN} \times t_{OFF}}{V_{OUT}} \times 105\mu F/\mu s$$

For DDR applications, the output capacitance requirement needs to be two times the above requirement. The output filter capacitor must have low enough equivalent series resistance (ESR) to meet output ripple and load-transient requirements, yet have high enough ESR to satisfy stability requirements.

For applications where the output is subject to violent load transients, the output capacitor's size depends on how much ESR is needed to prevent the output from dipping too low under a load transient. Ignoring the sag due to finite capacitance:

$$R_{ESR} \leq \frac{V_{STEP}}{\Delta I_{OUT(MAX)}}$$

In applications without large and fast load transients, the output capacitor's size often depends on how much ESR is needed to maintain an acceptable level of output voltage ripple. The output ripple voltage of a step-down controller equals the total inductor ripple current multiplied by the output capacitor's ESR. Therefore, the maximum ESR required to meet ripple specifications is:

$$R_{ESR} \leq \frac{V_{RIPPLE}}{I_{OUT(MAX)}\ LIR}$$

Low-Voltage, Internal Switch, Step-Down/DDR Regulator

The actual capacitance value required relates to the physical size needed to achieve low ESR, as well as to the chemistry of the capacitor technology. Thus, the capacitor is usually selected by ESR and voltage rating rather than by capacitance value (this is true of tantalums, OS-CONs, polymers, and other electrolytics).

Transient Response

The inductor ripple current also impacts transient-response performance, especially at low V_{IN} - V_{OUT} differentials. Low inductor values allow the inductor current to slew faster, replenishing charge removed from the output filter capacitors by a sudden load step. The worst-case output sag can be calculated from:

$$V_{SAG} \approx \frac{(\Delta I_{OUT} L + V_{OUT} t_{OFF})^2}{2L \times C_{OUT}(V_{IN} - V_{OUT})} + \frac{V_{OUT} t_{OFF}^2}{2L \times C_{OUT}} + \frac{\Delta I_{OUT} t_{OFF}}{C_{OUT}}$$

where ΔI_{OUT} is the maximum load transient.

Typically, the maximum load transient is equal to the maximum load current ($\Delta I_{OUT} = I_{LOAD(MAX)}$). For DDR-termination applications, the output must source and sink current. In these applications, the actual peak-to-peak transient current (ΔI_{OUT}) is defined as the sum of both the maximum source and sink load currents:

$$\Delta I_{OUT} = \left|I_{SOURCE(MAX)}\right| + \left|I_{SINK(MAX)}\right|$$

The amount of overshoot during a full-load to no-load transient due to stored inductor energy can be calculated as:

$$V_{SOAR} \approx \frac{(\Delta I_{OUT})^2 \ L}{2C_{OUT} \ V_{OUT}}$$

When using the pulse-skipping source/sink feature (MODE = V_{CC} and $\overline{SKIP}$ = GND), the output transient voltage should not exceed or drop below the sink and source (respectively) detection thresholds (V_{REFIN} ±20mV).

Applications Information

Dropout Operation

The MAX1515 improves dropout performance by having a maximum on-time of 10µs. When working with low input voltages, the duty-factor limit must be calculated using worst-case values for on- and off-times. Keep in mind that transient-response performance of step-down regulators operated too close to dropout is poor, and bulk output capacitance must often be added (see the V_{SAG} equation in the *Design Procedure* section).

The absolute point of dropout is when the inductor current ramps down during the off-time (ΔI_{DOWN}) as much as it ramps up during the on-time (ΔI_{UP}). The ratio h = $\Delta I_{UP}/\Delta I_{DOWN}$ indicates the controller's ability to slew the inductor current higher in response to increased load, and must always be greater than 1. As h approaches 1, the absolute minimum dropout point, the inductor current cannot increase as much during each switching cycle and V_{SAG} greatly increases unless additional output capacitance is used.

A reasonable minimum value for h is 1.5, but adjusting this up or down allows trade-offs between V_{SAG}, output capacitance, and minimum operating voltage. For a given value of h, the minimum operating voltage can be calculated as:

$$V_{IN(MIN)} = V_{OUT} + V_{CHG} + \frac{h \times t_{OFF} \times (V_{OUT} + V_{DISCHG})}{t_{ON(MAX)}}$$

where V_{CHG} and V_{DISCHG} are the parasitic voltage drops in the charge and discharge paths (see the *Frequency Variation with Output Current* section), $t_{ON(MAX)}$ is from the *Electrical Characteristics*, and t_{OFF} is the programmed off-time. The absolute minimum input voltage is calculated with h = 1.

If the calculated $V_{IN(MIN)}$ is greater than the required minimum input voltage, then t_{OFF} must be reduced or output capacitance added to obtain an acceptable V_{SAG}. If operation near dropout is anticipated, calculate V_{SAG} to be sure of adequate transient response.

Dropout Design Example:

V_{OUT} = 2.5V

t_{OFF} = 1µs

$V_{CHG} = V_{DISCHG}$ = 100mV

h = 1.5

$$V_{IN(MIN)} = 2.5V + 0.1V + \frac{1.5 \times 1\mu s \times (2.5V + 0.1V)}{10\mu s}$$

$$= 2.99V$$

Dynamic Output-Voltage Transitions

By changing the voltage at REFIN, the MAX1515 can be used in applications that require dynamic output-voltage changes between two set points. An n-channel MOSFET can be used to dynamically adjust the second controller's output voltage by changing the resistive

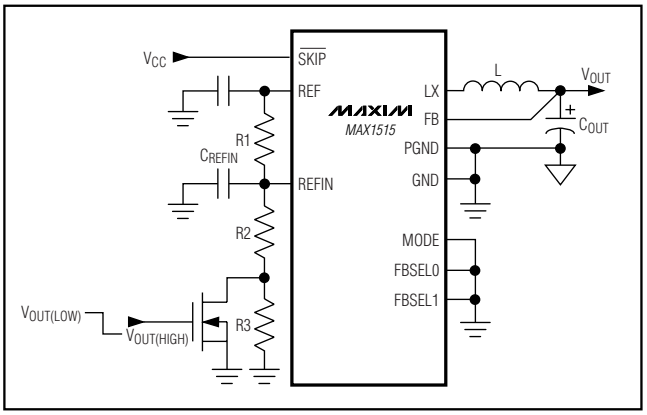


Figure 7. Dynamic Output Voltages

voltage-divider network at REFIN. The resulting output voltages are determined by the following equations:

$$V_{OUT(LOW)} = V_{REF}\left(\frac{R2}{R1+R2}\right)$$

$$V_{OUT(HIGH)} = V_{REF}\left(\frac{R2+R3}{R1+R2+R3}\right)$$

Forced-PWM operation is required to ensure fast, accurate negative voltage transitions when REFIN is lowered. Since forced-PWM operation disables the zero-crossing comparator, the inductor current can reverse under light loads, quickly discharging the output capacitors.

For a step voltage change at REFIN, the rate-of-change of the output voltage is limited by the inductor current ramp, the total output capacitance, the current limit, and the load during the transition. The inductor current ramp is limited by the voltage across the inductor and the inductance. The total output capacitance determines how much current is needed to change the output voltage. Additional load current slows down the output-voltage change during a positive REFIN voltage change, and speeds up the output-voltage change during a negative REFIN voltage change. Increasing the current-limit setting speeds up a positive output-voltage change.

To avoid tripping the power-good comparators, the reference-voltage slew rate must be slow enough that the output voltage (V_{OUT}) can accurately track the reference voltage (V_{REFIN}). Add a capacitor across REFIN and GND to control the rate-of-change of the REFIN voltage during dynamic transitions and filter noise.

With the additional capacitance, the REFIN voltage slews between the two set points with a time constant given by R_{EQ} x C_{REFIN}, where R_{EQ} is the equivalent parallel resistance seen by the slew capacitor. Referring to Figure 7, the time constant for a positive REFIN voltage transition is:

$$\tau_{POS} = \left[\frac{R1 \times (R2+R3)}{R1+R2+R3}\right] C_{REFIN}$$

and the time constant for a negative REFIN voltage transition is:

$$\tau_{POS} = \left[\frac{R1 \times R2}{R1+R2}\right] C_{REFIN}$$

PC Board Layout Guidelines

Good layout is necessary to achieve the intended output power level, high efficiency, and low noise. Good layout includes the use of a ground plane, careful component placement, and correct routing of traces using appropriate trace widths. Refer to the MAX1515 EV kit for a reference of a good layout.

The following points are in order of decreasing importance:

1) Minimize switched-current and high-current ground loops. Connect the input capacitor's ground, the output capacitor's ground, and PGND at a single point. Connect the resulting island to GND at only one point.
2) Connect the input filter capacitor less than 5mm away from IN. The connecting copper trace carries large currents and must be at least 1mm wide, preferably 2.5mm.
3) Place the LX node components as close together and as near to the device as possible. This reduces noise, resistive losses, and switching losses.
4) A ground plane is essential for optimal performance. In most applications, the circuit is located on a multilayer board, and full use of the four or more layers is recommended. Use the top and bottom layers for interconnections and the inner layers for an uninterrupted ground plane. Avoid large AC currents through the ground plane.

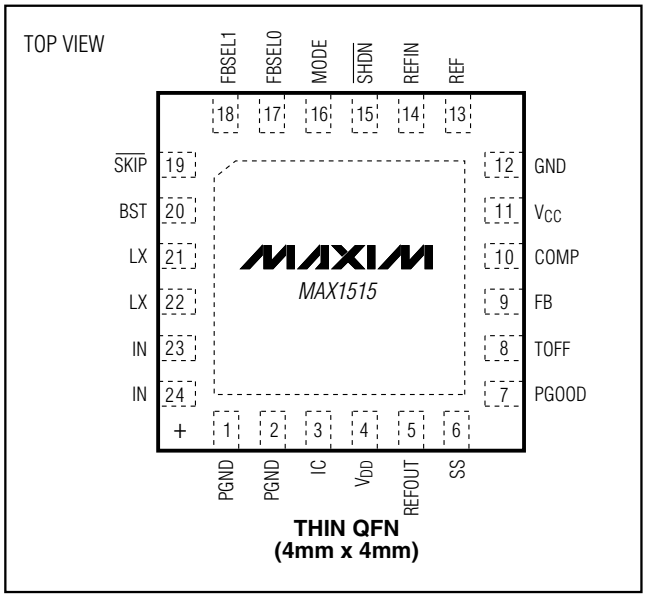
Chip Information

TRANSISTOR COUNT: 8258

PROCESS: BiCMOS

Low-Voltage, Internal Switch, Step-Down/DDR Regulator

Pin Configuration

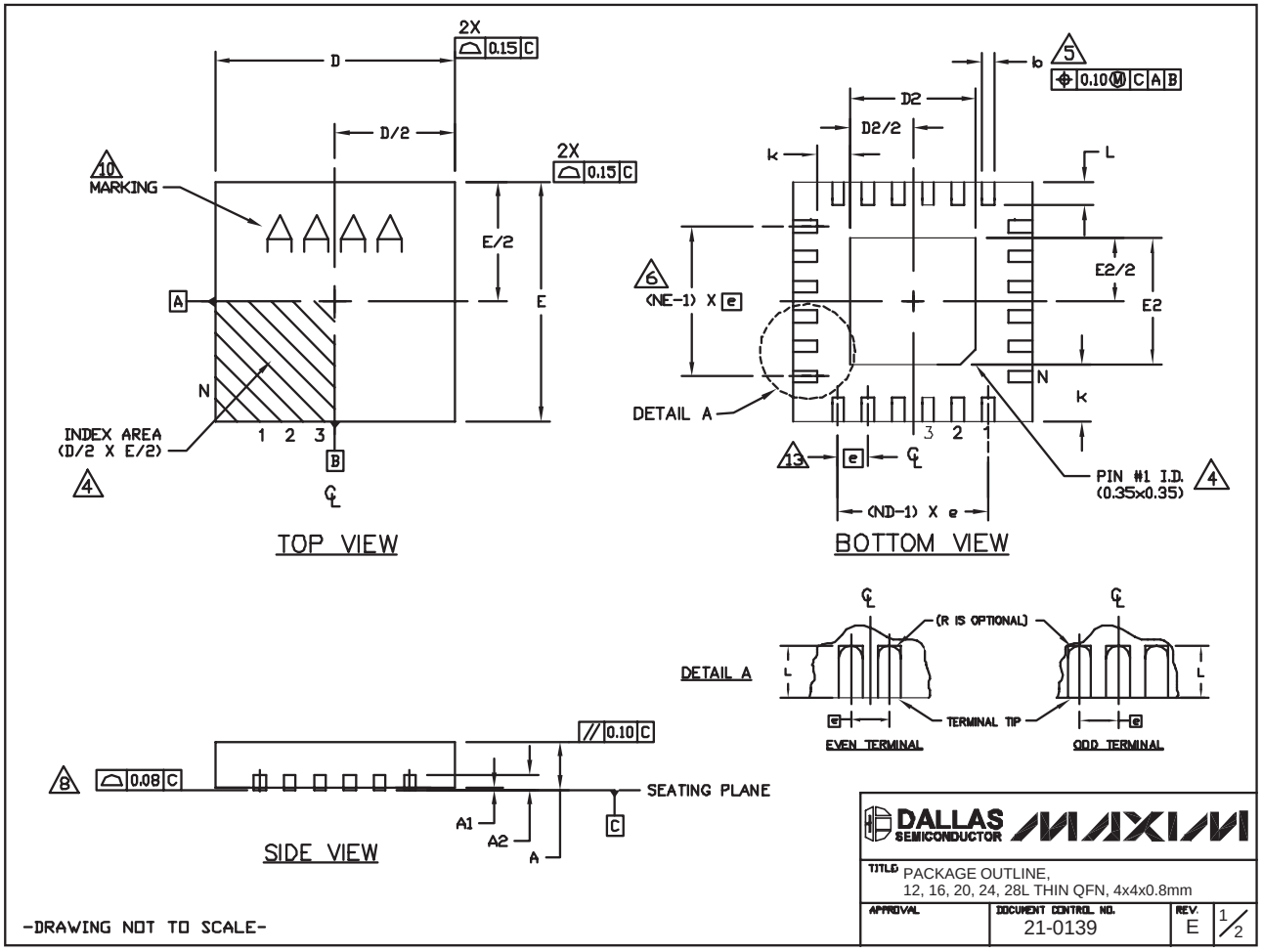


THIN QFN (4mm x 4mm)

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)

24L QFN THIN.EPS



Low-Voltage, Internal Switch, Step-Down/DDR Regulator

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)

COMMON DIMENSIONS

PKG	12L 4x4			16L 4x4			20L 4x4			24L 4x4			28L 4x4		
REF.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80
A1	0.0	0.02	0.05	0.0	0.02	0.05	0.0	0.02	0.05	0.0	0.02	0.05	0.0	0.02	0.05
A2	0.20 REF			0.20 REF			0.20 REF			0.20 REF			0.20 REF		
b	0.25	0.30	0.35	0.25	0.30	0.35	0.20	0.25	0.30	0.18	0.23	0.30	0.15	0.20	0.25
D	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10
E	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10
e	0.80 BSC.			0.65 BSC.			0.50 BSC.			0.50 BSC.			0.40 BSC.		
k	0.25	-	-	0.25	-	-	0.25	-	-	0.25	-	-	0.25	-	-
L	0.45	0.55	0.65	0.45	0.55	0.65	0.45	0.55	0.65	0.30	0.40	0.50	0.30	0.40	0.50
N	12			16			20			24			28		
ND	3			4			5			6			7		
NE	3			4			5			6			7		
Jedec Var.	WGGB			WGGC			WGGD-1			WGGD-2			WGGE		

EXPOSED PAD VARIATIONS

PKG. CODES	D2			E2			DOWN BONDS ALLOWED
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	
T1244-3	1.95	2.10	2.25	1.95	2.10	2.25	YES
T1244-4	1.95	2.10	2.25	1.95	2.10	2.25	NO
T1644-3	1.95	2.10	2.25	1.95	2.10	2.25	YES
T1644-4	1.95	2.10	2.25	1.95	2.10	2.25	NO
T2044-2	1.95	2.10	2.25	1.95	2.10	2.25	YES
T2044-3	1.95	2.10	2.25	1.95	2.10	2.25	NO
T2444-2	1.95	2.10	2.25	1.95	2.10	2.25	YES
T2444-3	2.45	2.60	2.63	2.45	2.60	2.63	YES
T2444-4	2.45	2.60	2.63	2.45	2.60	2.63	NO
T2844-1	2.50	2.60	2.70	2.50	2.60	2.70	NO

NOTES:

1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25 mm AND 0.30 mm FROM TERMINAL TIP.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
8. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
9. DRAWING CONFORMS TO JEDEC MO220, EXCEPT FOR T2444-3, T2444-4 AND T2844-1.
10. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
11. COPLANARITY SHALL NOT EXCEED 0.08mm
12. WARPAGE SHALL NOT EXCEEND 0.10mm
13. LEAD CENTERLINES TO BE AT TRUE POSITION AS DEFINED BY BASIC DIMENSION "e", ±0.05.
14. NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY

-DRAWING NOT TO SCALE-

DALLAS SEMICONDUCTOR MAXIM

TITLE: PACKAGE OUTLINE, 12, 16, 20, 24, 28L THIN QFN, 4x4x0.8mm

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0139	E	2/2