BENCHMARQ

# bq2212

## X2 PSRAM Nonvolatile Controller

### Features

- Power monitoring and switching for battery-backup of pseudo-static RAMs
- Complete nonvolatile and refresh control of pseudo-static RAMs
- Power-fail write-protection
- Controls up to 2 banks of PSRAM
- Nonrechargeable and rechargeable backup battery inputs
- Battery isolation pin for long storage periods
- Reset output for processor power-on reset
- Battery-fail flag indicates a low battery voltage condition
- 3V rechargeable battery input/output

### General Description

The CMOS bq2212 PSRAM Nonvolatile Controller provides all necessary functions for converting up to two banks of standard 3V CMOS pseudo-static RAM into nonvolatile read/write memory.

A precision comparator monitors the 5V $V_{CC}$ input for an out-of-tolerance condition. When an out-of-tolerance condition is detected, the two conditioned chip enable outputs are forced inactive to write-protect the two banks of PSRAM.

When an out-of-tolerance condition is detected and $V_{CC}$ falls below the battery voltage, the external energy source is switched on to sustain the memory until $V_{CC}$ returns valid. After $V_{CC}$ returns valid, the eight start-up cycles required by the PSRAMs are handled automatically during the chip enable recovery time.

An internal voltage regulator steps down $V_{OUT}$ voltage to approximately 3.0V. The regulator is bypassed when battery power is being used.

Because a read/write access might be requested during an internal refresh interval, a BUSY pin is provided to indicate when the selected device is busy with an internal refresh.

The controller handles all PSRAM refresh functions. During power-valid operation, the controller refreshes the PSRAMs using automatic refresh cycles. During power-fail operation, the PSRAMs are placed in self-refresh mode.

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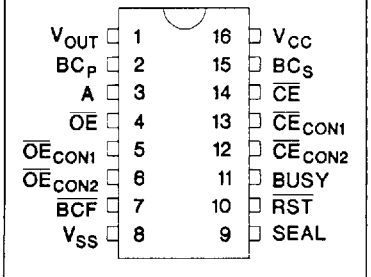
### Pin Connections




16-Pin Narrow DIP or SOIC

PN-43

### Pin Names

| | |
|---|---|
| $V_{OUT}$ | Regulated supply output |
| $BC_P$ | Nonrechargeable backup supply input |
| $BC_S$ | Rechargeable backup supply input/output |
| $\overline{BCF}$ | Battery fail output |
| A | Bank-select input |
| $\overline{OE}$ | Output enable input |
| $\overline{OE}_{CON1}$-$\overline{OE}_{CON2}$ | Conditioned output enable outputs |
| SEAL | Battery isolation signal |
| $\overline{RST}$ | Reset output |
| BUSY | Read/write cycle acknowledge open-drain output |
| $\overline{CE}_{CON1}$-$\overline{CE}_{CON2}$ | Conditioned chip enable outputs |
| $\overline{CE}$ | Chip enable active low input |
| $V_{CC}$ | +5 volt supply input |
| $V_{SS}$ | Ground |

## Pin Descriptions

**$V_{OUT}$** **Supply output**

$V_{OUT}$ supplies power to the external PSRAMs from one of several sources. If $V_{CC}$ is above $V_{BCS}$ (valid $V_{CC}$), then internally regulated power, derived from $V_{CC}$, is applied to $V_{OUT}$. The regulated power voltage is at 3.0V (±10%). If $V_{CC}$ falls below $V_{BCS}$, then the rechargeable battery $BC_S$ is applied to $V_{OUT}$. If the rechargeable battery voltage falls below about 2.5V, then $V_{OUT}$ is supplied from the nonrechargeable battery $BC_P$. As $V_{CC}$ returns valid, $V_{OUT}$ is switched from the backup supply back to the $V_{CC}$ supply. Hysteresis is built in around the switch-over voltages to prevent excessive bouncing between different power sources. If there is no need to retain data after $V_{CC}$ is removed, $V_{OUT}$ can be isolated from both backup inputs by using the SEAL input.

**$BC_P$** **Nonrechargeable backup supply input**

The $BC_P$ input is an external energy source connection that is not rechargeable. This backup can be a battery or a board-level backup system. The voltage input on this pin should be between 2.5V and 3.4V. This backup is used during a power-fail condition and when the backup system connected to $BC_S$ is below about 2.5V. This input should be tied to $V_{SS}$ if no battery is used.

**$BC_S$** **Rechargeable backup supply input/output**

The $BC_S$ input is to be used with 3V rechargeable vanadium-lithium batteries such as Panasonic's VL1220. This input supplies $V_{OUT}$ if $V_{CC}$ falls below the $BC_S$ voltage. During valid $V_{CC}$ operation, this pin sources a current-limited 3.3V to keep the batteries charged and ready for use. If no rechargeable battery is used, then this input should be tied to $V_{SS}$.

**$\overline{BCF}$** **Battery fail output**

If $V_{CC}$ and $BC_P$ are below their minimum valid voltage levels on power-up, the $\overline{BCF}$ output goes low and stays low on subsequent valid $V_{CC}$ to alert the user that data inside the PSRAMs may be corrupted.

**A** **Bank select address input**

Two banks of PSRAMs can be controlled by the bq2212, and these banks are selected by the "A" address input. For "A" low, $\overline{CE}_{CON1}$ and $\overline{OE}_{CON1}$ are activated. For "A" high, $\overline{CE}_{CON2}$ and $\overline{OE}_{CON2}$ are activated. Address setup time is measured to $\overline{CE}$, but address hold time is measured starting when BUSY goes low.

**$\overline{OE}$** **Output enable input**

During an active cycle, the $\overline{OE}$ input is passed directly onto $\overline{OE}_{CON1}$ or $\overline{OE}_{CON2}$, depending on the state of address "A," but is inhibited during $\overline{CE}$ inactive. $\overline{OE}$ is an active low input.

**$\overline{OE}_{CON1}$/ $\overline{OE}_{CON2}$** **Conditioned output enable outputs**

$\overline{OE}_{CON1}$ is connected to the $\overline{OE}/\overline{RFSH}$ inputs of the first bank of PSRAMs, and $\overline{OE}_{CON2}$ is connected to the $\overline{OE}/\overline{RFSH}$ inputs of the second bank. Either $\overline{OE}_{CON1}$ or $\overline{OE}_{CON2}$ is driven directly from the $\overline{OE}$ input during an active access, depending on the input address "A." During $\overline{CE}$ inactive, the bq2212 controls both the $\overline{OE}_{CON1}$ and $\overline{OE}_{CON2}$ outputs to handle the refresh requirements of both banks of PSRAMs simultaneously. During $\overline{CE}$ inactive, both outputs are held high until a bq2212 internal timer requests that an automatic refresh be done (about every 15µs).

To reduce instantaneous power demand, the refresh of the two banks is interlaced. Therefore, an auto-refresh operation occurs every 7.5µs.

If one of the banks is being accessed when the refresh is requested by the internal timer, the refresh is postponed until the end of that active cycle. During a power-fail condition, both $\overline{OE}_{CON1}$ and $\overline{OE}_{CON2}$ are held low until valid power is restored. Therefore, during a power-fail condition, and the control of refresh cycles for the PSRAMs passes from the bq2212 to the PSRAM internal circuitry, allowing the PSRAMs to self-refresh. Both outputs are active low.

**SEAL** **Battery isolation signal**

If data retention is not needed, unnecessary battery drain can be avoided by using the SEAL pin. If the SEAL input is taken high during valid $V_{CC}$, the external batteries are disconnected from $V_{OUT}$ after $V_{CC}$ falls below $V_{PFD}$. After a subsequent valid $V_{CC}$ level is detected, the SEAL function is removed, and battery backup occurs normally on all power failures until SEAL is activated again. This function is useful after an initial test but

before the device is actually used. All devices are sealed after manufacturing and testing.

**$\overline{RST}$ Reset output**

The $\overline{RST}$ output goes active (low) during a power-fail condition and remains low up to 120ms after valid $V_{CC}$ rises above $V_{PFD}$. This output can be used as the power-on reset for a microprocessor. Access to the PSRAMs is available after $\overline{RST}$ returns inactive (high).

**BUSY Read/write cycle acknowledge open-drain output**

The BUSY output is an open-drain output that goes low to tell the user that the requested $\overline{CE}$ cycle has started in the PSRAMs. BUSY is low when either $\overline{CE}_{CON1}$ or $\overline{CE}_{CON2}$ is low. Because the bq2212 independently handles the automatic refresh function of the PSRAMs, if the user requests a $\overline{CE}$ cycle during an automatic refresh, the $\overline{CE}$ cycle is delayed until the end of the refresh cycle. The BUSY output remains high until the refresh cycle is completed, and then goes low as the $\overline{CE}$ access is initiated in the selected PSRAM.

The refresh cycle takes less than 500ns and occurs about once every 7.5µs, so there is less than a 6% probability that the access will be delayed by some portion of an automatic refresh cycle. The BUSY output can be used as an input to a wait-state generator for the microprocessor.

**$\overline{CE}$ Chip enable input**

The $\overline{CE}$ input is an active low input used to initiate a read or write cycle to the PSRAMs. Under typical operation, the $\overline{CE}$ pin is passed to either $\overline{CE}_{CON1}$ or $\overline{CE}_{CON2}$, depending on the state of address "A." If the bq2212 is performing an automatic refresh on the PSRAMs when $\overline{CE}$ goes low, then neither $\overline{CE}_{CON1}$ nor $\overline{CE}_{CON2}$ is allowed to go low until the refresh cycle is completed.

**$\overline{CE}_{CON1}$/ $\overline{CE}_{CON2}$ Conditioned chip enable outputs**

$\overline{CE}_{CON1}$ is connected to the $\overline{CE}$ inputs of the first bank of PSRAMs, and $\overline{CE}_{CON2}$ is connected to the $\overline{CE}$ inputs of the second bank. During a user-requested $\overline{CE}$ access, either $\overline{CE}_{CON1}$ or $\overline{CE}_{CON2}$ is driven directly from the $\overline{CE}$ input, depending on the address "A." During $\overline{CE}$ inactive, during a power-fail condition, or during an automatic refresh, both $\overline{CE}_{CON1}$ and $\overline{CE}_{CON2}$ outputs are held high until the end of that condition. Both outputs are active low.

**$V_{CC}$ +5 volt supply input**

A valid $V_{CC}$ condition exists when $V_{CC}$ is above $V_{PFD}$, typically 4.37V. If $V_{CC}$ falls below this level, a power-fail condition is detected. $V_{CC}$ should not be allowed to fall faster than about 1V/600µs as it passes through the power-fail detection voltage, $V_{PFD}$. A faster rise time for $V_{CC}$ returning valid is allowed. During valid $V_{CC}$ operation, the bq2212 passes access requests on to the two banks of PSRAMs through the $\overline{CE}_{CON1}$, $\overline{CE}_{CON2}$, $\overline{OE}_{CON1}$, and $\overline{OE}_{CON2}$ outputs. Also during $V_{CC}$ valid operation, the bq2212 handles the PSRAM refresh requirements through $\overline{OE}_{CON1}$ and $\overline{OE}_{CON2}$.

During a power-fail condition, both banks of PSRAMs are write-protected and are unavailable for reads. Also during a power-fail condition, refresh control is passed to the PSRAMs by holding $\overline{CE}_{CON1}$ and $\overline{CE}_{CON2}$ high while holding $\overline{OE}_{CON1}$ and $\overline{OE}_{CON2}$ low, placing the PSRAMs in self-refresh mode.

**$V_{SS}$ Ground**

$V_{SS}$ is the system ground pin. All bq2212 voltages are defined relative to this pin.

## Functional Description

Two banks of CMOS pseudo-static RAM can be battery-backed using the $V_{OUT}$ and conditioned chip enable outputs from the bq2212. As the voltage input $V_{CC}$ slews down past $V_{PFD}$ during a power failure, the two conditioned chip enable outputs, $\overline{CE}_{CON1}$ and $\overline{CE}_{CON2}$, are forced inactive independent of the chip enable input $\overline{CE}$.

This activity unconditionally write-protects external PSRAM as $V_{CC}$ falls below an out-of-tolerance threshold $V_{PFD}$. Power-fail detection occurs typically at 4.37V.

If a memory access is in progress to any of the two external banks of PSRAM during power-fail detection, that memory cycle continues to completion before the memory is write-protected. If the memory cycle is not terminated within time $t_{WPT}$ (150µs maximum), the two chip enable outputs are unconditionally driven high, write-protecting the controlled PSRAMs.

As the supply continues to fall past $V_{PFD}$, an internal switching device forces $V_{OUT}$ to an external backup energy source. $\overline{CE}_{CON1}$ and $\overline{CE}_{CON2}$ are held high by the $V_{OUT}$ energy source.

During power-up, $V_{OUT}$ is switched back to the regulated supply as $V_{CC}$ rises above the backup cell input voltage

($V_{BCSO}$) sourcing $V_{OUT}$. Outputs $\overline{CE}_{CON1}$ and $\overline{CE}_{CON2}$ are held inactive for time $t_{CER}$ (120ms maximum) after the power supply has reached $V_{PFD}$, independent of the $\overline{CE}$ input, to allow for processor stabilization.

During power-valid operation, the $\overline{CE}$ input is passed through to one of the two $\overline{CE}_{CON}$ outputs with a propagation delay of less than 10 ns. The $\overline{CE}$ input asserts one of the two $\overline{CE}_{CON}$ output pins depending on the level of bank select input A, as shown in the Truth Table.

Bank select input A is usually tied to a high-order address pin so that a large nonvolatile memory can be designed using lower-density memory devices. Nonvolatility and decoding are achieved by hardware hookup as shown in Figure 1.

The reset output ($\overline{RST}$) goes active within $t_{PFD}$ (150µs maximum) after $V_{PFD}$, and remains active for a minimum of 40ms (120ms maximum) after power returns valid. The $\overline{RST}$ output can be used as the power-on reset for a microprocessor. Access to the external RAM may begin when $\overline{RST}$ returns inactive.

## Energy Cell Inputs—$BC_P$, $BC_S$

Two backup energy source inputs are provided on the bq2212—a nonrechargeable cell $BC_P$ and a rechargeable cell $BC_S$. The nonrechargeable cell input is designed to accept any nonrechargeable battery, typically some type of lithium chemistry. If a nonrechargeable cell is not used, the $BC_P$ pin should be grounded. The rechargeable cell input $BC_S$ is designed to accept constant-voltage, current-limited rechargeable vanadium-lithium cells such as Panasonic's VL1220.

During normal +5V power valid operation, 3.2V is output on the $BC_S$ pin and is current-limited internally.

If a rechargeable cell is not used, the $BC_S$ pin must be grounded. If both inputs are used, during power failure the $V_{OUT}$ and $\overline{CE}_{CON}$ outputs are forced high by the rechargeable cell so long as it is greater than 2.5V. Only the rechargeable cell is loaded by the data-retention current of the SRAM until the voltage at the $BC_S$ pin falls below 2.5V. If the voltage at $BC_S$ falls below 2.5V, an internal isolation switch automatically transfers the load from the rechargeable cell to the nonrechargeable cell.

To prevent battery drain when there is no valid data to retain, $V_{OUT}$, $\overline{CE}_{CON1}$, and $\overline{CE}_{CON2}$ are internally isolated from $BC_P$ and $BC_S$ by either:

- Initial connection of a battery to $BC_P$ or $BC_S$ or
- Taking the SEAL pin high during power-valid operation. The battery is connected to $V_{OUT}$, $\overline{CE}_{CON1}$, and $\overline{CE}_{CON2}$ immediately on subsequent application and removal of $V_{CC}$.

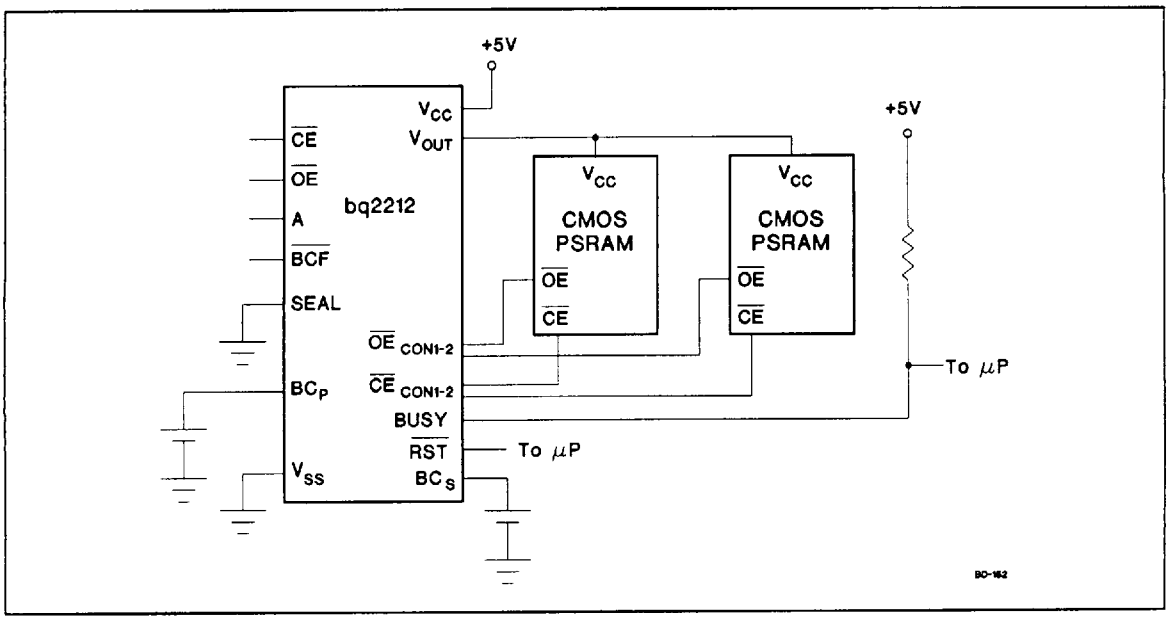



**Figure 1. Hardware Hookup**

## Truth Table

| Input | | Output | |
|---|---|---|---|
| $\overline{CE}$ | A | $\overline{CE}_{CON1}$ | $\overline{CE}_{CON2}$ |
| H | X | H | H |
| L | L | L | H |
| L | H | H | L |

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## Absolute Maximum Ratings

| Symbol | Parameter | Value | Unit | Conditions |
|---|---|---|---|---|
| $V_{CC}$ | DC voltage applied on $V_{CC}$ relative to Vss | -0.3 to 7.0 | V | |
| $V_T$ | DC voltage applied on any pin excluding $V_{CC}$ relative to Vss | -0.3 to 7.0 | V | $V_T \leq V_{CC} + 0.3$ |
| $T_{OPR}$ | Operating temperature | 0 to +70 | °C | |
| $T_{STG}$ | Storage temperature | -55 to +125 | °C | |
| $T_{BIAS}$ | Temperature under bias | -40 to 85 | °C | |
| $T_{SOLDER}$ | Soldering temperature | 260 | °C | For 10 seconds |
| $I_{OUT}$ | $V_{OUT}$ current | 300 | mA | |

**Note:** Permanent device damage may occur if **Absolute Maximum Ratings** are exceeded. Functional operation should be limited to the Recommended DC Operating Conditions detailed in this data sheet. Exposure to conditions beyond the operational limits for extended periods of time may affect device reliability.

## Recommended DC Operating Conditions ($T_A = T_{OPR}$)

| Symbol | Parameter | Minimum | Typical | Maximum | Unit | Notes |
|---|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | 4.50 | 5.0 | 5.5 | V | |
| $V_{BCP}$ | Backup cell input voltage | 2.5 | - | 3.4 | V | |
| $V_{BCS}$ | | 2.5 | - | 3.4 | | |
| $V_{SS}$ | Supply voltage | 0 | 0 | 0 | V | |
| $V_{IL}$ | Input low voltage | -0.3 | - | 0.8 | V | |
| $V_{IH}$ | Input high voltage | 2.2 | - | $V_{CC}$ + 0.3 | V | |

Note: Typical values indicate operation at $T_A$ = 25°C, $V_{CC}$ = 5V or $V_{BC}$.

## DC Electrical Characteristics ($T_A = T_{OPR}$, $V_{CC}$ = 5V ± 10%)

| Symbol | Parameter | Minimum | Typical | Maximum | Unit | Conditions/Notes |
|---|---|---|---|---|---|---|
| $I_{LI}$ | Input leakage current | - | - | ± 1 | µA | $V_{IN} = V_{SS}$ to $V_{CC}$ |
| $V_{OH}$ | Output high voltage | 2.4 | - | - | V | $I_{OH}$ = -2.0 mA |
| $V_{OHB}$ | $V_{OH}$, backup supply | $V_{BC}$ - 0.2 | - | - | V | $V_{BC} > V_{CC}$, $I_{OH}$ = -10µA |
| $V_{OL}$ | Output low voltage | - | - | 0.4 | V | $I_{OL}$ = 4.0 mA |
| $I_{CC}$ | Operating supply current | - | 3 | 6 | mA | No load on $V_{OUT}$, $\overline{CE}_{CON1}$, $\overline{CE}_{CON2}$, $\overline{OE}_{CON1}$, $\overline{OE}_{CON2}$, $\overline{RST}$, $\overline{BCF}$, and BUSY |
| $V_{PFD}$ | Power-fail detect voltage | 4.30 | 4.37 | 4.50 | V | |
| $V_{SO}$ | Supply switch-over voltage | - | $V_{BC}$ | - | V | |
| $I_{CCDR}$ | Data-retention mode current | - | - | 100 | nA | No load on $V_{OUT}$, $\overline{CE}_{CON1}$, $\overline{CE}_{CON2}$, $\overline{OE}_{CON1}$, $\overline{OE}_{CON2}$, $\overline{RST}$, $\overline{BCF}$, and BUSY |
| $V_{OUT1}$ | $V_{OUT}$ voltage | 2.7 | 3.0 | 3.3 | V | $V_{CC} > V_{BC}$; when $V_{CC}$ falls below 3.3V, $V_{OUT1}$ tracks $V_{CC}$ until battery switch-over occurs |
| $V_{OUT2}$ | $V_{OUT}$ voltage | $V_{BC}$ - 0.2 | - | - | V | $V_{CC} < V_{BC}$, $I_{OUT}$ = 140µA |
| $V_{BC}$ | Active backup cell voltage | - | $V_{BCS}$ | - | V | $V_{BCS} > 2.5V$ |
| | | - | $V_{BCP}$ | - | V | $V_{BCS} < 2.5V$ |
| $R_{BCS}$ | BCs charge output internal resistance | 500 | 1000 | 1500 | Ω | $V_{BCSO} \geq 3.0V$ |
| $V_{BCSO}$ | BCs charge output voltage | 3.1 | 3.2 | 3.3 | V | $V_{CC} > V_{PFD}$, $\overline{RST}$ inactive, full charge or no load |
| $V_{BCF}$ | Battery-fail voltage | 2.5 | - | - | V | |
| $I_{OUT1}$ | $V_{OUT}$ current | - | - | 80 | mA | $V_{CC} \geq V_{PFD}$ |
| $I_{OUT2}$ | $V_{OUT}$ current | - | 140 | - | µA | $V_{CC} < V_{PFD}$ |

Note: Typical values indicate operation at $T_A$ = 25°C, $V_{CC}$ = 5V or $V_{BC}$.

## Capacitance ($T_A$ = 25°C, F = 1MHz, $V_{CC}$ = 5.0V)

| Symbol | Parameter | Minimum | Typical | Maximum | Unit | Conditions |
|---|---|---|---|---|---|---|
| $C_{IN}$ | Input capacitance | - | - | 8 | pF | Input voltage = 0V |
| $C_{OUT}$ | Output capacitance | - | - | 10 | pF | Output voltage = 0V |

**Note:** This parameter is sampled and not 100% tested.



## AC Test Conditions

| Parameter | Test Conditions |
|---|---|
| Input pulse levels | 0 V to 3.0 V |
| Input rise and fall times | 5 ns |
| Input and output timing reference levels | 1.5 V (unless otherwise specified) |
| Output load (including scope and jig) | See Figure 2 |

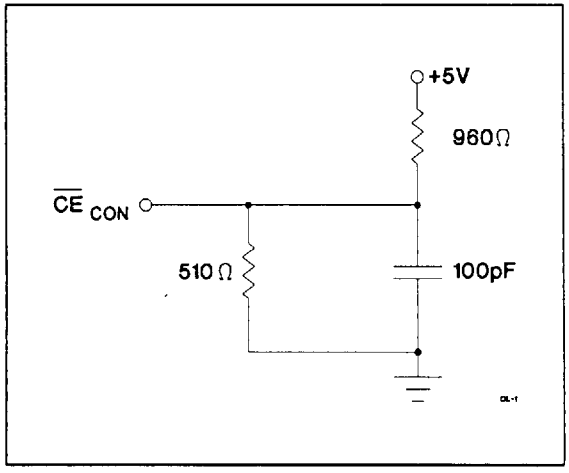


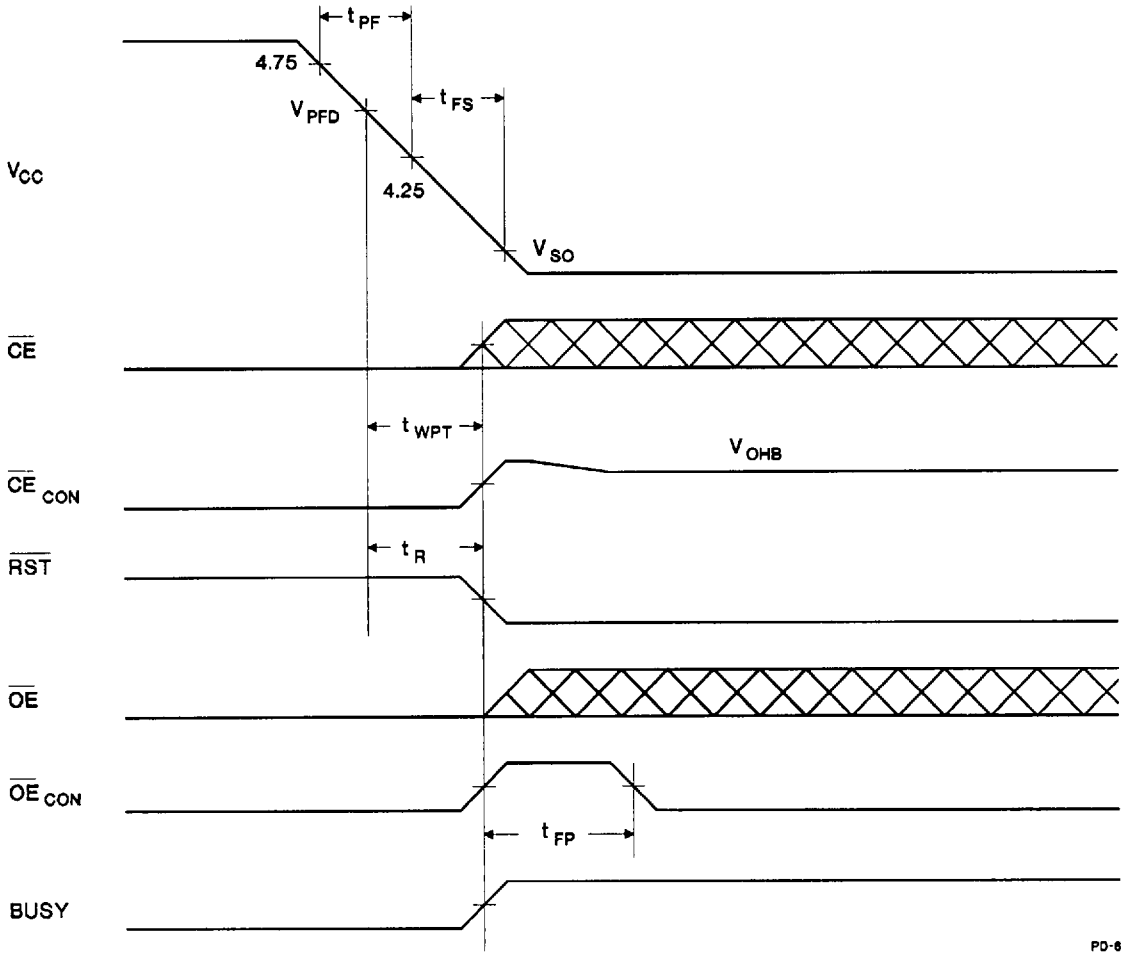

**Figure 2. Output Load**

## Power-Fail Control and Operation ($T_A$ = $T_{OPR}$)

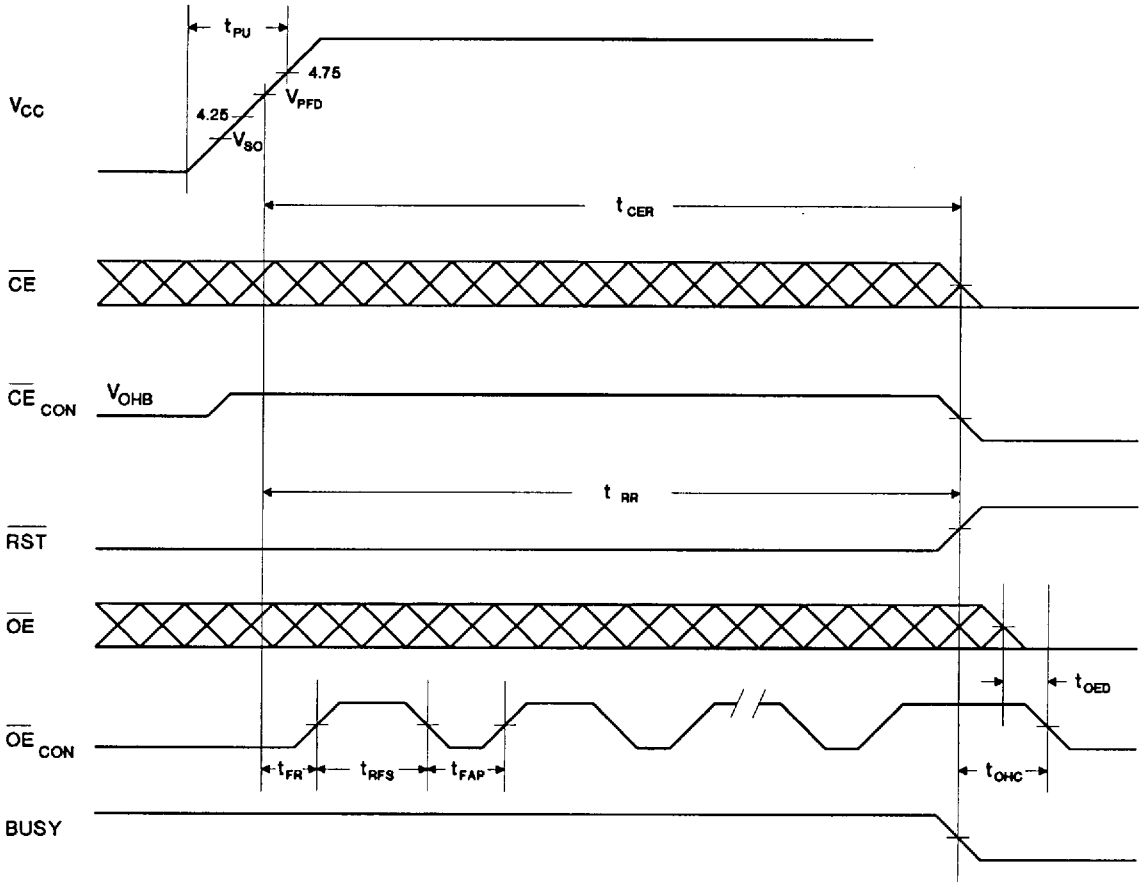
| Symbol | Parameter | Min. | Typ. | Max. | Unit | Conditions |
|---|---|---|---|---|---|---|
| $t_{PF}$ | $V_{CC}$ slew 4.75 to 4.25 V | 300 | - | - | µs | |
| $t_{FS}$ | $V_{CC}$ slew 4.25 V to $V_{SO}$ | 300 | - | - | µs | |
| $t_{PU}$ | $V_{CC}$ slew 0 to 4.75 V | 300 | - | - | µs | |
| $t_{CED}$ | Chip-enable propagation delay | - | 7 | 10 | ns | |
| | Chip-enable propagation delay if requested during a refresh cycle | - | - | 500 | ns | $t_{CED}$ has a <6% probability of being longer than 10ns due to the bq2212 finishing an internal refresh cycle. |
| $t_{BSD}$ | $\overline{CE}$ low to BUSY low | $t_{CED}$ | - | $t_{CED}$ | ns | |
| $t_{CE}$ | $\overline{CE}$ hold past BUSY | 80 | - | - | ns | Minimum $\overline{CE}$ pulse width starting with BUSY low |
| $t_P$ | $\overline{CE}$ precharge time | 40 | - | - | ns | |
| $t_{AS}$ | Input A set up to $\overline{CE}$ | 0 | - | - | ns | |
| $t_{RR}$ | $V_{PFD}$ to $\overline{RST}$ inactive | $t_{CER}$ | $t_{CER}$ | $t_{CER}$ | ms | Time, after $V_{CC}$ becomes valid, before $\overline{RST}$ is inactive |
| $t_{CER}$ | Chip-enable recovery time | 40 | 80 | 120 | ms | Time during which SRAM is write-protected after $V_{CC}$ passes $V_{PFD}$ on power-up |
| $t_{AH}$ | Input A hold time | 20 | - | - | ns | Address hold from busy low |
| $t_R$ | $V_{PFD}$ to $\overline{RST}$ active | 40 | 100 | 150 | µs | Delay after $V_{CC}$ slews down past $V_{PFD}$ before $\overline{RST}$ is active |
| $t_{WPT}$ | Write-protect time | $t_R$ | | $t_R$ | µs | Delay after $V_{CC}$ slews down past $V_{PFD}$ before SRAM is write-protected |
| $t_{FP}$ | PSRAM refresh precharge time | 40 | - | 60 | ns | |
| $t_{FR}$ | PSRAM data-retention recovery time | 5 | - | - | ms | |
| $t_{RFS}$ | PSRAM self-refresh recovery time | - | - | 15 | µs | |
| $t_{FAP}$ | PSRAM automatic refresh | 80 | - | - | ns | |
| $t_{OHC}$ | $\overline{CE}_{CON}$ low to $\overline{OE}_{CON}$ low delay | 20 | - | - | ns | |
| $t_{OF}$ | $\overline{CE}_{CON}$ high to $\overline{OE}_{CON}$ high | - | - | 15 | ns | |
| $t_{OED}$ | $\overline{OE}$ to $\overline{OE}_{CON}$ delay | - | - | 15 | ns | |
| $t_{SEAL}$ | Minimum seal pulse width | 50 | - | - | µs | |
| $t_{SPT}$ | Seal protect time | $t_{CER}$ | - | $t_{CER}$ | ms | Time during which SEAL input is ignored after $V_{CC}$ passes $V_{PFD}$ on power-up. |

**Note:** Typical values indicate operation at $T_A$ = 25°C, $V_{CC}$ = 5V.

## Power-Down Timing

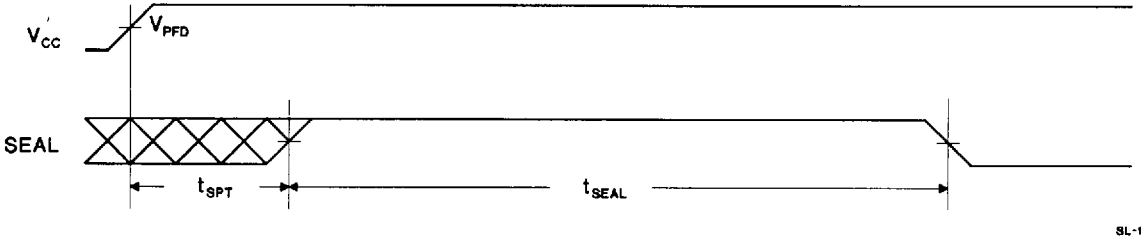


## Power-Up Timing




PU-10

## SEAL Timing

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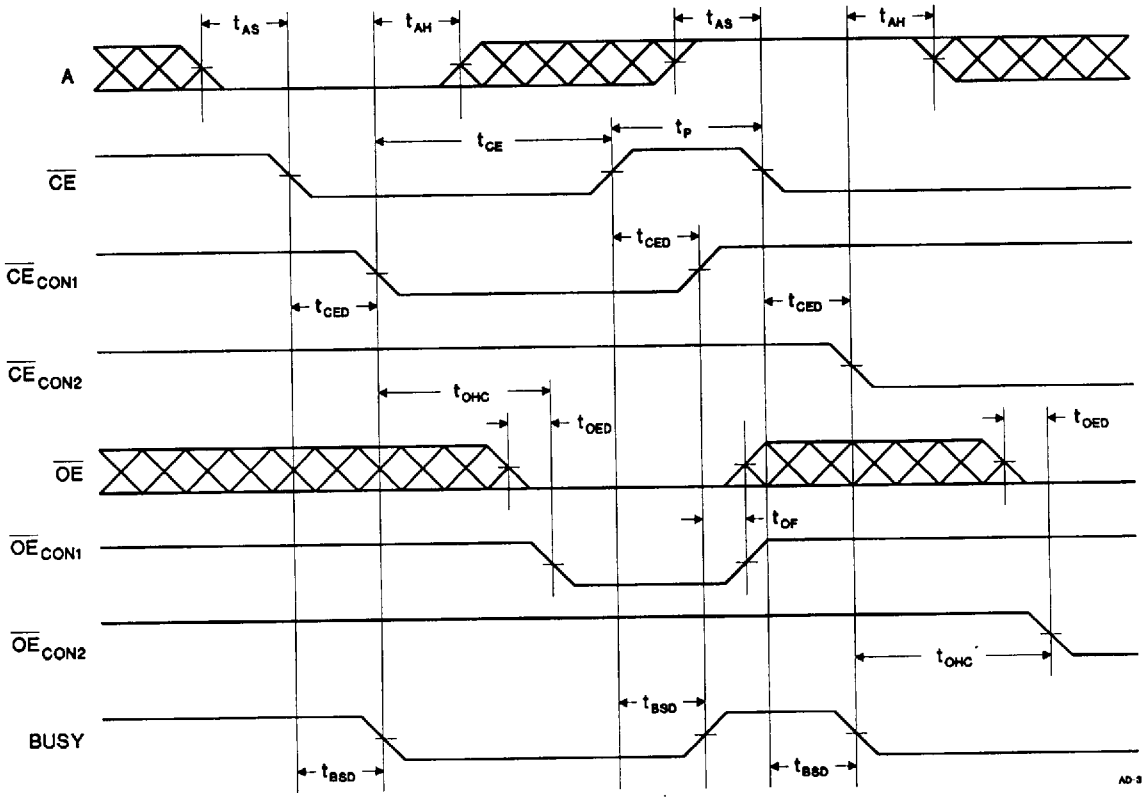
## Address-Decode Timing



## Ordering Information