Enhanced Memory Systems Inc.

DM2M36SJ6/DM2M32SJ6 Multibank EDO 2Mbx36/2Mbx32 Enhanced DRAM SIMM

Product Specification

Features

- 16KByte SRAM Cache Memory for 12ns Random Reads Within Eight Active Pages (Multibank Cache)
- Fast DRAM Array for 30ns Access to Any New Page
- Write Posting Register for 12ns Random Writes and Burst Writes Within a Page (Hit or Miss)
- 2KByte Wide DRAM to SRAM Bus for 113.6 Gigabytes/Sec Cache Fill
- On-chip Cache Hit/Miss Comparators Maintain Cache Coherency on Writes
- Hidden Precharge and Refresh Cycles
- Extended 64ms Refresh Period for Low Standby Power
- Standard CMOS/TTL Compatible I/O Levels and +5 or 3.3V Volt Supply
- Compatibility with JEDEC 2M x 36 DRAM SIMM Configuration Allows Performance Upgrade in System
- Multibank Extended Data Output (EDO) for Faster System Operation
- Low Power, Self Refresh Option
- Industrial Temperature Range Option

Description

The Enhanced Memory Systems Multibank EDO 8MB EDRAM SIMM module provides a single memory module solution for the main memory or local memory of fast PCs, workstations, servers, and other high performance systems. Due to its fast 12ns cache row register, the EDRAM memory module supports zero-wait-state burst read operations at up to 83MHz bus rates in a non-interleave configuration and >132MHz bus rates with a two-way interleave configuration.

On-chip write posting and fast page mode operation supports 12ns write and burst write operations. On a cache miss, the fast DRAM array reloads the 2KByte cache over a 2KByte-wide bus in 18ns for an effective bandwidth of 113.6 Gbytes/sec. This means very low latency and fewer wait states on a cache miss than a non-integrated cache/DRAM solution. The JEDEC compatible 72-bit SIMM configuration allows a single memory controller to be designed to support either JEDEC slow DRAMs or high speed EDRAMs to provide a simple upgrade path to higher system performance.

Architecture

The DM2M36SJ6 achieves 2Mb x 36 density by mounting 18 1Mb x 4 EDRAMs, packaged in 28-pin plastic SOJ packages, on both sides of the multi-layer substrate. Sixteen DM2242 and two DM2252 devices provide data and parity storage. The DM2M32SJ6 contains 16 DM2242 devices for data only.

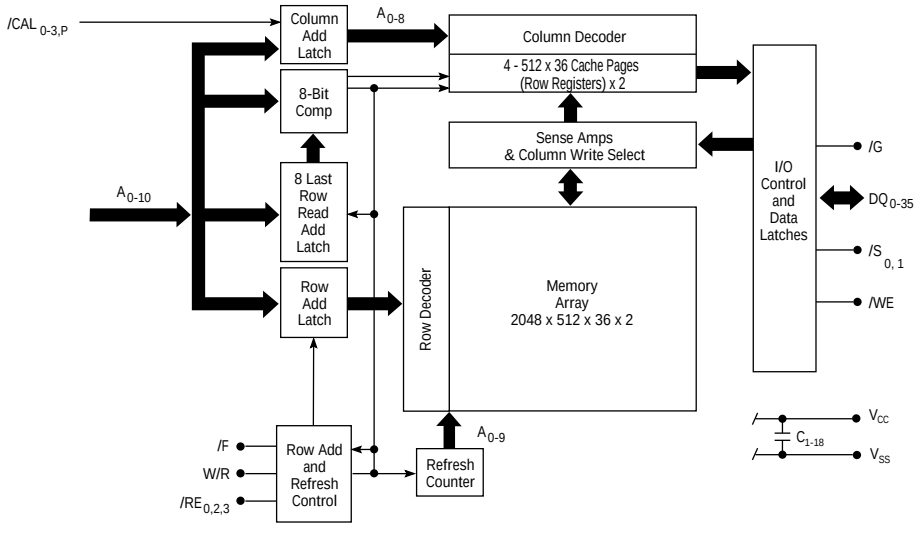
The EDRAM memory module architecture is very similar to a standard 8MB DRAM module with the addition of an integrated cache and on-chip control which allows it to operate much like an EDO DRAM.

The EDRAM's SRAM cache is integrated into the DRAM array as tightly coupled row registers. Each EDRAM Bank has a total of four independent DRAM memory banks each with its own SRAM row register. Memory reads always occur from the cache row register of one of these banks as specified by row address bits A_2 and A_9 (bank select). When the internal comparator detects that the row address matches the last row read from any of the four DRAM banks (page hit), the SRAM is accessed and data is available on the output pins in 12ns from the column address input. Subsequent reads within the page (burst reads or random reads) can continue at 12ns cycle time. When the row address does not match the last row read from any of the last four DRAM banks (page miss), the new DRAM row is accessed and loaded into the appropriate SRAM row register and data is available on the output pins all within 30ns from row enable. Subsequent reads within the page (burst reads or random reads) can continue at 12ns cycle time.

Since reads occur from the SRAM cache, the DRAM precharge can occur during burst reads. This eliminates the precharge time delay suffered by other DRAMs and SDRAMs when accessing a new page. The EDRAM has an independent on-chip refresh counter and dedicated refresh control pin to allow the DRAM array to be refreshed concurrently with cache read operations (hidden refresh).

Memory writes are posted to the input data latch and directed to the DRAM array. During a write hit, the on-chip address comparator activates a parallel write path to the SRAM cache to maintain

Functional Diagram



coherency. Random or page mode writes can be posted 5ns after column address and data are available. The EDRAM allows 12ns page mode cycle time for both write hits and write misses. Memory writes do not affect the contents of the cache row register except during a cache hit.

By integrating the SRAM cache as row registers in the DRAM array and keeping the on-chip control simple, the EDRAM is able to provide superior performance over standard slow DRAMs. By eliminating the need for SRAMs and cache controllers, system cost, board space, and power can all be reduced.

Functional Description

The EDRAM is designed to provide optimum memory performance with high speed microprocessors. As a result, it is possible to perform simultaneous operations to the DRAM and SRAM cache sections of the EDRAM. This feature allows the EDRAM to hide precharge and refresh operation during SRAM cache reads and maximize SRAM cache hit rate by maintaining valid cache contents during write operations even if data is written to another memory page. These new functions, in conjunction with the faster basic DRAM and cache speeds of the EDRAM, minimize processor wait states.

EDRAM Basic Operating Modes

The EDRAM operating modes are specified in the table.

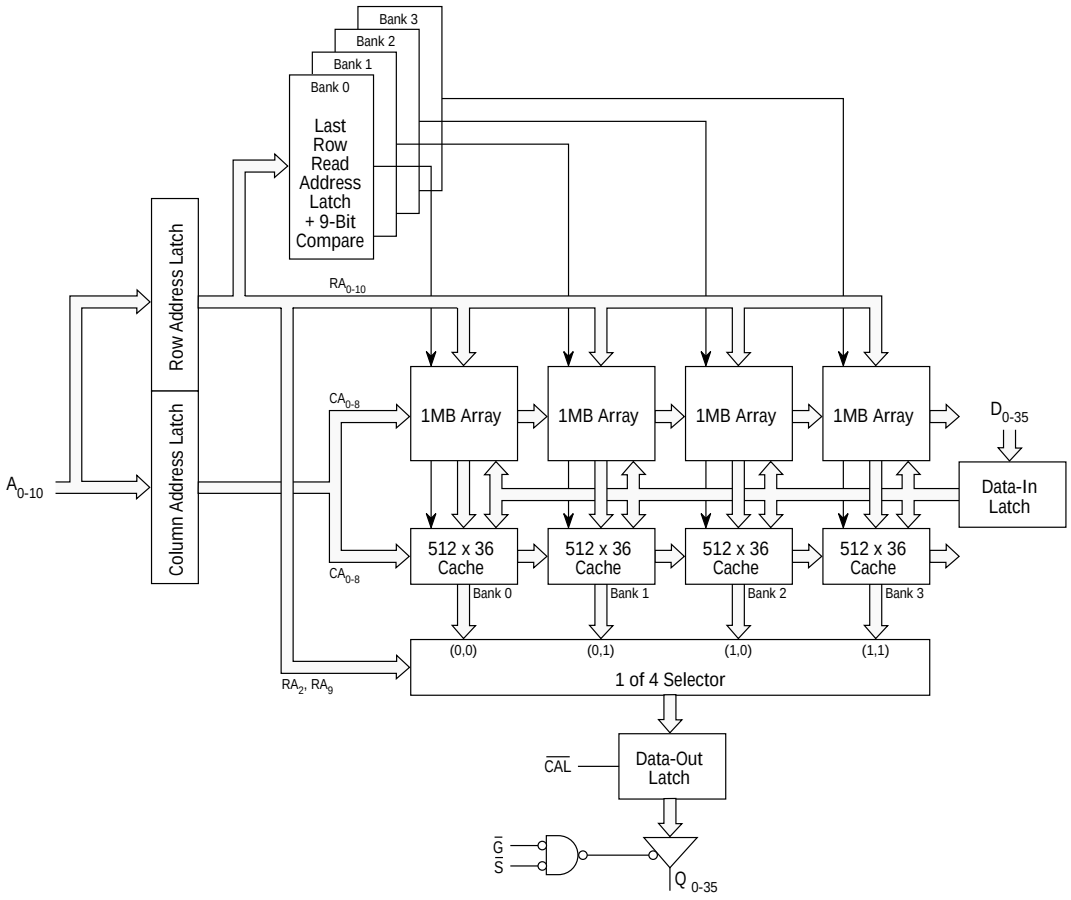
Hit and Miss Terminology

In this datasheet, "hit" and "miss" always refer to a hit or miss to any of the four pages of data contained in the SRAM cache row registers. There are four cache row registers, one for each of the four banks of DRAM. These registers are specified by the bank select row address bits A_2 and A_9. The contents of these cache row registers is always equal to the last row that was read from each of the four internal DRAM banks (as modified by any write hit data).

Bank Selection

The 8MByte EDRAM SIMM has two separate 4MByte banks on one module. The two banks share common data, multiplexed address, and control signals with the exception of /RE and /S. Bank selection is performed by using both /RE and /S to select a bank. The use of /S to select a bank is *required* on the 8MByte SIMM because /G is common between the two banks. If /S is grounded (i.e., not used to control bank selection), an output buffer conflict between the two banks *will* occur when /G is enabled. It is also necessary to clock the /RE signal for each bank separately since clocking /RE with /S disabled is *not* allowed (see "Unallowed Mode" description).

Four Bank Cache Architecture (One of Two Banks)



DRAM Read Hit

A DRAM read request is initiated by clocking /RE with W/R low and /F and /CAL high. The EDRAM will compare the new row address to the last row read address latch for the bank specified by row address $A_{2,9}$(LRR; an 9-bit latch loaded on each /RE active read cycle). If the row address matches the LRR, the requested data is already in the SRAM cache and no DRAM memory reference is initiated. The data specified by the column address is available at the output pins at the greater of times t_{RAC1}, t_{AC}, t_{GQV}, and $t_{ASC} + t_{CLV}$. Since no DRAM activity is initiated, /RE can be brought high after time t_{RE1}, and a shorter precharge time, t_{RP1}, is required. It is possible to access additional SRAM cache locations by providing new column addresses to the multiplex address inputs. New data is available at the output at time $t_{ASC} + t_{CLV}$ after each column address change.

DRAM Read Miss

A DRAM read request is initiated by clocking /RE with W/R low and /F. The EDRAM will compare the new row address to the LRR address latch for the bank specified by row address bits $A_{2,9}$(LRR: 9-bit row address latch for each internal DRAM bank which is reloaded on each /RE active read miss cycle). If the row address does not match the LRR, the requested data is not in SRAM cache and a new row must be fetched from the DRAM. The EDRAM will load the new row data into the SRAM cache and update the LRR latch. The data at the specified column address is available at the output pins at the greater of times t_{RAC}, t_{AC}, t_{GQV}, and $t_{ASC} + t_{CLV}$. It is possible to bring /RE high after time t_{RE} since the new row data is safely latched into SRAM cache. This allows the EDRAM to precharge the DRAM array while data is accessed from SRAM cache. It is possible to access additional SRAM cache locations by providing new column addresses to the multiplex address inputs. New data is available at the output at time $t_{ASC} + t_{CLV}$ after each column address change.

DRAM Write Hit

A DRAM write request is initiated by clocking /RE while W/R, W/E, and /F are high. The EDRAM will compare the new row address to the LRR address latch for the bank specified by row address bits $A_{2,9}$(LRR: a 9-bit row address latch for each internal DRAM bank which is reloaded on each /RE active read miss cycle). If the row address matches the LRR, the EDRAM will write data to both the DRAM page in the appropriate bank and its corresponding SRAM cache simultaneously to maintain coherency. The write address and data are posted to the DRAM as soon as the column address is latched by bringing /CAL low and the write data is latched by bringing /WE low (both /CAL and /WE must be high when initiating the write cycle with the falling edge of /RE). The write address and data can be latched very quickly after the fall of /RE ($t_{RAH} + t_{ASC}$ for the column address and t_{DS} for the data). During a write burst sequence, the second write data can be posted at time t_{RSW} after /RE. Subsequent writes within a page can occur with write cycle time t_{PC}. With /G enabled and /WE disabled, it is possible to perform cache read operations while the /RE is activated in write hit mode. This allows read-modify-write, write-verify, or random read-write sequences within the page with 12ns cycle times (the first read cannot complete until after time t_{RAC2}). At the end of a write sequence (after /CAL and /WE are brought high and t_{RE} is satisfied), /RE can be brought high to precharge the memory. It is possible to perform cache reads concurrently with precharge. During write sequences, a write operation is not performed unless both /CAL and /WE are low. As a result, the /CAL input can be used as a byte write select in multi-chip systems. If /CAL is not clocked on a write sequence, the memory will perform a /RE only refresh to the selected row and data will remain unmodified.

DRAM Write Miss

A DRAM write request is initiated by clocking /RE while W/R, W/E, and /F are high. The EDRAM will compare the new row address to the LRR address latch for the bank specified for row address bits $A_{2,9}$ (LRR: a 9-bit row address latch for each internal DRAM bank which is reloaded on each /RE active read miss cycle). If the row address does not match any of the LRRs, the EDRAM will write data to the DRAM page in the appropriate bank and the contents of the current cache is not modified. The write address and data are posted to the DRAM as soon as the column address is latched by bringing /CAL low and the write data is latched by bringing /WE low (both /CAL and /WE must be high when initiating the write cycle with the falling edge of /RE). The write address and data can be latched very quickly after the fall of /RE ($t_{RAH} + t_{ASC}$ for the column address and t_{DS} for the data). During a write burst sequence, the second write data can be posted at time t_{RSW} after /RE. Subsequent writes within a page can occur with write cycle time t_{PC}. During a write miss sequence, cache reads are inhibited and the output buffers are disabled (independently of /G) until time t_{WRR} after /RE goes high. At the end of a write sequence (after /CAL and /WE

EDRAM Basic Operating Modes

Function	/S	/RE	W/R	/F	/CAL	/WE	A_{0-10}	Comment
Read Hit	L	↓	L	H	H	X	Row = LRR	No DRAM Reference, Data in Cache
Read Miss	L	↓	L	H	H	X	Row ≠ LRR	DRAM Row to Cache
Write Hit	L	↓	H	H	H	H	Row = LRR	Write to DRAM and Cache, Reads Enabled
Write Miss	L	↓	H	H	H	H	Row ≠ LRR	Write to DRAM, Cache Not Updated, Reads Disabled
Internal Refresh	X	↓	X	L	X	X	X	Cache Reads Enabled
Low Power Standby	H	H	X	X	H	H	X	Standby Current
Unallowed Mode	H	L	X	H	X	X	X	Unallowed Mode (Except -L Option)
Low Power Self Refresh Option	H	↓	X	H	L	H	X	Standby Current, Internal Refresh Clock

H = High; L = Low; X = Don't Care; ↓ = High-to-Low Transition; LRR = Last Row Read

are brought high and t_{RE} is satisfied), /RE can be brought high to precharge the memory. It is possible to perform cache reads concurrently with the precharge. During write sequences, a write operation is not performed unless both /CAL and /WE are low. As a result, /CAL can be used as a byte write select in multi-chip systems. If /CAL is not clocked on a write sequence, the memory will perform a /RE only refresh to the selected row and data will remain unmodified.

/RE Inactive Operation

It is possible to read data from the SRAM cache without clocking /RE. This option is desirable when the external control logic is capable of fast hit/miss comparison. In this case, the controller can avoid the time required to perform row/column multiplexing on hit cycles. This capability also allows the EDRAM to perform cache read operations during precharge and refresh cycles to minimize wait states. It is only necessary to select /S for the selected bank ($/S_0$ or $/S_1$) and /G and provide the appropriate column address to read data. The row address of the SRAM cache accessed without clocking /RE will be specified by the LRR address latch loaded during the last /RE active read cycle. To perform a cache read, /CAL is clocked to latch the column address. The cache data is valid at time t_{CLV} after the column address is setup to /CAL.

Write-Per-Bit Operation

The DM2M36SJ EDRAM SIMM provides a write-per-bit capability to selectively modify individual parity bits ($DQ_{8,17,26,35}$) for byte write operations. The parity devices (DM2252) are selected via $/CAL_P$. Data bits do not require or support write-per-bit capability. Byte write selection to non-parity bits is accomplished via $/CAL_{0-3}$. The bits to be written are determined by a bit mask data word which is placed on the parity I/O data pins prior to clocking /RE. The logic one bits in the mask data select the bits to be written. As soon as the mask is latched by /RE, the mask data is removed and write data can be placed on the databus. The mask is only specified on the /RE transition. During page mode burst write operations, the same mask is used for all write operations.

Internal Refresh

If /F is active (low) on the assertion of /RE, an internal refresh cycle is executed. This cycle refreshes the row address supplied by an internal refresh counter. This counter is incremented at the end of the cycle in preparation for the next /F refresh cycle. At least 1,024 /F cycles must be executed every 64ms. /F refresh cycles can be hidden because cache memory can be read under column address control throughout the entire /F cycle. /F cycles are the only active cycles during which /S can be disabled.

/CAL Before /RE Refresh ("/CAS Before /RAS")

/CAL before /RE refresh, a special case of internal refresh, is discussed in the "Reduced Pin Count Operation" section below.

/RE Only Refresh Operation

Although /F refresh using the internal refresh counter is the recommended method of EDRAM refresh, it is possible to perform an /RE only refresh using an externally supplied row address. /RE refresh is performed by executing a *write cycle* (W/R and /F are high) where /CAL is not clocked. This is necessary so that the current cache contents and LRR are not modified by the refresh operation. All combinations of addresses A_{0-9} must be sequenced every 64ms refresh period. A_{10} does not need to be cycled. Read refresh cycles are not allowed because a DRAM refresh cycle does not occur when a read refresh address matches the LRR address latch.

+3.3 Volt Power Supply Operation

If the +3.3 volt power supply option is specified, the EDRAM will operate from a +3.3 volt $\pm$0.3 volt power supply and all inputs and outputs will have LVTTL/LVCMOS compatible signal levels. The +3.3 volt EDRAM will not accept input levels which exceed the power supply voltage. If mixed I/O levels are expected in your system, please specify the +5 volt version of the EDRAM.

Low Power Mode

The EDRAM enters its low power mode when /S is high. In this mode, the internal DRAM circuitry is powered down to reduce standby current.

Low Power, Self-Refresh Option

When the low power, self refresh mode option is specified when ordering the EDRAM, the EDRAM enters this mode when /RE is clocked while /S, W/R, /F, and /WE are high; and /CAL is low. In this mode, the power is turned off to all I/O pins except /RE to minimize chip power, and an on-board refresh clock is enabled to perform self-refresh cycles using the on-board refresh counter. The EDRAM remains in this low power mode until /RE is brought high again to terminate the mode. The EDRAM /RE input must remain high for t_{RP2} following exit from self-refresh mode to allow any on-going internal refresh to terminate prior to the next memory operation.

Initialization Cycles

A minimum of eight /RE active initialization cycle (read, write or refresh) are required before normal operations is guaranteed. Following these start-up cycles, two read cycles to different row addresses must be performed for each of the four internal banks of DRAM to initialize the internal cache logic. Row address bits A_2 and A_9 define the four internal DRAM banks. /RE must be high for 300ns prior to initialization.

Unallowed Mode

Read, write, or /RE only operations must not be initiated to unselected memory banks by clocking /RE when /S is high.

Reduced Pin Count Operation

It is possible to simplify the interface to the 8Mbyte SIMM to reduce the number of control lines. /RE0 and /RE2 could be tied together externally to provide a single row enable for bank 0. W/R and /G can be tied together if reads are not performed during write hit cycles. This external wiring simplifies the interface without any performance impact.

Pin Descriptions

$/RE_{0,2,3}$ — Row Enable

This input is used to initiate DRAM read and write operations and latch a row address as well as the states of W/R and /F. It is not necessary to clock /RE to read data from the EDRAM SRAM row registers. On read operations, /RE can be brought high as soon as data is loaded into cache to allow early precharge. /RE to bank 0 and bank 1 must be clocked separately and only clocked during DRAM operations to the selected bank.

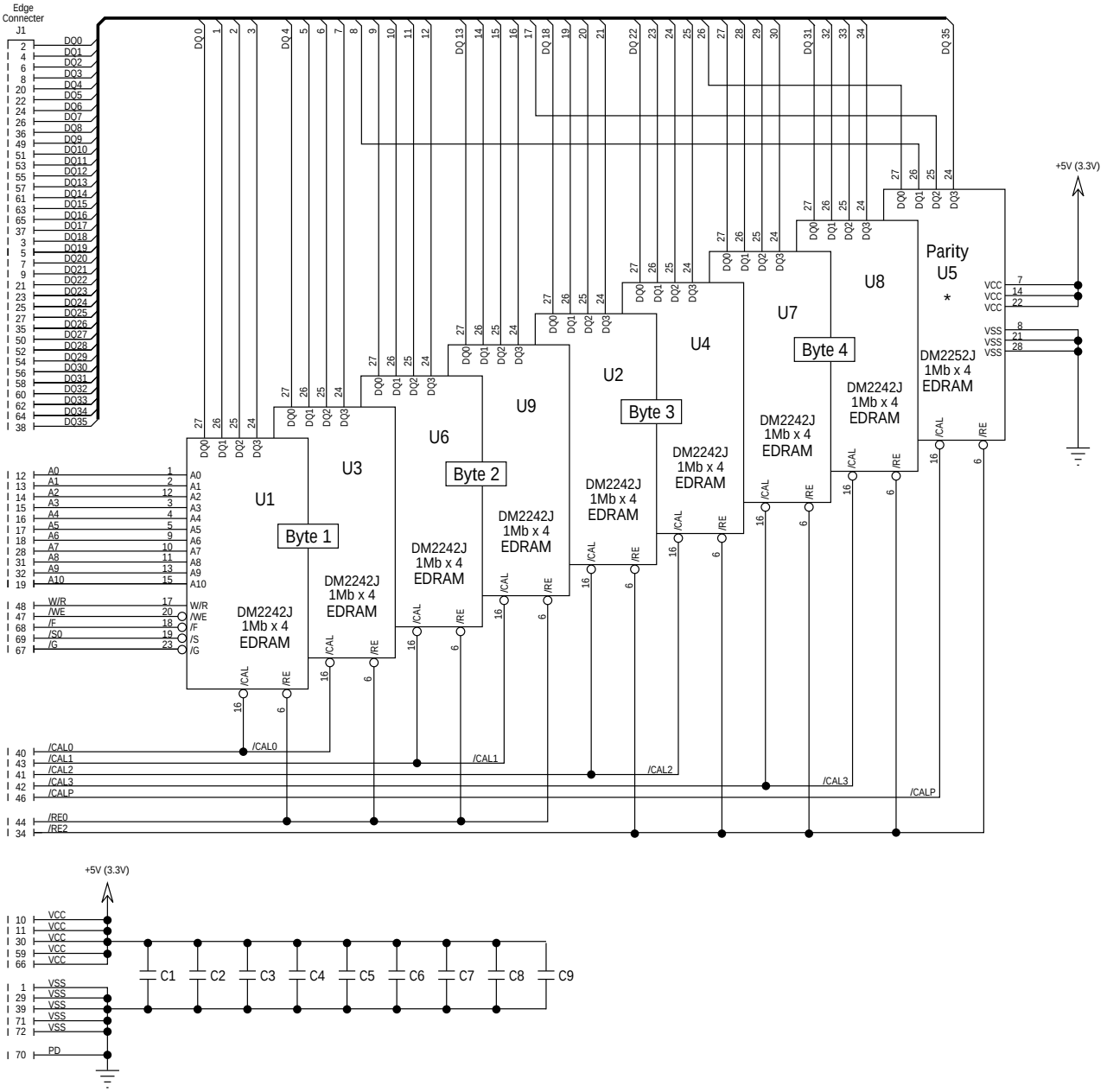
Pinout

Pin No.	*Function*	*Interconnect (Component Pin)*	*Organization*
1	GND	C (8,21,28)	Ground
2	DQ_0	U1,10 (27)	Byte 1 I/O 1
3	DQ_{18}	U2,11 (24)	Byte 3 I/O 1
4	DQ_1	U1,10 (26)	Byte 1 I/O 2
5	DQ_{19}	U2,11 (25)	Byte 3 I/O 2
6	DQ_2	U1,10 (25)	Byte 1 I/O 3
7	DQ_{20}	U2,11 (26)	Byte 3 I/O 3
8	DQ_3	U1,10 (24)	Byte 1 I/O 4
9	DQ_{21}	U2,11 (27)	Byte 3 I/O 4
10	+5/3.3 V	C (7,14,22)	V_{CC}
11	+5/3.3 V	C (7,14,22)	V_{CC}
12	A_0	C (1)	Address
13	A_1	C (2)	Address
14	A_2	C (12)	Address
15	A_3	C (3)	Address
16	A_4	C (4)	Address
17	A_5	C (5)	Address
18	A_6	C (9)	Address
19	A_{10}	C (15)	Address
20	DQ_4	U3,12 (27)	Byte 1 I/O 5
21	DQ_{22}	U4,13 (24)	Byte 3 I/O 5
22	DQ_5	U3,12 (26)	Byte 1 I/O 6
23	DQ_{23}	U4,13 (25)	Byte 3 I/O 6
24	DQ_6	U3,12 (25)	Byte 1 I/O 7
25	DQ_{24}	U4,13 (26)	Byte 3 I/O 7
26	DQ_7	U3,12 (24)	Byte 1 I/O 8
27	DQ_{25}	U4,13 (27)	Byte 3 I/O 8
28	A_7	C (10)	Address
29	GND	C (8,21,28)	Ground
30	+5/3.3 V	C (7,14,22)	V_{CC}
31	A_8	C (11)	Address
32	A_9	C (13)	Address
33	$/RE_3$	U10-18 (6)	Bank 1 Row Enable
34	$/RE_2$	U2,4,5,7,8 (6)	Bank 0 Row Enable (Bytes 3,4, Parity)
35	DQ_{26}*	U5,14 (27)	Parity I/O for Byte 3
36	DQ_8*	U5,14 (26)	Parity I/O for Byte 1
37	DQ_{17}*	U5,14 (25)	Parity I/O for Byte 2
38	DQ_{35}*	U5,14 (24)	Parity I/O for Byte 4
39	GND	C (8,21,28)	Ground
40	$/CAL_0$	U1,3,10,12 (16)	Byte 1 Column Address Latch
41	$/CAL_2$	U2,4,11,13 (16)	Byte 3 Column Address Latch
42	$/CAL_3$	U7,8,16,17 (16)	Byte 4 Column Address Latch
43	$/CAL_1$	U6,9,15,18 (16)	Byte 2 Column Address Latch
44	$/RE_0$	U1,3,6,9 (6)	Bank 0 Row Enable (Bytes 1,2)
45	$/S_1$	U10-18 (19)	Chip Select Bank 1
46	$/CAL_P$*	U5,14 (16)	Parity Column Address Latch
47	/WE	C (20)	Write Enable
48	W/R	C (17)	W/R Mode Control
49	DQ_9	U6,15 (27)	Byte 2 I/O 1
50	DQ_{27}	U7,16 (27)	Byte 4 I/O 1
51	DQ_{10}	U6,15 (26)	Byte 2 I/O 2
52	DQ_{28}	U7,16 (26)	Byte 4 I/O 2
53	DQ_{11}	U6,15 (25)	Byte 2 I/O 3
54	DQ_{29}	U7,16 (25)	Byte 4 I/O 3
55	DQ_{12}	U6,15 (24)	Byte 2 I/O 4
56	DQ_{30}	U7,16 (24)	Byte 4 I/O 4
57	DQ_{13}	U9,18 (24)	Byte 2 I/O 5
58	DQ_{31}	U8,17 (24)	Byte 4 I/O 5
59	+5/3.3 V	C (7,14,22)	V_{CC}
60	DQ_{32}	U8,17 (26)	Byte 4 I/O 6
61	DQ_{14}	U9,18 (25)	Byte 2 I/O 6
62	DQ_{33}	U8,17 (25)	Byte 4 I/O 7
63	DQ_{15}	U9,18 (26)	Byte 2 I/O 7
64	DQ_{34}	U8,17 (24)	Byte 4 I/O 8
65	DQ_{16}	U9,18 (27)	Byte 2 I/O 8
66	+5/3.3 V	C (7,14,22)	V_{CC}
67	/G	C (23)	Output Enable
68	/F	C (18)	Refresh Mode Control
69	$/S_0$	U1-9 (19)	Chip Select Bank 0
70	PD	Signal GND	Presence Detect
71	GND	C (8,21,28)	Ground
72	GND	C (8,21,28)	Ground

C = Common to All Memory Chips, U1 = Chip 1, etc.

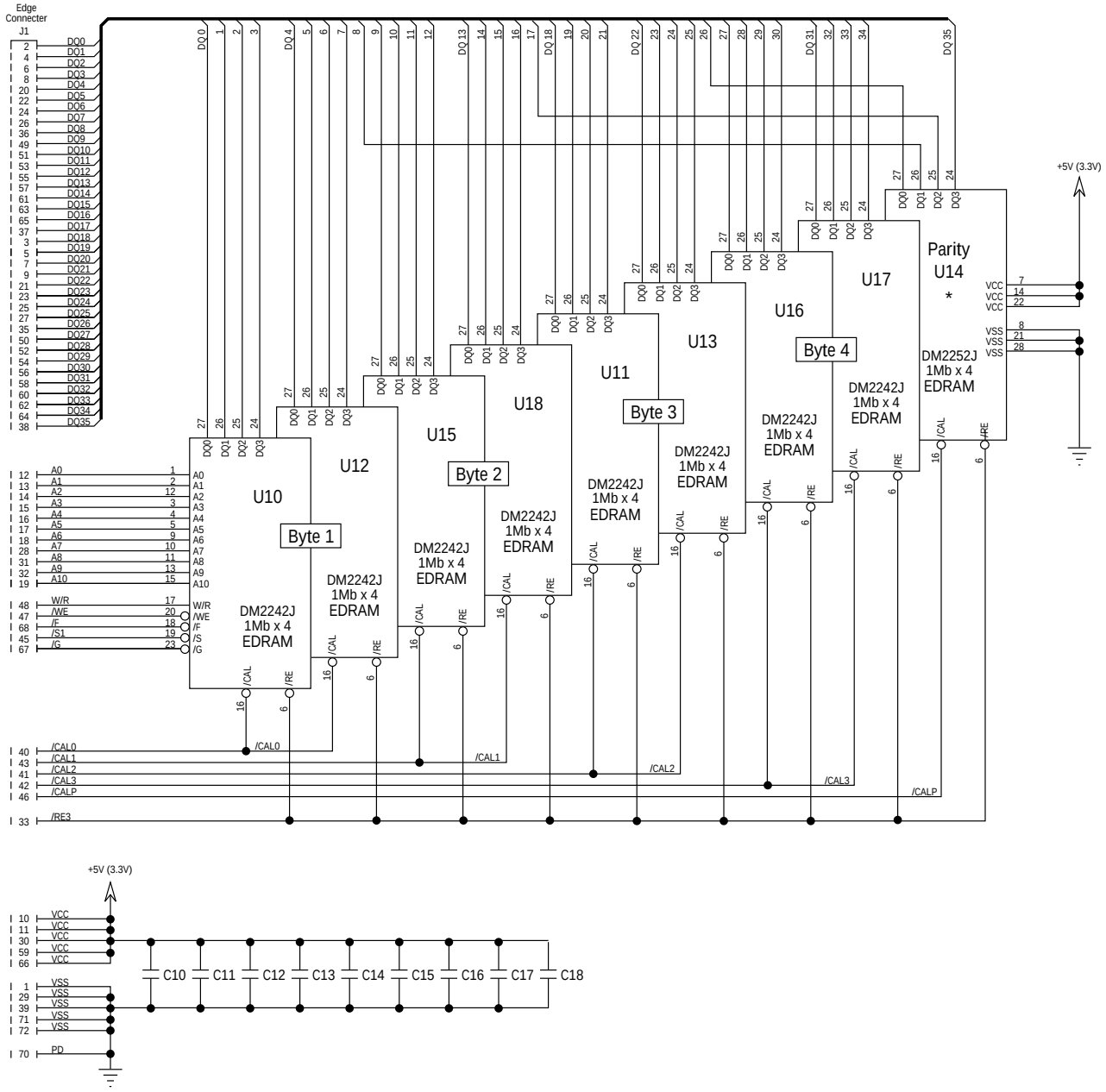
*No Connect for DM2M32SJ

Interconnect Diagram — Bank 0 (Components Mounted on Front Side)



*DM2212 is not present on the DM2M32SJ.

Interconnect Diagram — Bank 1 (Components Mounted on Back Side)



*DM2212 is not present on the DM2M32SJ.

/$CAL_{0-3,P}$ — Column Address Latch

This input is used to latch the column address and in combination with /WE to trigger write operations. When /CAL is high, the column address latch is transparent. When /CAL is low, the column address is closed and the output of the latch contains the address present while /CAL was high. It also controls the operation of the output data latch. Data is latched while /CAL is high and the latch is transparent when /CAL is low.

W/R — Write/Read

This input along with /F specifies the type of DRAM operation initiated on the low going edge of /RE. When /F is high, W/R specifies either a write (logic high) or read operation (logic low).

/F — Refresh

This input will initiate a DRAM refresh operation using the internal refresh counter as an address source when it is low on the low going edge of /RE.

/WE — Write Enable

This input controls the latching of write data on the input data pins. A write operation is initiated when both /CAL and /WE are low.

/G — Output Enable

This input controls the gating of read data to the output data pin during read operations.

/$S_{0,1}$ — Chip Select

This input is used to power up the I/O and clock circuitry. When /S is high, the EDRAM remains in its low power mode. /S must be used for bank selection on the 8Mbyte SIMM. /S must remain active throughout any read or write operation. With the exception of /F refresh cycles, /RE should never be clocked when /S is inactive.

DQ_{0-35} — Data Input/Output

These bidirectional data pins are used to read and write data to the EDRAM. On the DM2252 write-per-bit memory, these pins are also used to specify the bit mask used during write operations.

A_{0-10} — Multiplex Address

These inputs are used to specify the row and column addresses of the EDRAM data. The 11-bit row address is latched on the falling edge of /RE. The 9-bit column address can be specified at any other time to select read data from the SRAM cache or to specify the write column address during write cycles.

V_{CC} Power Supply

These inputs are connected to the +5 or 3.3 volt power supply.

V_{SS} Ground

These inputs are connected to the power supply ground connection.

Absolute Maximum Ratings

(Beyond Which Permanent Damage Could Result)

Description	3.3V Option Rating	Ratings
Input Voltage (V_{IN})	- .5 ~ 4.6v	- 1 ~ 7v
Output Voltage (V_{OUT})	- .5 ~ 4.6v	- 1 ~ 7v
Power Supply Voltage (V_{CC})	- .5 ~ 4.6v	- 1 ~ 7v
Ambient Operating Temperature (T_A)	-40 ~ +85°C	-40 ~ +85°C
Storage Temperature (T_S)	-55 ~ 150°C	-55 ~ 150°C
Static Discharge Voltage (Per MIL-STD-883 Method 3015)	Class 1	Class 1
Short Circuit O/P Current (I_{OUT})	20mA*	50mA*

* One output at a time per device; short duration

Capacitance

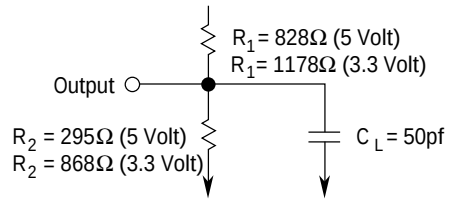
Description	Max*	Pins
Input Capacitance	130/136pf	A_{0-10}
Input Capacitance	165/180pf	W/R, /WE, /F
Input Capacitance	97/100pf	$/S_0$, $/S_1$
Input Capacitance	52pf	$/RE_0$
Input Capacitance	55/65pf	$/RE_2$
Input Capacitance	92/96pf	$/RE_3$
Input Capacitance	62/64pf	/G
Input Capacitance	52/55pf	$/CAL_{0-3}$
Input Capacitance	32pf	$/CAL_P$
I/O Capacitance	16pf	DQ_{0-35}

* DM2M32SJ6/DM2M36SJ6, respectively

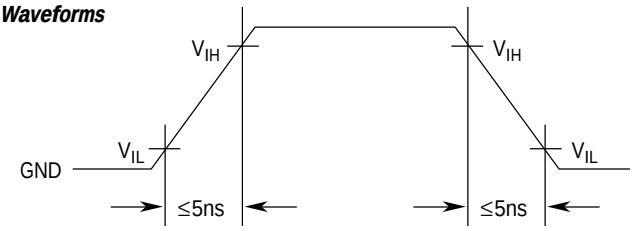
AC Test Load and Waveforms

V_{IN} Timing Reference Point at V_{IL} and V_{IH}

Load Circuit 5.0V (3.3V Option)



Input Waveforms



Electrical Characteristics T_A = 0 - 70°C, (Commercial), -40 ~ 85°C (Industrial)

Symbol	Parameters	3.3V Option Min	3.3V Option Max	Min	Max	Test Conditions
V_{CC}	Supply Voltage	3.0	3.6	4.75V	5.25V	All Voltages Referenced to V_{SS}
V_{IH}	Input High Voltage	2.0	V_{CC}+0.3V	2.4V	6.5V	
V_{IL}	Input Low Voltage	V_{SS}-0.3V	0.8V	-1.0V	0.8V	
V_{OH}	Output High Level	2.4V	—	2.4V	—	I_{OUT} = - 5mA (-2mA For 3.3V Option)
V_{OL}	Output Low Level	—	0.4V	—	0.4V	I_{OUT} = 4.2mA (2mA For 3.3V Option)
$I_{i(L)}$	Input Leakage Current	-90µA	90µA	-180µA	180µA	OV ≤ V_{IN} ≤ 6.5V, All Other Pins Not Under Test = 0V
$I_{O(L)}$	Output Leakage Current	-90µA	90µA	-180µA	180µA	OV ≤ V_{IN} , OV ≤ V_{OUT} ≤ 5.5V

Operating Current — DM2M32SJ

Symbol	Operating Current	33MHz Typ(1)	-12 Max	-15 Max	Test Condition	Notes
I_{CC1}	Random Read	880mA	1440mA	1440mA	/RE, /CAL, /G and Addresses Cycling: t_C = t_C Minimum	2, 3
I_{CC2}	Fast Page Mode Read	520mA	920mA	920mA	/CAL, /G and Addresses Cycling: t_{PC} = t_{PC} Minimum	2, 4
I_{CC3}	Static Column Read	440mA	720mA	720mA	/G and Addresses Cycling: t_{SC} = t_{SC} Minimum	2, 4
I_{CC4}	Random Write	1080mA	1200mA	1200mA	/RE, /CAL, /WE and Addresses Cycling: t_C = t_C Minimum	2, 3
I_{CC5}	Fast Page Mode Write	400mA	840mA	840mA	/CAL, /WE and Addresses Cycling: t_{PC} = t_{PC} Minimum	2, 4
I_{CC6}	Standby	16mA	16mA	16mA	All Control Inputs Stable ≥ V_{CC} - 0.2V	
I_{CC7}	Self-Refresh (-L Option)	1.6mA	1.6mA	1.6mA	/S, /F, W/R, /WE and A_{0-10} at ≥ V_{CC}-0.2V, /RE and /CAL at ≤V_{SS} + 0.2V, I/O Option	
I_{CCT}	Average Typical Operating Current	240mA	—	—	See "Estimating EDRAM Operating Power" Application Note	1

Operating Current — DM2M36SJ

Symbol	Operating Current	33MHz Typ(1)	-12 Max	-15 Max	Test Condition	Notes
I_{CC1}	Random Read	990mA	2025mA	1620mA	/RE, /CAL, /G and Addresses Cycling: t_C = t_C Minimum	2, 3
I_{CC2}	Fast Page Mode Read	585mA	1305mA	1035mA	/CAL, /G and Addresses Cycling: t_{PC} = t_{PC} Minimum	2, 4
I_{CC3}	Static Column Read	495mA	990mA	810mA	/G and Addresses Cycling: t_{SC} = t_{SC} Minimum	2, 4
I_{CC4}	Random Write	1215mA	1710mA	1350mA	/RE, /CAL, /WE and Addresses Cycling: t_C = t_C Minimum	2, 3
I_{CC5}	Fast Page Mode Write	450mA	1215mA	945mA	/CAL, /WE and Addresses Cycling: t_{PC} = t_{PC} Minimum	2, 4
I_{CC6}	Standby	18mA	18mA	18mA	All Control Inputs Stable ≥ V_{CC} - 0.2V, Outputs Driven	
I_{CC7}	Self-Refresh (-L Option)	1.8mA	1.8mA	1.8mA	/S, /F, W/R, /WE and A_{0-10} at ≥ V_{CC}-0.2V, /RE and /CAL at ≤V_{SS} +0.2V, I/O Option	
I_{CCT}	Average Typical Operating Current	270mA	—	—	See "Estimating EDRAM Operating Power" Application Note	1

(1) "33MHz Typ" refers to worst case I_{CC} expected in a system operating with a 33MHz memory bus. See power applications note for further details. This parameter is not 100% tested or guaranteed. (2) I_{CC} is dependent on cycle rates and is measured with CMOS levels and the outputs open. (3) I_{CC} is measured with a maximum of one address change while /RE = V_{IL} (4) I_{CC} is measured with a maximum of one address change while /CAL = V_{IH}.

Switching Characteristics

V_{CC} = 5V ± 5% (+5 Volt Option), Vcc = 3.3V ± 0.3V (+3.3 Volt Option), C_L = 50pf, T_A = 0 to 70°C (Commercial), -40 to 85°C (Industrial)

Symbol	Description	-12		-15		Units
		Min	Max	Min	Max	
t_{AC}[1]	Column Address Access Time		12		15	ns
t_{ACH}	Column Address Valid to /CAL Inactive (Write Cycle)	12		15		ns
t_{ACI}	Column Address	12		15		ns
t_{AQX}	Column Address Change to Output Data Invalid	5		5		ns
t_{ASC}	Column Address Setup Time	5		5		ns
t_{ASR}	Row Address Setup Time	5		5		ns
t_C	Row Enable Cycle Time	55		65		ns
t_{C1}	Row Enable Cycle Time, Cache Hit (Row=LRR), Read Cycle Only	20		25		ns
t_{CAE}	Column Address Latch Active Time	5		6		ns
t_{CAH}	Column Address Hold Time	0		0		ns
t_{CH}	Column Address Latch High Time (Latch Transparent)	5		5		ns
t_{CHR}	/CAL Inactive Lead Time to /RE Inactive (Write Cycles Only)	-2		-2		ns
t_{CHW}	Column Address Latch High to Write Enable Low (Multiple Writes)	0		0		ns
t_{CLV}	Column Address Latch High to Data Valid		7		7	ns
t_{CQH}	Column Address Latch Low to Data Invalid	0		5		ns
t_{CQV}	Column Address Latch High to Data Invalid		15		15	ns
t_{CRP}	Column Address Latch Setup Time to Row Enable	5		5		ns
t_{CWL}	/WE Low to /CAL Inactive	5		5		ns
t_{DH}	Data Input Hold Time	0		0		ns
t_{DMH}	Mask Hold Time From Row Enable (Write-Per-Bit)	1		1.5		ns
t_{DMS}	Mask Setup Time to Row Enable (Write-Per-Bit)	5		5		ns
t_{DS}	Data Input Setup Time	5		5		ns
t_{GQV}[1]	Output Enable Access Time		5		5	ns
t_{GQX}[2,3]	Output Enable to Output Drive Time	0	5	0	5	ns
t_{GQZ}[4,5]	Output Turn-Off Delay From Output Disabled (/G↑)	0	5	0	5	ns
t_{MH}	/F and W/R Mode Select Hold Time	0		0		ns
t_{MSU}	/F and W/R Mode Select Setup Time	5		5		ns
t_{NRH}	/CAL, /G, W/R, and /WE Hold Time For /RE-Only Refresh	0		0		ns
t_{NRS}	/CAL, /G, W/R, and /WE Setup Time For /RE-Only Refresh	5		5		ns
t_{PC}	Column Address Latch Cycle Time	12		15		ns
t_{RAC}[1]	Row Enable Access Time, On a Cache Miss		30		35	ns
t_{RAC1}[1]	Row Enable Access Time, On a Cache Hit (Limit Becomes t_{AC})		15		17	ns
t_{RAC2}[1,6]	Row Enable Access Time for a Cache Write Hit		30		35	ns
t_{RAH}	Row Address Hold Time	1		1.5		ns
t_{RE}	Row Enable Active Time	30	100000	35	100000	ns

Switching Characteristics (continued)

V_{CC} = 5V ± 5% (+5 Volt Option), Vcc = 3.3V ± 0.3V (+3.3 Volt Option), C_L = 50pf, T_A = 0 to 70°C (Commercial), -40 to 85°C (Industrial)

Symbol	Description	-12		-15		Units
		Min	Max	Min	Max	
t_{RE1}	Row Enable Active Time, Cache Hit (Row=LRR) Read Cycle	8		10		ns
t_{REF}	Refresh Period		64		64	ms
t_{RGX}	Output Enable Don't Care From Row Enable (Write, Cache Miss), O/P Hi Z	9		10		ns
t_{RQX1}(2,6)	Row Enable High to Output Turn-On After Write Miss	0	12	0	15	ns
t_{RP}(7)	Row Precharge Time	20		25		ns
t_{RP1}	Row Precharge Time, Cache Hit (Row=LRR) Read Cycle	8		10		ns
t_{RP2}	Row Precharge Time, Self-Refresh Mode	100		100		ns
t_{RRH}	Read Hold Time From Row Enable (Write Only)	0		0		ns
t_{RSH}	Last Write Address Latch to End of Write	12		15		ns
t_{RSW}	Row Enable to Column Address Latch Low For Second Write	35		40		ns
t_{RWL}	Last Write Enable to End of Write	12		15		ns
t_{SC}	Column Address Cycle Time	12		15		ns
t_{SHR}	Select Hold From Row Enable	0		0		ns
t_{SQV}(1)	Chip Select Access Time		12		15	ns
t_{SQX}(2,3)	Output Turn-On From Select Low	0	12	0	15	ns
t_{SQZ}(4,5)	Output Turn-Off From Chip Select	0	8	0	10	ns
t_{SSR}	Select Setup Time to Row Enable	5		5		ns
t_T	Transition Time (Rise and Fall)	1	10	1	10	ns
t_{WC}	Write Enable Cycle Time	12		15		ns
t_{WCH}	Column Address Latch Low to Write Enable Inactive Time	5		5		ns
t_{WHR}(7)	Write Enable Hold After /RE	0		0		ns
t_{WI}	Write Enable Inactive Time	5		5		ns
t_{WP}	Write Enable Active Time	5		5		ns
t_{WQV}(1)	Data Valid From Write Enable High		12		15	ns
t_{WQX}(2,5)	Data Output Turn-On From Write Enable High	0	12	0	15	ns
t_{WQZ}(3,4)	Data Turn-Off From Write Enable Low	0	12	0	15	ns
t_{WRP}	Write Enable Setup Time to Row Enable	5		5		ns
t_{WRR}	Write to Read Recovery (Following Write Miss)		16		18	ns

(1) V_{OUT} Timing Reference Point at 1.5V

(2) Parameter Defines Time When Output is Enabled (Sourcing or Sinking Current) and is Not Referenced to V_{OH} or V_{OL}

(3) Minimum Specification is Referenced from V_{IH} and Maximum Specification is Referenced from V_{IL} on Input Control Signal

(4) Parameter Defines Time When Output Achieves Open-Circuit Condition and is Not Referenced to V_{OH} or V_{OL}

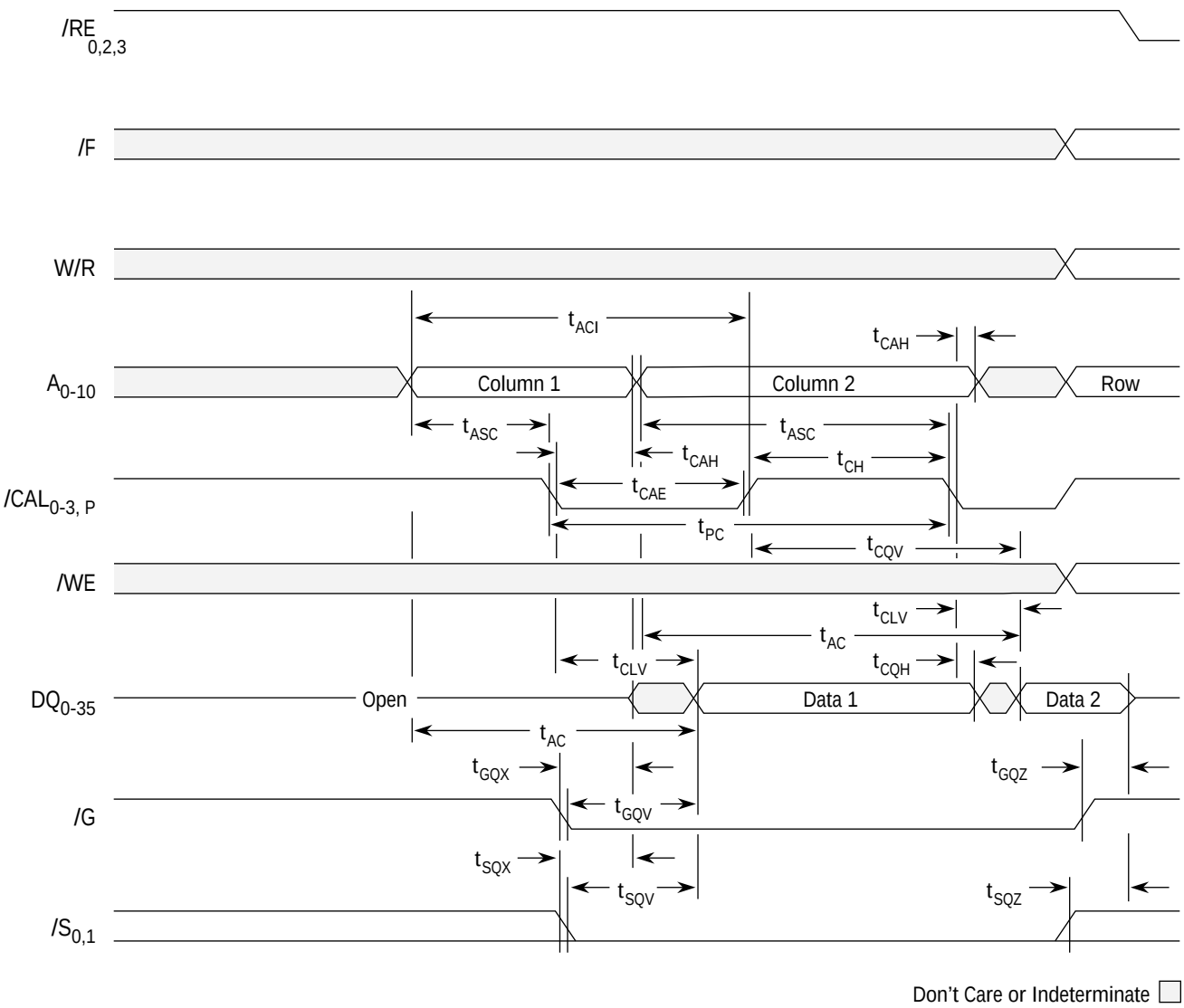
(5) Minimum Specification is Referenced from V_{IL} and Maximum Specification is Referenced from V_{IH} on Input Control Signal

(6) Access Parameter Applies When /CAL Has Not Been Asserted Prior to t_{RAC2}

(7) For Back-to-Back /F Refreshes, t_{RP} = 40ns. For Non-consecutive /F Refreshes, t_{RP} = 25ns and 32ns Respectively.

(8) For Write-Per-Bit Devices, t_{WHR} is Limited By Data Input Setup Time, t_{DS}

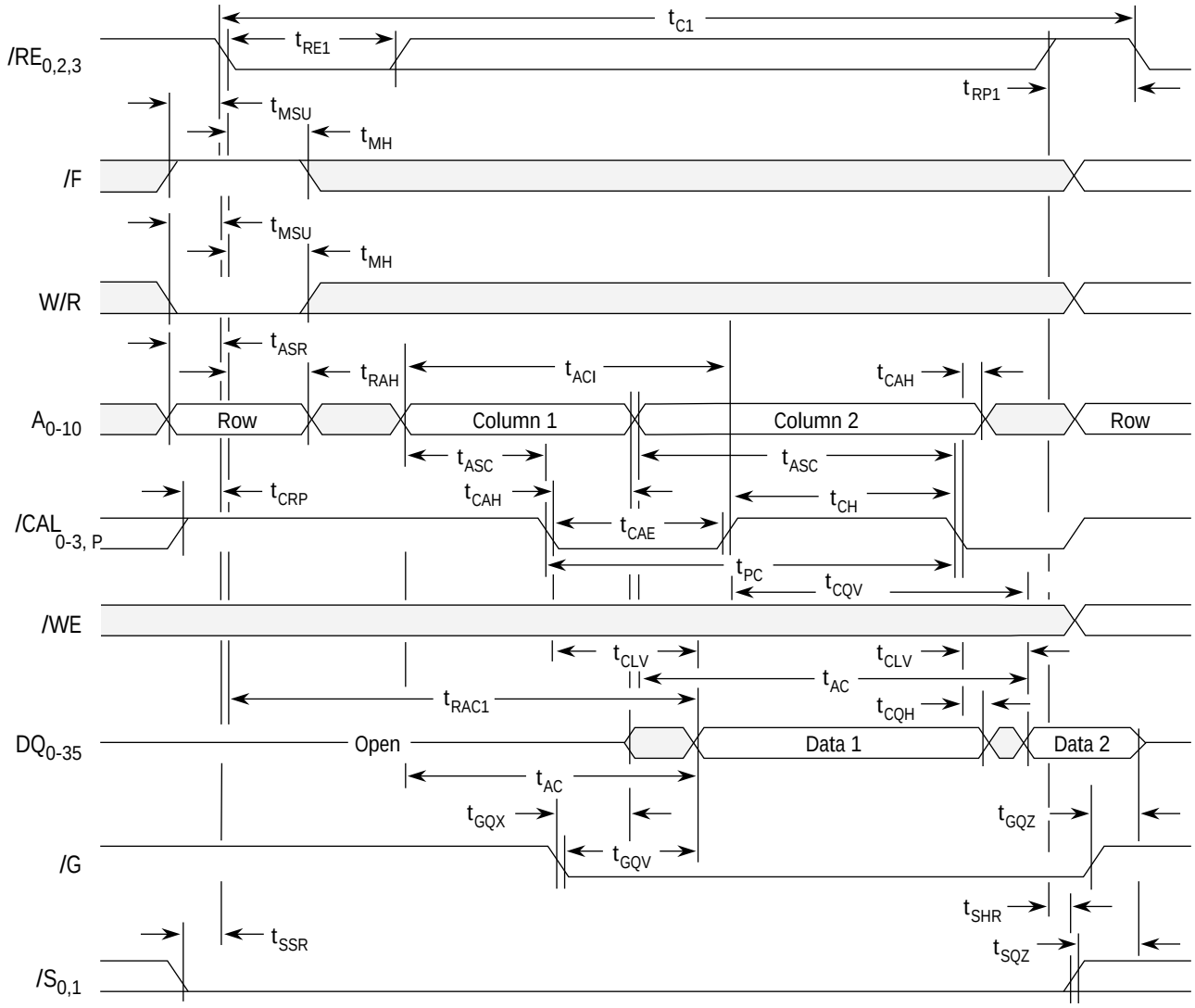
/RE Inactive Cache Read Hit (EDO Mode)



Notes: 1. Data accessed during /RE inactive read is from the row address specified during the last /RE active read cycle.

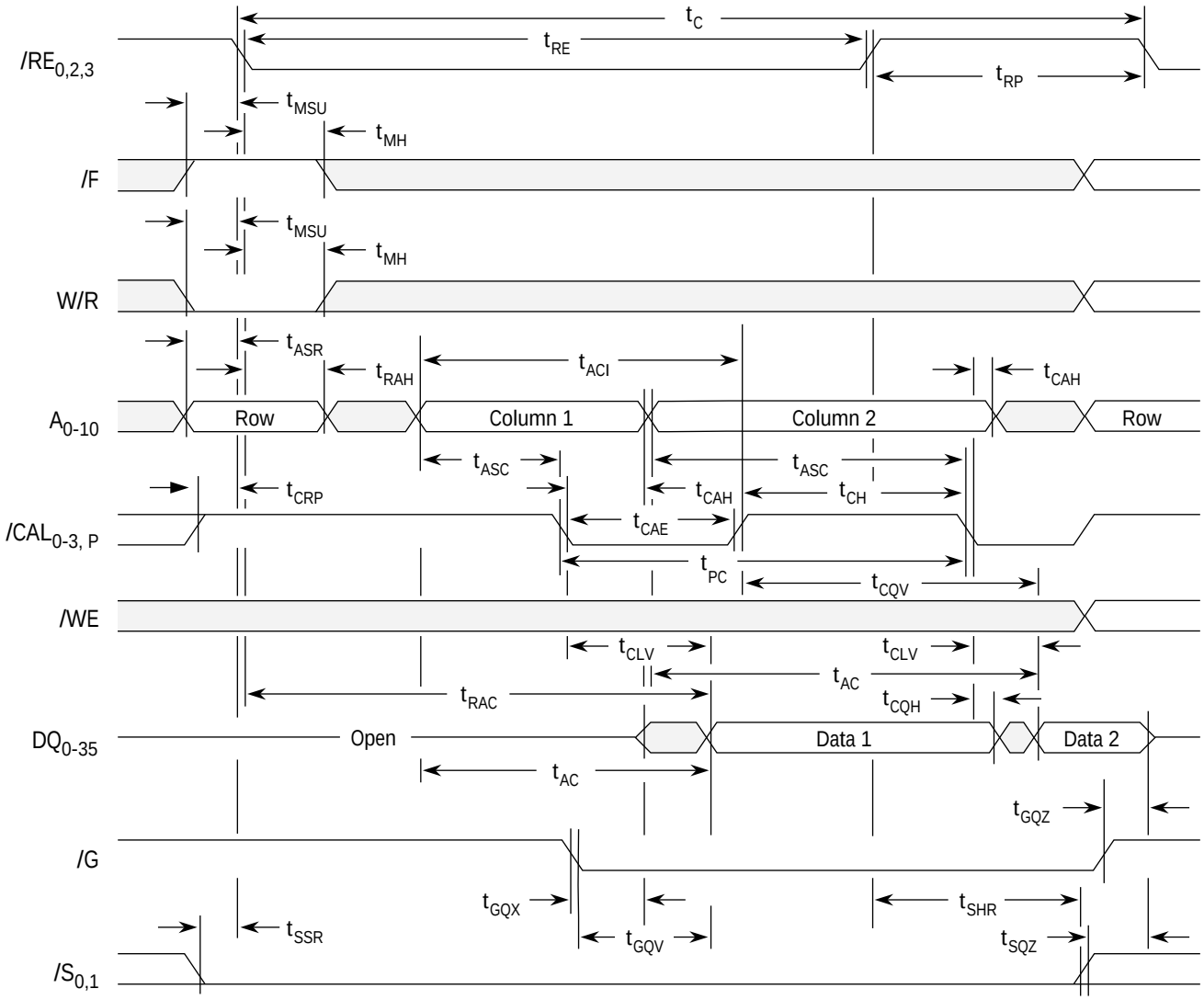
2. Latched data becomes invalid when /S is inactive.

/RE Active Cache Read Hit (EDO Mode)



Note: 1. Latched data becomes invalid when /S is inactive.

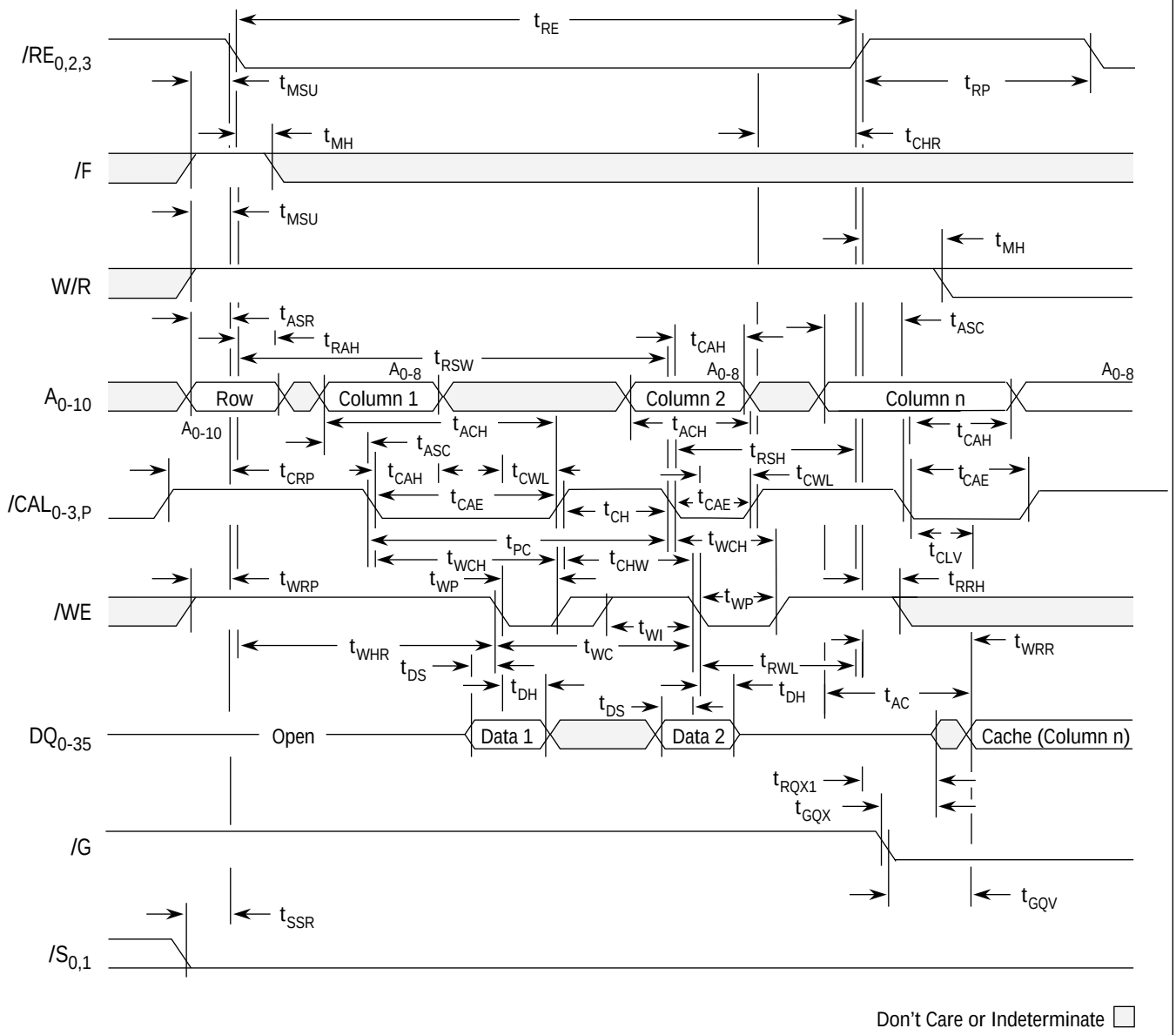
/RE Active Cache Read Miss (EDO Mode)



Don't Care or Indeterminate ☐

Note: 1. Latched data becomes invalid when /S is inactive.

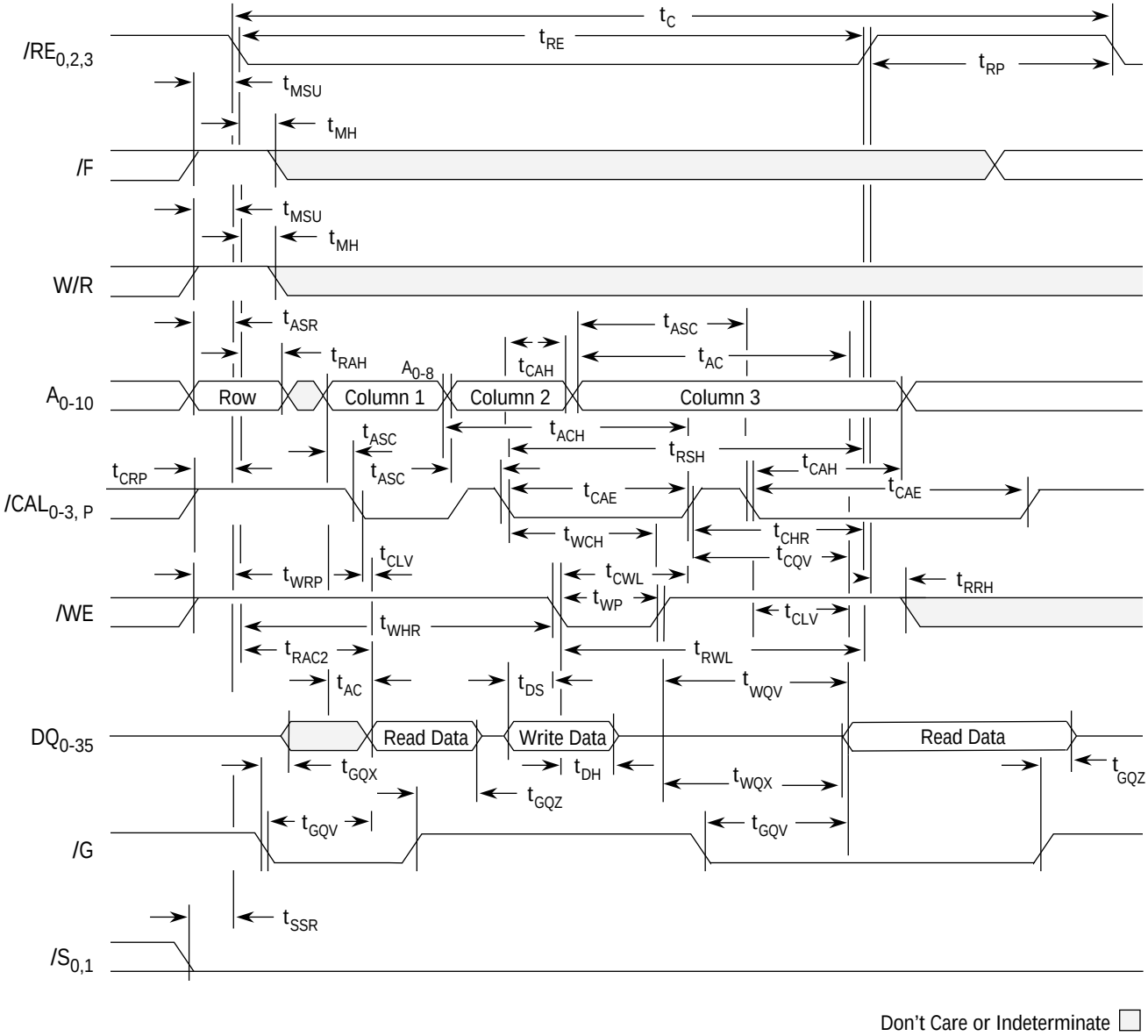
Burst Write (Hit or Miss) Followed By /RE Inactive Cache Reads



NOTES: 1. Parity bits $DQ_{8,17,26,35}$ must have mask provided at falling edge of /RE.

2. /G becomes a don't care after t_{RGX} during a write miss.

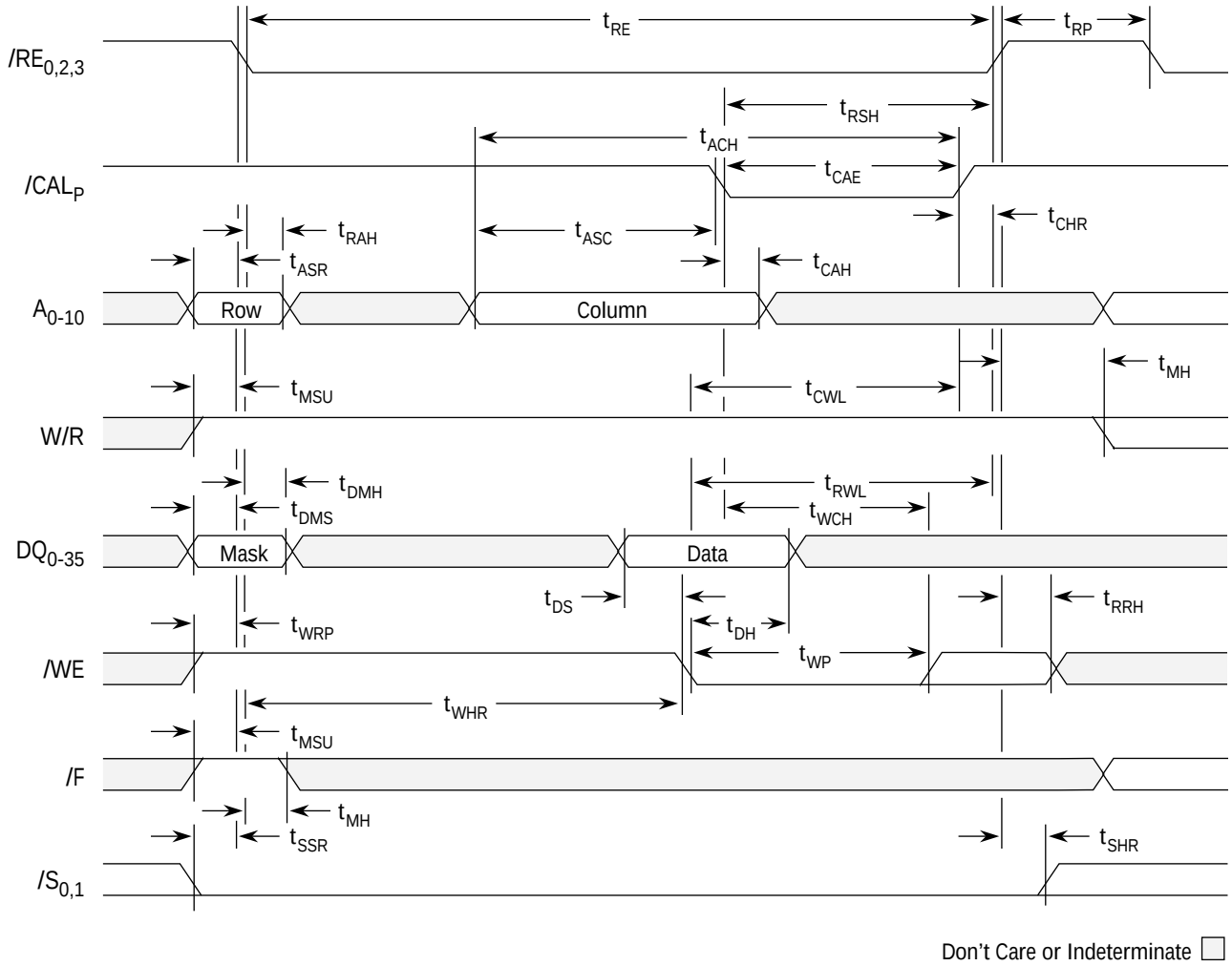
Page Read/Write During Write Hit Cycle



NOTES: 1. If column address 1 equals column address 2, then a read-modify-write cycle is performed.

2. Parity bits $DQ_{8,17,26,35}$ must have mask provided at falling edge of /RE.

Write-Per-Bit Cycle (/G = High)

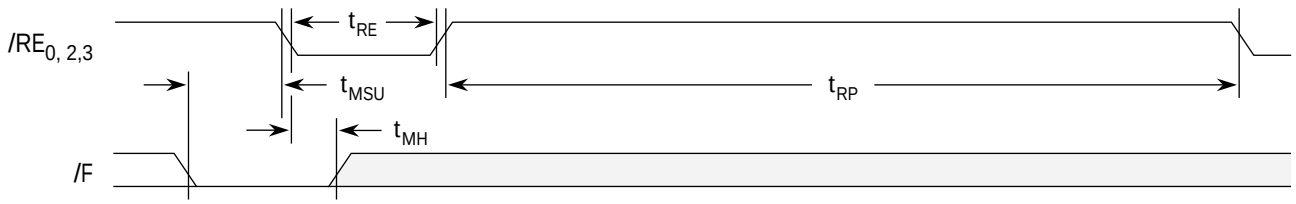


NOTES: 1. Data mask bit high (1) enables bit write; data mask bit low (0) inhibits bit write.

2. Write-per-bit cycle valid only for DM2M36SJ6.

3. Write-per-bit waveform applies to parity bits only ($DQ_{8,17,26,35}$).

/F Refresh Cycle

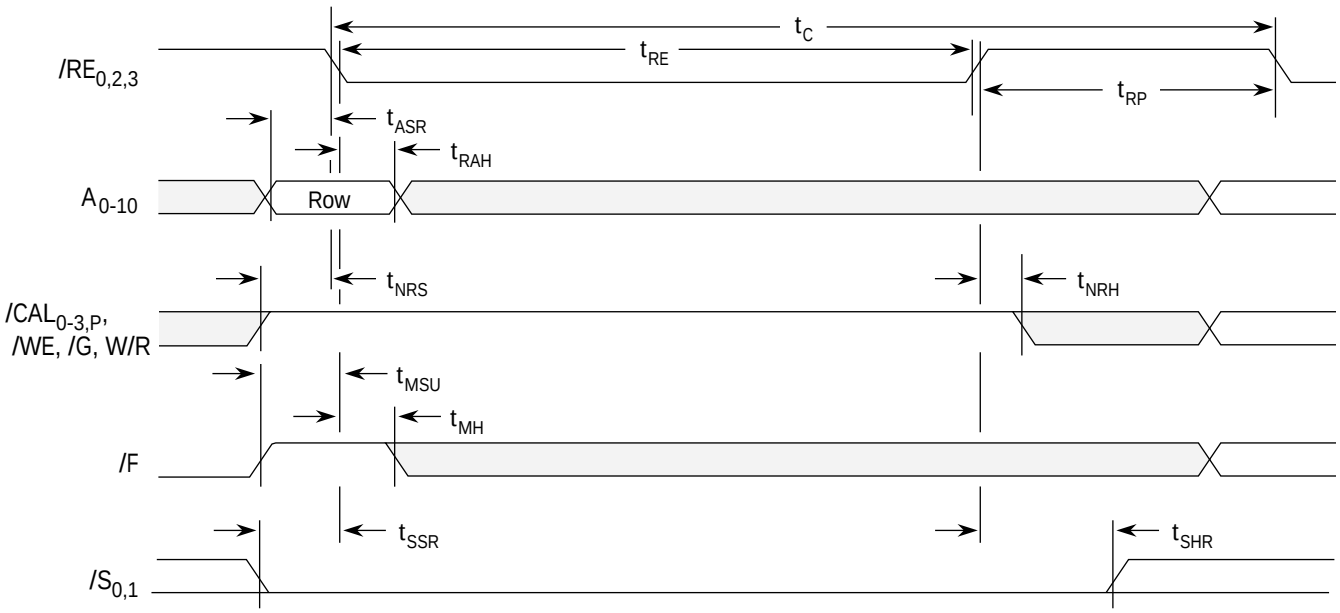


Don't Care or Indeterminate □

NOTES: 1. During /F refresh cycles, the status of W/R, /WE, A_{0-10}, /CAL, /S, and /G is a don't care.

2. /RE inactive cache reads may be performed in parallel with /F refresh cycles.

/RE-Only Refresh

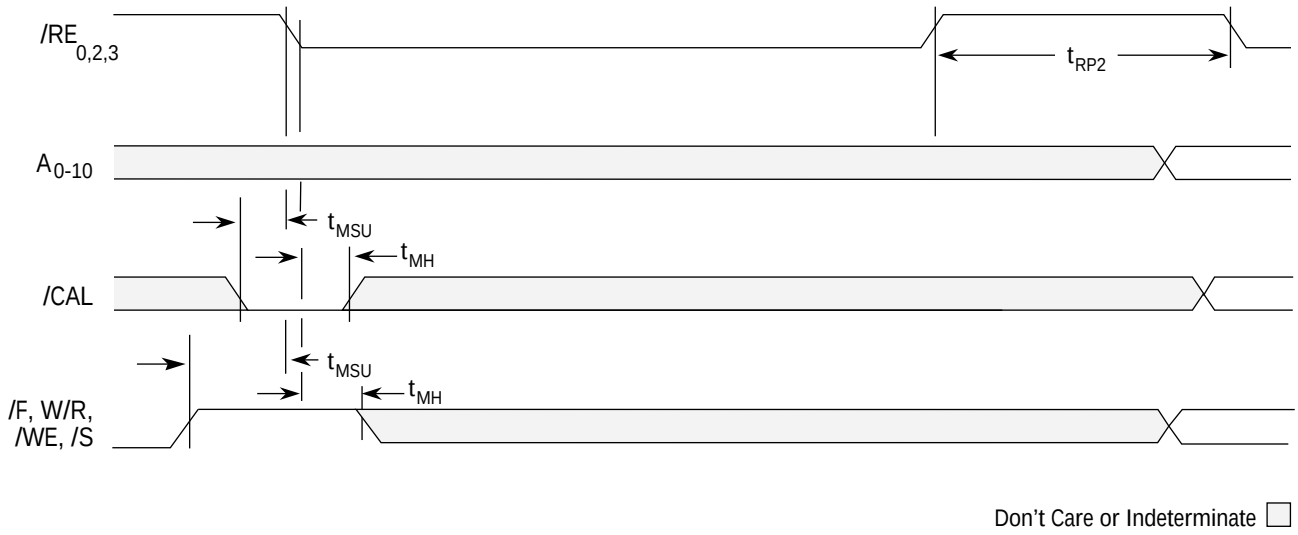


Don't Care or Indeterminate □

NOTES: 1. All binary combinations of A_{0-9} must be refreshed every 64ms interval. A_{10} does not have to be cycled, but must remain valid during row address setup and hold times.

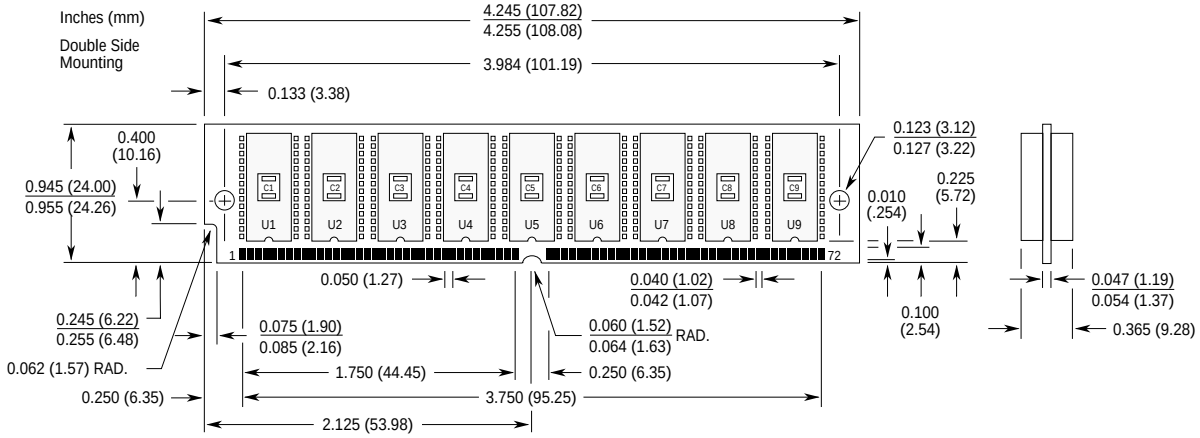
2. /RE refresh is write cycle with no /CAL active cycle.

Low Power Self-Refresh Mode Option



NOTES: 1. EDRAM self refreshes as long as /RE remains low. (Low Power Self-Refresh parts only).
2. When using the Low Power Self Refresh mode the following operations must be performed:
If row addresses are being refreshed in an *evenly distributed* manner over the refresh interval using /F refresh cycles, then at least one /F refresh cycle must be performed immediately after exit from the Low Power Self Refresh Mode. If row addresses are being refreshed in any other manner (/F burst or /RE distributed or burst), then all rows must be refresh immediately before entry to and immediately after exit from the Low Power Self Refresh.

Mechanical Data
72 Pin SIMM Module



U1-U4, U6-U9, U10-U13, U15-U17 — Enhanced DM2242J-XX, 1M x 4 EDRAMs, 300 Mil SOJ
U5, U14 — Enhanced DM2252J-XX, 1M x 4 EDRAM with Write-Per-Bit (Not present on DM2M32SJ)
C1-C18 — 0.22µF Chip Capacitors
Socket — Amp 822030-3 or Equivalent

Part Numbering System

DM2M36SJ 6- 12I

Temperature Range
No Designator = 0 to 70°C (Commercial)
I = -40 to 85°C (Industrial)
L = 0 to 70°C, Low Power Self-Refresh

Access Time from Cache in Nanoseconds
12ns
15ns

Configuration
6 = 5 Volt, Multibank EDO
7 = 3.3 Volt, Multibank EDO

Packaging System
J = 300 Mil, Plastic SOJ

Memory Module Configuration
S = SIMM

I/O Width (Including Parity)
32 = 32 Bits
36 = 36 Bits

Memory Depth (Megabits)
2M

Dynamic Memory