PD - 90679E

# International Rectifier

## REPETITIVE AVALANCHE AND dv/dt RATED HEXFET® TRANSISTOR

IRHN7250 IRHN8250 JANSR2N7269U JANSH2N7269U

(REF:MIL-PRF-19500/603)

N CHANNEL

MEGA RAD Hard™

#### 200Volt, 0.100Ω, MEGA RAD Hard™ HEXFET®

International Rectifier's RAD Hard technology HEXFETs demonstrate excellent threshold voltage stability and breakdown voltage stability at total radiation doses as high as 1x10<sup>6</sup> Rads(Si). Under **identical** pre- and post-irradiation test conditions, International Rectifier's RAD Hard HEXFETs retain **identical** electrical specifications up to 1 x 10<sup>5</sup> Rads (Si) total dose. No compensation in gate drive circuitry is required. These devices are also capable of surviving transient ionization pulses as high as 1 x 10<sup>12</sup> Rads (Si)/Sec, and return to normal operation within a few microseconds. Since the RAD Hard process utilizes International Rectifier's patented HEXFET technology, the user can expect the highest quality and reliability in the industry.

RAD Hard HEXFET transistors also feature all of the well-established advantages of MOSFETs, such as voltage control, very fast switching, ease of paralleling and temperature stability of the electrical parameters. They are well-suited for applications such as switching power supplies, motor controls, inverters, choppers, audio amplifiers and high-energy pulse circuits in space and weapons environments.

#### **Product Summary**

Part Number	BVDSS	RDS(on)	lD
IRHN7250	200V	0.100Ω	26A
IRHN8250	200V	0.100Ω	26A

#### Features:

- Radiation Hardened up to 1 x 10<sup>6</sup> Rads (Si)
- Single Event Burnout (SEB) Hardened
- Single Event Gate Rupture (SEGR) Hardened
- Gamma Dot (Flash X-Ray) Hardened
- Neutron Tolerant
- Identical Pre- and Post-Electrical Test Conditions
- Repetitive Avalanche Rating
- Dynamic dv/dt Rating
- Simple Drive Requirements
- Ease of Paralleling
- Hermetically Sealed
- Electrically Isolated
- Ceramic EyeletsSurface Mount
- Light Weight

#### **Absolute Maximum Ratings** ①

#### **Pre-Irradiation**

	Parameter		Units
ID @ VGS = 12V, TC = 25°C	Continuous Drain Current	26	
ID @ VGS = 12V, TC = 100°C	Continuous Drain Current	16	Α
IDM	Pulsed Drain Current @	104	
P <sub>D</sub> @ T <sub>C</sub> = 25°C	Max. Power Dissipation	150	W
	Linear Derating Factor	1.2	W/°C
VGS	Gate-to-Source Voltage	±20	V
EAS	Single Pulse Avalanche Energy ③	500	mJ
IAR	Avalanche Current ②	26	А
EAR	Repetitive Avalanche Energy@	15	mJ
dv/dt	Peak Diode Recovery dv/dt 4	5.0	V/ns
ТЈ	Operating Junction	-55 to 150	
TSTG Storage Temperature Range			°C
	Pckg. Mounting Surface Temp.	300 (for 5 s)	
	Weight	2.6 (typical)	g

#### **Pre-Irradiation**

#### **Electrical Characteristics** @ Tj = 25°C (Unless Otherwise Specified) ①

		_	_		
Parameter	Min	Тур	Max	Units	Test Conditions
Drain-to-Source Breakdown Voltage	200	_	_	V	VGS = 0V, ID = 1.0mA
Temperature Coefficient of Breakdown Voltage		0.27	_	V/°C	Reference to 25°C, ID = 1.0mA
Static Drain-to-Source On-State	_	_	0.10		VGS = 12V, ID = 16A (\$)
Resistance	_	_	0.11	1 12	VGS = 12V, ID = 26A ⑤
Gate Threshold Voltage	2.0	_	4.0	V	$V_{DS} = V_{GS}$ , $I_{D} = 1.0$ mA
Forward Transconductance	8.0	_	_	S (7)	VDS > 15V, IDS = 16A ⑤
Zero Gate Voltage Drain Current	_	_	25		V <sub>DS</sub> = 0.8 x Max Rating,V <sub>GS</sub> =0V
	_	_	250	μΑ	VDS = 0.8 x Max Rating
					VGS = 0V, TJ = 125°C
Gate-to-Source Leakage Forward	_	_	100	m Λ	VGS = 20V
Gate-to-Source Leakage Reverse	_	_	-100	nA	VGS = -20V
Total Gate Charge	_	_	170		VGS =12V, ID = 26A
Gate-to-Source Charge	_	_	30	nC	V <sub>DS</sub> = Max Rating x 0.5
Gate-to-Drain ('Miller') Charge	_	_	60		
Turn-On Delay Time	_	_	33		$V_{DD} = 100V, I_{D} = 26A,$
Rise Time	_		140		$R_G = 2.35\Omega$
Turn-Off Delay Time	_	_	140	ns	
Fall Time	_	_	140		
Internal Drain Inductance	_	2.0	_	nН	
Internal Source Inductance	_	4.1	_	11111	
Input Capacitance	_	4700	_		VGS = 0V, VDS = 25V
Output Capacitance	_	850	_	pF	f = 1.0MHz
Reverse Transfer Capacitance	_	210	_	1	
	Drain-to-Source Breakdown Voltage Temperature Coefficient of Breakdown Voltage Static Drain-to-Source On-State Resistance Gate Threshold Voltage Forward Transconductance Zero Gate Voltage Drain Current  Gate-to-Source Leakage Forward Gate-to-Source Leakage Reverse Total Gate Charge Gate-to-Source Charge Gate-to-Drain ('Miller') Charge Turn-On Delay Time Rise Time Turn-Off Delay Time Fall Time Internal Drain Inductance  Input Capacitance Output Capacitance	Drain-to-Source Breakdown Voltage Temperature Coefficient of Breakdown Voltage Static Drain-to-Source On-State — Resistance — Gate Threshold Voltage 2.0 Forward Transconductance 8.0 Zero Gate Voltage Drain Current — Gate-to-Source Leakage Forward — Gate-to-Source Leakage Reverse — Total Gate Charge — Gate-to-Source Charge — Gate-to-Drain ('Miller') Charge — Turn-On Delay Time — Rise Time — Turn-Off Delay Time — Fall Time — Internal Drain Inductance —  Input Capacitance — Output Capacitance —  Input Capacitance —  Input Capacitance —  Input Capacitance —  Output Capacitance —  Input Capacitance —  Input Capacitance —  Input Capacitance —  Input Capacitance —  Output Capacitance —  Input Capacit	Drain-to-Source Breakdown Voltage Temperature Coefficient of Breakdown Voltage Static Drain-to-Source On-State — — — — — — — — — — — — — — — — — — —	Drain-to-Source Breakdown Voltage         200         —         —           Temperature Coefficient of Breakdown Voltage         —         0.27         —           Static Drain-to-Source On-State         —         —         0.10           Resistance         —         —         0.11           Gate Threshold Voltage         2.0         —         4.0           Forward Transconductance         8.0         —         —           Zero Gate Voltage Drain Current         —         25         —         250           Gate-to-Source Leakage Forward         —         —         100         —         30         —         —         170         Gate-to-Source Leakage Reverse         —         —         170         Gate-to-Source Charge         —         —         170         Gate-to-Source Charge         —         —         170         Gate-to-Drain ('Miller') Charge         —         —         60         Turn-On Delay Time         —         —         140         Turn-Off Delay Time         —         —         140         Turn-Off Delay Time         —         —         140         —         —         —         —         —         —         —         —         —         —         —         —	Drain-to-Source Breakdown Voltage         200         —         V           Temperature Coefficient of Breakdown Voltage         —         0.27         —         V/°C           Static Drain-to-Source On-State Resistance         —         —         0.10         Ω           Resistance         —         —         0.11         Ω           Gate Threshold Voltage         2.0         —         4.0         V           Forward Transconductance         8.0         —         —         S (τ)           Zero Gate Voltage Drain Current         —         —         25         μΑ           Gate-to-Source Leakage Forward         —         —         100         nA           Gate-to-Source Leakage Reverse         —         —         -100         nA           Total Gate Charge         —         —         170         nC           Gate-to-Source Charge         —         —         30         nC           Gate-to-Drain ('Miller') Charge         —         —         60         n           Turn-On Delay Time         —         —         140         ns           Fall Time         —         —         140         n           Internal Drain Inductance         —

#### **Source-Drain Diode Ratings and Characteristics** ①

	Parameter	Min	Тур	Max	Units	Test Conditions		
Is	Continuous Source Current (Body Diode)	_	_	26	Α			
ISM	Pulse Source Current (Body Diode) ②	_	_	104	^			
VSD	Diode Forward Voltage	_	_	1.4	V	Tj = 25°C, IS = 26A, VGS = 0V ⑤		
trr	Reverse Recovery Time	_	_	820	ns	Tj = 25°C, IF = 26A, di/dt ≥100A/μs		
QRR	Reverse Recovery Charge	—	—	12	μС	V <sub>DD</sub> ≤ 25V ⑤		
ton	Forward Turn-On Time Intrinsic turn-or	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by LS + LD						

#### **Thermal Resistance**

	Parameter	Min	Тур	Max	Units	Test Conditions
RthJC	Junction-to-Case	_	_	0.83	°C/W	
RthJ-PCB	Junction-to-PC board	_	6.6	_	C/VV	Soldered to a 1 inch square clad PC board

#### **Radiation Characteristics**

### IRHN7250, IRHN8250, JANSR-, JANSH-, 2N7269U Devices

#### Radiation Performance of Rad Hard HEXFETs

International Rectifier Radiation Hardened HEXFETs are tested to verify their hardness capability. The hardness assurance program at International Rectifier comprises three radiation environments.

Every manufacturing lot is tested in a low dose rate (total dose) environment per MIL-STD-750, test method 1019 condition A. International Rectifier has imposed a standard gate condition of 12 volts per note 6 and a  $V_{\rm DS}$  bias condition equal to 80% of the device rated voltage per note 7. Pre- and post- irradiation limits of the devices irradiated to 1 x 10 $^{\rm 5}$  Rads (Si) are identical and are presented in Table 1, column 1, IRHN7250. Post-irradiation limits of the devices irradiated to 1 x 10 $^{\rm 6}$  Rads (Si) are presented in

Table 1, column 2, IRHN8250. The values in Table 1 will be met for either of the two low dose rate test circuits that are used. Both pre- and post-irradiation performance are tested and specified using the same drive circuitry and test conditions in order to provide a direct comparison.

High dose rate testing may be done on a special request basis using a dose rate up to 1 x  $10^{12}$  Rads (Si)/Sec (See Table 2).

International Rectifier radiation hardened HEXFETs have been characterized in heavy ion Single Event Effects (SEE) environments. Single Event Effects characterization is shown in Table 3.

Table 1. Low Dose Rate ©©IRHN7250IRHN8250

	Parameter	100K F	100K Rads (Si)		1000K Rads (Si)		Test Conditions ®
		Min	Max	Min	Max		
BV <sub>DSS</sub>	Drain-to-Source Breakdown Voltage		_	200	_	V	$V_{GS} = 0V, I_{D} = 1.0 \text{mA}$
VGS(th)	Gate Threshold Voltage	2.0	4.0	1.25	4.5		$V_{GS} = V_{DS}$ , $I_D = 1.0 \text{mA}$
IGSS	Gate-to-Source Leakage Forward	_	100	_	100	nA	V <sub>GS</sub> = 20V
I <sub>GSS</sub>	Gate-to-Source Leakage Reverse		-100	_	-100		V <sub>GS</sub> = -20 V
IDSS	Zero Gate Voltage Drain Current	_	25	_	50	μA	V <sub>DS</sub> =0.8 x Max Rating, V <sub>GS</sub> =0V
R <sub>DS(on)1</sub>	Static Drain-to-Source	_	0.100	_	0.155	Ω	Vgs = 12V, I <sub>D</sub> = 16A
	On-State Resistance One						
V <sub>SD</sub>	Diode Forward Voltage ⑤	_	1.4	_	1.4	V	$T_C = 25^{\circ}C$ , $I_S = 26A$ , $V_{GS} = 0V$

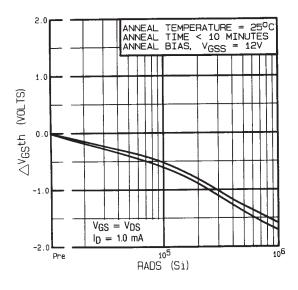
Table 2. High Dose Rate ®

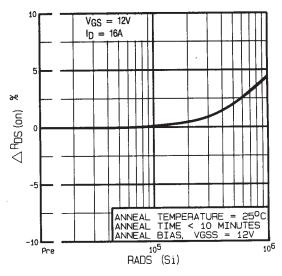
		10 <sup>11</sup> F	Rads	(Si)/sec	10 <sup>12</sup> F	Rads (	Si)/sec		
	Parameter	Min	Тур	Max	Min	Тур	Max	Units	Test Conditions
VDSS	Drain-to-Source Voltage	<u> </u>	_	160	_	_	160	V	Applied drain-to-source voltage during
									gamma-dot
IPP		_	15	_	_	15	_	Α	Peak radiation induced photo-current
di/dt		_	_	160	_	_	8.0	A/µsec	Rate of rise of photo-current
L <sub>1</sub>		1.0	_	_	20	-		μH	Circuit inductance required to limit di/dt

**Table 3. Single Event Effects** 

lon	LET (Si) Fluence (ions/cm²)		Range (µm)	V <sub>DS</sub> Bias (V)	V <sub>GS</sub> Bias (V)
Cu	28	3x 10⁵	43	180	-5

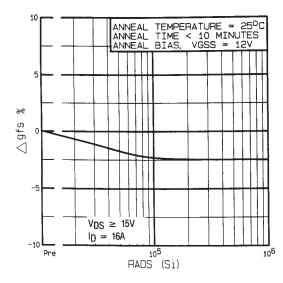
#### **Post-Irradiation**

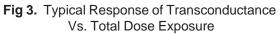


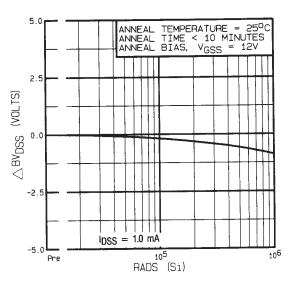


**Fig 1.** Typical Response of Gate Threshhold Voltage Vs. Total Dose Exposure

**Fig 2.** Typical Response of On-State Resistance Vs. Total Dose Exposure



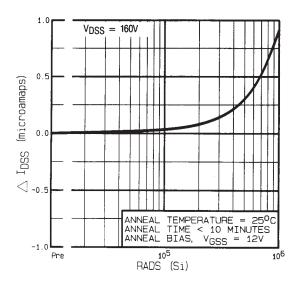




**Fig 4.** Typical Response of Drain to Source Breakdown Vs. Total Dose Exposure

#### **Post-Irradiation**

#### IRHN7250, IRHN8250, JANSR-, JANSH-, 2N7269U Devices

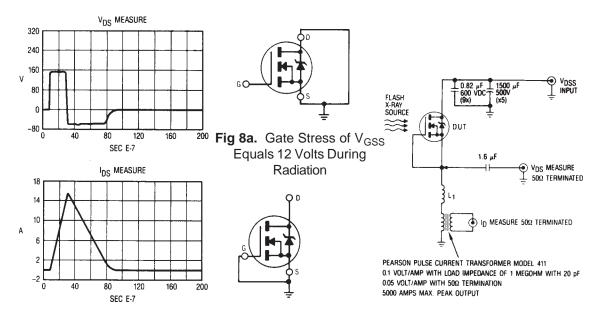


ANNEAL TEMPERATURE = 25°C
ANNEAL TIME < 10 MINUTES
ANNEAL BIAS, VGSS = 12V

NEUTRON FLUENCE (NEUTRON/CM²)

**Fig 5.** Typical Zero Gate Voltage Drain Current Vs. Total Dose Exposure

**Fig 6.** Typical On-State Resistance Vs. Neutron Fluence Level



**Fig 7.** Typical Transient Response of Rad Hard HEXFET During 1x10<sup>12</sup> Rad (Si)/Sec Exposure

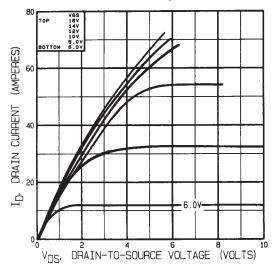
Fig 8b.  $V_{DSS}$  Stress Equals 80% of  $B_{VDSS}$  During Radiation

Fig 9. High Dose Rate (Gamma Dot) Test Circuit

#### **Radiation Characteristics**

**Devices** 

Note: Bias Conditions during radiation: Vgs = 12 Vdc, Vps = 0 Vdc



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**Fig 10.** Typical Output Characteristics Pre-Irradiation

**Fig 11.** Typical Output Characteristics Post-Irradiation 100K Rads (Si)

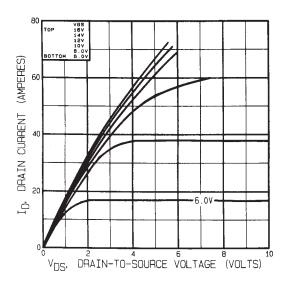


Fig 12. Typical Output Characteristics Post-Irradiation 300K Rads (Si)

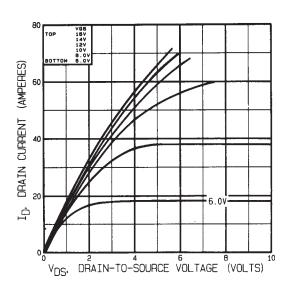
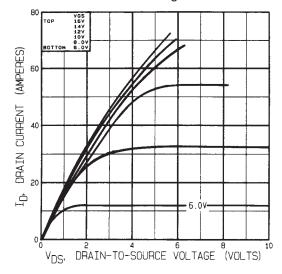


Fig 13. Typical Output Characteristics Post-Irradiation 1 Mega Rads(Si)

#### **Radiation Characteristics**

#### IRHN7250, IRHN8250, JANSR-, JANSH-, 2N7269U Devices

Note: Bias Conditions during radiation: Vgs = 0 Vdc, Vps = 160 Vdc



**Fig 14.** Typical Output Characteristics Pre-Irradiation

Fig 15. Typical Output Characteristics Post-Irradiation 100K Rads (Si)

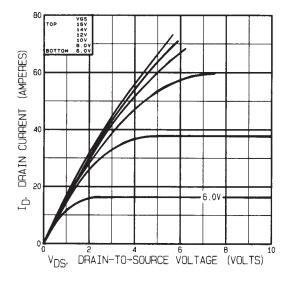


Fig 16. Typical Output Characteristics Post-Irradiation 300K Rads (Si)

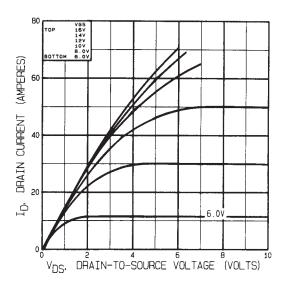
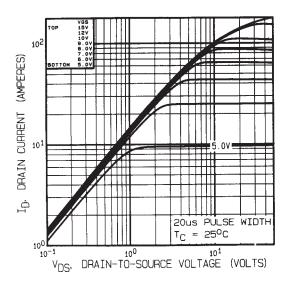


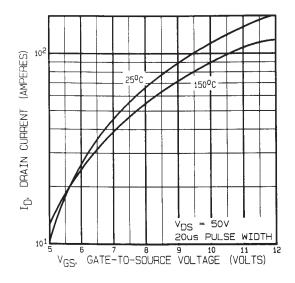
Fig 17. Typical Output Characteristics Post-Irradiation 1 Mega Rads(Si)



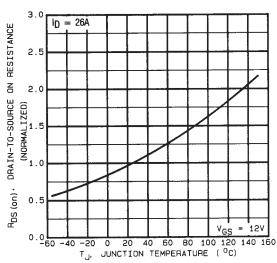
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Fig 18. Typical Output Characteristics

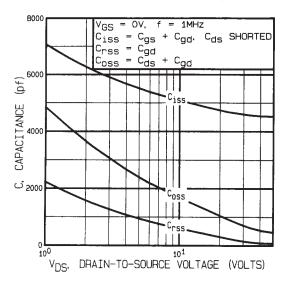
Fig 19. Typical Output Characteristics







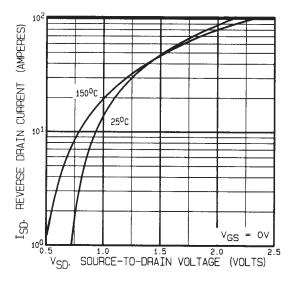
**Fig 21.** Normalized On-Resistance Vs. Temperature

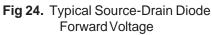


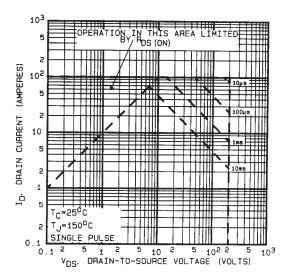
 $I_D = 26A$ = 80V V<sub>DS</sub> (VOLTS) V<sub>DS</sub> = 50V 16 ۷DŞ = 20V GATE-TO-SOURCE VOLTAGE 12 V<sub>GS</sub> FOR TEST CIRCUIT SEE FIGURE 30 60 90 120 150 TOTAL GATE CHARGE (nC)

**Fig 22.** Typical Capacitance Vs. Drain-to-Source Voltage

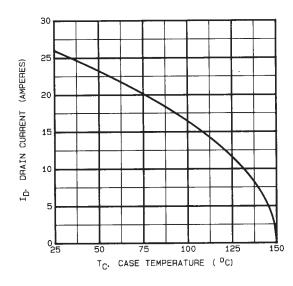
**Fig 23.** Typical Gate Charge Vs. Gate-to-Source Voltage







**Fig 25.** Maximum Safe Operating Area



**Fig 26.** Maximum Drain Current Vs. Case Temperature

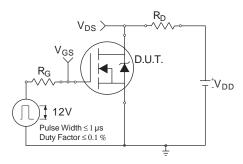


Fig 27a. Switching Time Test Circuit

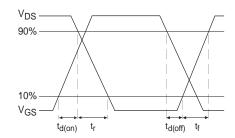


Fig 27b. Switching Time Waveforms

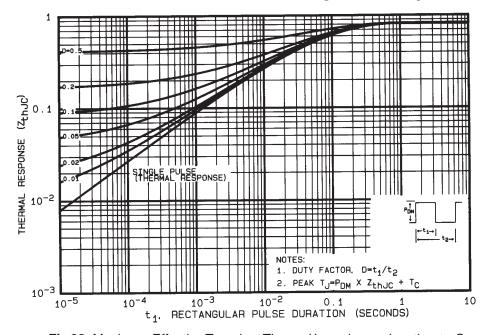


Fig 28. Maximum Effective Transient Thermal Impedance, Junction-to-Case

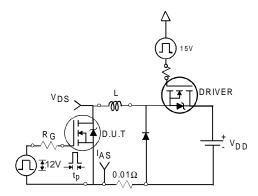


Fig 29a. Unclamped Inductive Test Circuit

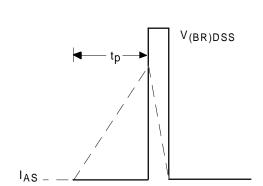


Fig 29b. Unclamped Inductive Waveforms

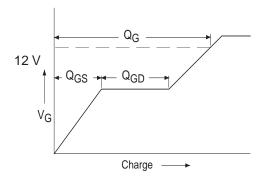
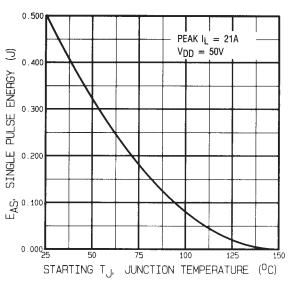


Fig30a. Basic Gate Charge Waveform



**Fig 29c.** Maximum Avalanche Energy Vs. Drain Current

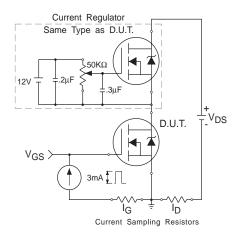


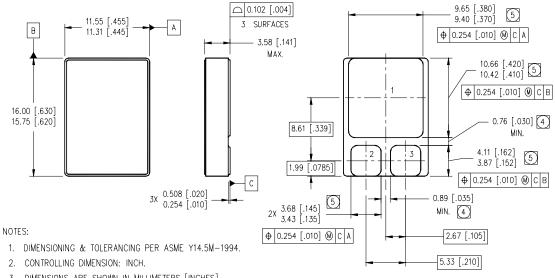
Fig 30b. Gate Charge Test Circuit

#### **Pre-Irradiation**

- ① See Figures 18 through 31 for pre-irradiation curves
- 2 Repetitive Rating; Pulse width limited by maximum junction temperature.
- $^{\circ}$  V<sub>DD</sub> = 25V, Starting T<sub>J</sub> = 25°C, Peak I<sub>L</sub> = 26A,L=1.9mH, R<sub>G</sub>= $25\Omega$
- $\P$  ISD  $\leq$  26A, di/dt  $\leq$  190A/ $\mu$ s,  $V_{DD} \le BV_{DSS}, T_{J} \le 150^{\circ}C$ Suggested RG = $2.35\Omega$
- ⑤ Pulse width  $\leq 300 \mu s$ ; Duty Cycle  $\leq 2\%$

- **© Total Dose Irradiation with VGS Bias.** 12 volt VGS applied and VDS = 0 during irradiation per MIL-STD-750, method 1019, codition A.
- **7** Total Dose Irradiation with V<sub>DS</sub> Bias. V<sub>DS</sub> = 0.8 rated BV<sub>DSS</sub> (pre-radiation) applied and VGS = 0 during irradiation per MIL-STD-750, method 1019, condition A.
- This test is performed using a flash x-ray source operated in the e-beam mode (energy ~2.5 MeV), 30 nsec pulse.
- 9 All Pre-Irradiation and Post-Irradiation test conditions are identical to facilitate direct comparison for circuit applications.

#### Case Outline and Dimensions — SMD-1



- DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
- DIMENSION INCLUDES METALLIZATION FLASH.
  - DIMENSION DOES NOT INCLUDE METALLIZATION FLASH.

#### PAD ASSIGNMENTS

1 = DRAIN

2 = GATE

3 = SOURCE

### International IOR Rectifier

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