

3-in-1 8-bit serial to parallel latch

Features

- Three 8-bit serial input
- Three 8-bit parallel output
- Operation voltage: 2.0V to 5.7V
- Storage register with 3-state outputs
- Shift register with direct clear
- 5 MHz (typical) shift out frequency
- Output capability:
 - ◆ Parallel outputs; bus driver
 - ◆ Serial output; standard

Selection Information

	MA007AH	MA007AP	MA007AD	MA007AF
Package / Dice	Dice	44-PLCC	48-LQFP	44-PQFP
Parallel Output	24 pins			
Sink Current	20mA			

Application Field

Serial-to-parallel data conversion

Remote control holding register

General Description

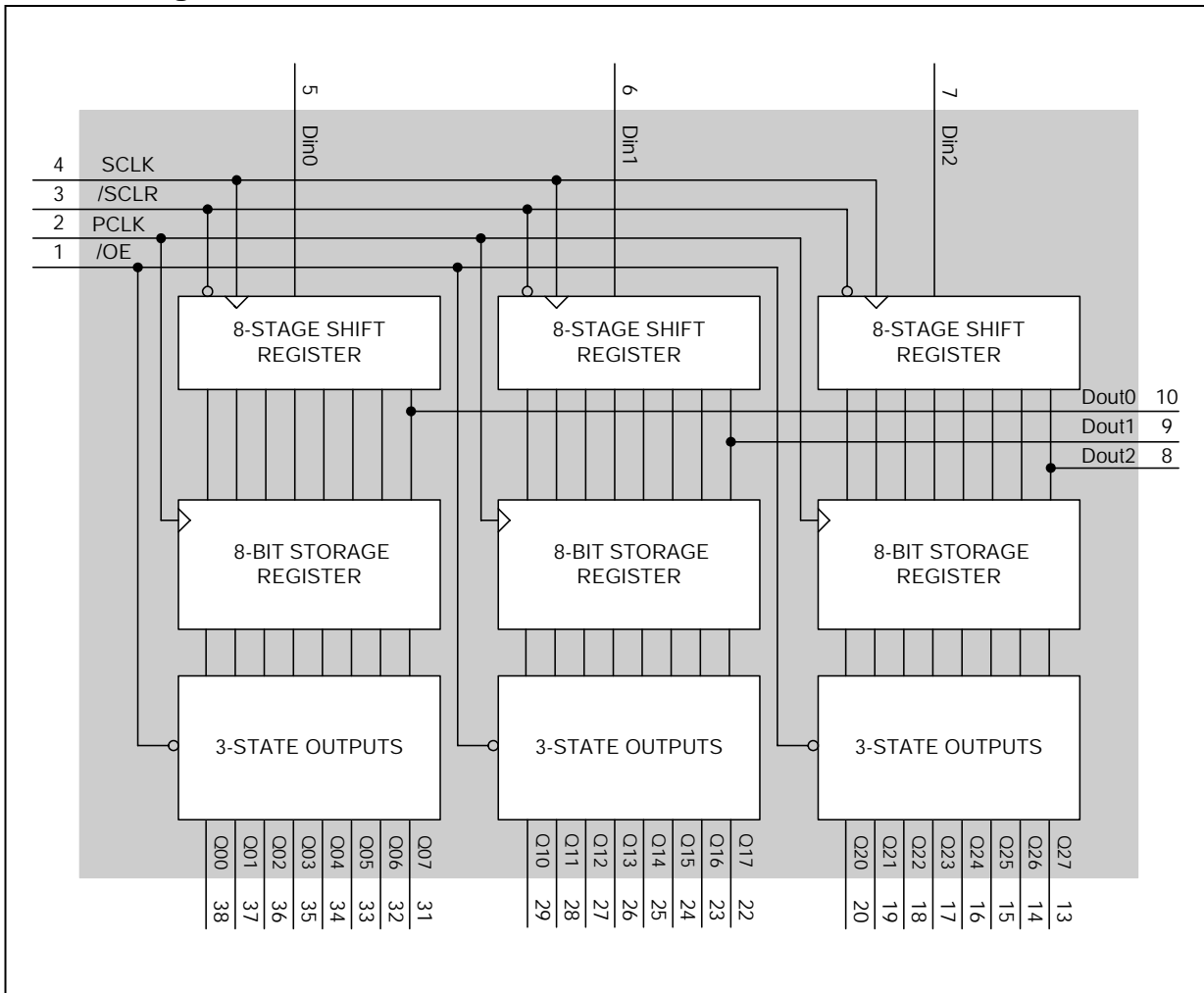
The MA007 are high-speed Si-gate CMOS devices. There are three groups 8-stage serial shift register with a storage register and 3-state outputs in MA007. The shift register and storage register have separate clocks. Data is shifted on the positive-going transitions of the SCLK input. The data in each register is transferred to the storage register on a positive-going transition of the PCLK input. If both clocks are connected

together, the shift register will always be one clock pulse ahead of the storage register. The shift register has a serial input (DIN_x) and a serial standard output (DOUT_x) for cascading. It is also provided with asynchronous reset (active LOW) for all 8 stages shift register. The storage register has 8 parallel 3-state bus driver outputs. Data in the storage register appears at the output whenever the output enable input (/OE) is LOW.

Pad Description

Pad No.	Pad Name	I/O	Description
1	/OE	I	Output enable (active LOW)
2	PCLK	I	Parallel register clock input
3	/SCLR	I	Serial register reset (active LOW)
4	SCLK	I	Shift register clock input
5, 6, 7	DIN0, DIN1, DIN2	I	Serial data input
10, 9, 8	DOUT0, DOUT1, DOUT2	O	Serial data output
20 to 13	Q20 to Q27	O	Parallel data group 2 output
29 to 22	Q10 to Q17	O	Parallel data group 1 output
38 to 31	Q00 to Q07	O	Parallel data group 0 output
12, 30, 40	VCC	P	Positive supply voltage
11, 21, 39, 41	GND	P	Power ground (0 V)

Block Diagram



Function Description

FUNCTION TABLE

INPUTS					OUTPUTS		FUNCTION
SCLK	PCLK	/OE	/SCLR	DINx	DOUTx	QxN	
X	X	L	L	X	L	NC	A LOW level on /SCLR only affects the shift registers
X	↑	L	L	X	L	L	Empty shift register loaded into storage register
X	X	H	L	X	L	Z	Shift register clear. Parallel outputs in high-impedance OFF-state
↑	X	L	H	H	Qx6'	NC	Logic high level shifted into shift register stage 0. Contents of all shift register stages shifted through, e.g. previous state of stage 6 (internal Qx6') appears on the serial output (DOUTx)
X	↑	L	H	X	NC	Qxn'	Contents of shift register stages (internal Qxn') are transferred to the storage register and parallel output stages
↑	↑	L	H	X	Qx6'	Qxn'	Contents of shift register shifted through. Previous contents of the shift register are transferred to the storage register and the parallel output stages.

Notes

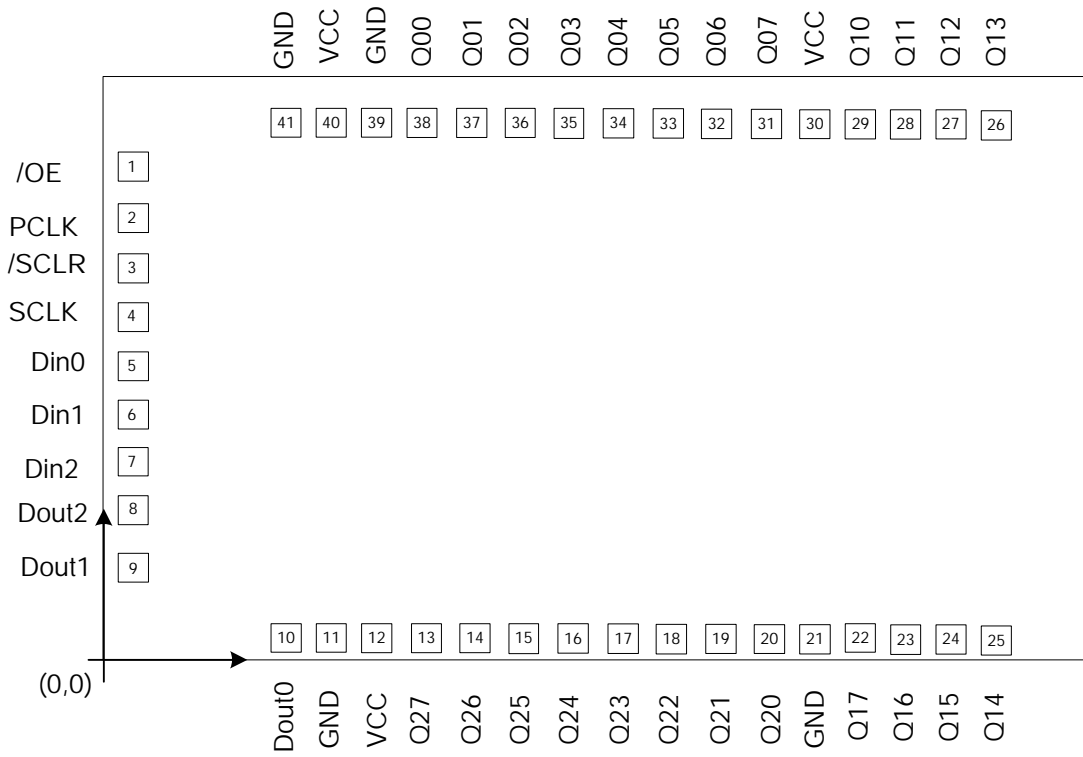
H = HIGH voltage level; L = LOW voltage level

↑ = LOW-to-HIGH transition; ↓ = HIGH-to-LOW

Z = high-impedance OFF-state; NC = no change

X = don't care.

Pad Assignment



Absolute Maximum Rating

PARAMETER	RATING	UNIT
Supply Voltage to Ground Potential	-0.3 to +6.0	V
Applied Input / Output Voltage	-0.3 to +6.0	V
Power Dissipation	500	mW
Ambient Operating Temperature	0 to +70	°C
Storage Temperature	-55 to +150	°C

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

DC Characteristics

(V_{CC}-GND = 5.0V, T_a = 25° C; unless otherwise specified)

PARAMETER	SYM.	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Op. Voltage	V _{CC}	-	2.0	5.0	6.0	V
Op. Current	I _{OP}	No load (Ext.-V)	-	4.0	16.0	μA
Input High Voltage	V _{IH}	-	0.7 V _{DD}	-	V _{DD}	V
Input Low Voltage	V _{IL}	-	0	-	0.3V _{DD}	V
DOUT _x sink current	IOL0	V _{OL} = 0.4V	-	3.0	4.5	mA
DOUT _x drive current	IOH0	V _{OH} = 4.5V	-	1.5	2.5	mA
Q _{x0} to Q _{x7} sink current	IOL1	V _{OL} = 0.4V	-	18	27	mA
		V _{OL} = 0.4V, V _{CC} = 6.0V	-	20	32	mA
Q _{x0} to Q _{x7} drive current	IOH1	V _{OH} = 4.5V	-	2.7	3.5	mA
		V _{OH} = 5.4V, V _{CC} = 6.0V	-	3.0	5.0	mA
All output sink current	IOL2	V _{OL} = 0.4V	-	16	24	mA
All output drive current	IOH2	V _{OH} = 4.5V	-	8	12	mA
Total output sink current	IOL3	V _{OL} = 0.4V	-	384	576	mA
Total output drive current	IOH3	V _{OH} = 4.5V	-	192	288	mA

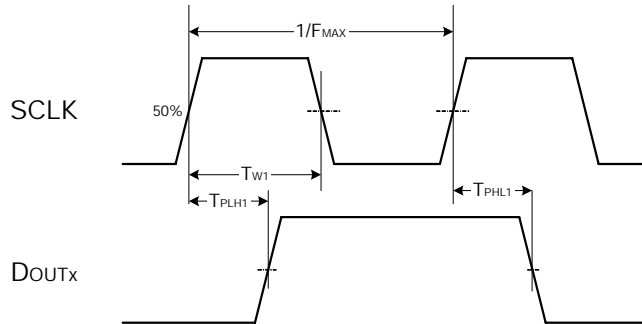
AC Characteristics

(VCC-GND = 5.0V, Ta = 25° C; unless otherwise specified)

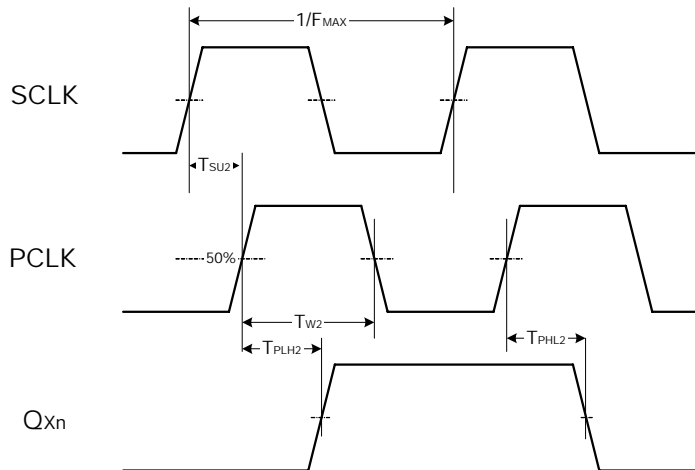
PARAMETER	SYM.	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Maximum clock pulse frequency (SCLK, PCLK)	FMAX	50 % duty cycle	-	2.5	5	MHz
Propagation delay	T _{PHL1} T _{PLH1}	SCLK to DOUT _x , CL = 15 pF	-	95	195	nS
	T _{PHL2} T _{PLH2}	PCLK to QX _n , CL = 15 pF	-	100	200	nS
	T _{PHL3}	/SCLR to DOUT _x , CL = 15 pF	-	100	200	nS
Setup Time	T _{SU1}	Din to SCLK	10	-	-	nS
	T _{SU2}	SCLK to PCLK	100	-	-	nS
	T _{SU3}	SCLK to PCLK	-	5	10	nS
Pulse Width	T _{W1}	SCLK	25	-	-	nS
	T _{W2}	PCLK	25	-	-	nS
	T _{W3}	/SCLR	25	-	-	nS
Tri-state output enable time	T _{PZH} T _{PZL}	/OE to QX _n	-	100	200	nS
Tri-state output disable time	T _{PHZ} T _{PLZ}	/OE to QX _n	-	100	200	nS
Hold time	T _H	Din to SCLK	5	-	-	nS
Removal time	T _{REM}	/SCLR to SCLK	10	-	-	nS

System Timing

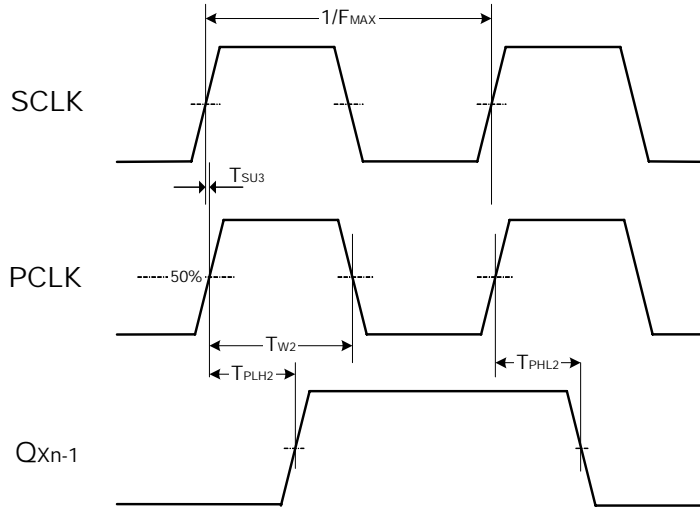
SCLK to DOUTx Propagation Delay Waveforms



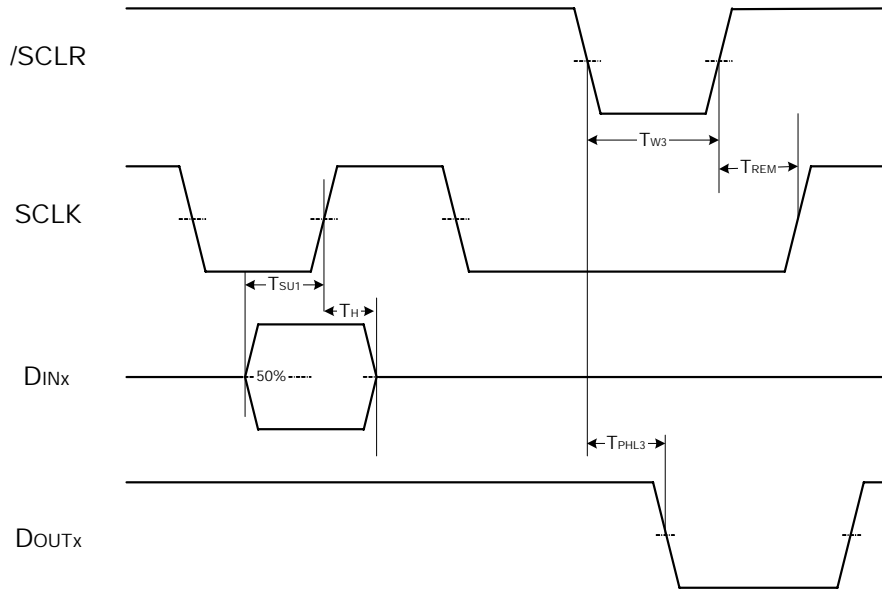
PCLK to QXn Propagation Delay and Setup Time Waveforms



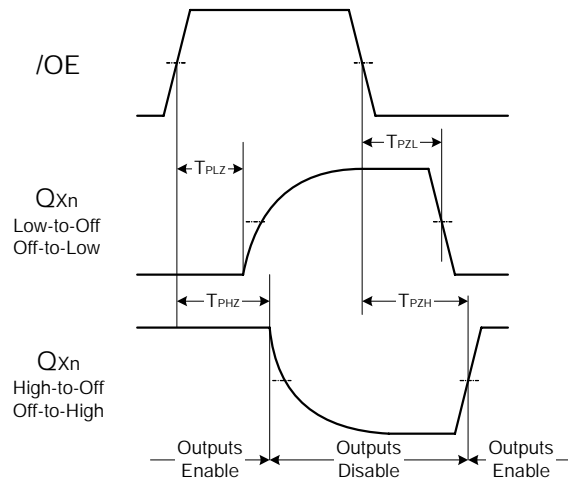
SCLK and PCLK are connected together to Q_{Xn-1} Propagation Delay and Setup Time Waveforms



PCLK to Q_{Xn} Propagation Delay and Setup Time Waveforms

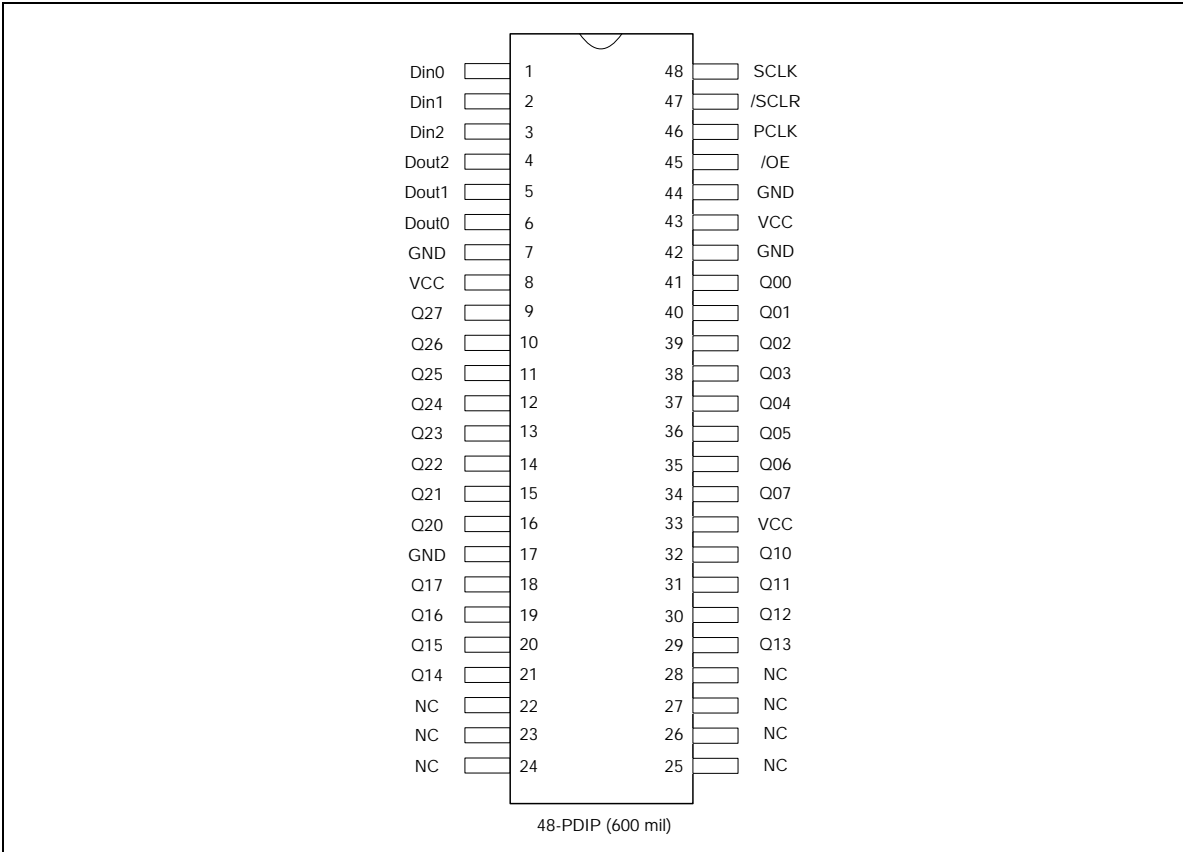


Tri-state Enable/Disable Time Waveforms

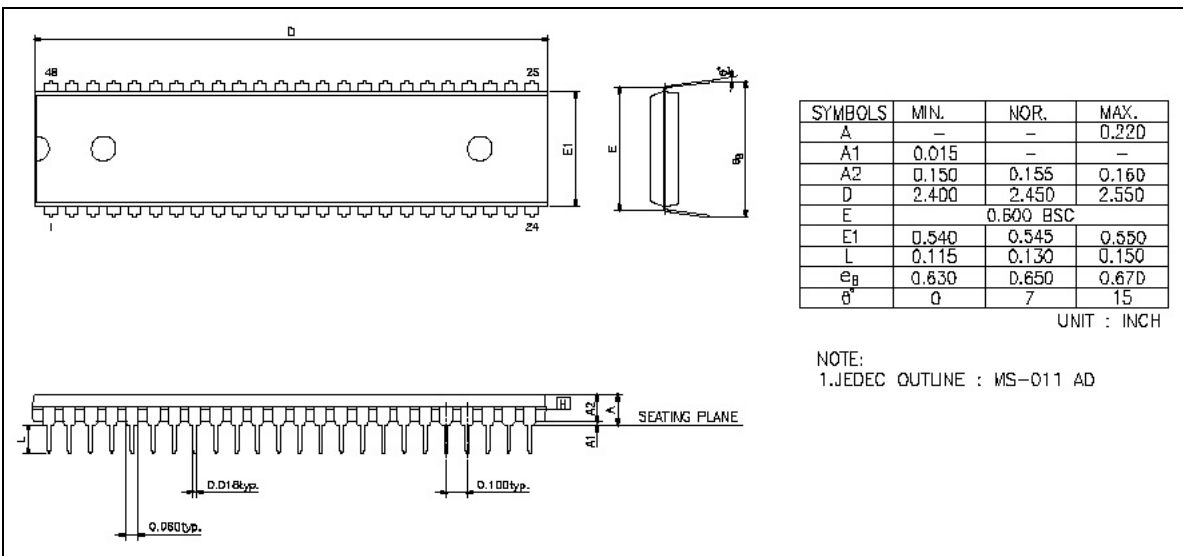


Package Information

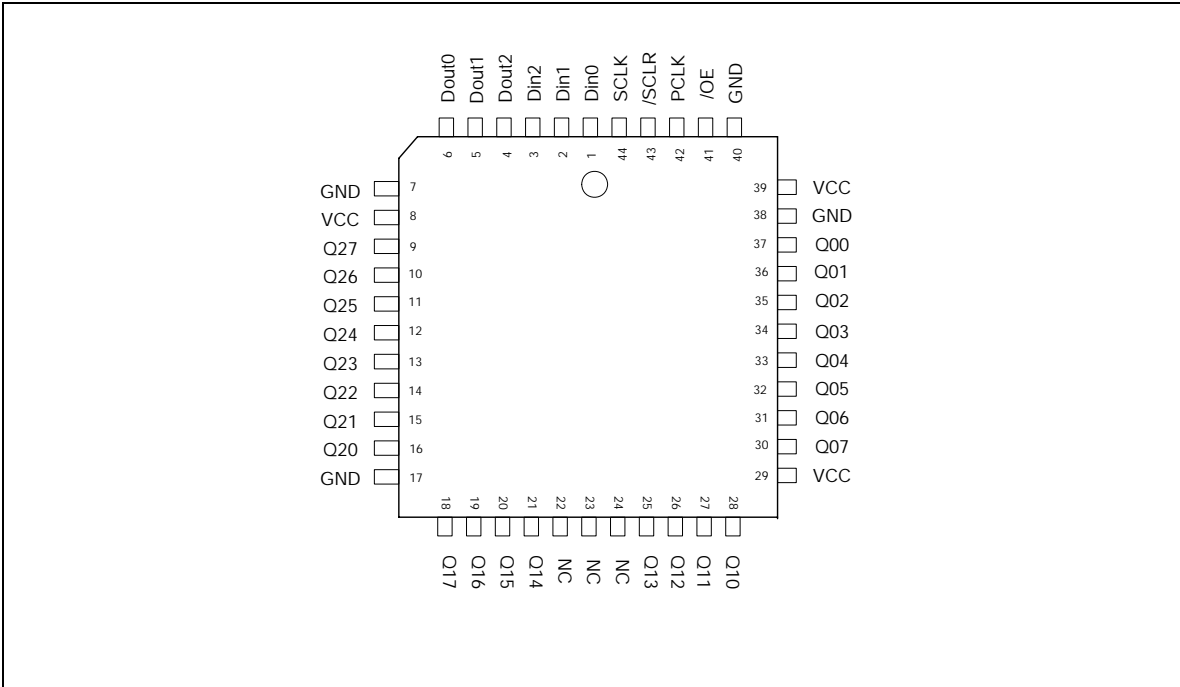
MA007AE 48 Pin PDIP (600mil) Configuration



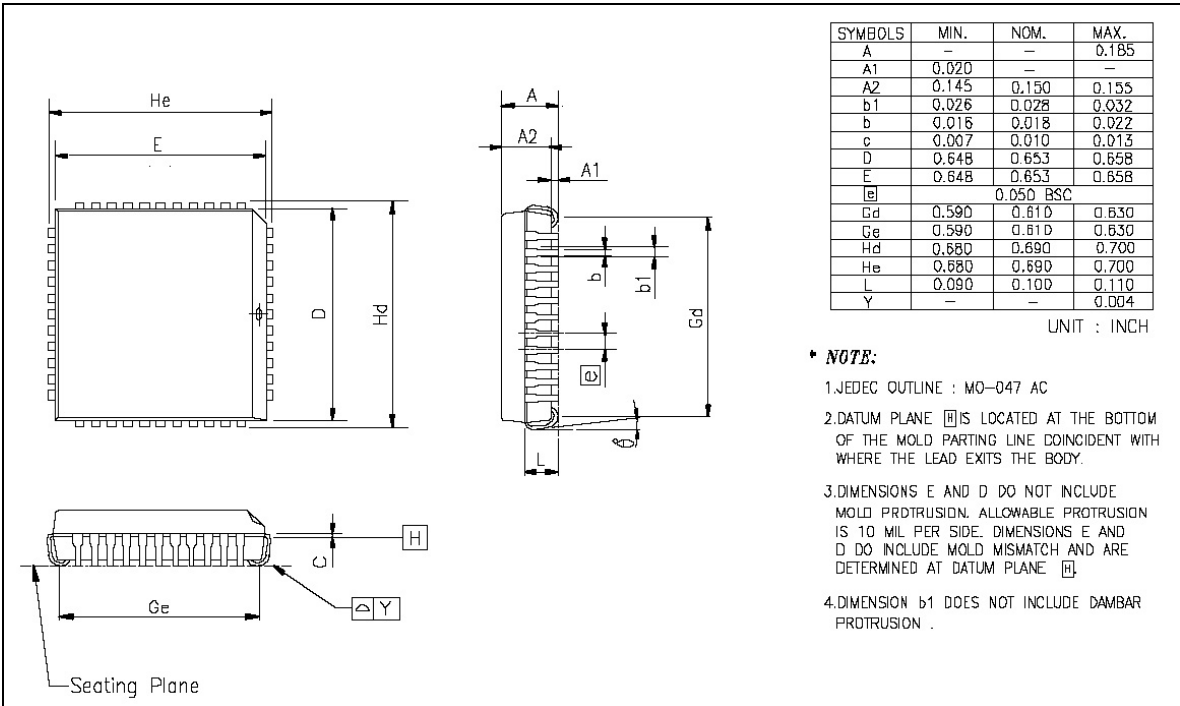
48 Pin PDIP Package Dimension



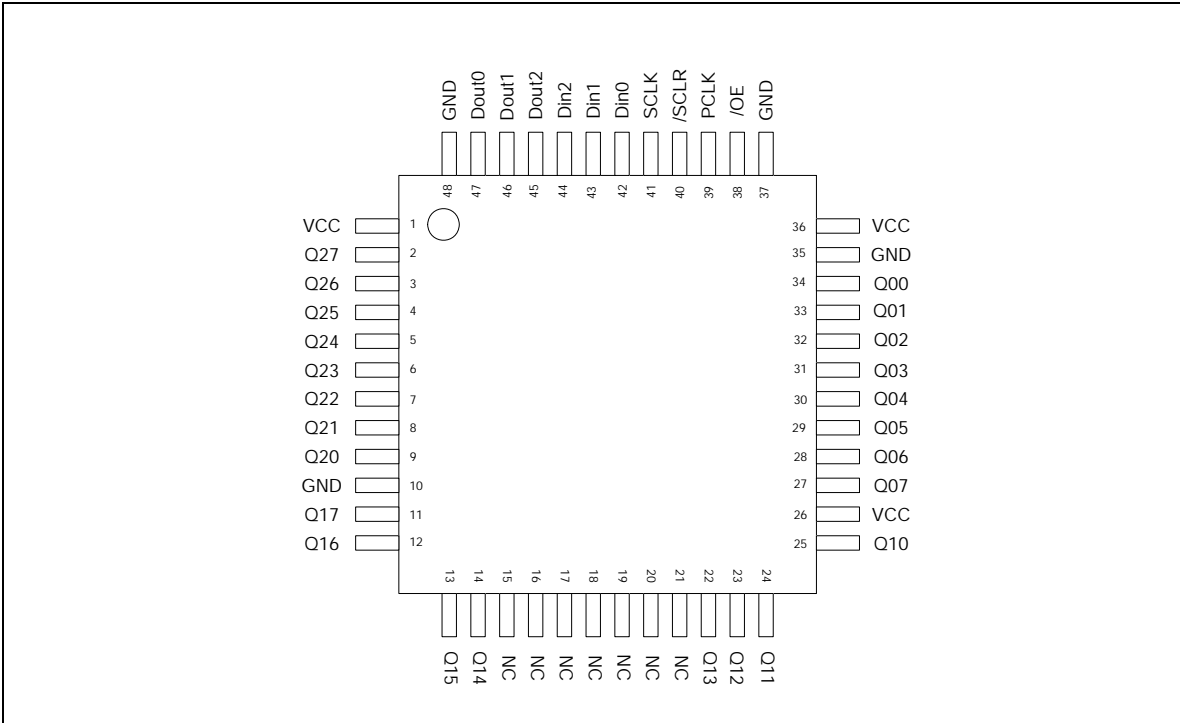
MA007AP 44 Pin PLCC Configuration



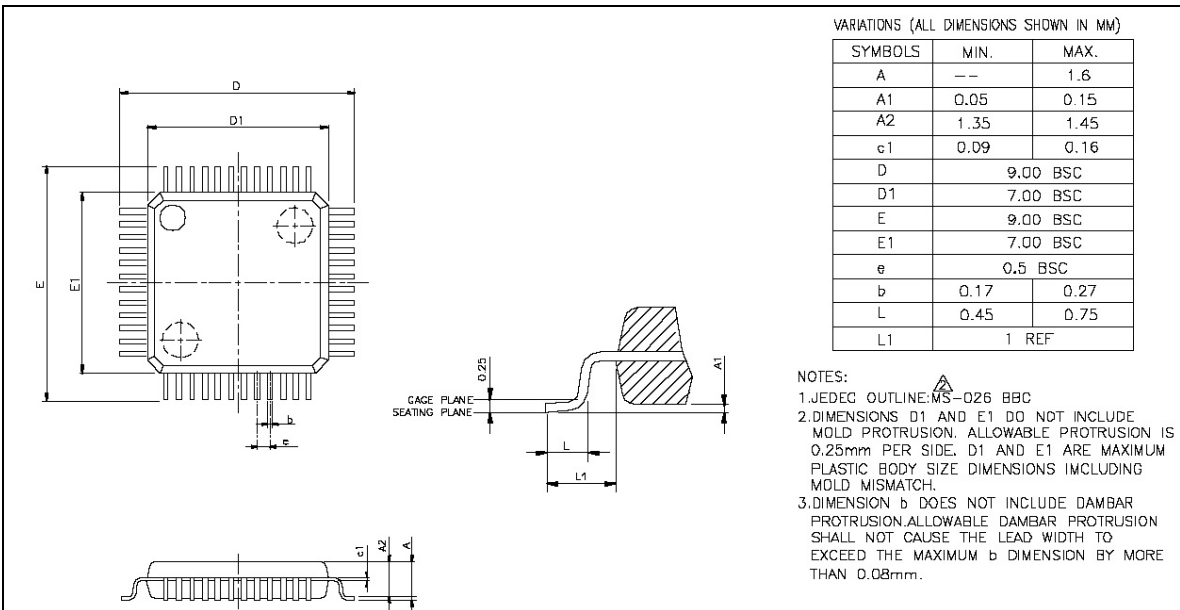
44 Pin PLCC Package Dimension



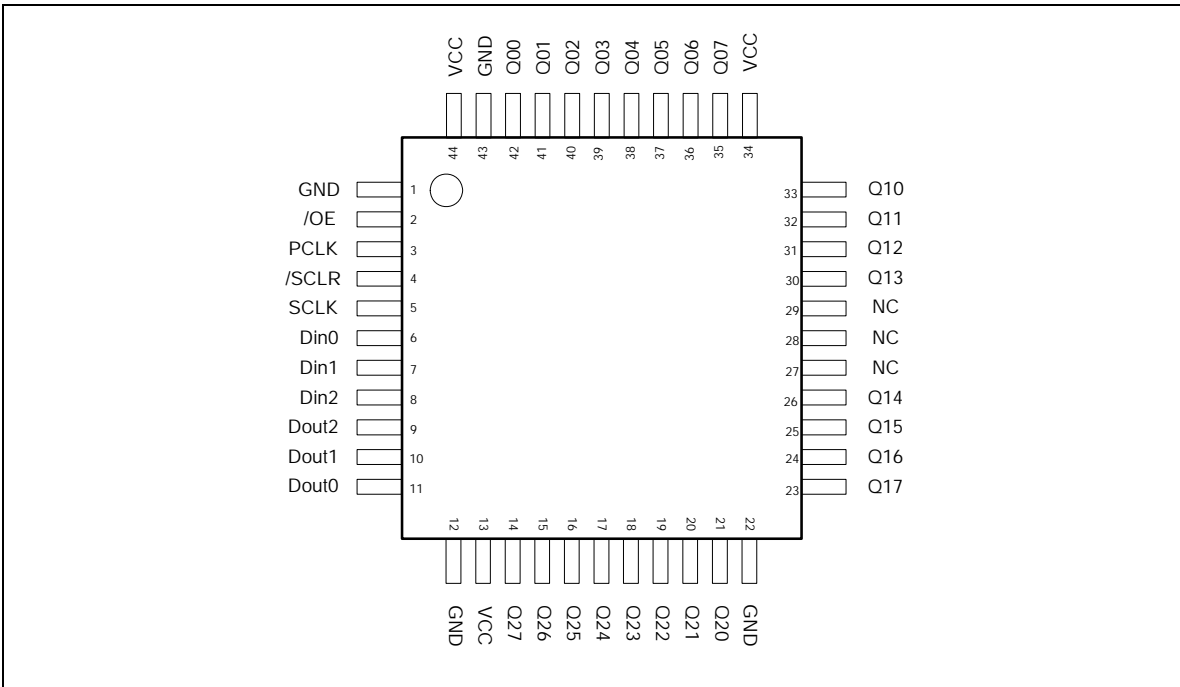
MA007AD 48 Pin LQFP Configuration



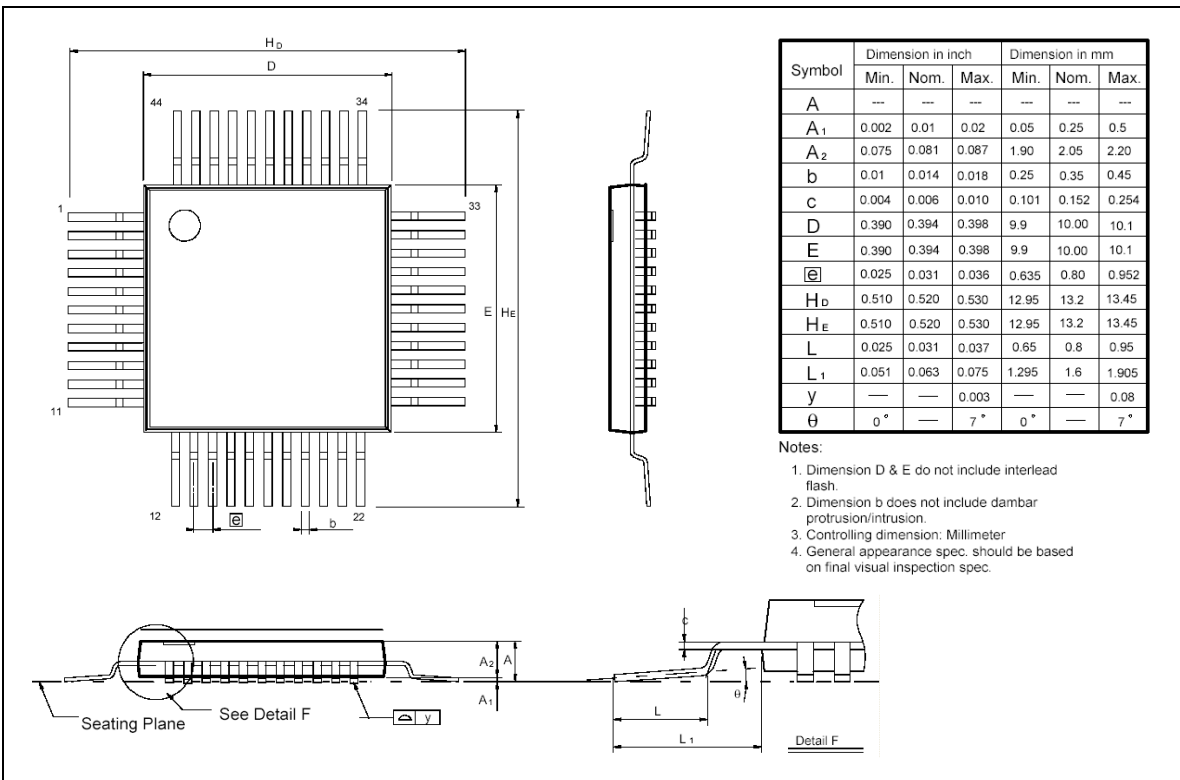
48 Pin LQFP Package Dimension



MA007AF 44 Pin PQFP Configuration



44 Pin PQFP Package Dimension



Notes:

Vision History

VERSION	DATE	PAGE	DESCRIPTION
A1	Nov. 2005		Initial issue.