

## K10P144M120SF3

### K10 Sub-Family Data Sheet

Supports the following:

MK10FX512VLQ12,  
MK10FN1M0VLQ12,  
MK10FX512VMD12,  
MK10FN1M0VMD12

#### Features

- Operating Characteristics
  - Voltage range: 1.71 to 3.6 V
  - Flash write voltage range: 1.71 to 3.6 V
  - Temperature range (ambient): -40 to 105°C
- Performance
  - Up to 120 MHz ARM Cortex-M4 core with DSP instructions delivering 1.25 Dhrystone MIPS per MHz
- Memories and memory interfaces
  - Up to 1024 KB program flash memory on non-FlexMemory devices
  - Up to 512 KB program flash memory on FlexMemory devices
  - Up to 512 KB FlexNVM on FlexMemory devices
  - 16 KB FlexRAM on FlexMemory devices
  - Up to 128 KB RAM
  - Serial programming interface (EzPort)
  - FlexBus external bus interface
  - NAND flash controller interface
- Clocks
  - 3 to 32 MHz crystal oscillator
  - 32 kHz crystal oscillator
  - Multi-purpose clock generator
- System peripherals
  - 10 low-power modes to provide power optimization based on application requirements
  - Memory protection unit with multi-master protection
  - 32-channel DMA controller, supporting up to 128 request sources
  - External watchdog monitor
  - Software watchdog
  - Low-leakage wakeup unit
- Security and integrity modules
  - Hardware CRC module to support fast cyclic redundancy checks
  - 128-bit unique identification (ID) number per chip
- Human-machine interface
  - Low-power hardware touch sensor interface (TSI)
  - General-purpose input/output
- Analog modules
  - Four 16-bit SAR ADCs
  - Programmable gain amplifier (PGA) (up to x64) integrated into each ADC
  - Two 12-bit DACs
  - Four analog comparators (CMP) containing a 6-bit DAC and programmable reference input
  - Voltage reference
- Timers
  - Programmable delay block
  - Two 8-channel motor control/general purpose/PWM timers
  - Two 2-channel quadrature decoder/general purpose timers
  - Periodic interrupt timers
  - 16-bit low-power timer
  - Carrier modulator transmitter
  - Real-time clock
- Communication interfaces
  - Two Controller Area Network (CAN) modules
  - Three SPI modules
  - Two I2C modules
  - Six UART modules
  - Secure Digital host controller (SDHC)
  - Two I2S modules

This document contains information on a new product. Specifications and information herein are subject to change without notice.

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# 1 Ordering parts

## 1.1 Determining valid orderable parts

Valid orderable part numbers are provided on the web. To determine the orderable part numbers for this device, go to <http://www.freescale.com> and perform a part number search for the following device numbers: PK10 and MK10.

## 2 Part identification

### 2.1 Description

Part numbers for the chip have fields that identify the specific part. You can use the values of these fields to determine the specific part you have received.

### 2.2 Format

Part numbers for this device have the following format:

Q K## A M FFF T PP CC N

### 2.3 Fields

This table lists the possible values for each field in the part number (not all combinations are valid):

Field	Description	Values
Q	Qualification status	<ul style="list-style-type: none"> <li>M = Fully qualified, general market flow</li> <li>P = Prequalification</li> </ul>
K##	Kinetis family	<ul style="list-style-type: none"> <li>K10</li> </ul>
A	Key attribute	<ul style="list-style-type: none"> <li>D = Cortex-M4 w/ DSP</li> <li>F = Cortex-M4 w/ DSP and FPU</li> </ul>
M	Flash memory type	<ul style="list-style-type: none"> <li>N = Program flash only</li> <li>X = Program flash and FlexMemory</li> </ul>

*Table continues on the next page...*

## Terminology and guidelines

Field	Description	Values
FFF	Program flash memory size	<ul style="list-style-type: none"><li>• 32 = 32 KB</li><li>• 64 = 64 KB</li><li>• 128 = 128 KB</li><li>• 256 = 256 KB</li><li>• 512 = 512 KB</li><li>• 1M0 = 1 MB</li></ul>
T	Temperature range (°C)	<ul style="list-style-type: none"><li>• V = -40 to 105</li><li>• C = -40 to 85</li></ul>
PP	Package identifier	<ul style="list-style-type: none"><li>• LQ = 144 LQFP (20 mm x 20 mm)</li><li>• MD = 144 MAPBGA (13 mm x 13 mm)</li></ul>
CC	Maximum CPU frequency (MHz)	<ul style="list-style-type: none"><li>• 12 = 120 MHz</li></ul>
N	Packaging type	<ul style="list-style-type: none"><li>• R = Tape and reel</li><li>• (Blank) = Trays</li></ul>

## 2.4 Example

This is an example part number:

MK10FN1M0VLQ12

## 3 Terminology and guidelines

### 3.1 Definition: Operating requirement

An *operating requirement* is a specified value or range of values for a technical characteristic that you must guarantee during operation to avoid incorrect operation and possibly decreasing the useful life of the chip.

#### 3.1.1 Example

This is an example of an operating requirement, which you must meet for the accompanying operating behaviors to be guaranteed:

Symbol	Description	Min.	Max.	Unit
V <sub>DD</sub>	1.0 V core supply voltage	0.9	1.1	V

## 3.2 Definition: Operating behavior

An *operating behavior* is a specified value or range of values for a technical characteristic that are guaranteed during operation if you meet the operating requirements and any other specified conditions.

### 3.2.1 Example

This is an example of an operating behavior, which is guaranteed if you meet the accompanying operating requirements:

Symbol	Description	Min.	Max.	Unit
I <sub>WP</sub>	Digital I/O weak pullup/ pulldown current	10	130	μA

## 3.3 Definition: Attribute

An *attribute* is a specified value or range of values for a technical characteristic that are guaranteed, regardless of whether you meet the operating requirements.

### 3.3.1 Example

This is an example of an attribute:

Symbol	Description	Min.	Max.	Unit
CIN_D	Input capacitance: digital pins	—	7	pF

## 3.4 Definition: Rating

A *rating* is a minimum or maximum value of a technical characteristic that, if exceeded, may cause permanent chip failure:

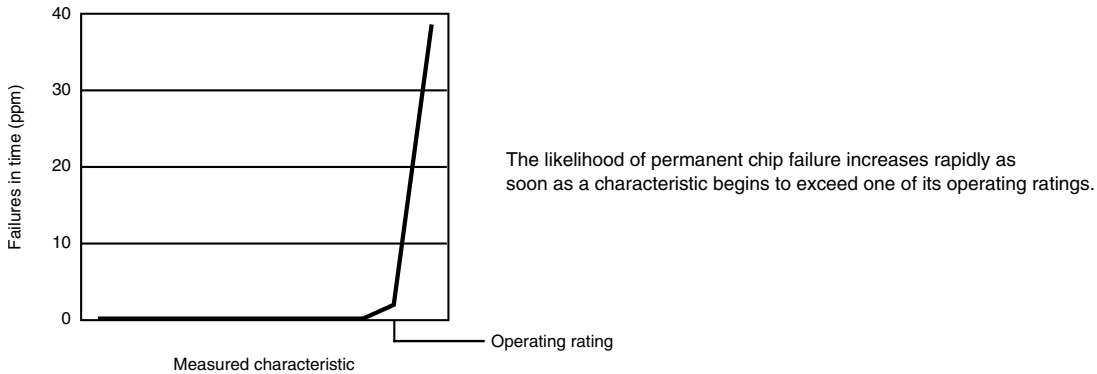
- *Operating ratings* apply during operation of the chip.
- *Handling ratings* apply when the chip is not powered.

### 3.4.1 Example

This is an example of an operating rating:

Symbol	Description	Min.	Max.	Unit
V <sub>DD</sub>	1.0 V core supply voltage	-0.3	1.2	V

### 3.5 Result of exceeding a rating



### 3.6 Relationship between ratings and operating requirements

<b>Fatal range</b> - Probable permanent failure	<b>Limited operating range</b> - No permanent failure - Possible decreased life - Possible incorrect operation	<b>Normal operating range</b> - No permanent failure - Correct operation	<b>Limited operating range</b> - No permanent failure - Possible decreased life - Possible incorrect operation	<b>Fatal range</b> - Probable permanent failure
<b>Handling range</b> - No permanent failure				

*Operating or handling rating (min.)*      *Operating requirement (min.)*      *Operating requirement (max.)*      *Operating or handling rating (max.)*

### 3.7 Guidelines for ratings and operating requirements

Follow these guidelines for ratings and operating requirements:

- Never exceed any of the chip’s ratings.

- During normal operation, don't exceed any of the chip's operating requirements.
- If you must exceed an operating requirement at times other than during normal operation (for example, during power sequencing), limit the duration as much as possible.

### 3.8 Definition: Typical value

A *typical value* is a specified value for a technical characteristic that:

- Lies within the range of values specified by the operating behavior
- Given the typical manufacturing process, is representative of that characteristic during operation when you meet the typical-value conditions or other specified conditions

Typical values are provided as design guidelines and are neither tested nor guaranteed.

#### 3.8.1 Example 1

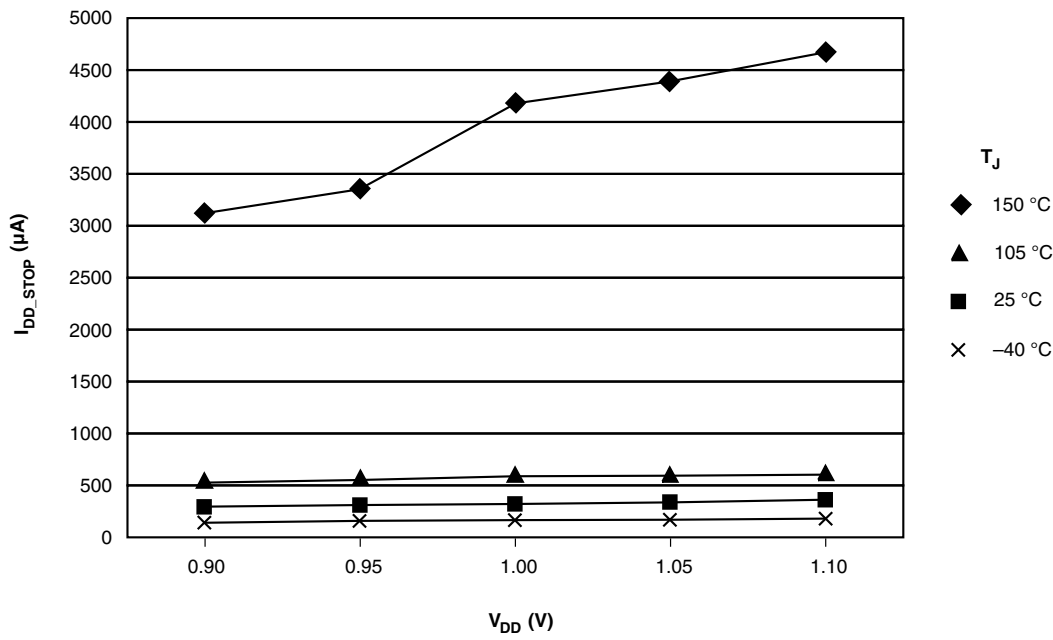
This is an example of an operating behavior that includes a typical value:

Symbol	Description	Min.	Typ.	Max.	Unit
$I_{WP}$	Digital I/O weak pullup/pulldown current	10	70	130	$\mu A$

#### 3.8.2 Example 2

This is an example of a chart that shows typical values for various voltage and temperature conditions:

## Ratings



## 3.9 Typical value conditions

Typical values assume you meet the following conditions (or other conditions as specified):

Symbol	Description	Value	Unit
T <sub>A</sub>	Ambient temperature	25	°C
V <sub>DD</sub>	3.3 V supply voltage	3.3	V

## 4 Ratings

### 4.1 Thermal handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
T <sub>STG</sub>	Storage temperature	-55	150	°C	1
T <sub>SDR</sub>	Solder temperature, lead-free	—	260	°C	2

1. Determined according to JEDEC Standard JESD22-A103, *High Temperature Storage Life*.
2. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.



## 4.2 Moisture handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
MSL	Moisture sensitivity level	—	3	—	1

1. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

## 4.3 ESD handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
$V_{HBM}$	Electrostatic discharge voltage, human body model	-2000	+2000	V	1
$V_{CDM}$	Electrostatic discharge voltage, charged-device model	-500	+500	V	2
$I_{LAT}$	Latch-up current at ambient temperature of 105°C	-100	+100	mA	

1. Determined according to JEDEC Standard JESD22-A114, *Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)*.
2. Determined according to JEDEC Standard JESD22-C101, *Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components*.

## 4.4 Voltage and current operating ratings

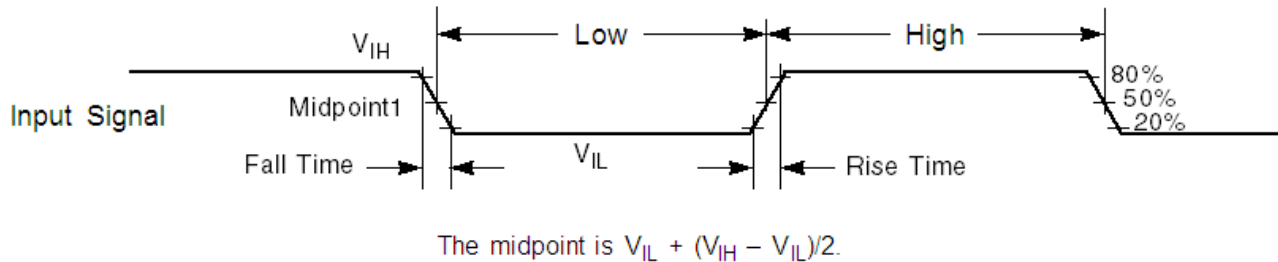
Symbol	Description	Min.	Max.	Unit
$V_{DD}$	Digital supply voltage <sup>1</sup>	-0.3	3.8	V
$I_{DD}$	Digital supply current	—	300	mA
$V_{DIO}$	Digital input voltage (except $\overline{RESET}$ , EXTAL0/XTAL0, and EXTAL1/XTAL1) <sup>2</sup>	-0.3	5.5	V
$V_{AIO}$	Analog <sup>3</sup> , $\overline{RESET}$ , EXTAL0/XTAL0, and EXTAL1/XTAL1 input voltage	-0.3	$V_{DD} + 0.3$	V
$I_D$	Instantaneous maximum current single pin limit (applies to all digital pins except pins)	-25	25	mA
$V_{DDA}$	Analog supply voltage	$V_{DD} - 0.3$	$V_{DD} + 0.3$	V
$V_{BAT}$	RTC battery supply voltage	-0.3	3.8	V

1. It applies for all port pins.
2. It covers digital pins.
3. Analog pins are defined as pins that do not have an associated general purpose I/O port function.

## 5 General

## 5.1 AC electrical characteristics

Unless otherwise specified, propagation delays are measured from the 50% to the 50% point, and rise and fall times are measured at the 20% and 80% points, as shown in the following figure.



**Figure 1. Input signal measurement reference**

All digital I/O switching characteristics assume:

1. output pins
  - have  $C_L=30\text{pF}$  loads,
  - are configured for fast slew rate ( $\text{PORTx\_PCRn[SRE]}=0$ ), and
  - are configured for high drive strength ( $\text{PORTx\_PCRn[DSE]}=1$ )
2. input pins
  - have their passive filter disabled ( $\text{PORTx\_PCRn[PFE]}=0$ )

## 5.2 Nonswitching electrical specifications

### 5.2.1 Voltage and current operating requirements

**Table 1. Voltage and current operating requirements**

Symbol	Description	Min.	Max.	Unit	Notes
$V_{DD}$	Supply voltage	1.71	3.6	V	
$V_{DDA}$	Analog supply voltage	1.71	3.6	V	
$V_{DD} - V_{DDA}$	$V_{DD}$ -to- $V_{DDA}$ differential voltage	-0.1	0.1	V	
$V_{SS} - V_{SSA}$	$V_{SS}$ -to- $V_{SSA}$ differential voltage	-0.1	0.1	V	
$V_{BAT}$	RTC battery supply voltage	1.71	3.6	V	

Table continues on the next page...

**Table 1. Voltage and current operating requirements (continued)**

Symbol	Description	Min.	Max.	Unit	Notes
V <sub>IH</sub>	Input high voltage (digital pins) <ul style="list-style-type: none"> <li>• 2.7 V ≤ V<sub>DD</sub> ≤ 3.6 V</li> <li>• 1.7 V ≤ V<sub>DD</sub> ≤ 2.7 V</li> </ul>	0.7 × V <sub>DD</sub>	—	V	
		0.75 × V <sub>DD</sub>	—	V	
V <sub>IL</sub>	Input low voltage (digital pins) <ul style="list-style-type: none"> <li>• 2.7 V ≤ V<sub>DD</sub> ≤ 3.6 V</li> <li>• 1.7 V ≤ V<sub>DD</sub> ≤ 2.7 V</li> </ul>	—	0.35 × V <sub>DD</sub>	V	
		—	0.3 × V <sub>DD</sub>	V	
V <sub>HYS</sub>	Input hysteresis (digital pins)	0.06 × V <sub>DD</sub>	—	V	
I <sub>ICDIO</sub>	Digital pin negative DC injection current — single pin <ul style="list-style-type: none"> <li>• V<sub>IN</sub> &lt; V<sub>SS</sub>-0.3V</li> </ul>	-5	—	mA	1
I <sub>ICAIO</sub>	Analog <sup>2</sup> , EXTAL0/XTAL0, and EXTAL1/XTAL1 pin DC injection current — single pin <ul style="list-style-type: none"> <li>• V<sub>IN</sub> &lt; V<sub>SS</sub>-0.3V (Negative current injection)</li> <li>• V<sub>IN</sub> &gt; V<sub>DD</sub>+0.3V (Positive current injection)</li> </ul>	-5 —	— +5	mA	3
I <sub>ICcont</sub>	Contiguous pin DC injection current — regional limit, includes sum of negative injection currents or sum of positive injection currents of 16 contiguous pins <ul style="list-style-type: none"> <li>• Negative current injection</li> <li>• Positive current injection</li> </ul>	-25 —	— +25	mA	
V <sub>RAM</sub>	V <sub>DD</sub> voltage required to retain RAM	1.2	—	V	
V <sub>RFVBAT</sub>	V <sub>BAT</sub> voltage required to retain the VBAT register file	V <sub>POR_VBAT</sub>	—	V	

1. All 5 V tolerant digital I/O pins are internally clamped to V<sub>SS</sub> through a ESD protection diode. There is no diode connection to V<sub>DD</sub>. If V<sub>IN</sub> greater than V<sub>DIO\_MIN</sub> (=V<sub>SS</sub>-0.3V) is observed, then there is no need to provide current limiting resistors at the pads. If this limit cannot be observed then a current limiting resistor is required. The negative DC injection current limiting resistor is calculated as  $R=(V_{DIO\_MIN}-V_{IN})/|I_{IC}|$ .
2. Analog pins are defined as pins that do not have an associated general purpose I/O port function.
3. All analog pins are internally clamped to V<sub>SS</sub> and V<sub>DD</sub> through ESD protection diodes. If V<sub>IN</sub> is greater than V<sub>AIO\_MIN</sub> (=V<sub>SS</sub>-0.3V) and V<sub>IN</sub> is less than V<sub>AIO\_MAX</sub>(=V<sub>DD</sub>+0.3V) is observed, then there is no need to provide current limiting resistors at the pads. If these limits cannot be observed then a current limiting resistor is required. The negative DC injection current limiting resistor is calculated as  $R=(V_{AIO\_MIN}-V_{IN})/|I_{IC}|$ . The positive injection current limiting resistor is calculated as  $R=(V_{IN}-V_{AIO\_MAX})/|I_{IC}|$ . Select the larger of these two calculated resistances.

## 5.2.2 LVD and POR operating requirements

**Table 2. LVD and POR operating requirements**

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V <sub>POR</sub>	Falling VDD POR detect voltage	0.8	1.1	1.5	V	

Table continues on the next page...

**Table 2. LVD and POR operating requirements (continued)**

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V <sub>LVDH</sub>	Falling low-voltage detect threshold — high range (LVDV=01)	2.48	2.56	2.64	V	
V <sub>LVW1H</sub>	Low-voltage warning thresholds — high range <ul style="list-style-type: none"> <li>• Level 1 falling (LVWV=00)</li> <li>• Level 2 falling (LVWV=01)</li> <li>• Level 3 falling (LVWV=10)</li> <li>• Level 4 falling (LVWV=11)</li> </ul>	2.62	2.70	2.78	V	1
V <sub>LVW2H</sub>		2.72	2.80	2.88	V	
V <sub>LVW3H</sub>		2.82	2.90	2.98	V	
V <sub>LVW4H</sub>		2.92	3.00	3.08	V	
V <sub>HYSH</sub>	Low-voltage inhibit reset/recover hysteresis — high range	—	±80	—	mV	
V <sub>LVDL</sub>	Falling low-voltage detect threshold — low range (LVDV=00)	1.54	1.60	1.66	V	
V <sub>LVW1L</sub>	Low-voltage warning thresholds — low range <ul style="list-style-type: none"> <li>• Level 1 falling (LVWV=00)</li> <li>• Level 2 falling (LVWV=01)</li> <li>• Level 3 falling (LVWV=10)</li> <li>• Level 4 falling (LVWV=11)</li> </ul>	1.74	1.80	1.86	V	1
V <sub>LVW2L</sub>		1.84	1.90	1.96	V	
V <sub>LVW3L</sub>		1.94	2.00	2.06	V	
V <sub>LVW4L</sub>		2.04	2.10	2.16	V	
V <sub>HYSL</sub>	Low-voltage inhibit reset/recover hysteresis — low range	—	±60	—	mV	
V <sub>BG</sub>	Bandgap voltage reference	0.97	1.00	1.03	V	
t <sub>LPO</sub>	Internal low power oscillator period factory trimmed	900	1000	1100	μs	

1. Rising thresholds are falling threshold + hysteresis voltage

**Table 3. VBAT power operating requirements**

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V <sub>POR_VBAT</sub>	Falling VBAT supply POR detect voltage	0.8	1.1	1.5	V	

## 5.2.3 Voltage and current operating behaviors

**Table 4. Voltage and current operating behaviors**

Symbol	Description	Min.	Max.	Unit	Notes
V <sub>OH</sub>	Output high voltage — high drive strength <ul style="list-style-type: none"> <li>• 2.7 V ≤ V<sub>DD</sub> ≤ 3.6 V, I<sub>OH</sub> = -9mA</li> <li>• 1.71 V ≤ V<sub>DD</sub> ≤ 2.7 V, I<sub>OH</sub> = -3mA</li> </ul>	V <sub>DD</sub> - 0.5	—	V	
	Output high voltage — low drive strength <ul style="list-style-type: none"> <li>• 2.7 V ≤ V<sub>DD</sub> ≤ 3.6 V, I<sub>OH</sub> = -2mA</li> <li>• 1.71 V ≤ V<sub>DD</sub> ≤ 2.7 V, I<sub>OH</sub> = -0.6mA</li> </ul>	V <sub>DD</sub> - 0.5	—	V	
I <sub>OHT</sub>	Output high current total for all ports	—	100	mA	
I <sub>OHT_io60</sub>	Output high current total for fast digital ports	—	100	mA	
V <sub>OL</sub>	Output low voltage — high drive strength <ul style="list-style-type: none"> <li>• 2.7 V ≤ V<sub>DD</sub> ≤ 3.6 V, I<sub>OL</sub> = 9mA</li> <li>• 1.71 V ≤ V<sub>DD</sub> ≤ 2.7 V, I<sub>OL</sub> = 3mA</li> </ul>	—	0.5	V	
	Output low voltage — low drive strength <ul style="list-style-type: none"> <li>• 2.7 V ≤ V<sub>DD</sub> ≤ 3.6 V, I<sub>OL</sub> = 2mA</li> <li>• 1.71 V ≤ V<sub>DD</sub> ≤ 2.7 V, I<sub>OL</sub> = 0.6mA</li> </ul>	—	0.5	V	
I <sub>OLT</sub>	Output low current total for all ports	—	TBD	mA	
I <sub>OLT_io60</sub>	Output low current total for fast digital ports	—	TBD	mA	
I <sub>IN</sub>	Input leakage current (per pin) for full temperature range	—	1	μA	1
I <sub>IN</sub>	Input leakage current (per pin) at 25°C	—	0.025	μA	1
I <sub>OZ</sub>	Hi-Z (off-state) leakage current (per pin)	—	1	μA	
R <sub>PU</sub>	Internal pullup resistors	20	50	kΩ	2
R <sub>PD</sub>	Internal pulldown resistors	20	50	kΩ	3

1. Measured at V<sub>DD</sub>=3.6V

2. Measured at V<sub>DD</sub> supply voltage = V<sub>DD</sub> min and V<sub>input</sub> = V<sub>SS</sub>

3. Measured at V<sub>DD</sub> supply voltage = V<sub>DD</sub> min and V<sub>input</sub> = V<sub>DD</sub>

## 5.2.4 Power mode transition operating behaviors

All specifications except t<sub>POR</sub>, and V<sub>L</sub>L<sub>S</sub>x→RUN recovery times in the following table assume this clock configuration:

- CPU and system clocks = FEI 100 MHz
- Bus clock = 50 MHz

## General

- FlexBus clock = 50 MHz
- Flash clock = 25 MHz

**Table 5. Power mode transition operating behaviors**

Symbol	Description	Min.	Max.	Unit	Notes
$t_{POR}$	After a POR event, amount of time from the point $V_{DD}$ reaches 1.71 V to execution of the first instruction across the operating temperature range of the chip.	—	300	$\mu s$	1
	• VLLS1 → RUN	—	126	$\mu s$	
	• VLLS2 → RUN	—	82	$\mu s$	
	• VLLS3 → RUN	—	82	$\mu s$	
	• LLS → RUN	—	5.0	$\mu s$	
	• VLPS → RUN	—	TBD	$\mu s$	
	• STOP → RUN	—	TBD	$\mu s$	

1. Normal boot (FTFE\_FOFT[LPBOOT]=1)

## 5.2.5 Power consumption operating behaviors

**Table 6. Power consumption operating behaviors**

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
$I_{DDA}$	Analog supply current	—	—	See note	mA	1
$I_{DD\_RUN}$	Run mode current — all peripheral clocks disabled, code executing from flash	—	65	TBD	mA	2
	• @ 1.8V	—	65	TBD	mA	
	• @ 3.0V					
$I_{DD\_RUN}$	Run mode current — all peripheral clocks enabled, code executing from flash	—	95	TBD	mA	3
	• @ 1.8V	—	95	TBD	mA	
	• @ 3.0V					
$I_{DD\_WAIT}$	Wait mode high frequency current at 3.0 V — all peripheral clocks disabled	—	37	TBD	mA	2
$I_{DD\_WAIT}$	Wait mode reduced frequency current at 3.0 V — all peripheral clocks disabled	—	21	TBD	mA	4

Table continues on the next page...

**Table 6. Power consumption operating behaviors (continued)**

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
I <sub>DD_STOP</sub>	Stop mode current at 3.0 V	—	TBD	TBD	mA	
	• @ -40 to 25°C	—	TBD	TBD	mA	
	• @ 70°C	—	TBD	TBD	mA	
	• @ 105°C	—	TBD	TBD	mA	
I <sub>DD_VLPR</sub>	Very-low-power run mode current at 3.0 V — all peripheral clocks disabled	—	2.3	TBD	mA	5
I <sub>DD_VLPR</sub>	Very-low-power run mode current at 3.0 V — all peripheral clocks enabled	—	3.1	TBD	mA	6
I <sub>DD_VLPW</sub>	Very-low-power wait mode current at 3.0 V	—	1.8	TBD	mA	7
I <sub>DD_VLPS</sub>	Very-low-power stop mode current at 3.0 V	—	200	TBD	μA	
	• @ -40 to 25°C	—	TBD	TBD	μA	
	• @ 70°C	—	TBD	TBD	μA	
	• @ 105°C	—	TBD	TBD	μA	
I <sub>DD_LLS</sub>	Low leakage stop mode current at 3.0 V	—	200	TBD	μA	8
	• @ -40 to 25°C	—	TBD	TBD	μA	
	• @ 70°C	—	TBD	TBD	μA	
	• @ 105°C	—	TBD	TBD	μA	
I <sub>DD_VLLS3</sub>	Very low-leakage stop mode 3 current at 3.0 V	—	6.5	TBD	μA	#new-reference/ llsramtbn
	• @ -40 to 25°C	—	37.4	TBD	μA	
	• @ 70°C	—	148.3	TBD	μA	
	• @ 105°C	—				
I <sub>DD_VLLS2</sub>	Very low-leakage stop mode 2 current at 3.0 V	—	3.4	TBD	μA	
	• @ -40 to 25°C	—	13.4	TBD	μA	
	• @ 70°C	—	58.5	TBD	μA	
	• @ 105°C	—				
I <sub>DD_VLLS1</sub>	Very low-leakage stop mode 1 current at 3.0 V	—	2.9	TBD	μA	
	• @ -40 to 25°C	—	9.8	TBD	μA	
	• @ 70°C	—	44.7	TBD	μA	
	• @ 105°C	—				
I <sub>DD_VBAT</sub>	Average current when CPU is not accessing RTC registers at 3.0 V	—	0.91	1.1	μA	9
	• @ -40 to 25°C	—	1.5	1.85	μA	
	• @ 70°C	—	4.3	4.3	μA	
	• @ 105°C	—				

1. The analog supply current is the sum of the active or disabled current for each of the analog modules on the device. See each module's specification for its supply current.

## General

- 120 MHz core and system clock, 60 MHz bus, 30 MHz FlexBus clock, and 20 MHz flash clock. MCG configured for PEE mode. All peripheral clocks disabled.
- 120 MHz core and system clock, 60 MHz bus, 50 MHz FlexBus clock, and 20 MHz flash clock. MCG configured for PEE mode. All peripheral clocks enabled, but peripherals are not in active operation.
- 25 MHz core and system clock, 25 MHz bus clock, and 12.5 MHz FlexBus and flash clock. MCG configured for FEI mode.
- 4 MHz core, system, 2 MHz FlexBus, and 2 MHz bus clock and 1 MHz flash clock. MCG configured for BLPE mode. All peripheral clocks disabled.
- 4 MHz core, system, 2 MHz FlexBus, and 2 MHz bus clock and 1 MHz flash clock. MCG configured for BLPE mode. All peripheral clocks disabled.
- 4 MHz core, system, 2 MHz FlexBus, and 2 MHz bus clock and 1 MHz flash clock. MCG configured for BLPE mode. All peripheral clocks disabled.
- Data reflects devices with 128 KB of RAM. For devices with 64 KB of RAM, power consumption is reduced by 2  $\mu$ A. For devices with 32 KB of RAM, power consumption is reduced by 3  $\mu$ A.
- Includes 32kHz oscillator current and RTC operation.

### 5.2.5.1 Diagram: Typical IDD\_RUN operating behavior

The following data was measured under these conditions:

- MCG in FBE mode for 50 MHz and lower frequencies. MCG in FEE mode at greater than 50 MHz frequencies. MCG in PEE mode is greater than 100 MHz frequencies.
- No GPIOs toggled
- Code execution from flash with cache enabled
- For the ALLOFF curve, all peripheral clocks are disabled except FTFL



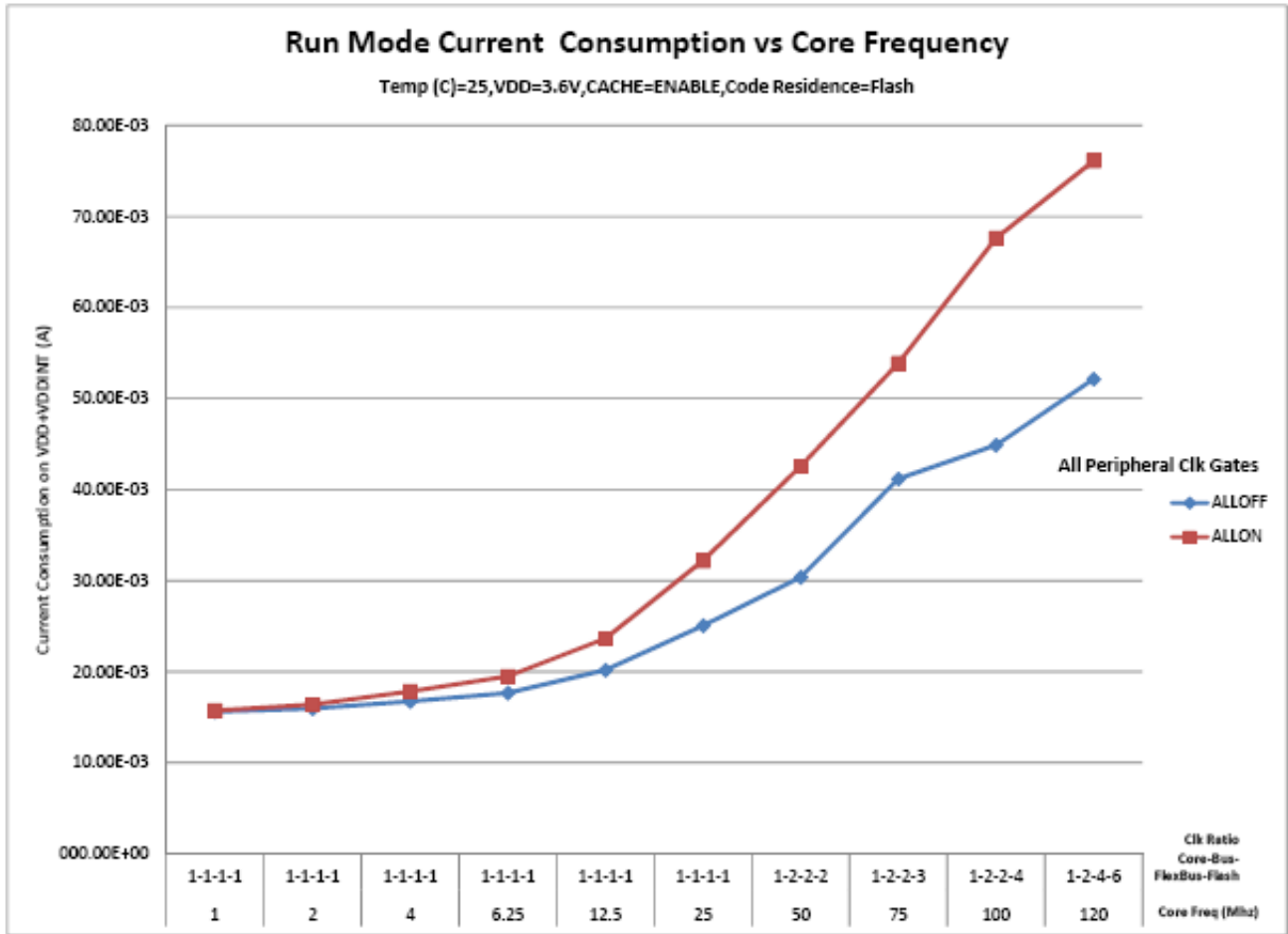


Figure 2. Run mode supply current vs. core frequency

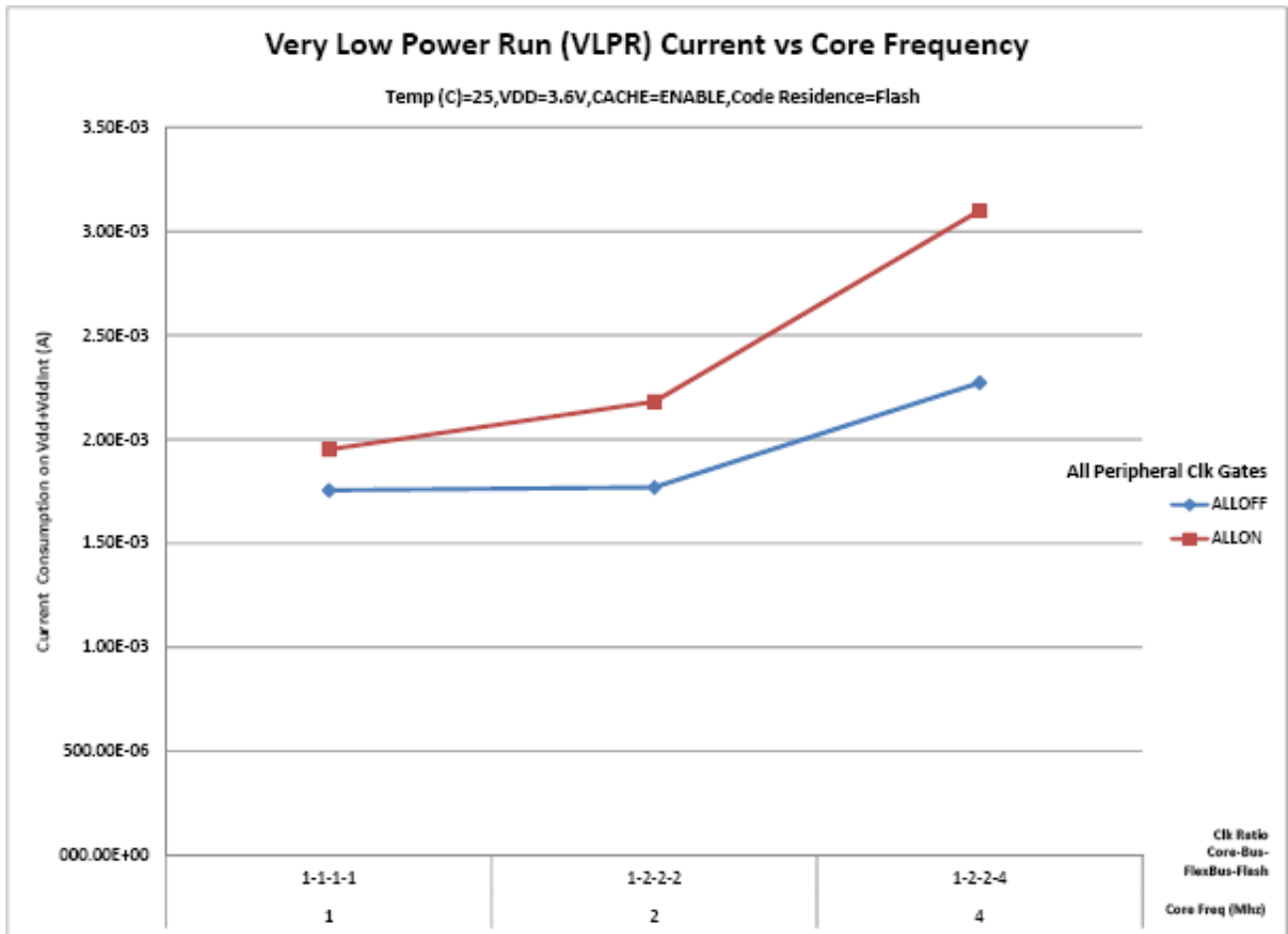


Figure 3. VLPR mode supply current vs. core frequency

### 5.2.6 EMC radiated emissions operating behaviors

Table 7. EMC radiated emissions operating behaviors for 256MAPBGA

Symbol	Description	Frequency band (MHz)	Typ.	Unit	Notes
V <sub>RE1</sub>	Radiated emissions voltage, band 1	0.15–50	TBD	dBμV	1, 2
V <sub>RE2</sub>	Radiated emissions voltage, band 2	50–150	TBD	dBμV	
V <sub>RE3</sub>	Radiated emissions voltage, band 3	150–500	TBD	dBμV	
V <sub>RE4</sub>	Radiated emissions voltage, band 4	500–1000	TBD	dBμV	
V <sub>RE_IEC</sub>	IEC level	0.15–1000	K	—	2, 3

1. Determined according to IEC Standard 61967-1, *Integrated Circuits - Measurement of Electromagnetic Emissions, 150 kHz to 1 GHz Part 1: General Conditions and Definitions* and IEC Standard 61967-2, *Integrated Circuits - Measurement of Electromagnetic Emissions, 150 kHz to 1 GHz Part 2: Measurement of Radiated Emissions – TEM Cell and Wideband TEM Cell Method*. Measurements were made while the microcontroller was running basic application code. The reported emission level is the value of the maximum measured emission, rounded up to the next whole number, from among the measured orientations in each frequency range.
2. V<sub>DD</sub> = 3.3 V, T<sub>A</sub> = 25 °C, f<sub>OSC</sub> = 12 MHz (crystal), f<sub>SYS</sub> = 96 MHz, f<sub>BUS</sub> = 48 MHz

3. Specified according to Annex D of IEC Standard 61967-2, *Measurement of Radiated Emissions—TEM Cell and Wideband TEM Cell Method*

## 5.2.7 Designing with radiated emissions in mind

To find application notes that provide guidance on designing your system to minimize interference from radiated emissions:

1. Go to <http://www.freescale.com>.
2. Perform a keyword search for “EMC design.”

## 5.2.8 Capacitance attributes

**Table 8. Capacitance attributes**

Symbol	Description	Min.	Max.	Unit
$C_{IN\_A}$	Input capacitance: analog pins	—	7	pF
$C_{IN\_D}$	Input capacitance: digital pins	—	7	pF
$C_{IN\_D\_io60}$	Input capacitance: fast digital pins	—	9	pF

## 5.3 Switching specifications

### 5.3.1 Device clock specifications

**Table 9. Device clock specifications**

Symbol	Description	Min.	Max.	Unit	Notes
Normal run mode					
$f_{SYS}$	System and core clock	—	120	MHz	
$f_{BUS}$	Bus clock	—	60	MHz	
FB_CLK	FlexBus clock	—	50	MHz	
$f_{FLASH}$	Flash clock	—	25	MHz	
$f_{LPTMR}$	LPTMR clock	—	25	MHz	
VLPR mode <sup>1</sup>					
$f_{SYS}$	System and core clock	—	4	MHz	
$f_{BUS}$	Bus clock	—	4	MHz	
FB_CLK	FlexBus clock	—	4	MHz	
$f_{FLASH}$	Flash clock	—	1	MHz	

*Table continues on the next page...*

**Table 9. Device clock specifications (continued)**

Symbol	Description	Min.	Max.	Unit	Notes
$f_{LPTMR}$	LPTMR clock	—	4	MHz	

1. The frequency limitations in VLPR mode here override any frequency specification listed in the timing specification for any other module.

### 5.3.2 General switching specifications

These general purpose specifications apply to all signals configured for GPIO, UART, CAN, CMT, and I<sup>2</sup>C signals.

**Table 10. General switching specifications**

Symbol	Description	Min.	Max.	Unit	Notes
	GPIO pin interrupt pulse width (digital glitch filter disabled) — Synchronous path	1.5	—	Bus clock cycles	1
	GPIO pin interrupt pulse width (digital glitch filter disabled, analog filter enabled) — Asynchronous path	100	—	ns	2
	GPIO pin interrupt pulse width (digital glitch filter disabled, analog filter disabled) — Asynchronous path	16	—	ns	2
	External reset pulse width (digital glitch filter disabled)	100	—	ns	2
	Mode select (EZP_CS) hold time after reset deassertion	2	—	Bus clock cycles	
$t_{i050}$	Port rise and fall time (high drive strength) <ul style="list-style-type: none"> <li>• Slew disabled</li> <li>• Slew enabled</li> </ul>	—	TBD	ns	3
		—	TBD	ns	4
$t_{i050}$	Port rise and fall time (low drive strength) <ul style="list-style-type: none"> <li>• Slew disabled</li> <li>• Slew enabled</li> </ul>	—	TBD	ns	3
		—	TBD	ns	4
$t_{i060}$	Port rise and fall time (high drive strength) <ul style="list-style-type: none"> <li>• Slew disabled</li> <li>• Slew enabled</li> </ul>	—	TBD	ns	3
		—	TBD	ns	4
$t_{i060}$	Port rise and fall time (low drive strength) <ul style="list-style-type: none"> <li>• Slew disabled</li> <li>• Slew enabled</li> </ul>	—	TBD	ns	3
		—	TBD	ns	4
$t_{tamper}$	Port rise and fall time (high drive strength) <ul style="list-style-type: none"> <li>• Slew disabled</li> <li>• Slew enabled</li> </ul>	—	TBD	ns	5
		—	TBD	ns	6

Table continues on the next page...

**Table 10. General switching specifications (continued)**

Symbol	Description	Min.	Max.	Unit	Notes
$t_{\text{tamper}}$	Port rise and fall time (low drive strength)	—	TBD	ns	7
	• Slew disabled	—	TBD	ns	8
	• Slew enabled				

1. The greater synchronous and asynchronous timing must be met.
2. This is the shortest pulse that is guaranteed to be recognized.
3. 25pF load
4. 15pF load
5. 75pF load
6. 15pF load
7. 75pF load
8. 15pF load

## 5.4 Thermal specifications

### 5.4.1 Thermal operating requirements

**Table 11. Thermal operating requirements**

Symbol	Description	Min.	Max.	Unit
$T_J$	Die junction temperature	−40	125	°C
$T_A$	Ambient temperature	−40	105	°C

### 5.4.2 Thermal attributes

Board type	Symbol	Description	144 LQFP	144 MAPBGA	Unit	Notes
Single-layer (1s)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	45	50	°C/W	1
Four-layer (2s2p)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	36	30	°C/W	1
Single-layer (1s)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./min. air speed)	36	41	°C/W	1

Table continues on the next page...

## Peripheral operating requirements and behaviors

Board type	Symbol	Description	144 LQFP	144 MAPBGA	Unit	Notes
Four-layer (2s2p)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./min. air speed)	30	27	°C/W	1
—	$R_{\theta JB}$	Thermal resistance, junction to board	24	17	°C/W	2
—	$R_{\theta JC}$	Thermal resistance, junction to case	9	10	°C/W	3
—	$\Psi_{JT}$	Thermal characterization parameter, junction to package top outside center (natural convection)	2	2	°C/W	4

1. Determined according to JEDEC Standard JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions—Natural Convection (Still Air)*, or EIA/JEDEC Standard JESD51-6, *Integrated Circuit Thermal Test Method Environmental Conditions—Forced Convection (Moving Air)*.
2. Determined according to JEDEC Standard JESD51-8, *Integrated Circuit Thermal Test Method Environmental Conditions—Junction-to-Board*.
3. Determined according to Method 1012.1 of MIL-STD 883, *Test Method Standard, Microcircuits*, with the cold plate temperature used for the case temperature. The value includes the thermal resistance of the interface material between the top of the package and the cold plate.
4. Determined according to JEDEC Standard JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions—Natural Convection (Still Air)*.

## 6 Peripheral operating requirements and behaviors

### 6.1 Core modules

#### 6.1.1 Debug trace timing specifications

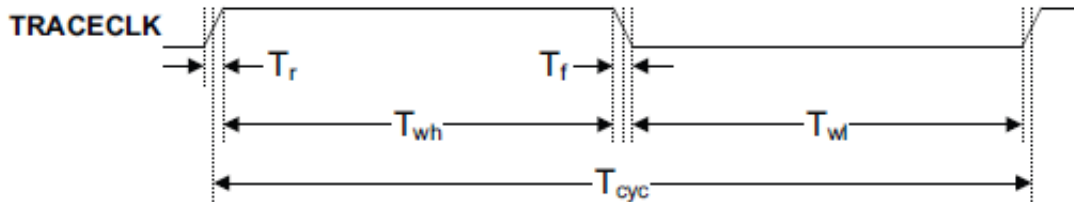
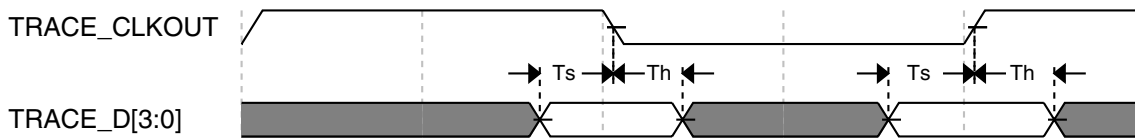
Table 12. Debug trace operating behaviors

Symbol	Description	Min.	Max.	Unit
$T_{cyc}$	Clock period	Frequency dependent		MHz
$T_{wl}$	Low pulse width	2	—	ns
$T_{wh}$	High pulse width	2	—	ns
$T_r$	Clock and data rise time	—	3	ns

Table continues on the next page...

**Table 12. Debug trace operating behaviors (continued)**

Symbol	Description	Min.	Max.	Unit
$T_f$	Clock and data fall time	—	3	ns
$T_s$	Data setup	3	—	ns
$T_h$	Data hold	2	—	ns

**Figure 4. TRACE\_CLKOUT specifications****Figure 5. Trace data specifications**

## 6.1.2 JTAG electricals

**Table 13. JTAG voltage range electricals**

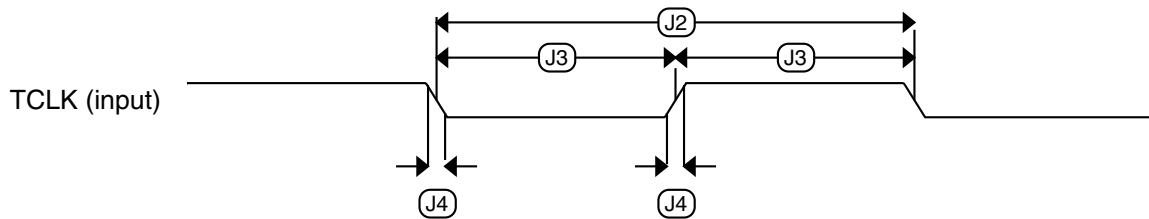
Symbol	Description	Min.	Max.	Unit
	Operating voltage	2.7	5.5	V
J1	TCLK frequency of operation <ul style="list-style-type: none"> <li>• JTAG</li> <li>• CJTAG</li> </ul>	—	10	MHz
J2	TCLK cycle period	1/J1	—	ns
J3	TCLK clock pulse width <ul style="list-style-type: none"> <li>• JTAG</li> <li>• CJTAG</li> </ul>	100	—	ns
		200	—	ns
J4	TCLK rise and fall times	—	1	ns
J5	TMS input data setup time to TCLK rise <ul style="list-style-type: none"> <li>• JTAG</li> <li>• CJTAG</li> </ul>	53	—	ns
		112	—	ns

Table continues on the next page...

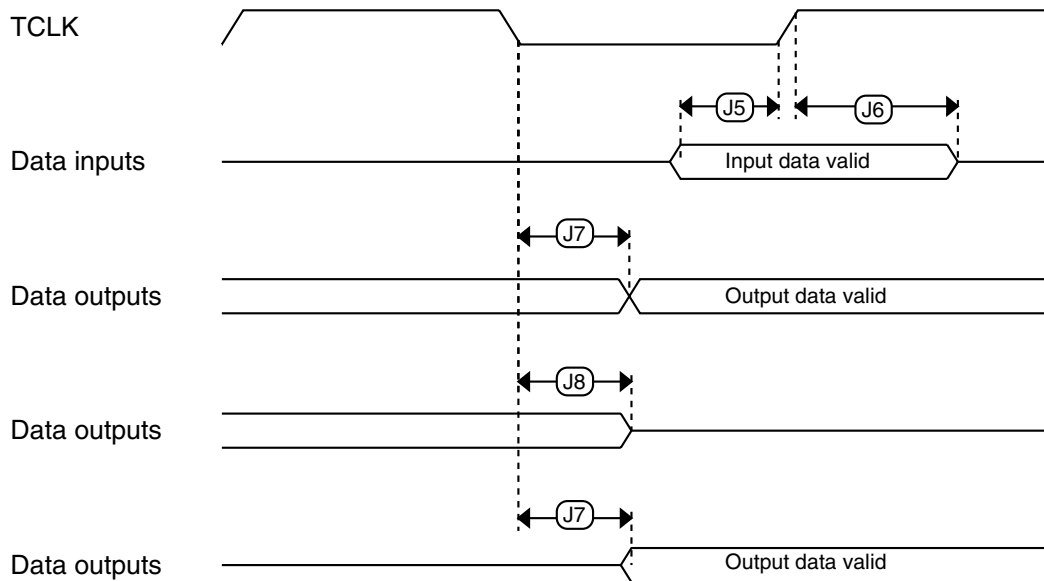
**Table 13. JTAG voltage range electricals (continued)**

Symbol	Description	Min.	Max.	Unit
J6	TDI input data setup time to TCLK rise	8	—	ns
J7	TMS input data hold time after TCLK rise • JTAG • CJTAG	3.4	—	ns
		3.4		
J8	TDI input data hold time after TCLK rise	3.4	—	ns
J9	TCLK low to TMS data valid • JTAG • CJTAG	—	48	ns
			85	
J10	TCLK low to TDO data valid	—	48	ns
J11	Output data hold/invalid time after clock edge <sup>1</sup>	—	3	ns

1. They are common for JTAG and CJTAG.



**Figure 6. Test clock input timing**



**Figure 7. Boundary scan (JTAG) timing**





**Figure 8. Test Access Port timing**



**Figure 9.  $\overline{\text{TRST}}$  timing**

## 6.2 System modules

There are no specifications necessary for the device's system modules.

## 6.3 Clock modules

## 6.3.1 MCG specifications

**Table 14. MCG specifications**

Symbol	Description	Min.	Typ.	Max.	Unit	Notes	
$f_{ints\_ft}$	Internal reference frequency (slow clock) — factory trimmed at nominal VDD and 25 °C	—	32.768	—	kHz		
$f_{ints\_t}$	Internal reference frequency (slow clock) — user trimmed	31.25	—	39.0625	kHz		
$I_{ints}$	Internal reference (slow clock) current	—	TBD	—	μA		
$\Delta f_{dco\_res\_t}$	Resolution of trimmed average DCO output frequency at fixed voltage and temperature — using SCTRIM and SCFTRIM	—	± 0.3	± 0.6	% $f_{dco}$	1	
$\Delta f_{dco\_res\_t}$	Resolution of trimmed average DCO output frequency at fixed voltage and temperature — using SCTRIM only	—	± 0.2	± 0.5	% $f_{dco}$	1	
$\Delta f_{dco\_t}$	Total deviation of trimmed average DCO output frequency over voltage and temperature	—	± 10	—	% $f_{dco}$	1	
$\Delta f_{dco\_t}$	Total deviation of trimmed average DCO output frequency over fixed voltage and temperature range of 0–70°C	—	± 1.5	± 4.5	% $f_{dco}$	1	
$f_{intf\_ft}$	Internal reference frequency (fast clock) — factory trimmed at nominal VDD and 25°C			4	MHz		
$f_{intf\_t}$	Internal reference frequency (fast clock) — user trimmed at nominal VDD and 25 °C	3	—	5	MHz		
$I_{intf}$	Internal reference (fast clock) current	—	TBD	—	μA		
$f_{loc\_low}$	Loss of external clock minimum frequency — RANGE = 00	$(3/5) \times f_{ints\_t}$	—	—	kHz		
$f_{loc\_high}$	Loss of external clock minimum frequency — RANGE = 01, 10, or 11	$(16/5) \times f_{ints\_t}$	—	—	kHz		
FLL							
$f_{fill\_ref}$	FLL reference frequency range	31.25	—	39.0625	kHz		
$f_{dco}$	DCO output frequency range	Low range (DRS=00) $640 \times f_{fill\_ref}$	20	20.97	25	MHz	2, 3
		Mid range (DRS=01) $1280 \times f_{fill\_ref}$	40	41.94	50	MHz	
		Mid-high range (DRS=10) $1920 \times f_{fill\_ref}$	60	62.91	75	MHz	
		High range (DRS=11) $2560 \times f_{fill\_ref}$	80	83.89	100	MHz	

Table continues on the next page...

**Table 14. MCG specifications (continued)**

Symbol	Description	Min.	Typ.	Max.	Unit	Notes	
$f_{\text{dco\_t\_DMX32}}$	DCO output frequency	Low range (DRS=00) $732 \times f_{\text{fill\_ref}}$	—	23.99	—	MHz	4, 5
		Mid range (DRS=01) $1464 \times f_{\text{fill\_ref}}$	—	47.97	—	MHz	
		Mid-high range (DRS=10) $2197 \times f_{\text{fill\_ref}}$	—	71.99	—	MHz	
		High range (DRS=11) $2929 \times f_{\text{fill\_ref}}$	—	95.98	—	MHz	
$J_{\text{cyc\_fll}}$	FLL period jitter <ul style="list-style-type: none"> <li><math>f_{\text{VCO}} = 48 \text{ MHz}</math></li> <li><math>f_{\text{VCO}} = 98 \text{ MHz}</math></li> </ul>	—	180	—	ps		
$J_{\text{acc\_fll}}$	FLL accumulated jitter of DCO output over a 1 $\mu$ s time window	—	TBD	—	ps		
$t_{\text{fill\_acquire}}$	FLL target frequency acquisition time	—	—	1	ms	6	
PLL0,1							
$f_{\text{pll\_ref}}$	PLL reference frequency range	8	—	16	MHz		
$f_{\text{vcoclk\_2x}}$	VCO output frequency	180	—	360	MHz		
$f_{\text{vcoclk}}$	PLL output frequency	90	—	180	MHz		
$f_{\text{vcoclk\_90}}$	PLL quadrature output frequency	90	—	180	MHz		
$I_{\text{pll}}$	PLL operating current (fast)	—	TBD	—	$\mu$ A	7	
$I_{\text{pll}}$	PLL operating current (fast)	—	TBD	—	$\mu$ A	7	
$t_{\text{pll\_lock}}$	Lock detector detection time	—	—	$100 \times 10^{-6} + 1075(1/f_{\text{pll\_ref}})$	s	8	
$J_{\text{cyc\_pll}}$	Jitter (cycle to cycle)	—	50	TBD	ps		
$J_{\text{acc\_pll}}$	Jitter (accumulated)	—	500	TBD	ps	9	

1. This parameter is measured with the internal reference (slow clock) being used as a reference to the FLL (FEI clock mode).
2. These typical values listed are with the slow internal reference clock (FEI) using factory trim and DMX32=0.
3. The resulting system clock frequencies should not exceed their maximum specified values. The DCO frequency deviation ( $\Delta f_{\text{dco\_t}}$ ) over voltage and temperature should be considered.
4. These typical values listed are with the slow internal reference clock (FEI) using factory trim and DMX32=1.
5. The resulting clock frequency must not exceed the maximum specified clock frequency of the device.
6. This specification applies to any time the FLL reference source or reference divider is changed, trim value is changed, DMX32 bit is changed, DRS bits are changed, or changing from FLL disabled (BLPE, BLPI) to FLL enabled (FEI, FEE, FBE, FBI). If a crystal/resonator is being used as the reference, this specification assumes it is already running.
7. Excludes any oscillator currents that are also consuming power while PLL is in operation.
8. This specification applies to any time the PLL VCO divider or reference divider is changed, or changing from PLL disabled (BLPE, BLPI) to PLL enabled (PBE, PEE). If a crystal/resonator is being used as the reference, this specification assumes it is already running.

## Peripheral operating requirements and behaviors

9. Accumulated jitter will depend on VCO frequency and VDIV.

### 6.3.2 Oscillator electrical specifications

This section provides the electrical characteristics of the module.

#### 6.3.2.1 Oscillator DC electrical specifications

Table 15. Oscillator DC electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V <sub>DD</sub>	Supply voltage	1.71	—	3.6	V	
I <sub>DDOSC</sub>	Supply current — low-power mode (HGO=0) <ul style="list-style-type: none"> <li>32 kHz</li> <li>4 MHz</li> <li>8 MHz (RANGE=01)</li> <li>16 MHz</li> <li>24 MHz</li> <li>32 MHz</li> </ul>	—	500	—	nA	1
I <sub>DDOSC</sub>	Supply current — high gain mode (HGO=1) <ul style="list-style-type: none"> <li>32 kHz</li> <li>4 MHz</li> <li>8 MHz (RANGE=01)</li> <li>16 MHz</li> <li>24 MHz</li> <li>32 MHz</li> </ul>	—	25	—	μA	1
C <sub>x</sub>	EXTAL load capacitance	—	—	—		2, 3
C <sub>y</sub>	XTAL load capacitance	—	—	—		2, 3
R <sub>F</sub>	Feedback resistor — low-frequency, low-power mode (HGO=0)	—	—	—	MΩ	2, 4
	Feedback resistor — low-frequency, high-gain mode (HGO=1)	—	10	—	MΩ	
	Feedback resistor — high-frequency, low-power mode (HGO=0)	—	—	—	MΩ	
	Feedback resistor — high-frequency, high-gain mode (HGO=1)	—	1	—	MΩ	

Table continues on the next page...

**Table 15. Oscillator DC electrical specifications (continued)**

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
R <sub>S</sub>	Series resistor — low-frequency, low-power mode (HGO=0)	—	—	—	kΩ	
	Series resistor — low-frequency, high-gain mode (HGO=1)	—	200	—	kΩ	
	Series resistor — high-frequency, low-power mode (HGO=0)	—	—	—	kΩ	
	Series resistor — high-frequency, high-gain mode (HGO=1)	—	0	—	kΩ	
V <sub>pp</sub> <sup>5</sup>	Peak-to-peak amplitude of oscillation (oscillator mode) — low-frequency, low-power mode (HGO=0)	—	0.6	—	V	
	Peak-to-peak amplitude of oscillation (oscillator mode) — low-frequency, high-gain mode (HGO=1)	—	V <sub>DD</sub>	—	V	
	Peak-to-peak amplitude of oscillation (oscillator mode) — high-frequency, low-power mode (HGO=0)	—	0.6	—	V	
	Peak-to-peak amplitude of oscillation (oscillator mode) — high-frequency, high-gain mode (HGO=1)	—	V <sub>DD</sub>	—	V	

1. V<sub>DD</sub>=3.3 V, Temperature =25 °C
2. See crystal or resonator manufacturer's recommendation
3. C<sub>x</sub>,C<sub>y</sub> can be provided by using either the integrated capacitors or by using external components.
4. When low power mode is selected, R<sub>F</sub> is integrated and must not be attached externally.
5. The EXTAL and XTAL pins should only be connected to required oscillator components and must not be connected to any other devices.

### 6.3.2.2 Oscillator frequency specifications

**Table 16. Oscillator frequency specifications**

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
f <sub>osc_lo</sub>	Oscillator crystal or resonator frequency — low frequency mode (MCG_C2[RANGE]=00)	32	—	40	kHz	
f <sub>osc_hi_1</sub>	Oscillator crystal or resonator frequency — high frequency mode (low range) (MCG_C2[RANGE]=01)	3	—	8	MHz	1
f <sub>osc_hi_2</sub>	Oscillator crystal or resonator frequency — high frequency mode (high range) (MCG_C2[RANGE]=1x)	8	—	32	MHz	
f <sub>ec_extal</sub>	Input clock frequency (external clock mode)	—	—	60	MHz	2, 3
t <sub>dc_extal</sub>	Input clock duty cycle (external clock mode)	40	50	60	%	

Table continues on the next page...

**Table 16. Oscillator frequency specifications (continued)**

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
$t_{cst}$	Crystal startup time — 32 kHz low-frequency, low-power mode (HGO=0)	—	1000	—	ms	4, 5
	Crystal startup time — 32 kHz low-frequency, high-gain mode (HGO=1)	—	500	—	ms	
	Crystal startup time — 8 MHz high-frequency (MCG_C2[RANGE]=01), low-power mode (HGO=0)	—	0.6	—	ms	
	Crystal startup time — 8 MHz high-frequency (MCG_C2[RANGE]=01), high-gain mode (HGO=1)	—	1	—	ms	

- Frequencies less than 8 MHz are not in the PLL range.
- Other frequency limits may apply when external clock is being used as a reference for the FLL or PLL.
- When transitioning from FBE to FEI mode, restrict the frequency of the input clock so that, when it is divided by FRDIV, it remains within the limits of the DCO input clock frequency.
- Proper PC board layout procedures must be followed to achieve specifications.
- Crystal startup time is defined as the time between the oscillator being enabled and the OSCINIT bit in the MCG\_S register being set.

### 6.3.3 32kHz Oscillator Electrical Characteristics

This section describes the module electrical characteristics.

#### 6.3.3.1 32kHz oscillator DC electrical specifications

**Table 17. 32kHz oscillator DC electrical specifications**

Symbol	Description	Min.	Typ.	Max.	Unit
$V_{BAT}$	Supply voltage	1.71	—	3.6	V
$R_F$	Internal feedback resistor	—	100	—	M $\Omega$
$C_{para}$	Parasitical capacitance of EXTAL32 and XTAL32	—	5	7	pF
$V_{pp}^1$	Peak-to-peak amplitude of oscillation	—	0.6	—	V

- The EXTAL32 and XTAL32 pins should only be connected to required oscillator components and must not be connected to any other devices.

#### 6.3.3.2 32kHz oscillator frequency specifications

**Table 18. 32kHz oscillator frequency specifications**

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
$f_{osc\_lo}$	Oscillator crystal	—	32.768	—	kHz	
$t_{start}$	Crystal start-up time	—	1000	—	ms	1

- Proper PC board layout procedures must be followed to achieve specifications.

## 6.4 Memories and memory interfaces

### 6.4.1 Flash (FTFE) electrical specifications

This section describes the electrical characteristics of the FTFE module.

#### 6.4.1.1 Flash timing specifications — program and erase

The following specifications represent the amount of time the internal charge pumps are active and do not include command overhead.

**Table 19. NVM program/erase timing specifications**

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
$t_{hvp\text{pgm}4}$	Program Phrase high-voltage time	—	7.5	TBD	$\mu\text{s}$	
$t_{h\text{versscr}}$	Erase Flash Sector high-voltage time	—	13	TBD	ms	1
$t_{h\text{versblk}}$	Erase Flash Block high-voltage time	—	425	TBD	ms	1

1. Maximum time based on expectations at cycling end-of-life.

#### 6.4.1.2 Flash timing specifications — commands

**Table 20. Flash command timing specifications**

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
$t_{rd1\text{blk}}$	Read 1s Block execution time	—	1.5	TBD	ms	
$t_{rd1\text{sec}4\text{k}}$	Read 1s Section execution time (4KB flash)	—	50	TBD	$\mu\text{s}$	1
$t_{pgm\text{chk}}$	Program Check execution time	—	35	TBD	$\mu\text{s}$	1
$t_{rd\text{src}}$	Read Resource execution time	—	35	TBD	$\mu\text{s}$	1
$t_{pgm8}$	Program Phrase execution time	—	65	TBD	$\mu\text{s}$	
$t_{ers\text{blk}}$	Erase Flash Block execution time	—	450	TBD	ms	2
$t_{ers\text{scr}}$	Erase Flash Sector execution time	—	15	TBD	ms	2
$t_{pgm\text{sec}4\text{k}}$	Program Section execution time (4KB flash)	—	20	TBD	ms	
$t_{rd1\text{all}}$	Read 1s All Blocks execution time	—	1.5	TBD	ms	
$t_{rd\text{once}}$	Read Once execution time	—	17	TBD	$\mu\text{s}$	1
$t_{pgm\text{once}}$	Program Once execution time	—	65	TBD	$\mu\text{s}$	
$t_{ers\text{all}}$	Erase All Blocks execution time	—	900	TBD	ms	2
$t_{\text{vfykey}}$	Verify Backdoor Access Key execution time	—	25	TBD	$\mu\text{s}$	1

Table continues on the next page...

**Table 20. Flash command timing specifications (continued)**

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
$t_{\text{swapx01}}$	Swap Control execution time • control code 0x01	—	185	TBD	$\mu\text{s}$	
$t_{\text{swapx02}}$	• control code 0x02	—	65	TBD	$\mu\text{s}$	
$t_{\text{swapx04}}$	• control code 0x04	—	65	TBD	$\mu\text{s}$	
$t_{\text{swapx08}}$	• control code 0x08	—	25	TBD	$\mu\text{s}$	
$t_{\text{pgmpart}}$	Program Partition for EEPROM execution time	—	TBD	TBD	ms	
$t_{\text{setram64k}}$	Set FlexRAM Function execution time: • 64 KB EEPROM backup	—	TBD	TBD	ms	
$t_{\text{setram128k}}$	• 128 KB EEPROM backup	—	TBD	TBD	ms	
$t_{\text{setram256k}}$	• 256 KB EEPROM backup	—	TBD	TBD	ms	
$t_{\text{setram512k}}$	• 512 KB EEPROM backup	—	TBD	TBD	ms	
$t_{\text{eewr8bers}}$	Byte-write to erased FlexRAM location execution time	—	100	TBD	$\mu\text{s}$	3
$t_{\text{eewr8b64k}}$	Byte-write to FlexRAM execution time: • 64 KB EEPROM backup	—	TBD	TBD	ms	
$t_{\text{eewr8b128k}}$	• 128 KB EEPROM backup	—	TBD	TBD	ms	
$t_{\text{eewr8b256k}}$	• 256 KB EEPROM backup	—	TBD	TBD	ms	
$t_{\text{eewr8b512k}}$	• 512 KB EEPROM backup	—	TBD	TBD	ms	
$t_{\text{eewr16bers}}$	16-bit write to erased FlexRAM location execution time	—	100	TBD	$\mu\text{s}$	
$t_{\text{eewr16b64k}}$	16-bit write to FlexRAM execution time: • 64 KB EEPROM backup	—	TBD	TBD	ms	
$t_{\text{eewr16b128k}}$	• 128 KB EEPROM backup	—	TBD	TBD	ms	
$t_{\text{eewr16b256k}}$	• 256 KB EEPROM backup	—	TBD	TBD	ms	
$t_{\text{eewr16b512k}}$	• 512 KB EEPROM backup	—	TBD	TBD	ms	
$t_{\text{eewr32bers}}$	32-bit write to erased FlexRAM location execution time	—	200	TBD	$\mu\text{s}$	
$t_{\text{eewr32b64k}}$	32-bit-write to FlexRAM execution time: • 64 KB EEPROM backup	—	TBD	TBD	ms	
$t_{\text{eewr32b128k}}$	• 128 KB EEPROM backup	—	TBD	TBD	ms	
$t_{\text{eewr32b256k}}$	• 256 KB EEPROM backup	—	TBD	TBD	ms	
$t_{\text{eewr32b512k}}$	• 512 KB EEPROM backup	—	TBD	TBD	ms	

1. Assumes 25MHz flash clock frequency.
2. Maximum times for erase parameters based on expectations at cycling end-of-life.
3. For byte-writes to an erased FlexRAM location, the aligned word containing the byte must be erased.



### 6.4.1.3 Flash (FTFE) current and power specifications

Table 21. Flash (FTFE) current and power specifications

Symbol	Description	Typ.	Unit
I <sub>DD_PGM</sub>	Worst case programming current in program flash	10	mA

### 6.4.1.4 Reliability specifications

Table 22. NVM reliability specifications

Symbol	Description	Min.	Typ. <sup>1</sup>	Max.	Unit	Notes
Program Flash						
t <sub>nvmpretp10k</sub>	Data retention after up to 10 K cycles	5	50	—	years	2
t <sub>nvmpretp1k</sub>	Data retention after up to 1 K cycles	10	100	—	years	2
t <sub>nvmpretp100</sub>	Data retention after up to 100 cycles	15	100	—	years	2
n <sub>nvmpcyp</sub>	Cycling endurance	10 K	35 K	—	cycles	3
Data Flash						
t <sub>nvmdretd10k</sub>	Data retention after up to 10 K cycles	5	50	—	years	2
t <sub>nvmdretd1k</sub>	Data retention after up to 1 K cycles	10	100	—	years	2
t <sub>nvmdretd100</sub>	Data retention after up to 100 cycles	15	100	—	years	2
n <sub>nvmdcycd</sub>	Cycling endurance	10 K	35 K	—	cycles	3
FlexRAM as EEPROM						
t <sub>nvmdretee100</sub>	Data retention up to 100% of write endurance	5	50	—	years	2
t <sub>nvmdretee10</sub>	Data retention up to 10% of write endurance	10	100	—	years	2
t <sub>nvmdretee1</sub>	Data retention up to 1% of write endurance	15	100	—	years	2
n <sub>nvmdwree16</sub>	Write endurance	TBD	TBD	—	writes	4
n <sub>nvmdwree128</sub>	• EEPROM backup to FlexRAM ratio = 16	TBD	TBD	—	writes	
n <sub>nvmdwree512</sub>	• EEPROM backup to FlexRAM ratio = 128	TBD	TBD	—	writes	
n <sub>nvmdwree4k</sub>	• EEPROM backup to FlexRAM ratio = 512	TBD	TBD	—	writes	
n <sub>nvmdwree32k</sub>	• EEPROM backup to FlexRAM ratio = 4096	TBD	TBD	—	writes	
	• EEPROM backup to FlexRAM ratio = 32,768	TBD	TBD	—	writes	

1. Typical data retention values are based on measured response accelerated at high temperature and derated to a constant 25°C profile. Engineering Bulletin EB618 does not apply to this technology.
2. Data retention is based on T<sub>javg</sub> = 55°C (temperature profile over the lifetime of the application).
3. Cycling endurance represents number of program/erase cycles at -40°C ≤ T<sub>j</sub> ≤ 125°C.
4. Write endurance represents the number of writes to each FlexRAM location at -40°C ≤ T<sub>j</sub> ≤ 125°C influenced by the cycling endurance of the FlexNVM (same value as data flash) and the allocated EEPROM backup per subsystem. Minimum and typical values assume all byte-writes to FlexRAM.

### 6.4.1.5 Write endurance to FlexRAM for EEPROM

TBD

### 6.4.2 EzPort Switching Specifications

Table 23. EzPort switching specifications

Num	Description	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
EP1	EZP_CK frequency of operation (all commands except READ)	—	$f_{SYS}/2$	MHz
EP1a	EZP_CK frequency of operation (READ command)	—	$f_{SYS}/8$	MHz
EP2	EZP_CS negation to next EZP_CS assertion	$2 \times t_{EZP\_CK}$	—	ns
EP3	EZP_CS input valid to EZP_CK high (setup)	5	—	ns
EP4	EZP_CK high to EZP_CS input invalid (hold)	5	—	ns
EP5	EZP_D input valid to EZP_CK high (setup)	2	—	ns
EP6	EZP_CK high to EZP_D input invalid (hold)	5	—	ns
EP7	EZP_CK low to EZP_Q output valid	—	16	ns
EP8	EZP_CK low to EZP_Q output invalid (hold)	0	—	ns
EP9	EZP_CS negation to EZP_Q tri-state	—	12	ns

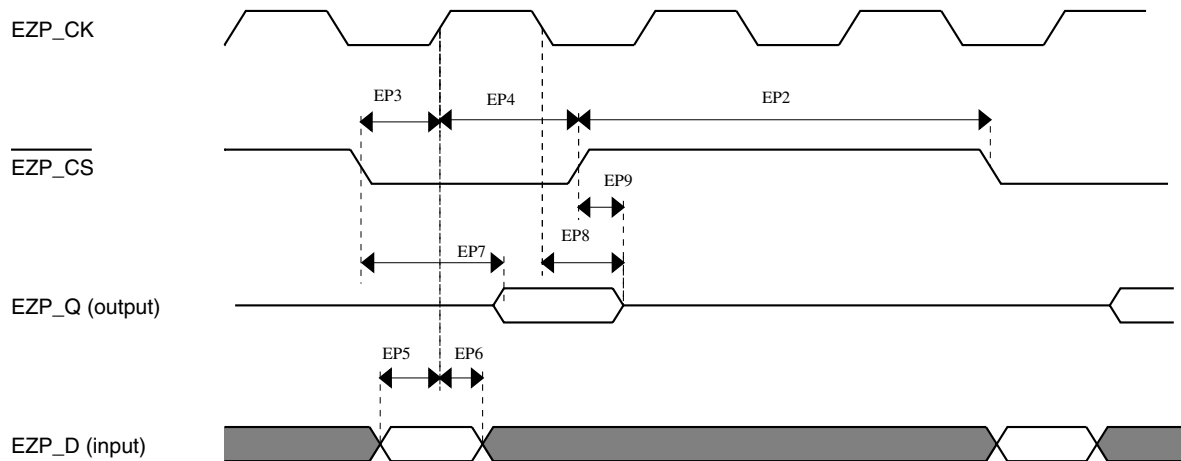


Figure 10. EzPort Timing Diagram

### 6.4.3 NFC specifications

The NAND flash controller (NFC) implements the interface to standard NAND flash memory devices. This section describes the timing parameters of the NFC.

In the following table:

- $T_H$  is the flash clock high time and
- $T_L$  is flash clock low time,

which are defined as:

$$T_{NFC} = T_L + T_H = \frac{T_{\text{input clock}}}{\text{SCALER}}$$

The SCALER value is derived from the fractional divider specified in the SIM's CLKDIV4 register:

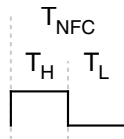
$$\text{SCALER} = \frac{\text{SIM\_CLKDIV4[NFCFRAC]} + 1}{\text{SIM\_CLKDIV4[NFCDIV]} + 1}$$

In case the reciprocal of SCALER is an integer, the duty cycle of NFC clock is 50%, means  $T_H = T_L$ . In case the reciprocal of SCALER is not an integer:

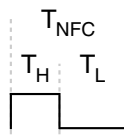
$$T_L = (1 + \text{SCALER} / 2) \times \frac{T_{NFC}}{2}$$

$$T_H = (1 - \text{SCALER} / 2) \times \frac{T_{NFC}}{2}$$

For example, if SCALER is 0.2, then  $T_H = T_L = T_{NFC}/2$ .



However, if SCALER is 0.667, then  $T_L = 2/3 \times T_{NFC}$  and  $T_H = 1/3 \times T_{NFC}$ .

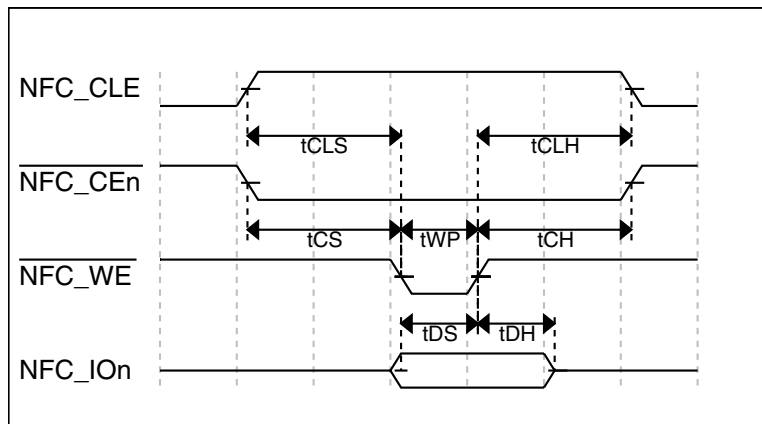


#### NOTE

The reciprocal of SCALER must be a multiple of 0.5. For example, 1, 1.5, 2, 2.5, etc.

**Table 24. NFC specifications**

Num	Description	Min.	Max.	Unit
$t_{CLS}$	NFC_CLE setup time	$2T_H + T_L - 1$	—	ns
$t_{CLH}$	NFC_CLE hold time	$T_H + T_L - 1$	—	ns
$t_{CS}$	$\overline{\text{NFC\_CEn}}$ setup time	$2T_H + T_L - 1$	—	ns
$t_{CH}$	$\overline{\text{NFC\_CEn}}$ hold time	$T_H + T_L$	—	ns
$t_{WP}$	NFC_WP pulse width	$T_L - 1$	—	ns
$t_{ALS}$	NFC_ALE setup time	$2T_H + T_L$	—	ns
$t_{ALH}$	NFC_ALE hold time	$T_H + T_L$	—	ns
$t_{DS}$	Data setup time	$T_L - 1$	—	ns
$t_{DH}$	Data hold time	$T_H - 1$	—	ns
$t_{WC}$	Write cycle time	$T_H + T_L - 1$	—	ns
$t_{WH}$	$\overline{\text{NFC\_WE}}$ hold time	$T_H - 1$	—	ns
$t_{RR}$	Ready to NFC_RE low	$4T_H + 3T_L + 90$	—	ns
$t_{RP}$	NFC_RE pulse width	$T_L + 1$	—	ns
$t_{RC}$	Read cycle time	$T_L + T_H - 1$	—	ns
$t_{REH}$	NFC_RE high hold time	$T_H - 1$	—	ns
$t_{IS}$	Data input setup time	11	—	ns

**Figure 11. Command latch cycle timing**

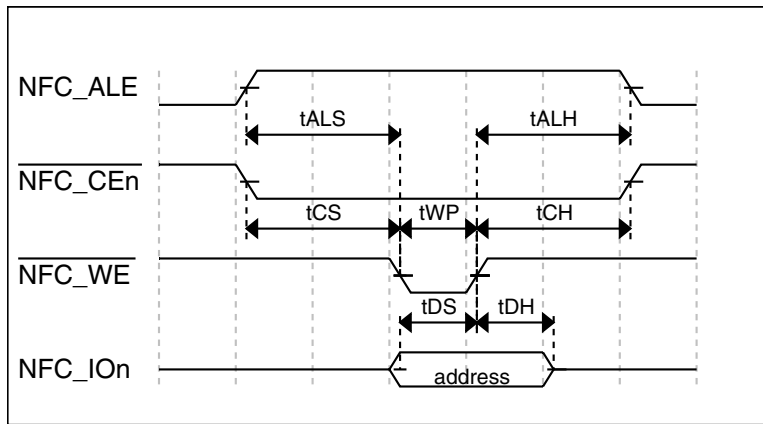


Figure 12. Address latch cycle timing

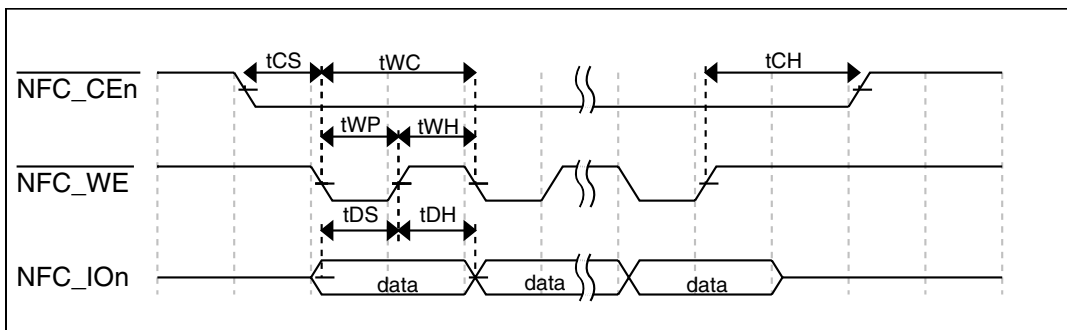


Figure 13. Write data latch cycle timing

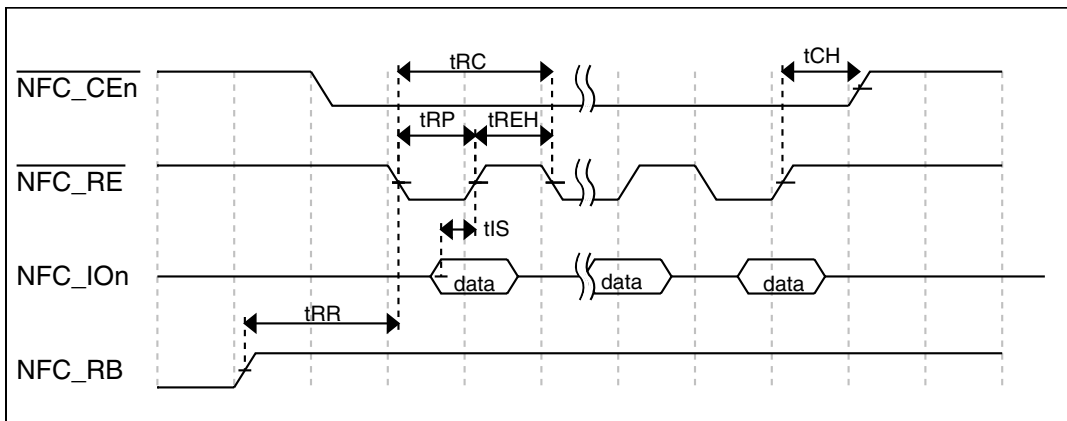


Figure 14. Read data latch cycle timing in non-fast mode

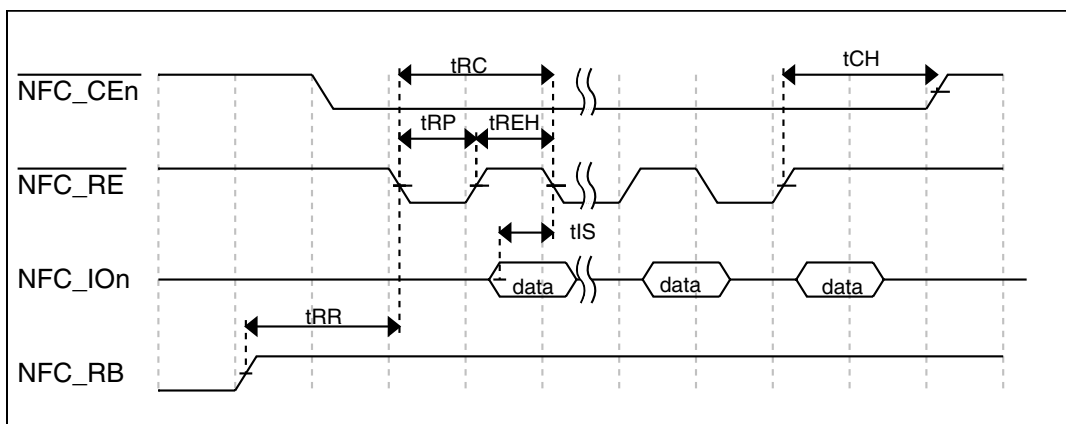


Figure 15. Read data latch cycle timing in fast mode

### 6.4.4 Flexbus Switching Specifications

All processor bus timings are synchronous; input setup/hold and output delay are given in respect to the rising edge of a reference clock, FB\_CLK. The FB\_CLK frequency may be the same as the internal system bus frequency or an integer divider of that frequency.

The following timing numbers indicate when data is latched or driven onto the external bus, relative to the Flexbus output clock (FB\_CLK). All other timing relationships can be derived from these values.

Table 25. Flexbus limited voltage range switching specifications

Num	Description	Min.	Max.	Unit	Notes
	Operating voltage	2.7	3.6	V	
	Frequency of operation	—	FB_CLK	MHz	
FB1	Clock period	20	—	ns	
FB2	Address, data, and control output valid	—	11.5	ns	1
FB3	Address, data, and control output hold	0.5	—	ns	1
FB4	Data and $\overline{\text{FB\_TA}}$ input setup	8.5	—	ns	2
FB5	Data and $\overline{\text{FB\_TA}}$ input hold	0.5	—	ns	2

1. Specification is valid for all FB\_AD[31:0], FB\_BE/BWEn, FB\_CSn, FB\_OE, FB\_R/W, FB\_TBST, FB\_TSIZ[1:0], FB\_ALE, and FB\_TS.
2. Specification is valid for all FB\_AD[31:0] and  $\overline{\text{FB\_TA}}$ .

Table 26. Flexbus full voltage range switching specifications

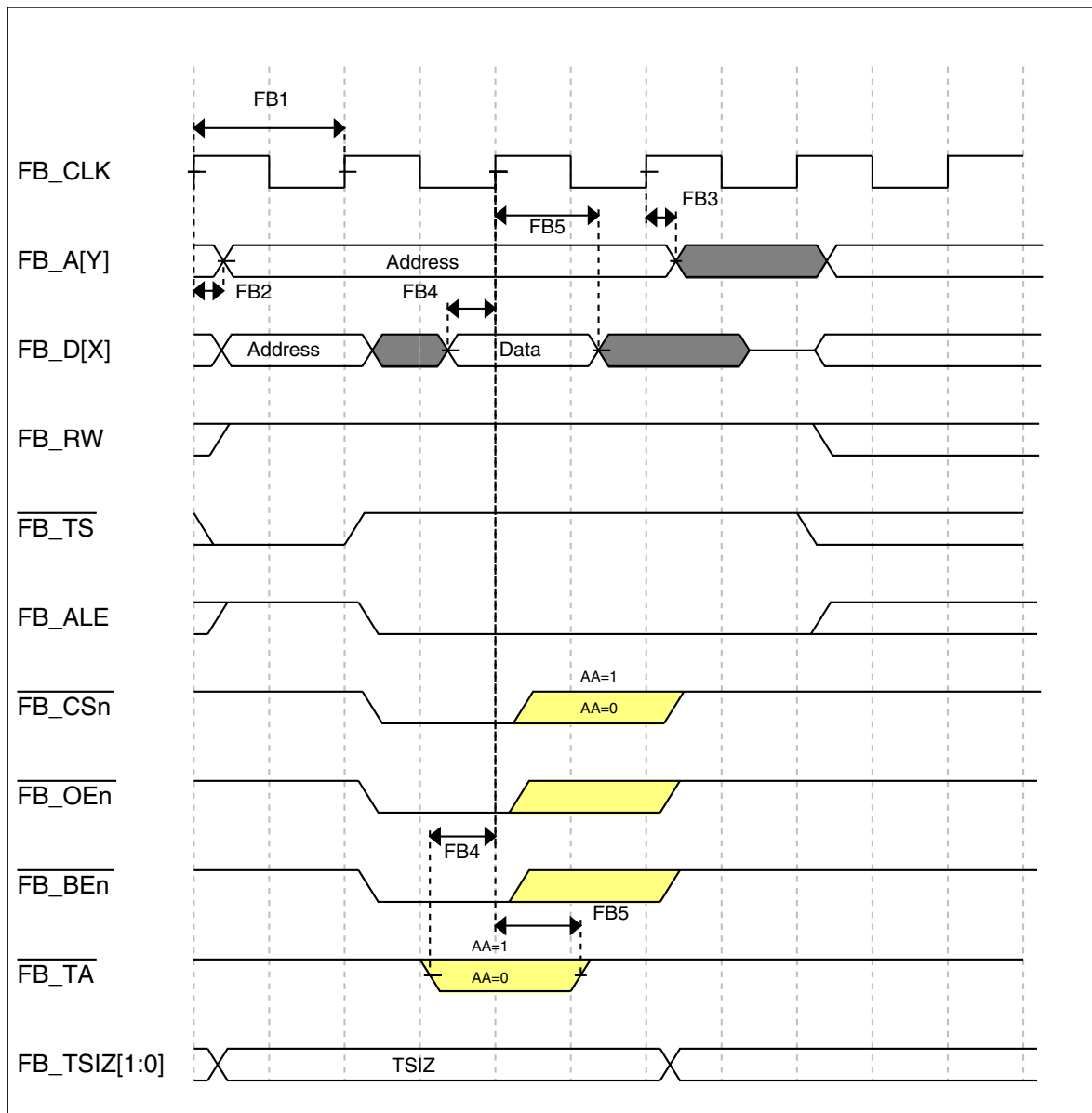
Num	Description	Min.	Max.	Unit	Notes
	Operating voltage	1.71	3.6	V	
	Frequency of operation	—	FB_CLK	MHz	

Table continues on the next page...

**Table 26. Flexbus full voltage range switching specifications (continued)**

Num	Description	Min.	Max.	Unit	Notes
FB1	Clock period	1/FB_CLK	—	ns	
FB2	Address, data, and control output valid	—	13.5	ns	1
FB3	Address, data, and control output hold	0	—	ns	1
FB4	Data and $\overline{\text{FB\_TA}}$ input setup	13.7	—	ns	2
FB5	Data and $\overline{\text{FB\_TA}}$ input hold	0.5	—	ns	2

1. Specification is valid for all FB\_AD[31:0],  $\overline{\text{FB\_BE/BWEn}}$ ,  $\overline{\text{FB\_CSn}}$ ,  $\overline{\text{FB\_OEn}}$ ,  $\overline{\text{FB\_R/W}}$ ,  $\overline{\text{FB\_TBST}}$ ,  $\overline{\text{FB\_TSIZ}}[1:0]$ ,  $\overline{\text{FB\_ALE}}$ , and  $\overline{\text{FB\_TS}}$ .
2. Specification is valid for all FB\_AD[31:0] and  $\overline{\text{FB\_TA}}$ .

**Figure 16. FlexBus read timing diagram**

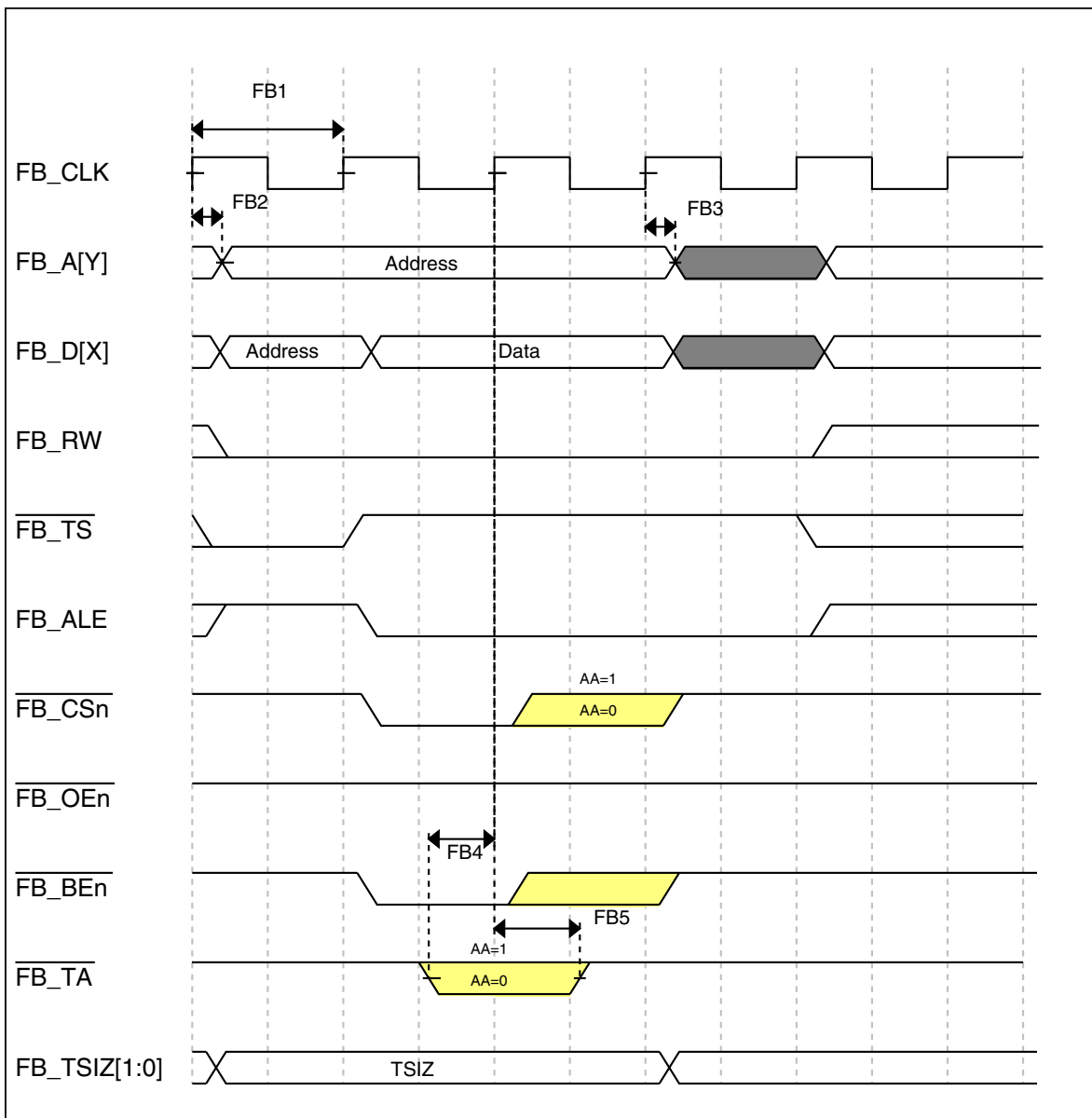


Figure 17: FlexBus write timing diagram

## 6.5 Security and integrity modules

There are no specifications necessary for the device's security and integrity modules.

## 6.6 Analog



## 6.6.1 ADC electrical specifications

The 16-bit accuracy specifications listed in [Table 27](#) and [Table 28](#) are achievable on the differential pins ADC<sub>x</sub>\_DP0, ADC<sub>x</sub>\_DM0.

The ADC<sub>x</sub>\_DP2 and ADC<sub>x</sub>\_DM2 ADC inputs are connected to the PGA outputs and are not direct device pins. Accuracy specifications for these pins are defined in [Table 29](#) and [Table 30](#).

All other ADC channels meet the 13-bit differential/12-bit single-ended accuracy specifications.

### 6.6.1.1 16-bit ADC operating conditions

**Table 27. 16-bit ADC operating conditions**

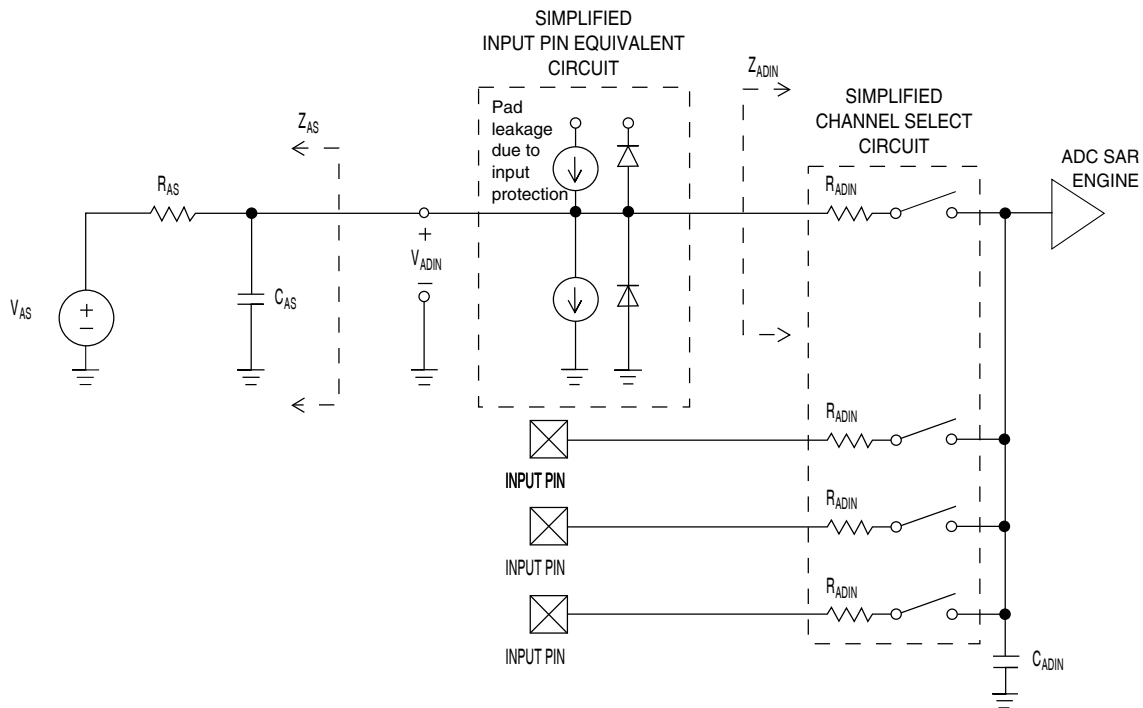
Symbol	Description	Conditions	Min.	Typ. <sup>1</sup>	Max.	Unit	Notes
V <sub>DDA</sub>	Supply voltage	Absolute	1.71	—	3.6	V	
ΔV <sub>DDA</sub>	Supply voltage	Delta to V <sub>DD</sub> (V <sub>DD</sub> -V <sub>DDA</sub> )	-100	0	+100	mV	<a href="#">2</a>
ΔV <sub>SSA</sub>	Ground voltage	Delta to V <sub>SS</sub> (V <sub>SS</sub> -V <sub>SSA</sub> )	-100	0	+100	mV	<a href="#">2</a>
V <sub>REFH</sub>	ADC reference voltage high		1.13	V <sub>DDA</sub>	V <sub>DDA</sub>	V	
V <sub>REFL</sub>	Reference voltage low		V <sub>SSA</sub>	V <sub>SSA</sub>	V <sub>SSA</sub>	V	
V <sub>ADIN</sub>	Input voltage		V <sub>REFL</sub>	—	V <sub>REFH</sub>	V	
C <sub>ADIN</sub>	Input capacitance	<ul style="list-style-type: none"> <li>16 bit modes</li> <li>8/10/12 bit modes</li> </ul>	—	8	10	pF	
R <sub>ADIN</sub>	Input resistance		—	2	5	kΩ	
R <sub>AS</sub>	Analog source resistance	13/12 bit modes f <sub>ADCK</sub> < 4MHz	—	—	5	kΩ	<a href="#">3</a>
f <sub>ADCK</sub>	ADC conversion clock frequency	≤ 13 bit modes	1.0	—	18.0	MHz	<a href="#">4</a>
f <sub>ADCK</sub>	ADC conversion clock frequency	16 bit modes	2.0	—	12.0	MHz	<a href="#">4</a>

*Table continues on the next page...*

**Table 27. 16-bit ADC operating conditions (continued)**

Symbol	Description	Conditions	Min.	Typ. <sup>1</sup>	Max.	Unit	Notes
$C_{rate}$	ADC conversion rate	≤ 13 bit modes No ADC hardware averaging Continuous conversions enabled, subsequent conversion time	20.000	—	818.330	Ksps	5
$C_{rate}$	ADC conversion rate	16 bit modes No ADC hardware averaging Continuous conversions enabled, subsequent conversion time	37.037	—	461.467	Ksps	5

1. Typical values assume  $V_{DDA} = 3.0\text{ V}$ ,  $\text{Temp} = 25^\circ\text{C}$ ,  $f_{ADCK} = 1.0\text{ MHz}$  unless otherwise stated. Typical values are for reference only and are not tested in production.
2. DC potential difference.
3. This resistance is external to MCU. The analog source resistance should be kept as low as possible in order to achieve the best results. The results in this datasheet were derived from a system which has  $<8\ \Omega$  analog source resistance. The  $R_{AS}/C_{AS}$  time constant should be kept to  $<1\text{ ns}$ .
4. To use the maximum ADC conversion clock frequency, the ADHSC bit should be set and the ADLPC bit should be clear.
5. For guidelines and examples of conversion rate calculation, download the ADC calculator tool: [http://cache.freescale.com/files/soft\\_dev\\_tools/software/app\\_software/converters/ADC\\_CALCULATOR\\_CNV.zip?fp=1](http://cache.freescale.com/files/soft_dev_tools/software/app_software/converters/ADC_CALCULATOR_CNV.zip?fp=1)



**Figure 18. ADC input impedance equivalency diagram**

## 6.6.1.2 16-bit ADC electrical characteristics

Table 28. 16-bit ADC characteristics ( $V_{REFH} = V_{DDA}$ ,  $V_{REFL} = V_{SSA}$ )

Symbol	Description	Conditions <sup>1</sup>	Min.	Typ. <sup>2</sup>	Max.	Unit	Notes
$I_{DDA\_ADC}$	Supply current		0.215	—	1.7	mA	3
$f_{ADACK}$	ADC asynchronous clock source	• ADLPC=1, ADHSC=0	1.2	2.4	3.9	MHz	$t_{ADACK} = 1/f_{ADACK}$
		• ADLPC=1, ADHSC=1	3.0	4.0	7.3	MHz	
		• ADLPC=0, ADHSC=0	2.4	5.2	6.1	MHz	
		• ADLPC=0, ADHSC=1	4.4	6.2	9.5	MHz	
	Sample Time	See Reference Manual chapter for sample times					
TUE	Total unadjusted error	• 12 bit modes • <12 bit modes	— —	$\pm 4$ $\pm 1.4$	$\pm 6.8$ $\pm 2.1$	LSB <sup>4</sup>	5
DNL	Differential non-linearity	• 12 bit modes  • <12 bit modes	— —	$\pm 0.7$ $\pm 0.2$	-1.1 to +1.9 -0.3 to 0.5	LSB <sup>4</sup>	5
INL	Integral non-linearity	• 12 bit modes	—	$\pm 1.0$	-2.7 to +1.9	LSB <sup>4</sup>	5
		• <12 bit modes	—	$\pm 0.5$	-0.7 to +0.5		
$E_{FS}$	Full-scale error	• 12 bit modes	—	-4	-5.4	LSB <sup>4</sup>	$V_{ADIN} = V_{DDA}$ 5
		• <12 bit modes	—	-1.4	-1.8		
$E_Q$	Quantization error	• 16 bit modes	—	-1 to 0	—	LSB <sup>4</sup>	
		• $\leq 13$ bit modes	—	—	$\pm 0.5$		
ENOB	Effective number of bits	16 bit differential mode					6
		• Avg=32	12.8	14.5	—	bits	
		• Avg=4	11.9	13.8	—	bits	
		16 bit single-ended mode					
• Avg=32	12.2	13.9	—	bits			
• Avg=4	11.4	13.1	—	bits			
SINAD	Signal-to-noise plus distortion	See ENOB	6.02 × ENOB + 1.76			dB	
THD	Total harmonic distortion	16 bit differential mode					7
		• Avg=32	—	-94	—	dB	
		16 bit single-ended mode					
		• Avg=32	—	-85	—	dB	

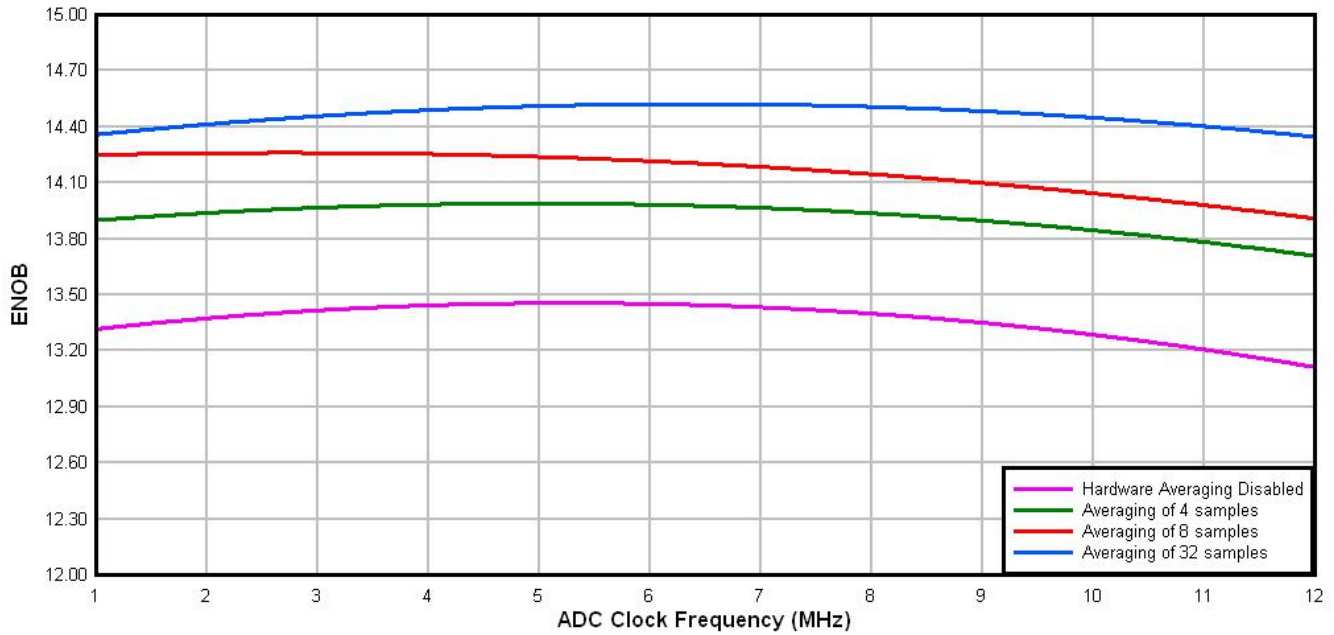
Table continues on the next page...

**Table 28. 16-bit ADC characteristics ( $V_{REFH} = V_{DDA}$ ,  $V_{REFL} = V_{SSA}$ ) (continued)**

Symbol	Description	Conditions <sup>1</sup>	Min.	Typ. <sup>2</sup>	Max.	Unit	Notes
SFDR	Spurious free dynamic range	16 bit differential mode • Avg=32	82	95	—	dB	7
		16 bit single-ended mode • Avg=32	78	90	—	dB	
E <sub>IL</sub>	Input leakage error		$I_{in} \times R_{AS}$			mV	I <sub>in</sub> = leakage current (refer to the MCU's voltage and current operating ratings)
	Temp sensor slope	−40°C to 105°C	—	1.715	—	mV/°C	
V <sub>TEMP25</sub>	Temp sensor voltage	25°C	—	719	—	mV	

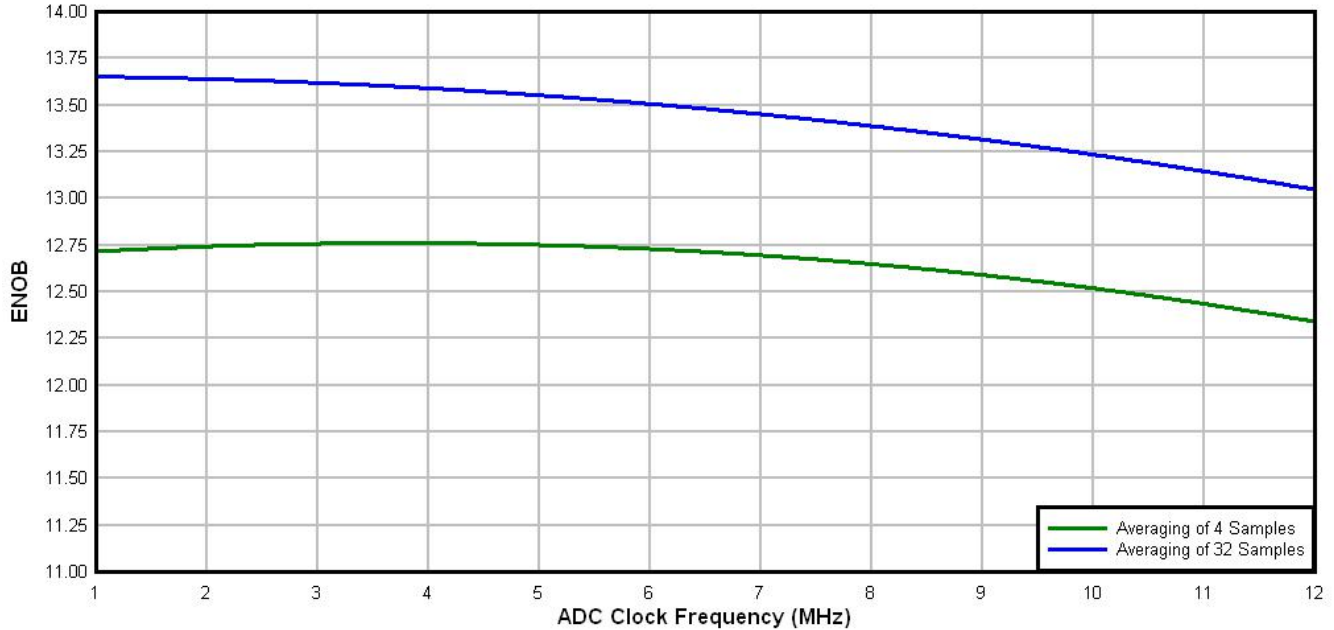
- All accuracy numbers assume the ADC is calibrated with  $V_{REFH} = V_{DDA}$
- Typical values assume  $V_{DDA} = 3.0$  V, Temp = 25°C,  $f_{ADCK} = 2.0$  MHz unless otherwise stated. Typical values are for reference only and are not tested in production.
- The ADC supply current depends on the ADC conversion clock speed, conversion rate and the ADLPC bit (low power). For lowest power operation the ADLPC bit should be set, the HSC bit should be clear with 1MHz ADC conversion clock speed.
- 1 LSB =  $(V_{REFH} - V_{REFL})/2^N$
- ADC conversion clock <16MHz, Max hardware averaging (AVGE = %1, AVGS = %11)
- Input data is 100 Hz sine wave. ADC conversion clock <12MHz.
- Input data is 1 kHz sine wave. ADC conversion clock <12MHz.

**Typical ADC 16-bit Differential ENOB vs ADC Clock**  
**100Hz, 90% FS Sine Input**



**Figure 19. Typical ENOB vs. ADC\_CLK for 16-bit differential mode**

**Typical ADC 16-bit Single-Ended ENOB vs ADC Clock**  
**100Hz, 90% FS Sine Input**



**Figure 20. Typical ENOB vs. ADC\_CLK for 16-bit single-ended mode**

**6.6.1.3 16-bit ADC with PGA operating conditions****Table 29. 16-bit ADC with PGA operating conditions**

Symbol	Description	Conditions	Min.	Typ. <sup>1</sup>	Max.	Unit	Notes
V <sub>DDA</sub>	Supply voltage	Absolute	1.71	—	3.6	V	
V <sub>REFPGA</sub>	PGA ref voltage		VREF_OUT T	VREF_OUT T	VREF_OUT T	V	2, 3
V <sub>ADIN</sub>	Input voltage		V <sub>SSA</sub>	—	V <sub>DDA</sub>	V	
V <sub>CM</sub>	Input Common Mode range		V <sub>SSA</sub>	—	V <sub>DDA</sub>	V	
R <sub>PGAD</sub>	Differential input impedance	Gain = 1, 2, 4, 8 Gain = 16, 32 Gain = 64	— — —	128 64 32	— — —	kΩ	IN+ to IN- <sup>4</sup>
R <sub>AS</sub>	Analog source resistance		—	100	—	Ω	5
T <sub>S</sub>	ADC sampling time		1.25	—	—	μs	6
C <sub>rate</sub>	ADC conversion rate	≤ 13 bit modes No ADC hardware averaging Continuous conversions enabled Peripheral clock = 50 MHz	18.484	—	450	Ksps	7
		16 bit modes No ADC hardware averaging Continuous conversions enabled Peripheral clock = 50 MHz	37.037	—	250	Ksps	8

1. Typical values assume V<sub>DDA</sub> = 3.0 V, Temp = 25°C, f<sub>ADCK</sub> = 6 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.
2. ADC must be configured to use the internal voltage reference (VREF\_OUT)
3. PGA reference is internally connected to the VREF\_OUT pin. If the user wishes to drive VREF\_OUT with a voltage other than the output of the VREF module, the VREF module must be disabled.
4. For single ended configurations the input impedance of the driven input is R<sub>PGAD</sub>/2
5. The analog source resistance (R<sub>AS</sub>), external to MCU, should be kept as minimum as possible. Increased R<sub>AS</sub> causes drop in PGA gain without affecting other performances. This is not dependent on ADC clock frequency.
6. The minimum sampling time is dependent on input signal frequency and ADC mode of operation. A minimum of 1.25μs time should be allowed for F<sub>in</sub>=4 kHz at 16-bit differential mode. Recommended ADC setting is: ADLSMP=1, ADLSTS=2 at 8 MHz ADC clock.
7. ADC clock = 18 MHz, ADLSMP = 1, ADLST = 00, ADHSC = 1
8. ADC clock = 12 MHz, ADLSMP = 1, ADLST = 01, ADHSC = 1

## 6.6.1.4 16-bit ADC with PGA characteristics

Table 30. 16-bit ADC with PGA characteristics

Symbol	Description	Conditions	Min.	Typ. <sup>1</sup>	Max.	Unit	Notes
I <sub>DDA_PGA</sub>	Supply current	Low power (ADC_PGA[PGALPb]=0)	—	420	644	μA	2
I <sub>DC_PGA</sub>	Input DC current		$\frac{2}{R_{PGAD}} \left( \frac{V_{REFPGA} \times 0.583 - V_{CM}}{\text{Gain} + 1} \right)$			A	3
		Gain =1, V <sub>REFPGA</sub> =1.2V, V <sub>CM</sub> =0.5V	—	1.54	—	μA	
		Gain =64, V <sub>REFPGA</sub> =1.2V, V <sub>CM</sub> =0.1V	—	0.57	—	μA	
G	Gain <sup>4</sup>	• PGAG=0	0.95	1	1.05		R <sub>AS</sub> < 100Ω
		• PGAG=1	1.9	2	2.1		
		• PGAG=2	3.8	4	4.2		
		• PGAG=3	7.6	8	8.4		
		• PGAG=4	15.2	16	16.6		
		• PGAG=5	30.0	31.6	33.2		
		• PGAG=6	58.8	63.3	67.8		
BW	Input signal bandwidth	• 16-bit modes	—	—	4	kHz	
		• < 16-bit modes	—	—	40	kHz	
PSRR	Power supply rejection ratio	Gain=1	—	-84	—	dB	V <sub>DDA</sub> = 3V ±100mV, f <sub>VDDA</sub> = 50Hz, 60Hz
CMRR	Common mode rejection ratio	• Gain=1	—	-84	—	dB	V <sub>CM</sub> = 500mVpp, f <sub>VCM</sub> = 50Hz, 100Hz
		• Gain=64	—	-85	—	dB	
V <sub>OFS</sub>	Input offset voltage	• Chopping disabled (ADC_PGA[PGACHPb]=1)	—	2.4	TBD	mV	Output offset = V <sub>OFS</sub> *(Gain+1)
		• Chopping enabled (ADC_PGA[PGACHPb]=0)	—	0.2	—	mV	
T <sub>GSW</sub>	Gain switching settling time		—	—	10	μs	5
dG/dT	Gain drift over temperature	• Gain=1	—	TBD	TBD	ppm/°C	0 to 50°C
		• Gain=64	—	TBD	TBD	ppm/°C	
dV <sub>OFS</sub> /dT	Offset drift over temperature	Gain=1	—	TBD	TBD	ppm/°C	0 to 50°C, ADC Averaging=32
dG/dV <sub>DDA</sub>	Gain drift over supply voltage	• Gain=1	—	TBD	TBD	%/V	V <sub>DDA</sub> from 1.71 to 3.6V
		• Gain=64	—	TBD	TBD	%/V	

Table continues on the next page...

**Table 30. 16-bit ADC with PGA characteristics (continued)**

Symbol	Description	Conditions	Min.	Typ. <sup>1</sup>	Max.	Unit	Notes
$E_{IL}$	Input leakage error	All modes	$I_{in} \times R_{AS}$			mV	$I_{in}$ = leakage current (refer to the MCU's voltage and current operating ratings)
$V_{PP,DIFF}$	Maximum differential input signal swing		$\left(\frac{(\min(V_X, V_{DDA} - V_X) - 0.2) \times 4}{Gain}\right)$ where $V_X = V_{REFPGA} \times 0.583$			V	6
SNR	Signal-to-noise ratio	• Gain=1	80	90	—	dB	16-bit differential mode, Average=32
		• Gain=64	52	66	—	dB	
THD	Total harmonic distortion	• Gain=1	85	100	—	dB	16-bit differential mode, Average=32, $f_{in}=100\text{Hz}$
		• Gain=64	49	95	—	dB	
SFDR	Spurious free dynamic range	• Gain=1	85	105	—	dB	16-bit differential mode, Average=32, $f_{in}=100\text{Hz}$
		• Gain=64	53	88	—	dB	
ENOB	Effective number of bits	• Gain=1, Average=4	11.6	13.4	—	bits	16-bit differential mode, $f_{in}=100\text{Hz}$ z
		• Gain=1, Average=8	TBD	12.7	—	bits	
		• Gain=64, Average=4	7.2	9.6	—	bits	
		• Gain=64, Average=8	TBD	8.7	—	bits	
		• Gain=1, Average=32	12.8	14.5	—	bits	
		• Gain=2, Average=32	11.0	14.3	—	bits	
		• Gain=4, Average=32	7.9	13.8	—	bits	
		• Gain=8, Average=32	7.3	13.1	—	bits	
		• Gain=16, Average=32	6.8	12.5	—	bits	
		• Gain=32, Average=32	6.8	11.5	—	bits	
• Gain=64, Average=32	7.5	10.6	—	bits			
SINAD	Signal-to-noise plus distortion ratio	See ENOB	$6.02 \times \text{ENOB} + 1.76$			dB	

1. Typical values assume  $V_{DDA} = 3.0\text{V}$ ,  $\text{Temp} = 25^\circ\text{C}$ ,  $f_{ADCK} = 6\text{MHz}$  unless otherwise stated.
2. This current is a PGA module adder, in addition to and ADC conversion currents.
3. Between  $IN+$  and  $IN-$ . The PGA draws a DC current from the input terminals. The magnitude of the DC current is a strong function of input common mode voltage ( $V_{CM}$ ) and the PGA gain.
4.  $\text{Gain} = 2^{\text{PGAG}}$
5. After changing the PGA gain setting, a minimum of 2 ADC+PGA conversions should be ignored.



6. Limit the input signal swing so that the PGA does not saturate during operation. Input signal swing is dependent on the PGA reference voltage and gain setting.

## 6.6.2 CMP and 6-bit DAC electrical specifications

**Table 31. Comparator and 6-bit DAC electrical specifications**

Symbol	Description	Min.	Typ.	Max.	Unit
$V_{DD}$	Supply voltage	1.71	—	3.6	V
$I_{DDHS}$	Supply current, High-speed mode (EN=1, PMODE=1)	—	—	200	$\mu$ A
$I_{DDL S}$	Supply current, low-speed mode (EN=1, PMODE=0)	—	—	20	$\mu$ A
$V_{AIN}$	Analog input voltage	$V_{SS} - 0.3$	—	$V_{DD}$	V
$V_{AIO}$	Analog input offset voltage	—	—	20	mV
$V_H$	Analog comparator hysteresis <sup>1</sup> <ul style="list-style-type: none"> <li>• CR0[HYSTCTR] = 00</li> <li>• CR0[HYSTCTR] = 01</li> <li>• CR0[HYSTCTR] = 10</li> <li>• CR0[HYSTCTR] = 11</li> </ul>	—	5	—	mV
		—	10	—	mV
		—	20	—	mV
		—	30	—	mV
$V_{CMPOH}$	Output high	$V_{DD} - 0.5$	—	—	V
$V_{CMPOI}$	Output low	—	—	0.5	V
$t_{DHS}$	Propagation delay, high-speed mode (EN=1, PMODE=1)	20	50	200	ns
$t_{DLS}$	Propagation delay, low-speed mode (EN=1, PMODE=0)	80	250	600	ns
	Analog comparator initialization delay <sup>2</sup>	—	—	40	$\mu$ s
$I_{DAC6b}$	6-bit DAC current adder (enabled)	—	7	—	$\mu$ A
INL	6-bit DAC integral non-linearity	-0.5	—	0.5	LSB <sup>3</sup>
DNL	6-bit DAC differential non-linearity	-0.3	—	0.3	LSB

1. Typical hysteresis is measured with input voltage range limited to 0.6 to  $V_{DD}-0.6V$ .
2. Comparator initialization delay is defined as the time between software writes to change control inputs (Writes to DACEN, VRSEL, PSEL, MSEL, VOSEL) and the comparator output settling to a stable level.
3. 1 LSB =  $V_{reference}/64$

Peripheral operating requirements and behaviors

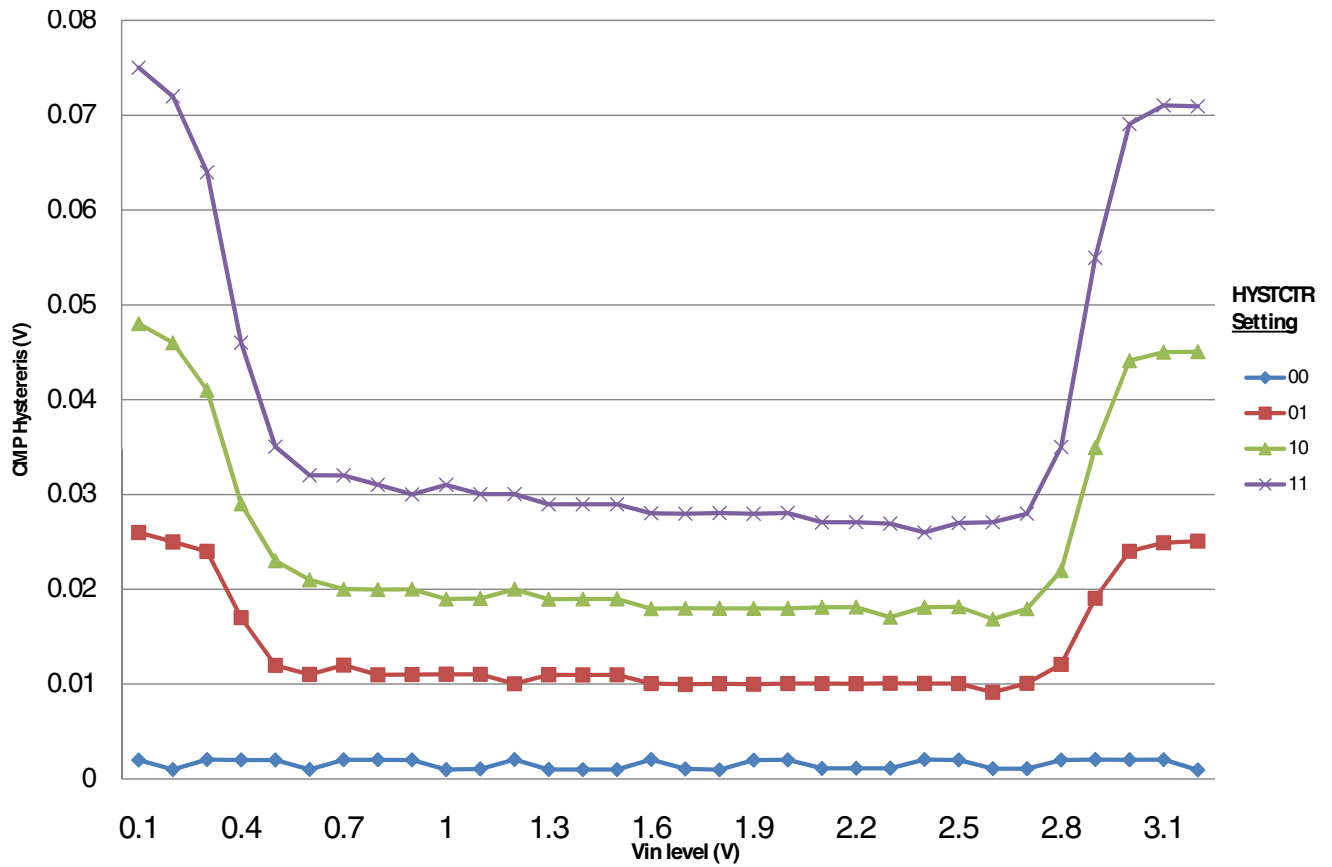


Figure 21. Typical hysteresis vs. Vin level (VDD=3.3V, PMODE=0)



Figure 22. Typical hysteresis vs. Vin level (VDD=3.3V, PMODE=1)

## 6.6.3 12-bit DAC electrical characteristics

### 6.6.3.1 12-bit DAC operating requirements

Table 32. 12-bit DAC operating requirements

Symbol	Description	Min.	Max.	Unit	Notes
$V_{DDA}$	Supply voltage	1.71	3.6	V	
$V_{DACR}$	Reference voltage	1.13	3.6	V	1
$T_A$	Temperature	-40	105	°C	
$C_L$	Output load capacitance	—	100	pF	2
$I_L$	Output load current	—	1	mA	

1. The DAC reference can be selected to be VDDA or the voltage output of the VREF module (VREF\_OUT)
2. A small load capacitance (47 pF) can improve the bandwidth performance of the DAC

## 6.6.3.2 12-bit DAC operating behaviors

Table 33. 12-bit DAC operating behaviors

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
$I_{DDA\_DACL\_P}$	Supply current — low-power mode	—	—	150	$\mu\text{A}$	
$I_{DDA\_DAC\_HP}$	Supply current — high-speed mode	—	—	700	$\mu\text{A}$	
$t_{DACLP}$	Full-scale settling time (0x080 to 0xF7F) — low-power mode	—	100	200	$\mu\text{s}$	1
$t_{DACHP}$	Full-scale settling time (0x080 to 0xF7F) — high-power mode	—	15	30	$\mu\text{s}$	1
$t_{CCDACLP}$	Code-to-code settling time (0xBF8 to 0xC08) — low-power mode and high-speed mode	—	0.7	1	$\mu\text{s}$	1
$V_{dacoutl}$	DAC output voltage range low — high-speed mode, no load, DAC set to 0x000	—	—	100	mV	
$V_{dacouth}$	DAC output voltage range high — high-speed mode, no load, DAC set to 0xFFF	$V_{DACR} - 100$	—	$V_{DACR}$	mV	
INL	Integral non-linearity error — high speed mode	—	—	$\pm 8$	LSB	2
DNL	Differential non-linearity error — $V_{DACR} > 2\text{ V}$	—	—	$\pm 1$	LSB	3
DNL	Differential non-linearity error — $V_{DACR} = V_{REF\_OUT}$	—	—	$\pm 1$	LSB	4
$V_{OFFSET}$	Offset error	—	$\pm 0.4$	$\pm 0.8$	%FSR	5
$E_G$	Gain error	—	$\pm 0.1$	$\pm 0.6$	%FSR	5
PSRR	Power supply rejection ratio, $V_{DDA} > = 2.4\text{ V}$	60	—	90	dB	
$T_{CO}$	Temperature coefficient offset voltage	—	3.7	—	$\mu\text{V}/\text{C}$	6
$T_{GE}$	Temperature coefficient gain error	—	0.000421	—	%FSR/C	
$R_{op}$	Output resistance load = 3 k $\Omega$	—	—	250	$\Omega$	
SR	Slew rate -80h → F7Fh → 80h <ul style="list-style-type: none"> <li>High power (<math>SP_{HP}</math>)</li> <li>Low power (<math>SP_{LP}</math>)</li> </ul>	1.2 0.05	1.7 0.12	— —	V/ $\mu\text{s}$	
CT	Channel to channel cross talk	—	—	-80	dB	
BW	3dB bandwidth <ul style="list-style-type: none"> <li>High power (<math>SP_{HP}</math>)</li> <li>Low power (<math>SP_{LP}</math>)</li> </ul>	550 40	— —	— —	kHz	

1. Settling within  $\pm 1$  LSB
2. The INL is measured for 0+100mV to  $V_{DACR} - 100\text{ mV}$
3. The DNL is measured for 0+100 mV to  $V_{DACR} - 100\text{ mV}$
4. The DNL is measured for 0+100mV to  $V_{DACR} - 100\text{ mV}$  with  $V_{DDA} > 2.4\text{V}$
5. Calculated by a best fit curve from  $V_{SS} + 100\text{ mV}$  to  $V_{DACR} - 100\text{ mV}$

6. VDDA = 3.0V, reference select set for VDDA (DACx\_CO:DACRFS = 1), high power mode(DACx\_C0:LPEN = 0), DAC set to 0x800, Temp range from -40C to 105C

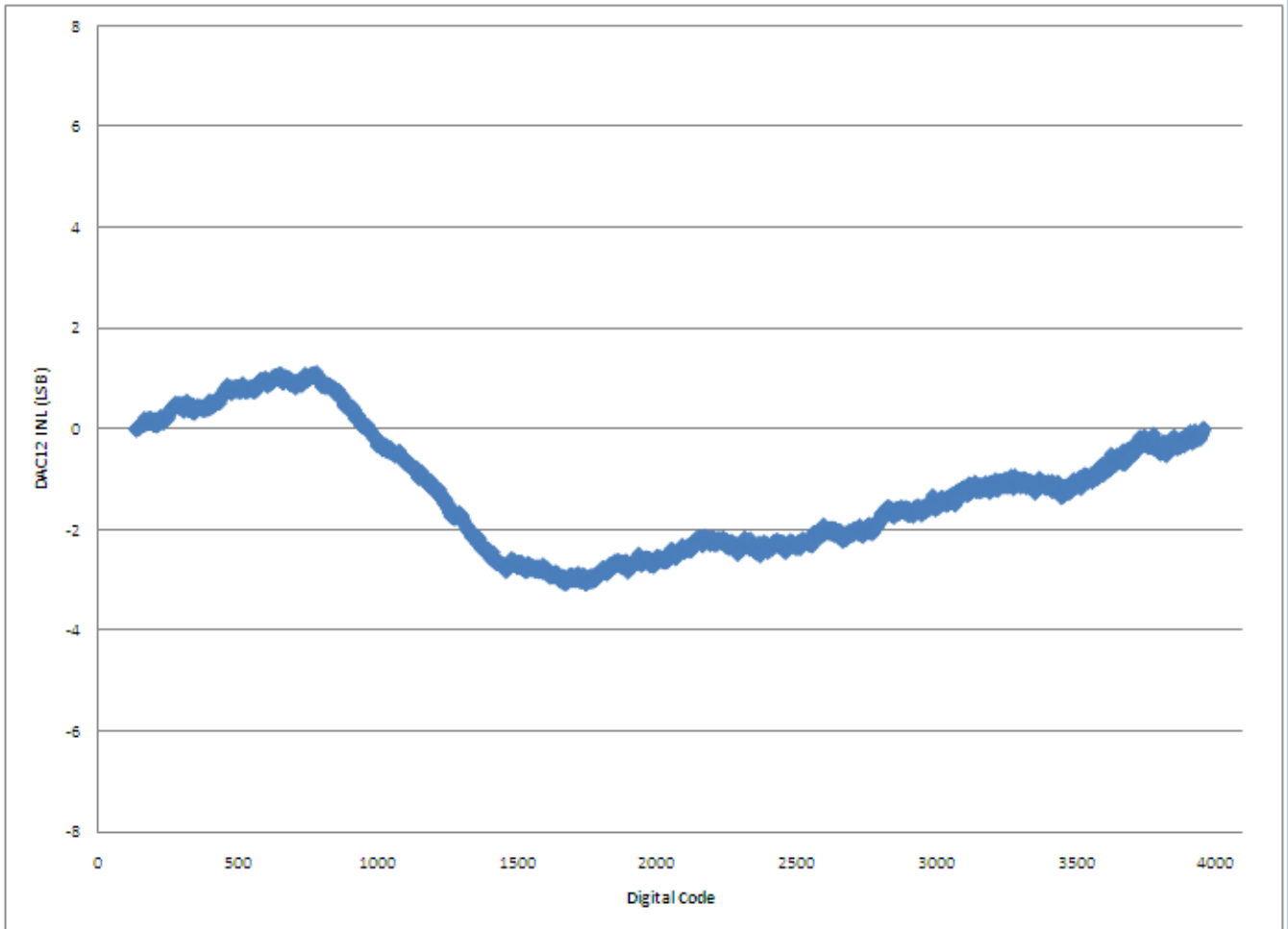


Figure 23. Typical INL error vs. digital code

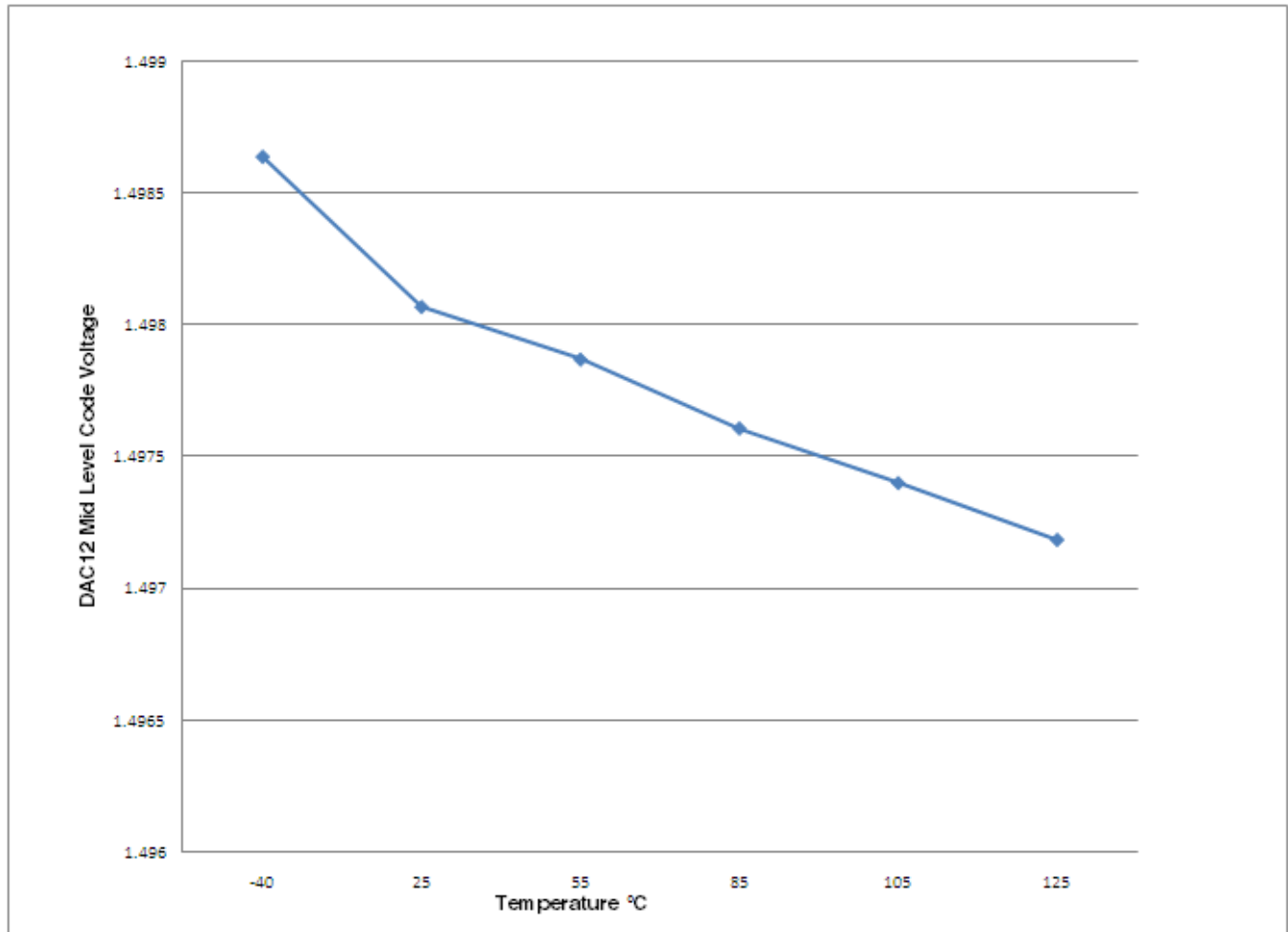


Figure 24. Offset at half scale vs. temperature

## 6.6.4 Voltage reference electrical specifications

Table 34. VREF full-range operating requirements

Symbol	Description	Min.	Max.	Unit	Notes
$V_{DDA}$	Supply voltage	1.71	3.6	V	
$T_A$	Temperature	-40	105	°C	
$C_L$	Output load capacitance	100		nF	1, 2

- $C_L$  must be connected to VREF\_OUT if the VREF\_OUT functionality is being used for either an internal or external reference.
- The load capacitance should not exceed +/-25% of the nominal specified  $C_L$  value over the operating temperature range of the device.

**Table 35. VREF full-range operating behaviors**

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
$V_{out}$	Voltage reference output with factory trim at nominal $V_{DDA}$ and temperature=25C	1.1965	1.2	1.2027	V	
$V_{out}$	Voltage reference output with— factory trim	1.1584	—	1.2376	V	
$V_{out}$	Voltage reference output — user trim	1.198	—	1.202	V	
$V_{step}$	Voltage reference trim step	—	0.5	—	mV	
$V_{tdrift}$	Temperature drift ( $V_{max} - V_{min}$ across the full temperature range)	—	—	80	mV	
$I_{bg}$	Bandgap only current	—	—	80	$\mu$ A	1
$I_{tr}$	High-power buffer current	—	—	TBD	mA	1
$\Delta V_{LOAD}$	Load regulation <ul style="list-style-type: none"> <li>current = + 1.0 mA</li> <li>current = - 1.0 mA</li> </ul>	—	2	—	mV	1, 2
$T_{stup}$	Buffer startup time	—	—	100	$\mu$ s	
$V_{vdrift}$	Voltage drift ( $V_{max} - V_{min}$ across the full voltage range)	—	2	—	mV	1

1. See the chip's Reference Manual for the appropriate settings of the VREF Status and Control register.
2. Load regulation voltage is the difference between the VREF\_OUT voltage with no load vs. voltage with defined load

**Table 36. VREF limited-range operating requirements**

Symbol	Description	Min.	Max.	Unit	Notes
$T_A$	Temperature	0	50	$^{\circ}$ C	

**Table 37. VREF limited-range operating behaviors**

Symbol	Description	Min.	Max.	Unit	Notes
$V_{out}$	Voltage reference output with factory trim	1.173	1.225	V	

## 6.7 Timers

See [General switching specifications](#).

## 6.8 Communication interfaces

## 6.8.1 CAN switching specifications

See [General switching specifications](#).

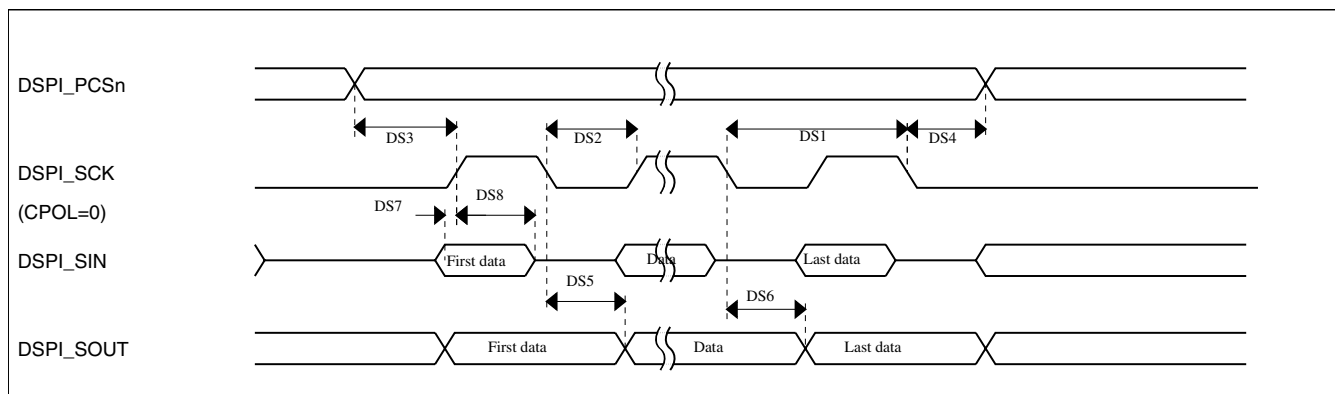
## 6.8.2 DSPI switching specifications (limited voltage range)

The DMA Serial Peripheral Interface (DSPI) provides a synchronous serial bus with master and slave operations. Many of the transfer attributes are programmable. The tables below provide DSPI timing characteristics for classic SPI timing modes. Refer to the DSPI chapter of the Reference Manual for information on the modified transfer formats used for communicating with slower peripheral devices.

**Table 38. Master mode DSPI timing (limited voltage range)**

Num	Description	Min.	Max.	Unit	Notes
	Operating voltage	2.7	3.6	V	
	Frequency of operation	—	30	MHz	
DS1	DSPI_SCK output cycle time	$2 \times t_{\text{BUS}}$	—	ns	
DS2	DSPI_SCK output high/low time	$(t_{\text{SCK}}/2) - 2$	$(t_{\text{SCK}}/2) + 2$	ns	
DS3	DSPI_PCS $n$ valid to DSPI_SCK delay	$(t_{\text{BUS}} \times 2) - 2$	—	ns	1
DS4	DSPI_SCK to DSPI_PCS $n$ invalid delay	$(t_{\text{BUS}} \times 2) - 2$	—	ns	2
DS5	DSPI_SCK to DSPI_SOUT valid	—	8.5	ns	
DS6	DSPI_SCK to DSPI_SOUT invalid	-2	—	ns	
DS7	DSPI_SIN to DSPI_SCK input setup	15	—	ns	
DS8	DSPI_SCK to DSPI_SIN input hold	0	—	ns	

1. The delay is programmable in SPI $x$ \_CTAR $n$ [PSSCK] and SPI $x$ \_CTAR $n$ [CSSCK].
2. The delay is programmable in SPI $x$ \_CTAR $n$ [PASC] and SPI $x$ \_CTAR $n$ [ASC].

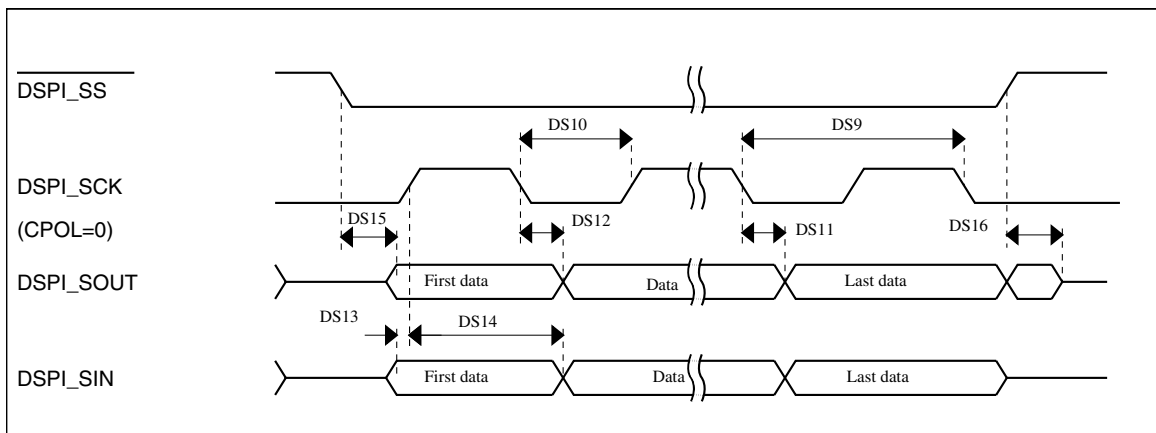


**Figure 25. DSPI classic SPI timing — master mode**



**Table 39. Slave mode DSPI timing (limited voltage range)**

Num	Description	Min.	Max.	Unit
	Operating voltage	2.7	3.6	V
	Frequency of operation		15	MHz
DS9	DSPI_SCK input cycle time	$4 \times t_{\text{BUS}}$	—	ns
DS10	DSPI_SCK input high/low time	$(t_{\text{SCK}}/2) - 2$	$(t_{\text{SCK}}/2) + 2$	ns
DS11	DSPI_SCK to DSPI_SOUT valid	—	10	ns
DS12	DSPI_SCK to DSPI_SOUT invalid	0	—	ns
DS13	DSPI_SIN to DSPI_SCK input setup	2	—	ns
DS14	DSPI_SCK to DSPI_SIN input hold	7	—	ns
DS15	$\overline{\text{DSPI\_SS}}$ active to DSPI_SOUT driven	—	14	ns
DS16	$\overline{\text{DSPI\_SS}}$ inactive to DSPI_SOUT not driven	—	14	ns

**Figure 26. DSPI classic SPI timing — slave mode**

### 6.8.3 DSPI switching specifications (full voltage range)

The DMA Serial Peripheral Interface (DSPI) provides a synchronous serial bus with master and slave operations. Many of the transfer attributes are programmable. The tables below provides DSPI timing characteristics for classic SPI timing modes. Refer to the DSPI chapter of the Reference Manual for information on the modified transfer formats used for communicating with slower peripheral devices.

**Table 40. Master mode DSPI timing (full voltage range)**

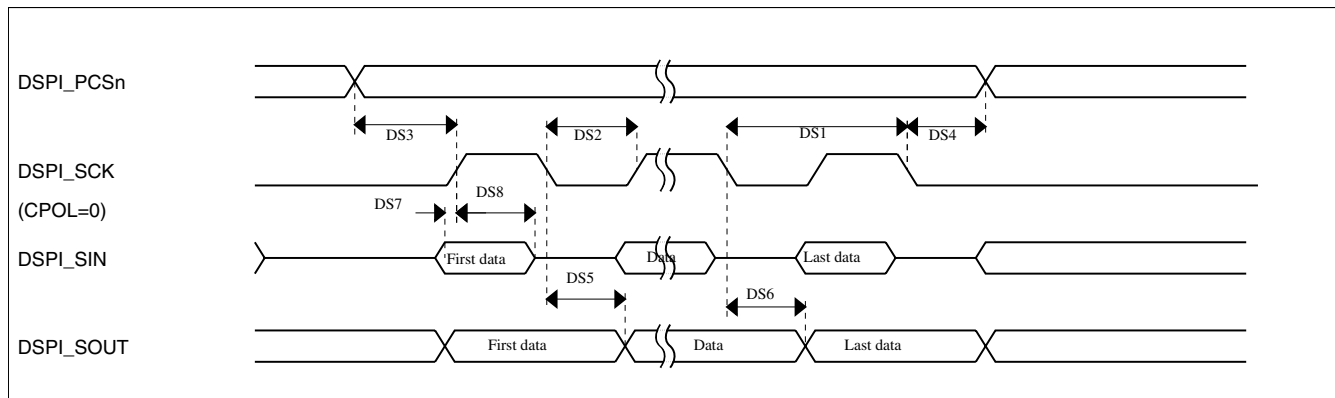
Num	Description	Min.	Max.	Unit	Notes
	Operating voltage	1.71	3.6	V	1
	Frequency of operation	—	15	MHz	

Table continues on the next page...

**Table 40. Master mode DSPI timing (full voltage range) (continued)**

Num	Description	Min.	Max.	Unit	Notes
DS1	DSPI_SCK output cycle time	$4 \times t_{BUS}$	—	ns	
DS2	DSPI_SCK output high/low time	$(t_{SCK}/2) - 4$	$(t_{SCK}/2) + 4$	ns	
DS3	DSPI_PCSn valid to DSPI_SCK delay	$(t_{BUS} \times 2) - 4$	—	ns	2
DS4	DSPI_SCK to DSPI_PCSn invalid delay	$(t_{BUS} \times 2) - 4$	—	ns	3
DS5	DSPI_SCK to DSPI_SOUT valid	—	10	ns	
DS6	DSPI_SCK to DSPI_SOUT invalid	-4.5	—	ns	
DS7	DSPI_SIN to DSPI_SCK input setup	20.5	—	ns	
DS8	DSPI_SCK to DSPI_SIN input hold	0	—	ns	

1. The DSPI module can operate across the entire operating voltage for the processor, but to run across the full voltage range the maximum frequency of operation is reduced.
2. The delay is programmable in SPIx\_CTARn[PSSCK] and SPIx\_CTARn[CSSCK].
3. The delay is programmable in SPIx\_CTARn[PASC] and SPIx\_CTARn[ASC].



**Figure 27. DSPI classic SPI timing — master mode**

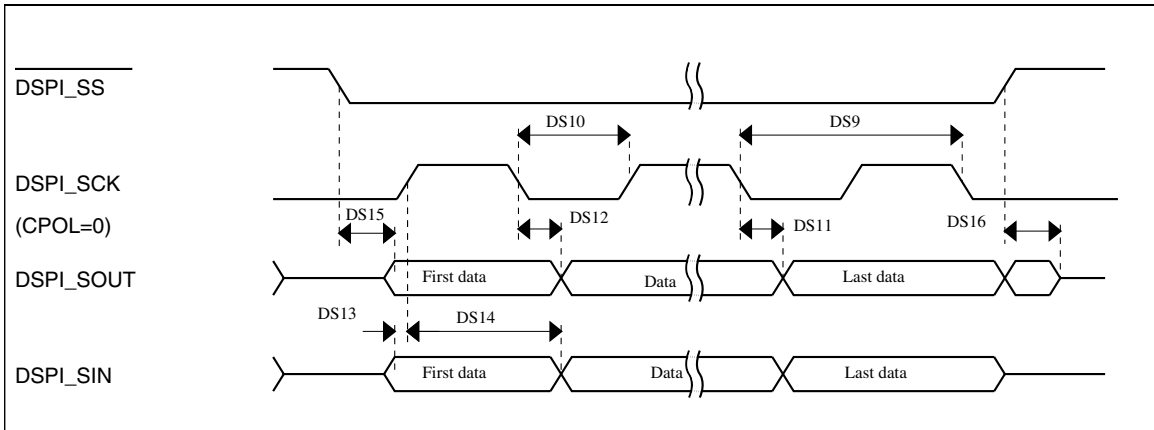
**Table 41. Slave mode DSPI timing (full voltage range)**

Num	Description	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
	Frequency of operation	—	7.5	MHz
DS9	DSPI_SCK input cycle time	$8 \times t_{BUS}$	—	ns
DS10	DSPI_SCK input high/low time	$(t_{SCK}/2) - 4$	$(t_{SCK}/2) + 4$	ns
DS11	DSPI_SCK to DSPI_SOUT valid	—	20	ns
DS12	DSPI_SCK to DSPI_SOUT invalid	0	—	ns
DS13	DSPI_SIN to DSPI_SCK input setup	2	—	ns
DS14	DSPI_SCK to DSPI_SIN input hold	7	—	ns
DS15	DSPI_SS active to DSPI_SOUT driven	—	19	ns

Table continues on the next page...

**Table 41. Slave mode DSPI timing (full voltage range) (continued)**

Num	Description	Min.	Max.	Unit
DS16	$\overline{\text{DSPI\_SS}}$ inactive to DSPI_SOUT not driven	—	19	ns

**Figure 28. DSPI classic SPI timing — slave mode**

## 6.8.4 I<sup>2</sup>C switching specifications

See [General switching specifications](#).

## 6.8.5 UART switching specifications

See [General switching specifications](#).

## 6.8.6 SDHC specifications

The following timing specs are defined at the chip I/O pin and must be translated appropriately to arrive at timing specs/constraints for the physical interface.

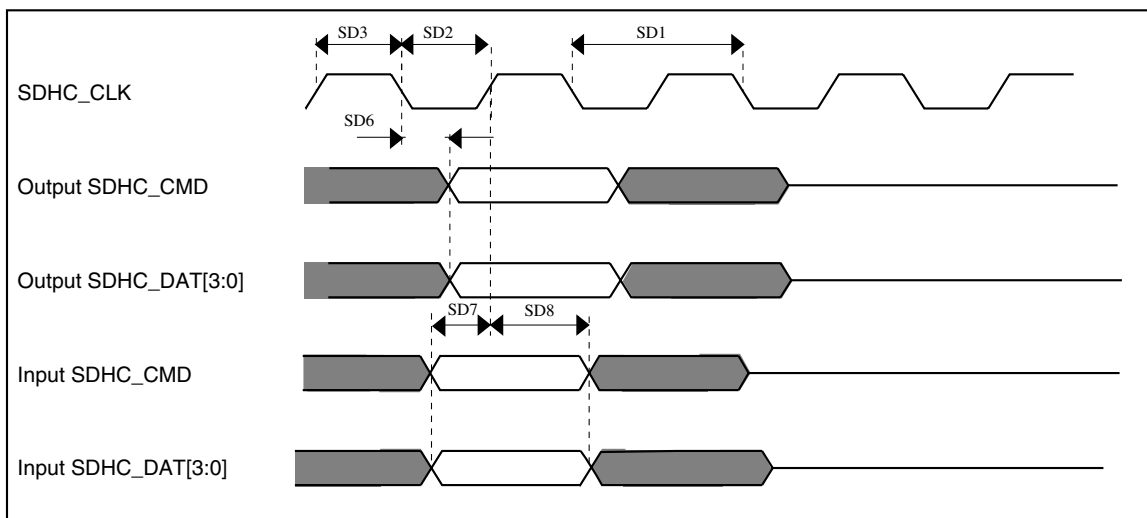
**Table 42. SDHC switching specifications**

Num	Symbol	Description	Min.	Max.	Unit
		Operating voltage	2.7	3.6	V
<b>Card input clock</b>					

*Table continues on the next page...*

**Table 42. SDHC switching specifications (continued)**

Num	Symbol	Description	Min.	Max.	Unit
SD1	f <sub>pp</sub>	Clock frequency (low speed)	0	400	kHz
	f <sub>pp</sub>	Clock frequency (SD\SDIO full speed)	0	25	MHz
	f <sub>pp</sub>	Clock frequency (MMC full speed)	0	20	MHz
	f <sub>OD</sub>	Clock frequency (identification mode)	0	400	kHz
SD2	t <sub>WL</sub>	Clock low time	7	—	ns
SD3	t <sub>WH</sub>	Clock high time	7	—	ns
SD4	t <sub>TLH</sub>	Clock rise time	—	3	ns
SD5	t <sub>THL</sub>	Clock fall time	—	3	ns
<b>SDHC output / card inputs SDHC_CMD, SDHC_DAT (reference to SDHC_CLK)</b>					
SD6	t <sub>OD</sub>	SDHC output delay (output valid)	-5	6.5	ns
<b>SDHC input / card inputs SDHC_CMD, SDHC_DAT (reference to SDHC_CLK)</b>					
SD7	t <sub>ISU</sub>	SDHC input setup time	5	—	ns
SD8	t <sub>IH</sub>	SDHC input hold time	0	—	ns



**Figure 29. SDHC timing**

### 6.8.7 I2S/SAI Switching Specifications

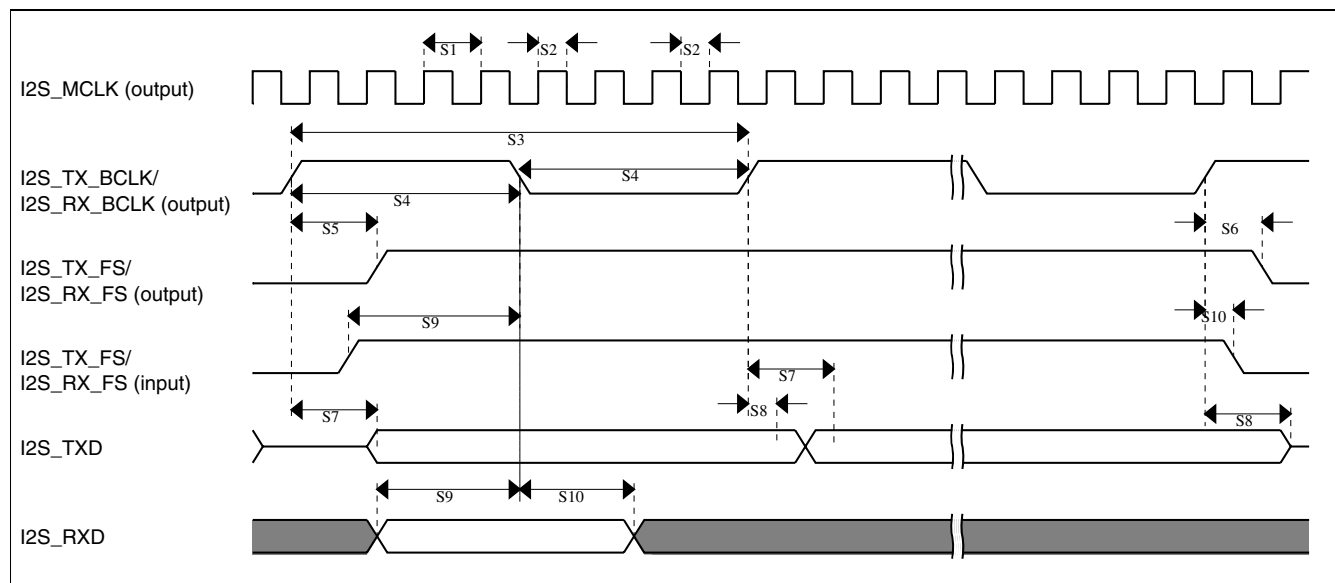
This section provides the AC timing for the I2S/SAI module in master mode (clocks are driven) and slave mode (clocks are input). All timing is given for noninverted serial clock polarity (TCR2[BCP] is 0, RCR2[BCP] is 0) and a noninverted frame sync (TCR4[FSP]

is 0, RCR4[FSP] is 0). If the polarity of the clock and/or the frame sync have been inverted, all the timing remains valid by inverting the bit clock signal (BCLK) and/or the frame sync (FS) signal shown in the following figures.

**Table 43. I2S/SAI master mode timing**

Num.	Characteristic	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
S1	I2S_MCLK cycle time <sup>1</sup>	40		ns
S2	I2S_MCLK pulse width high/low	45%	55%	MCLK period
S3	I2S_TX_BCLK cycle time (output) <sup>1</sup>	80	—	ns
	I2S_RX_BCLK cycle time (output) <sup>1</sup>	160	—	
S4	I2S_TX_BCLK pulse width high/low	45%	55%	BCLK period
S5	I2S_TX_BCLK/I2S_RX_BCLK to I2S_TX_FS/ I2S_RX_FS output valid	—	15	ns
S6	I2S_TX_BCLK/I2S_RX_BCLK to I2S_TX_FS/ I2S_RX_FS output invalid	0	—	ns
S7	I2S_TX_BCLK to I2S_TXD valid	—	15	ns
S8	I2S_TX_BCLK to I2S_TXD invalid	0	—	ns
S9	I2S_RXD/I2S_RX_FS input setup before I2S_RX_BCLK	25	—	ns
S10	I2S_RXD/I2S_RX_FS input hold after I2S_RX_BCLK	0	—	ns
S11	I2S_TX_FS input assertion to I2S_TXD output valid <sup>2</sup>	—	21	ns

1. This parameter is limited in VLPx modes.
2. Applies to first bit in each frame and only if the TCR4[FSE] bit is clear

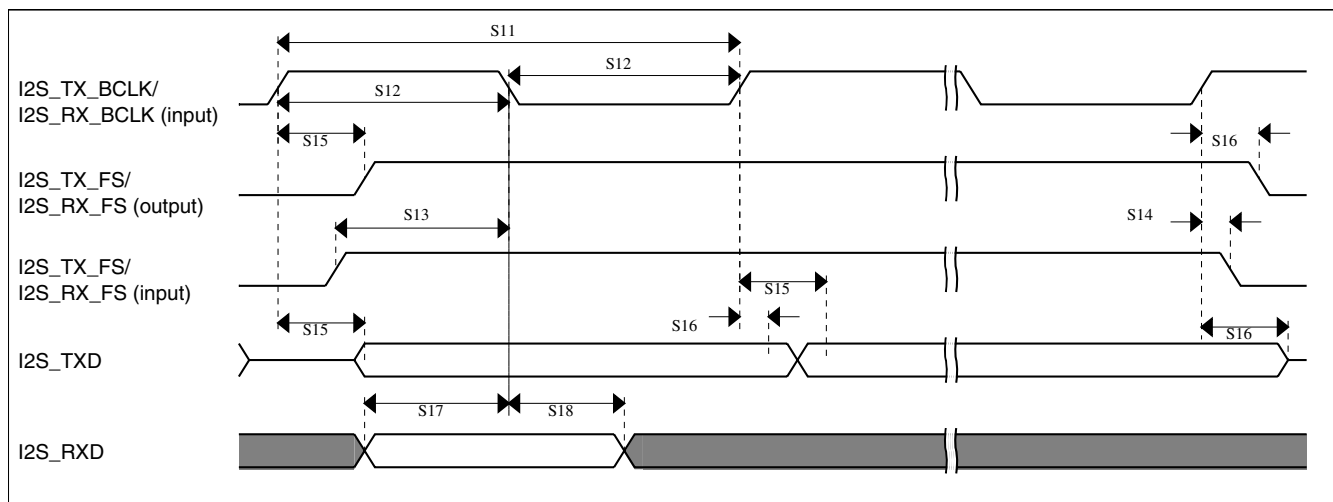


**Figure 30. I2S/SAI timing — master modes**

**Table 44. I2S/SAI slave mode timing**

Num.	Characteristic	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
S11	I2S_RX_BCLK cycle time (input) I2S_TX_BCLK cycle time (input)	80	—	ns
S12	I2S_TX_BCLK/I2S_RX_BCLK pulse width high/low (input)	45%	55%	MCLK period
S13	I2S_TX_FS/I2S_RX_FS input setup before I2S_TX_BCLK/I2S_RX_BCLK	10	—	ns
S14	I2S_TX_FS/I2S_RX_FS input hold after I2S_TX_BCLK/I2S_RX_BCLK	2	—	ns
S15	I2S_TX_BCLK to I2S_TXD/I2S_TX_FS output valid	—	29	ns
S16	I2S_TX_BCLK to I2S_TXD/I2S_TX_FS output invalid	0	—	ns
S17	I2S_RXD setup before I2S_RX_BCLK	10	—	ns
S18	I2S_RXD hold after I2S_RX_BCLK	2	—	ns
S19	I2S_TX_FS input assertion to I2S_TXD output valid <sup>1</sup>	—	21	ns

1. Applies to first bit in each frame and only if the TCR4[FSE] bit is clear



**Figure 31. I2S/SAI timing — slave modes**

## 6.9 Human-machine interfaces (HMI)

## 6.9.1 TSI electrical specifications

**Table 45. TSI electrical specifications**

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V <sub>DDTSI</sub>	Operating voltage	1.71	—	3.6	V	
C <sub>ELE</sub>	Target electrode capacitance range	1	20	500	pF	1
f <sub>REFmax</sub>	Reference oscillator frequency	—	8	TBD	MHz	2
f <sub>ELEmax</sub>	Electrode oscillator frequency	—	0.5	TBD	MHz	2
C <sub>REF</sub>	Internal reference capacitor	TBD	1	TBD	pF	
V <sub>DELTA</sub>	Oscillator delta voltage	TBD	600	TBD	mV	2
I <sub>REF</sub>	Reference oscillator current source base current <ul style="list-style-type: none"> <li>• 1uA setting (REFCHRG=0)</li> <li>• 32uA setting (REFCHRG=31)</li> </ul>	—	1.133	1.5	μA	2, 3
I <sub>ELE</sub>	Electrode oscillator current source base current <ul style="list-style-type: none"> <li>• 1uA setting (EXTCHRG=0)</li> <li>• 32uA setting (EXTCHRG=31)</li> </ul>	—	1.133	1.5	μA	2, 4
Pres5	Electrode capacitance measurement precision	—	8.3333	38.4	pF/count	5
Pres20	Electrode capacitance measurement precision	—	8.3333	38.4	pF/count	6
Pres100	Electrode capacitance measurement precision	—	8.3333	38.4	pF/count	7
MaxSens	Maximum sensitivity	0.003	12.5	—	fF/count	8
Res	Resolution	—	—	16	bits	
T <sub>Con20</sub>	Response time @ 20 pF	8	15	25	μs	9
I <sub>TSI_RUN</sub>	Current added in run mode	—	55	—	μA	
I <sub>TSI_LP</sub>	Low power mode current adder	—	1.3	TBD	μA	10

1. The TSI module is functional with capacitance values outside this range. However, optimal performance is not guaranteed.
2. Fixed external capacitance of 20 pF.
3. The programmable current source value is generated by multiplying the SCANC[REFCHRG] value and the base current.
4. The programmable current source value is generated by multiplying the SCANC[EXTCHRG] value and the base current.
5. Measured with a 5 pF electrode, reference oscillator frequency of 10 MHz, PS = 128, NSCN = 8; I<sub>ext</sub> = 16.
6. Measured with a 20 pF electrode, reference oscillator frequency of 10 MHz, PS = 128, NSCN = 2; I<sub>ext</sub> = 16.
7. Measured with a 20 pF electrode, reference oscillator frequency of 10 MHz, PS = 16, NSCN = 3; I<sub>ext</sub> = 16.
8. Sensitivity defines the minimum capacitance change when a single count from the TSI module changes, it is equal to (C<sub>ref</sub> \* I<sub>ext</sub>) / (I<sub>ref</sub> \* PS \* NSCN). Sensitivity depends on the configuration used. The typical value listed is based on the following configuration: I<sub>ext</sub> = 5 μA, EXTCHRG = 4, PS = 128, NSCN = 2, I<sub>ref</sub> = 16 μA, REFCHRG = 15, C<sub>ref</sub> = 1.0 pF. The minimum sensitivity describes the smallest possible capacitance that can be measured by a single count (this is the best sensitivity but is described as a minimum because it's the smallest number). The minimum sensitivity parameter is based on the following configuration: I<sub>ext</sub> = 1 μA, EXTCHRG = 0, PS = 128, NSCN = 32, I<sub>ref</sub> = 32 μA, REFCHRG = 31, C<sub>ref</sub> = 0.5 pF
9. Time to do one complete measurement of the electrode. Sensitivity resolution of 0.0133 pF, PS = 0, NSCN = 0, 1 electrode, EXTCHRG = 15.
10. REFCHRG=0, EXTCHRG=4, PS=7, NSCN=0F, LPSCNITV=F, LPO is selected (1 kHz), and fixed external capacitance of 20 pF. Data is captured with an average of 7 periods window.

## 7 Dimensions

## 7.1 Obtaining package dimensions

Package dimensions are provided in package drawings.

To find a package drawing, go to <http://www.freescale.com> and perform a keyword search for the drawing's document number:

If you want the drawing for this package	Then use this document number
144-pin LQFP	98ASS23177W
144-pin MAPBGA	98ASA00222D

## 8 Pinout

### 8.1 K10 Signal Multiplexing and Pin Assignments

The following table shows the signals available on each pin and the locations of these pins on the devices supported by this document. The Port Control Module is responsible for selecting which ALT functionality is available on each pin.

144 LQFP	144 MAPBGA	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EzPort
—	L5	RTC_WAKEUP_B	RTC_WAKEUP_B	RTC_WAKEUP_B								
—	M5	NC	NC	NC								
—	A10	NC	NC	NC								
—	B10	NC	NC	NC								
—	C10	NC	NC	NC								
1	D3	PTE0	ADC1_SE4a	ADC1_SE4a	PTE0	SPI1_PCS1	UART1_TX	SDHC0_D1		I2C1_SDA	RTC_CLKOUT	
2	D2	PTE1/LLWU_P0	ADC1_SE5a	ADC1_SE5a	PTE1/LLWU_P0	SPI1_SOUT	UART1_RX	SDHC0_D0		I2C1_SCL	SPI1_SIN	
3	D1	PTE2/LLWU_P1	ADC1_SE6a	ADC1_SE6a	PTE2/LLWU_P1	SPI1_SCK	UART1_CTS_b	SDHC0_DCLK				
4	E4	PTE3	ADC1_SE7a	ADC1_SE7a	PTE3	SPI1_SIN	UART1_RTS_b	SDHC0_CMD			SPI1_SOUT	
5	E5	VDD	VDD	VDD								
6	F6	VSS	VSS	VSS								
7	E3	PTE4/LLWU_P2	DISABLED		PTE4/LLWU_P2	SPI1_PCS0	UART3_TX	SDHC0_D3				
8	E2	PTE5	DISABLED		PTE5	SPI1_PCS2	UART3_RX	SDHC0_D2		FTM3_CH0		



144 LQFP	144 MAP BGA	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EzPort
9	E1	PTE6	DISABLED		PTE6	SPI1_PCS3	UART3_CTS_b	I2S0_MCLK		FTM3_CH1		
10	F4	PTE7	DISABLED		PTE7		UART3_RTS_b	I2S0_RXD0		FTM3_CH2		
11	F3	PTE8	ADC2_SE16	ADC2_SE16	PTE8	I2S0_RXD1	UART5_TX	I2S0_RX_FS		FTM3_CH3		
12	F2	PTE9	ADC2_SE17	ADC2_SE17	PTE9	I2S0_TXD1	UART5_RX	I2S0_RX_BCLK		FTM3_CH4		
13	F1	PTE10	DISABLED		PTE10		UART5_CTS_b	I2S0_TXD0		FTM3_CH5		
14	G4	PTE11	ADC3_SE16	ADC3_SE16	PTE11		UART5_RTS_b	I2S0_TX_FS		FTM3_CH6		
15	G3	PTE12	ADC3_SE17	ADC3_SE17	PTE12			I2S0_TX_BCLK		FTM3_CH7		
16	E6	VDD	VDD	VDD								
17	F7	VSS	VSS	VSS								
18	H1	PTE16	ADC0_SE4a	ADC0_SE4a	PTE16	SPI0_PCS0	UART2_TX	FTM_CLKIN0		FTM0_FLT3		
19	H2	PTE17	ADC0_SE5a	ADC0_SE5a	PTE17	SPI0_SCK	UART2_RX	FTM_CLKIN1		LPTMR0_ALT3		
20	G1	PTE18	ADC0_SE6a	ADC0_SE6a	PTE18	SPI0_SOUT	UART2_CTS_b	I2C0_SDA				
21	G2	PTE19	ADC0_SE7a	ADC0_SE7a	PTE19	SPI0_SIN	UART2_RTS_b	I2C0_SCL		CMP3_OUT		
22	H3	VSS	VSS	VSS								
23	J1	PGA2_DP/ ADC2_DP0/ ADC3_DP3/ ADC0_DP1	PGA2_DP/ ADC2_DP0/ ADC3_DP3/ ADC0_DP1	PGA2_DP/ ADC2_DP0/ ADC3_DP3/ ADC0_DP1								
24	J2	PGA2_DM/ ADC2_DM0/ ADC3_DM3/ ADC0_DM1	PGA2_DM/ ADC2_DM0/ ADC3_DM3/ ADC0_DM1	PGA2_DM/ ADC2_DM0/ ADC3_DM3/ ADC0_DM1								
25	K1	PGA3_DP/ ADC3_DP0/ ADC2_DP3/ ADC1_DP1	PGA3_DP/ ADC3_DP0/ ADC2_DP3/ ADC1_DP1	PGA3_DP/ ADC3_DP0/ ADC2_DP3/ ADC1_DP1								
26	K2	PGA3_DM/ ADC3_DM0/ ADC2_DM3/ ADC1_DM1	PGA3_DM/ ADC3_DM0/ ADC2_DM3/ ADC1_DM1	PGA3_DM/ ADC3_DM0/ ADC2_DM3/ ADC1_DM1								
27	L1	PGA0_DP/ ADC0_DP0/ ADC1_DP3	PGA0_DP/ ADC0_DP0/ ADC1_DP3	PGA0_DP/ ADC0_DP0/ ADC1_DP3								
28	L2	PGA0_DM/ ADC0_DM0/ ADC1_DM3	PGA0_DM/ ADC0_DM0/ ADC1_DM3	PGA0_DM/ ADC0_DM0/ ADC1_DM3								

## Pinout

144 LQFP	144 MAP BGA	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EzPort
29	M1	PGA1_DP/ ADC1_DP0/ ADC0_DP3	PGA1_DP/ ADC1_DP0/ ADC0_DP3	PGA1_DP/ ADC1_DP0/ ADC0_DP3								
30	M2	PGA1_DM/ ADC1_DM0/ ADC0_DM3	PGA1_DM/ ADC1_DM0/ ADC0_DM3	PGA1_DM/ ADC1_DM0/ ADC0_DM3								
31	H5	VDDA	VDDA	VDDA								
32	G5	VREFH	VREFH	VREFH								
33	G6	VREFL	VREFL	VREFL								
34	H6	VSSA	VSSA	VSSA								
35	K3	ADC1_SE1 6/ CMP2_IN2/ ADC0_SE2 2	ADC1_SE1 6/ CMP2_IN2/ ADC0_SE2 2	ADC1_SE1 6/ CMP2_IN2/ ADC0_SE2 2								
36	J3	ADC0_SE1 6/ CMP1_IN2/ ADC0_SE2 1	ADC0_SE1 6/ CMP1_IN2/ ADC0_SE2 1	ADC0_SE1 6/ CMP1_IN2/ ADC0_SE2 1								
37	M3	VREF_OUT/ CMP1_IN5/ CMP0_IN5/ ADC1_SE1 8	VREF_OUT/ CMP1_IN5/ CMP0_IN5/ ADC1_SE1 8	VREF_OUT/ CMP1_IN5/ CMP0_IN5/ ADC1_SE1 8								
38	L3	DAC0_OUT/ CMP1_IN3/ ADC0_SE2 3	DAC0_OUT/ CMP1_IN3/ ADC0_SE2 3	DAC0_OUT/ CMP1_IN3/ ADC0_SE2 3								
39	L4	DAC1_OUT/ CMP0_IN4/ CMP2_IN3/ ADC1_SE2 3	DAC1_OUT/ CMP0_IN4/ CMP2_IN3/ ADC1_SE2 3	DAC1_OUT/ CMP0_IN4/ CMP2_IN3/ ADC1_SE2 3								
40	M7	XTAL32	XTAL32	XTAL32								
41	M6	EXTAL32	EXTAL32	EXTAL32								
42	L6	VBAT	VBAT	VBAT								
43	—	VDD	VDD	VDD								
44	—	VSS	VSS	VSS								
45	M4	PTE24	ADC0_SE1 7/EXTAL1	ADC0_SE1 7/EXTAL1	PTE24	CAN1_TX	UART4_TX	I2S1_TX_F S		EWM_OUT _b	I2S1_RXD1	
46	K5	PTE25	ADC0_SE1 8/XTAL1	ADC0_SE1 8/XTAL1	PTE25	CAN1_RX	UART4_RX	I2S1_TX_B CLK		EWM_IN	I2S1_TXD1	
47	K4	PTE26	ADC3_SE5 b	ADC3_SE5 b	PTE26		UART4_CT S_b	I2S1_TXD0		RTC_CLKO UT		
48	J4	PTE27	ADC3_SE4 b	ADC3_SE4 b	PTE27		UART4_RT S_b	I2S1_MCLK				

144 LQFP	144 MAP BGA	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EzPort
49	H4	PTE28	ADC3_SE7a	ADC3_SE7a	PTE28							
50	J5	PTA0	JTAG_TCLK/ SWD_CLK/ EZP_CLK	TSIO_CH1	PTA0	UART0_CTS_b/ UART0_COL_b	FTM0_CH5				JTAG_TCLK/ SWD_CLK	EZP_CLK
51	J6	PTA1	JTAG_TDI/ EZP_DI	TSIO_CH2	PTA1	UART0_RX	FTM0_CH6				JTAG_TDI	EZP_DI
52	K6	PTA2	JTAG_TDO/ TRACE_SWO/ EZP_DO	TSIO_CH3	PTA2	UART0_TX	FTM0_CH7				JTAG_TDO/ TRACE_SWO	EZP_DO
53	K7	PTA3	JTAG_TMS/ SWD_DIO	TSIO_CH4	PTA3	UART0_RTS_b	FTM0_CH0				JTAG_TMS/ SWD_DIO	
54	L7	PTA4/ LLWU_P3	NMI_b/ EZP_CS_b	TSIO_CH5	PTA4/ LLWU_P3		FTM0_CH1				NMI_b	EZP_CS_b
55	M8	PTA5	DISABLED		PTA5		FTM0_CH2		CMP2_OUT	I2S0_TX_B CLK	JTAG_TRST_b	
56	E7	VDD	VDD	VDD								
57	G7	VSS	VSS	VSS								
58	J7	PTA6	ADC3_SE6a	ADC3_SE6a	PTA6		FTM0_CH3	I2S1_RXD0	CLKOUT		TRACE_CLKOUT	
59	J8	PTA7	ADC0_SE10	ADC0_SE10	PTA7		FTM0_CH4	I2S1_RX_B CLK			TRACE_D3	
60	K8	PTA8	ADC0_SE11	ADC0_SE11	PTA8		FTM1_CH0	I2S1_RX_FS		FTM1_QD_PHA	TRACE_D2	
61	L8	PTA9	ADC3_SE5a	ADC3_SE5a	PTA9		FTM1_CH1			FTM1_QD_PHB	TRACE_D1	
62	M9	PTA10	ADC3_SE4a	ADC3_SE4a	PTA10		FTM2_CH0			FTM2_QD_PHA	TRACE_D0	
63	L9	PTA11	ADC3_SE15	ADC3_SE15	PTA11		FTM2_CH1			FTM2_QD_PHB		
64	K9	PTA12	CMP2_IN0	CMP2_IN0	PTA12	CAN0_TX	FTM1_CH0			I2S0_TXD0	FTM1_QD_PHA	
65	J9	PTA13/ LLWU_P4	CMP2_IN1	CMP2_IN1	PTA13/ LLWU_P4	CAN0_RX	FTM1_CH1			I2S0_TX_FS	FTM1_QD_PHB	
66	L10	PTA14	CMP3_IN0	CMP3_IN0	PTA14	SPI0_PCS0	UART0_TX			I2S0_RX_B CLK	I2S0_TXD1	
67	L11	PTA15	CMP3_IN1	CMP3_IN1	PTA15	SPI0_SCK	UART0_RX			I2S0_RXD0		
68	K10	PTA16	CMP3_IN2	CMP3_IN2	PTA16	SPI0_SOUT	UART0_CTS_b/ UART0_COL_b			I2S0_RX_FS	I2S0_RXD1	
69	K11	PTA17	ADC1_SE17	ADC1_SE17	PTA17	SPI0_SIN	UART0_RTS_b			I2S0_MCLK		
70	E8	VDD	VDD	VDD								
71	G8	VSS	VSS	VSS								

## Pinout

144 LQFP	144 MAP BGA	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EzPort
72	M12	PTA18	EXTAL0	EXTAL0	PTA18		FTM0_FLT2	FTM_CLKIN0				
73	M11	PTA19	XTAL0	XTAL0	PTA19		FTM1_FLT0	FTM_CLKIN1		LPTMR0_ALT1		
74	L12	RESET_b	RESET_b	RESET_b								
75	K12	PTA24	CMP3_IN4	CMP3_IN4	PTA24					FB_A29		
76	J12	PTA25	CMP3_IN5	CMP3_IN5	PTA25					FB_A28		
77	J11	PTA26	ADC2_SE15	ADC2_SE15	PTA26					FB_A27		
78	J10	PTA27	ADC2_SE14	ADC2_SE14	PTA27					FB_A26		
79	H12	PTA28	ADC2_SE13	ADC2_SE13	PTA28					FB_A25		
80	H11	PTA29	ADC2_SE12	ADC2_SE12	PTA29					FB_A24		
81	H10	PTB0/LLWU_P5	ADC0_SE8/ADC1_SE8/ADC2_SE8/ADC3_SE8/TSI0_CH0	ADC0_SE8/ADC1_SE8/ADC2_SE8/ADC3_SE8/TSI0_CH0	PTB0/LLWU_P5	I2C0_SCL	FTM1_CH0			FTM1_QD_PHA		
82	H9	PTB1	ADC0_SE9/ADC1_SE9/ADC2_SE9/ADC3_SE9/TSI0_CH6	ADC0_SE9/ADC1_SE9/ADC2_SE9/ADC3_SE9/TSI0_CH6	PTB1	I2C0_SDA	FTM1_CH1			FTM1_QD_PHB		
83	G12	PTB2	ADC0_SE12/TSI0_CH7	ADC0_SE12/TSI0_CH7	PTB2	I2C0_SCL	UART0_RTS_b			FTM0_FLT3		
84	G11	PTB3	ADC0_SE13/TSI0_CH8	ADC0_SE13/TSI0_CH8	PTB3	I2C0_SDA	UART0_CTS_b/UART0_COL_b			FTM0_FLT0		
85	G10	PTB4	ADC1_SE10	ADC1_SE10	PTB4					FTM1_FLT0		
86	G9	PTB5	ADC1_SE11	ADC1_SE11	PTB5					FTM2_FLT0		
87	F12	PTB6	ADC1_SE12	ADC1_SE12	PTB6					FB_AD23		
88	F11	PTB7	ADC1_SE13	ADC1_SE13	PTB7					FB_AD22		
89	F10	PTB8	DISABLED		PTB8		UART3_RTS_b			FB_AD21		
90	F9	PTB9	DISABLED		PTB9	SPI1_PCS1	UART3_CTS_b			FB_AD20		
91	E12	PTB10	ADC1_SE14	ADC1_SE14	PTB10	SPI1_PCS0	UART3_RX	I2S1_TX_BCLK	FB_AD19	FTM0_FLT1		
92	E11	PTB11	ADC1_SE15	ADC1_SE15	PTB11	SPI1_SCK	UART3_TX	I2S1_TX_FS	FB_AD18	FTM0_FLT2		
93	H7	VSS	VSS	VSS								

144 LQFP	144 MAP BGA	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EzPort
94	F5	VDD	VDD	VDD								
95	E10	PTB16	TSIO_CH9	TSIO_CH9	PTB16	SPI1_SOUT	UART0_RX	I2S1_TXD0	FB_AD17	EWM_IN		
96	E9	PTB17	TSIO_CH10	TSIO_CH10	PTB17	SPI1_SIN	UART0_TX	I2S1_TXD1	FB_AD16	EWM_OUT_b		
97	D12	PTB18	TSIO_CH11	TSIO_CH11	PTB18	CAN0_TX	FTM2_CH0	I2S0_TX_B CLK	FB_AD15	FTM2_QD_PHA		
98	D11	PTB19	TSIO_CH12	TSIO_CH12	PTB19	CAN0_RX	FTM2_CH1	I2S0_TX_FS	FB_OE_b	FTM2_QD_PHB		
99	D10	PTB20	ADC2_SE4a	ADC2_SE4a	PTB20	SPI2_PCS0			FB_AD31/NFC_DATA15	CMP0_OUT		
100	D9	PTB21	ADC2_SE5a	ADC2_SE5a	PTB21	SPI2_SCK			FB_AD30/NFC_DATA14	CMP1_OUT		
101	C12	PTB22	DISABLED		PTB22	SPI2_SOUT			FB_AD29/NFC_DATA13	CMP2_OUT		
102	C11	PTB23	DISABLED		PTB23	SPI2_SIN	SPI0_PCS5		FB_AD28/NFC_DATA12	CMP3_OUT		
103	B12	PTC0	ADC0_SE14/TSIO_CH13	ADC0_SE14/TSIO_CH13	PTC0	SPI0_PCS4	PDB0_EXT RG		FB_AD14/NFC_DATA11	I2S0_TXD1		
104	B11	PTC1/LLWU_P6	ADC0_SE15/TSIO_CH14	ADC0_SE15/TSIO_CH14	PTC1/LLWU_P6	SPI0_PCS3	UART1_RTS_b	FTM0_CH0	FB_AD13/NFC_DATA10	I2S0_TXD0		
105	A12	PTC2	ADC0_SE4b/CMP1_IN0/TSIO_CH15	ADC0_SE4b/CMP1_IN0/TSIO_CH15	PTC2	SPI0_PCS2	UART1_CTS_b	FTM0_CH1	FB_AD12/NFC_DATA9	I2S0_TX_FS		
106	A11	PTC3/LLWU_P7	CMP1_IN1	CMP1_IN1	PTC3/LLWU_P7	SPI0_PCS1	UART1_RX	FTM0_CH2	CLKOUT	I2S0_TX_B CLK		
107	H8	VSS	VSS	VSS								
108	—	VDD	VDD	VDD								
109	A9	PTC4/LLWU_P8	DISABLED		PTC4/LLWU_P8	SPI0_PCS0	UART1_TX	FTM0_CH3	FB_AD11/NFC_DATA8	CMP1_OUT	I2S1_TX_B CLK	
110	D8	PTC5/LLWU_P9	DISABLED		PTC5/LLWU_P9	SPI0_SCK	LPTMR0_ALT2	I2S0_RXD0	FB_AD10/NFC_DATA7	CMP0_OUT	I2S1_TX_FS	
111	C8	PTC6/LLWU_P10	CMP0_IN0	CMP0_IN0	PTC6/LLWU_P10	SPI0_SOUT	PDB0_EXT RG	I2S0_RX_B CLK	FB_AD9/NFC_DATA6	I2S0_MCLK		
112	B8	PTC7	CMP0_IN1	CMP0_IN1	PTC7	SPI0_SIN		I2S0_RX_FS	FB_AD8/NFC_DATA5			
113	A8	PTC8	ADC1_SE4b/CMP0_IN2	ADC1_SE4b/CMP0_IN2	PTC8		FTM3_CH4	I2S0_MCLK	FB_AD7/NFC_DATA4			

## Pinout

144 LQFP	144 MAP BGA	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EzPort
114	D7	PTC9	ADC1_SE5 b/ CMP0_IN3	ADC1_SE5 b/ CMP0_IN3	PTC9		FTM3_CH5	I2S0_RX_B CLK	FB_AD6/ NFC_DATA3	FTM2_FLT0		
115	C7	PTC10	ADC1_SE6 b	ADC1_SE6 b	PTC10	I2C1_SCL	FTM3_CH6	I2S0_RX_FS	FB_AD5/ NFC_DATA2	I2S1_MCLK		
116	B7	PTC11/ LLWU_P11	ADC1_SE7 b	ADC1_SE7 b	PTC11/ LLWU_P11	I2C1_SDA	FTM3_CH7	I2S0_RXD1	FB_RW_b/ NFC_WE			
117	A7	PTC12	DISABLED		PTC12		UART4_RTS_b		FB_AD27	FTM3_FLT0		
118	D6	PTC13	DISABLED		PTC13		UART4_CTS_b		FB_AD26			
119	C6	PTC14	DISABLED		PTC14		UART4_RX		FB_AD25			
120	B6	PTC15	DISABLED		PTC15		UART4_TX		FB_AD24			
121	—	VSS	VSS	VSS								
122	—	VDD	VDD	VDD								
123	A6	PTC16	DISABLED		PTC16	CAN1_RX	UART3_RX		FB_CS5_b/ FB_TSIZ1/ FB_BE23_16_b	NFC_RB		
124	D5	PTC17	DISABLED		PTC17	CAN1_TX	UART3_TX		FB_CS4_b/ FB_TSIZ0/ FB_BE31_24_b	NFC_CE0_b		
125	C5	PTC18	DISABLED		PTC18		UART3_RTS_b		FB_TBST_b/ FB_CS2_b/ FB_BE15_8_b	NFC_CE1_b		
126	B5	PTC19	DISABLED		PTC19		UART3_CTS_b		FB_CS3_b/ FB_BE7_0_b	FB_TA_b		
127	A5	PTD0/ LLWU_P12	DISABLED		PTD0/ LLWU_P12	SPI0_PCS0	UART2_RTS_b	FTM3_CH0	FB_ALE/ FB_CS1_b/ FB_TS_b	I2S1_RXD1		
128	D4	PTD1	ADC0_SE5 b	ADC0_SE5 b	PTD1	SPI0_SCK	UART2_CTS_b	FTM3_CH1	FB_CS0_b	I2S1_RXD0		
129	C4	PTD2/ LLWU_P13	DISABLED		PTD2/ LLWU_P13	SPI0_SOUT	UART2_RX	FTM3_CH2	FB_AD4	I2S1_RX_FS		
130	B4	PTD3	DISABLED		PTD3	SPI0_SIN	UART2_TX	FTM3_CH3	FB_AD3	I2S1_RX_B CLK		
131	A4	PTD4/ LLWU_P14	DISABLED		PTD4/ LLWU_P14	SPI0_PCS1	UART0_RTS_b	FTM0_CH4	FB_AD2/ NFC_DATA1	EWM_IN		
132	A3	PTD5	ADC0_SE6 b	ADC0_SE6 b	PTD5	SPI0_PCS2	UART0_CTS_b/ UART0_COL_b	FTM0_CH5	FB_AD1/ NFC_DATA0	EWM_OUT_b		
133	A2	PTD6/ LLWU_P15	ADC0_SE7 b	ADC0_SE7 b	PTD6/ LLWU_P15	SPI0_PCS3	UART0_RX	FTM0_CH6	FB_AD0	FTM0_FLT0		

144 LQF P	144 MAP BGA	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EzPort
134	M10	VSS	VSS	VSS								
135	F8	VDD	VDD	VDD								
136	A1	PTD7	DISABLED		PTD7	CMT_IRO	UART0_TX	FTM0_CH7		FTM0_FLT1		
137	C9	PTD8	DISABLED		PTD8	I2C0_SCL	UART5_RX			FB_A16/ NFC_CLE		
138	B9	PTD9	DISABLED		PTD9	I2C0_SDA	UART5_TX			FB_A17/ NFC_ALE		
139	B3	PTD10	DISABLED		PTD10		UART5_RT S_b			FB_A18/ NFC_RE		
140	B2	PTD11	DISABLED		PTD11	SPI2_PCS0	UART5_CT S_b	SDHC0_CL KIN		FB_A19		
141	B1	PTD12	DISABLED		PTD12	SPI2_SCK	FTM3_FLT0	SDHC0_D4		FB_A20		
142	C3	PTD13	DISABLED		PTD13	SPI2_SOUT		SDHC0_D5		FB_A21		
143	C2	PTD14	DISABLED		PTD14	SPI2_SIN		SDHC0_D6		FB_A22		
144	C1	PTD15	DISABLED		PTD15	SPI2_PCS1		SDHC0_D7		FB_A23		

## 8.2 K10 Pinouts

The below figure shows the pinout diagram for the devices supported by this document. Many signals may be multiplexed onto a single pin. To determine what signals can be used on which pin, see the previous section.

# Pinout

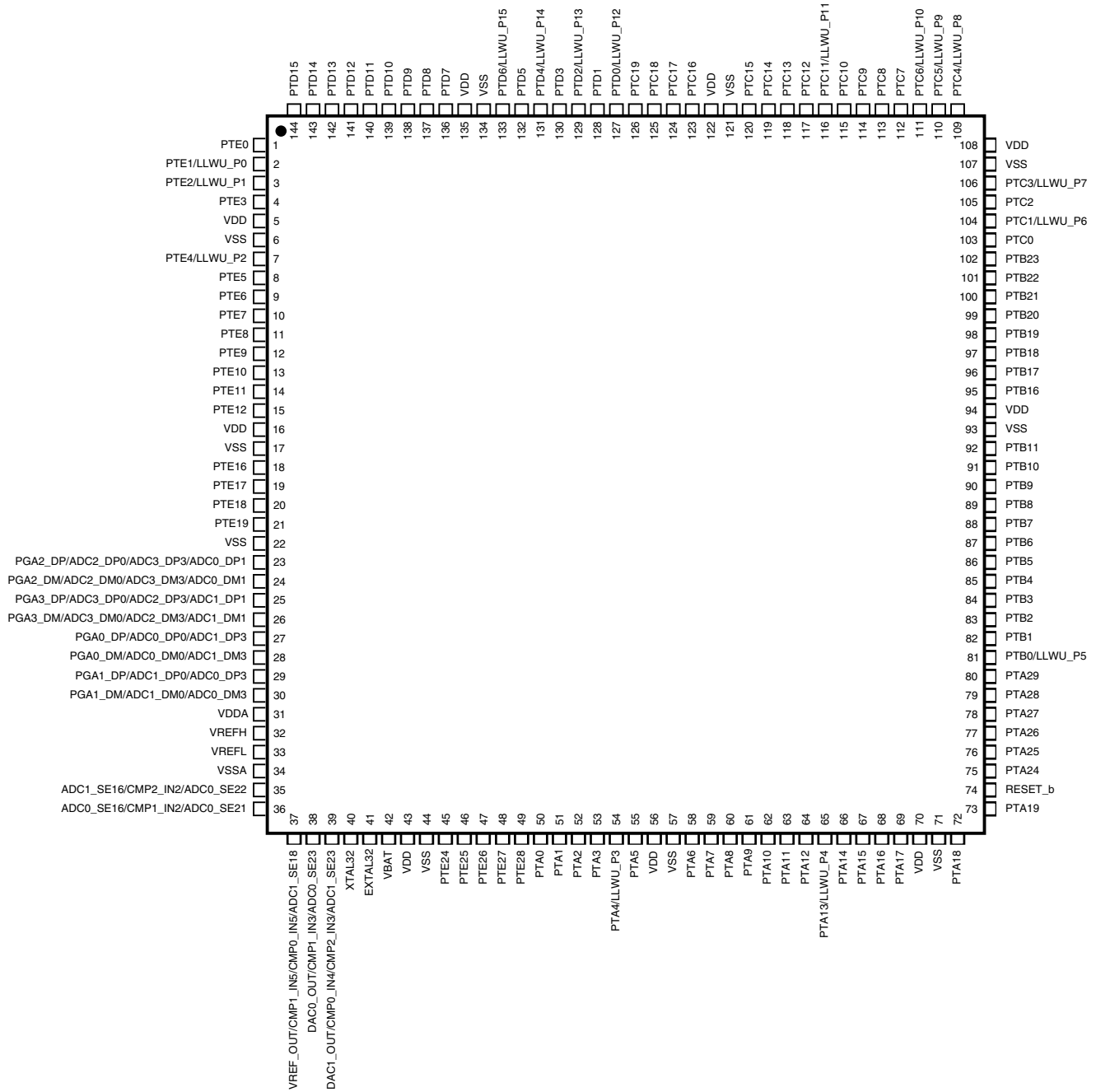


Figure 32. K10 144 LQFP Pinout Diagram



	1	2	3	4	5	6	7	8	9	10	11	12	
A	PTD7	PTD6/ LLWU_P15	PTD5	PTD4/ LLWU_P14	PTD0/ LLWU_P12	PTC16	PTC12	PTC8	PTC4/ LLWU_P8	NC	PTC3/ LLWU_P7	PTC2	A
B	PTD12	PTD11	PTD10	PTD3	PTC19	PTC15	PTC11/ LLWU_P11	PTC7	PTD9	NC	PTC1/ LLWU_P6	PTC0	B
C	PTD15	PTD14	PTD13	PTD2/ LLWU_P13	PTC18	PTC14	PTC10	PTC6/ LLWU_P10	PTD8	NC	PTB23	PTB22	C
D	PTE2/ LLWU_P1	PTE1/ LLWU_P0	PTE0	PTD1	PTC17	PTC13	PTC9	PTC5/ LLWU_P9	PTB21	PTB20	PTB19	PTB18	D
E	PTE6	PTE5	PTE4/ LLWU_P2	PTE3	VDD	VDD	VDD	VDD	PTB17	PTB16	PTB11	PTB10	E
F	PTE10	PTE9	PTE8	PTE7	VDD	VSS	VSS	VDD	PTB9	PTB8	PTB7	PTB6	F
G	PTE18	PTE19	PTE12	PTE11	VREFH	VREFL	VSS	VSS	PTB5	PTB4	PTB3	PTB2	G
H	PTE16	PTE17	VSS	PTE28	VDDA	VSSA	VSS	VSS	PTB1	PTB0/ LLWU_P5	PTA29	PTA28	H
J	PGA2_DP/ ADC2_DP0/ ADC3_DP3/ ADC0_DP1	PGA2_DM/ ADC2_DM0/ ADC3_DM3/ ADC0_DM1	ADC0_SE16/ CMP1_IN2/ ADC0_SE21	PTE27	PTA0	PTA1	PTA6	PTA7	PTA13/ LLWU_P4	PTA27	PTA26	PTA25	J
K	PGA3_DP/ ADC3_DP0/ ADC2_DP3/ ADC1_DP1	PGA3_DM/ ADC3_DM0/ ADC2_DM3/ ADC1_DM1	ADC1_SE16/ CMP2_IN2/ ADC0_SE22	PTE26	PTE25	PTA2	PTA3	PTA8	PTA12	PTA16	PTA17	PTA24	K
L	PGA0_DP/ ADC0_DP0/ ADC1_DP3	PGA0_DM/ ADC0_DM0/ ADC1_DM3	DAC0_OUT/ CMP1_IN3/ ADC0_SE23	DAC1_OUT/ CMP0_IN4/ CMP2_IN3/ ADC1_SE23	RTC_ WAKEUP_B	VBAT	PTA4/ LLWU_P3	PTA9	PTA11	PTA14	PTA15	RESET_b	L
M	PGA1_DP/ ADC1_DP0/ ADC0_DP3	PGA1_DM/ ADC1_DM0/ ADC0_DM3	VREF_OUT/ CMP1_IN5/ CMP0_IN5/ ADC1_SE18	PTE24	NC	EXTAL32	XTAL32	PTA5	PTA10	VSS	PTA19	PTA18	M

Figure 33. K10 144 MAPBGA Pinout Diagram

## 9 Revision History

The following table provides a revision history for this document.

**Table 46. Revision History**

Rev. No.	Date	Substantial Changes
1	6/2011	Initial public revision.

*Table continues on the next page...*

**Table 46. Revision History (continued)**

Rev. No.	Date	Substantial Changes
2	11/2011	<ul style="list-style-type: none"> <li>• Added AC electrical specifications.</li> <li>• Updated Part identification section for 120 MHz CPU frequency.</li> <li>• Updated Voltage and current operating ratings section.</li> <li>• Updated Voltage and current operating requirements section.</li> <li>• Updated LVD and POR operating requirements section.</li> <li>• Updated Voltage and current operating behaviors section.</li> <li>• Updated Power mode transition operating behaviors section.</li> <li>• Updated Power consumption operating behaviors section.</li> <li>• In Run mode supply current vs. core frequency section, added Run and VLPR modes supply current vs. core frequency diagrams.</li> <li>• In Device clock specifications section, updated flash clock frequency and DDR clock frequency.</li> <li>• Updated Thermal attributes.</li> <li>• In MCG specifications section, updated total deviation of trimmed average DCO output Frequency, PLL reference frequency range, and lock detector detection time.</li> <li>• In Oscillator frequency specifications section, updated crystal startup time — 32 kHz.</li> <li>• Updated NFC specifications section.</li> <li>• In DSPI switching specifications section, updated master and slave modes frequency of operation for limited voltage and full voltage ranges.</li> <li>• In I2S/SAI Switching Specifications section, updated cycle time for master and slave modes.</li> <li>• In TSI electrical specifications, updated reference oscillator frequency.</li> <li>• Updated Pinouts.</li> <li>• Updated Pinouts.</li> </ul>

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