

## Sirius SDARS channel, service & source decoder

Data Brief

### Features

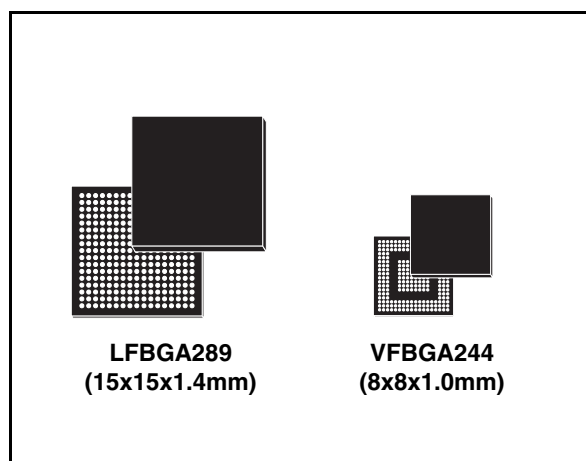
- 2 Satellite and 1 terrestrial signal demodulators and decoders
- Advanced DSP processor to implement PAC audio decoder
- Requires a single 17MHz clock reference; all high-speed clock signals are derived using on-chip PLL
- Programmable I<sup>2</sup>S to support 32K/48K/44.1K audio sample rate (32K/48K Sample rates use internal clocks, 44.1K Sample rate uses external clock)
- I<sup>2</sup>C master interface to control tuner and audio DAC
- External control through UART interface using Sirius Standard Protocol (SSP) over RS-232

### Analog to digital converters

- Three internal 10 BIT A/D converters for 76.5MHZ if signals conversion

### Low power technology

- 1.2V, 90 μm technology
- 2.5V capable I/OS



### Description

STA260 is a fully integrated 3rd generation Baseband signal processor for Sirius Satellite Digital Audio Radio Service (SDARS). It is implemented using ST Micro's advanced 90 μm CMOS090 technology.

It allows a highly efficient implementation of a Sirius "SDARS Satellite Digital Audio Radio Service" receiver when used with its companion STA210 tuner ASIC.

STA260 is packaged in a Low profile Fine pitch Ball Grid Array (LFBGA 15x15) and in Very thin Fine pitch Ball Grid Array (VFBGA 8x8).

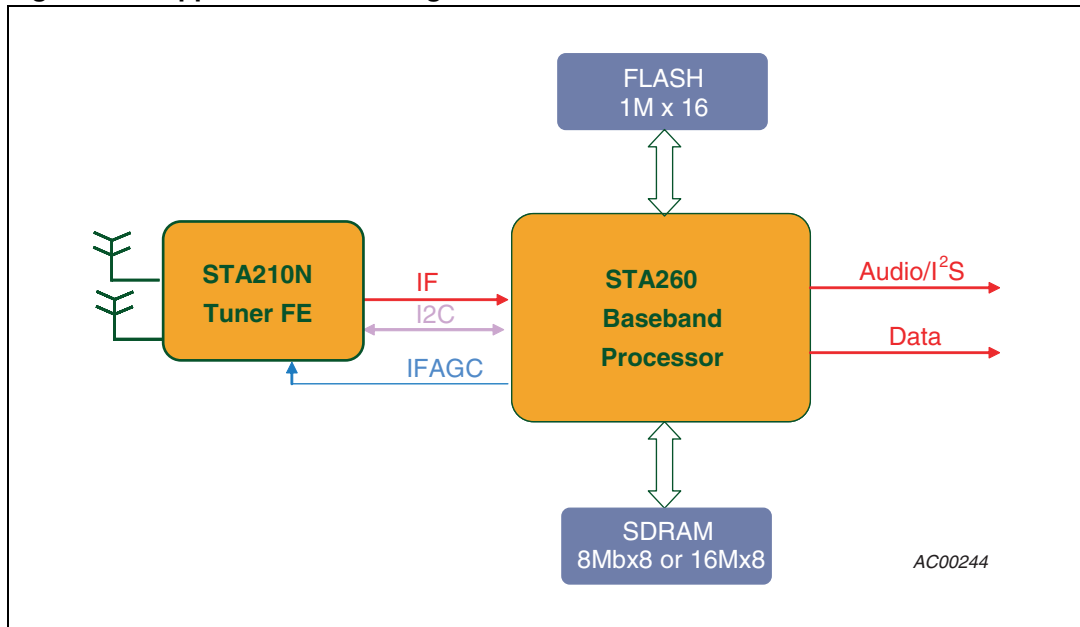
**Table 1. Device summary**

Part Number <sup>(1)</sup>	Package	Packing
STA260	LFBGA289	Tray
STA260TR	LFBGA289	Tape & reel
STA260-8x8	VFBGA244	Tray

1. This device is Pb-Free ECOPACK® see [Chapter 3: Package information](#).

# 1 Application block diagram

Figure 1. Application block diagram



## 2 Electrical specifications

### 2.1 Absolute maximum ratings

**Table 2. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
V <sub>DD</sub>	1.2V Power supply Voltage	1.32	V
V <sub>DDIO</sub>	2.5V Power Supply Voltage	2.75	V
A <sub>D_VDD</sub>	1.2V Power supply Voltage	1.32	V
A <sub>D_VDD2</sub>	2.5V Power Supply Voltage	2.75	V
A <sub>PLL_VDD</sub>	2.5V Power Supply Voltage	2.75	V
V <sub>i</sub>	Voltage on input pin	-0.5 to (V <sub>DDIO</sub> + 0.5)	V
V <sub>o</sub>	Voltage on output pin	-0.5 to (V <sub>DDIO</sub> + 0.5)	V
T <sub>stg</sub>	Storage Temperature	-55 to +150	°C
T <sub>op</sub>	Operative Ambient Temperature	-40 to +85	°C
T <sub>j</sub>	Operative Junction Temperature	-40 to +125	°C

### 2.2 Thermal data

**Table 3. Thermal data**

Symbol	Parameter	LFBGA	VFBGA	Unit
R <sub>th j-amb</sub>	Thermal resistance Junction to ambient <sup>(1)</sup>	35	50	°C/W

1. According to JEDEC specification on a 4 layers board

### 3 Package information

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second Level Interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label.

ECOPACK is an ST trademark. ECOPACK specifications are available at: [www.st.com](http://www.st.com).

**Figure 2. LFBGA (15x15x1.4mm 289 ball) mechanical data & package dimensions**

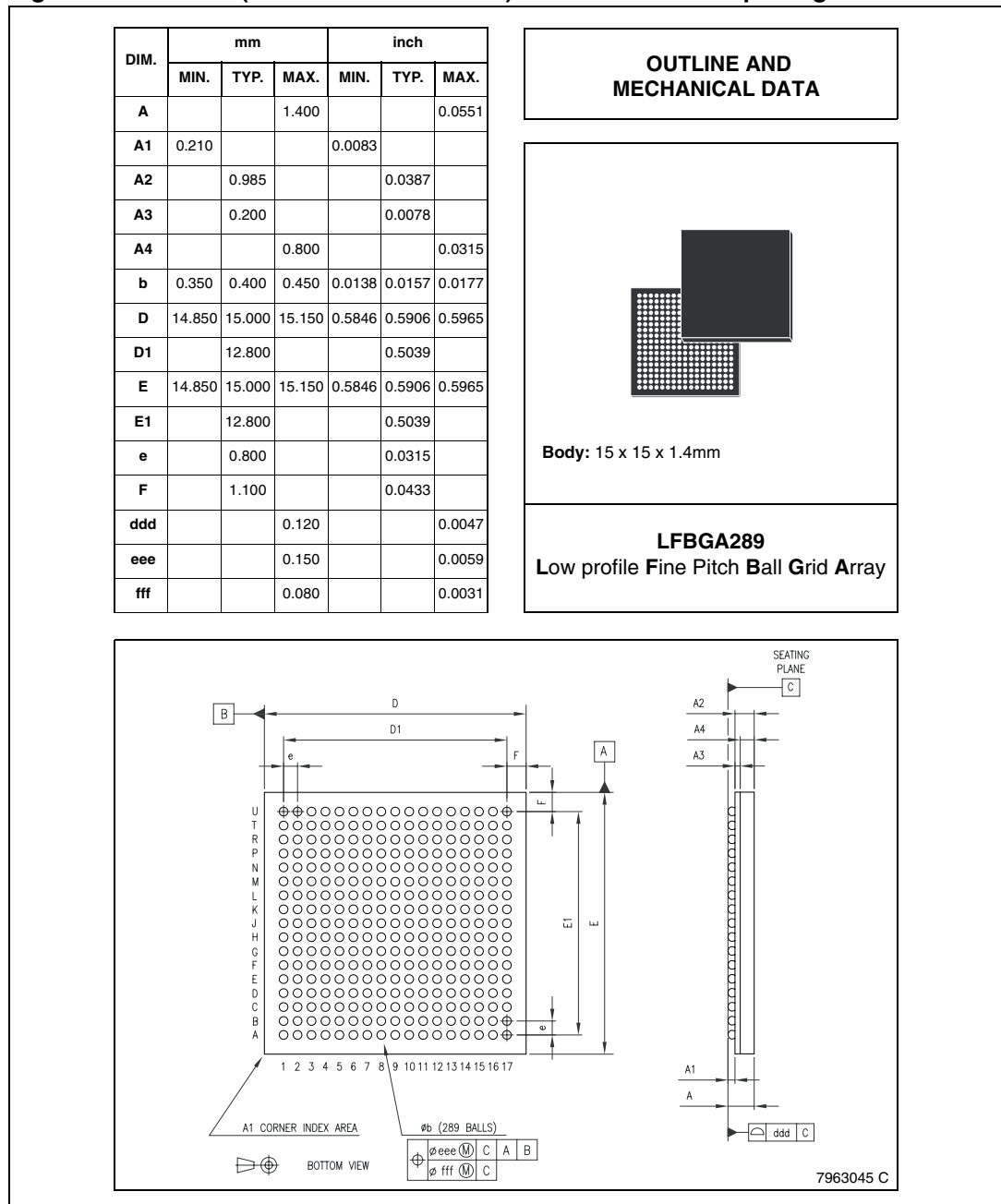
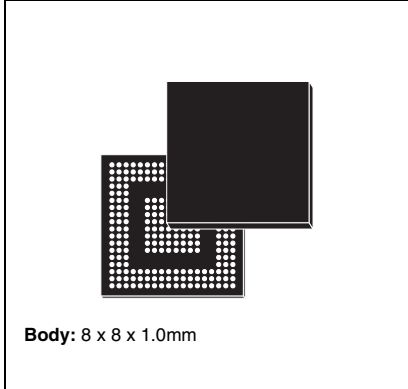


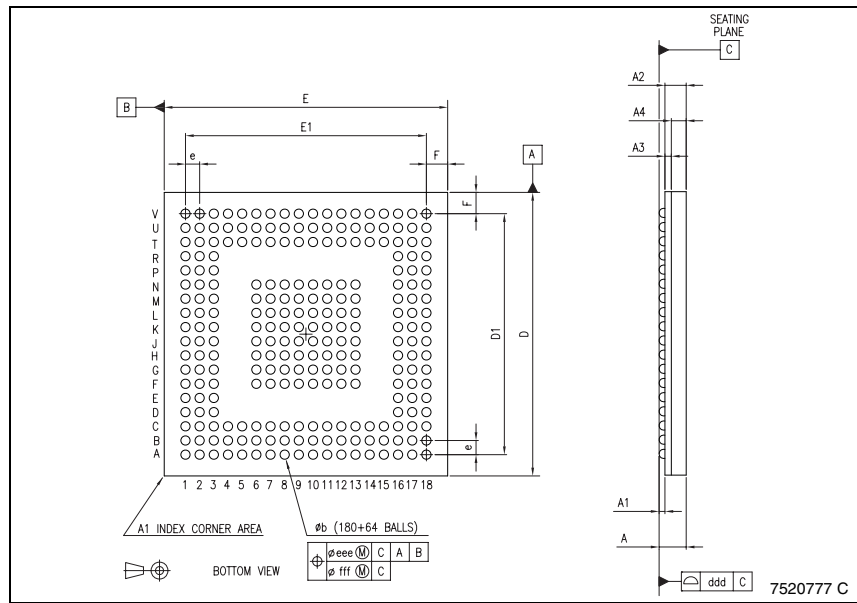
Figure 3. VFBGA (8x8x1.0mm 180+64 ball) mechanical data & package dimensions

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.000			0.0394
A1	0.130	0.170	0.210	0.0051	0.0067	0.0083
A2		0.620			0.0244	
A3		0.180			0.0071	
A4			0.450			0.0177
b	0.220	0.260	0.300	0.0087	0.0102	0.0118
D	7.950	8.000	8.050	0.3130	0.3150	0.3169
D1		6.800			0.2677	
E	7.950	8.000	8.050	0.3130	0.3150	0.3169
E1		6.800			0.2677	
e		0.400			0.0157	
F		0.600			0.0236	
ddd			0.080			0.0031
eee			0.130			0.0051
fff			0.040			0.0016

**OUTLINE AND MECHANICAL DATA**



**VFBGA244**  
Very thin profile Fine Pitch Ball Grid Array



## 4 Revision history

**Table 4. Document revision history**

Date	Revision	Changes
18-Jun-2007	1	Initial release.

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