



HIGH-SPEED CMOS BUS INTERFACE 10-BIT REGISTER

IDT74FCTL2821T

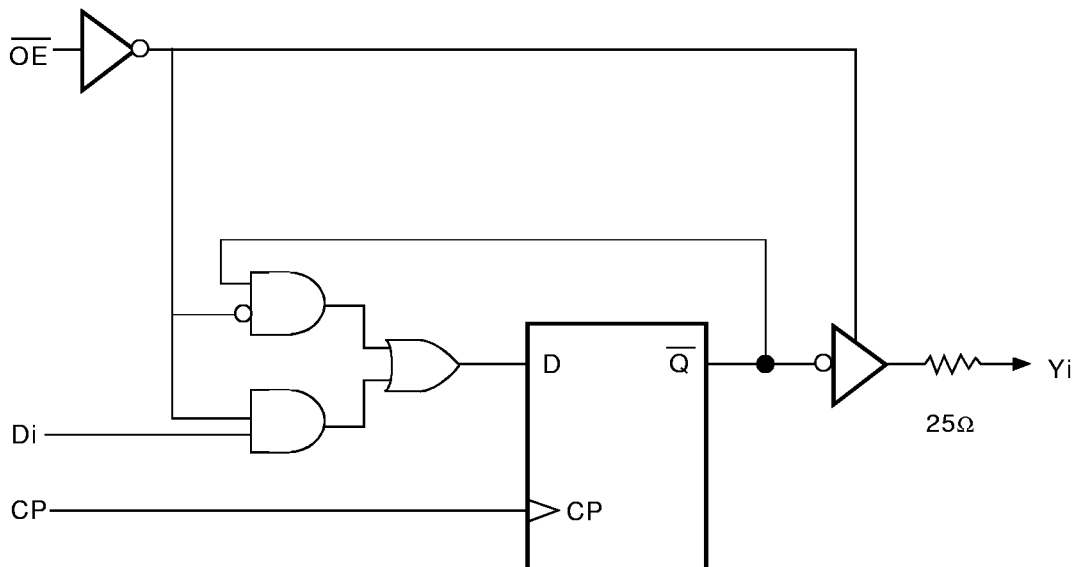
FEATURES:

- Pin and function compatible to the Quality QS74FCT Family
- Extended commercial range of -40°C to $+85^{\circ}\text{C}$
- CMOS power levels: $<7.5\text{mW}$ static
- Available in PDIP, SOIC, and QSOP packages
- Undershoot clamp diodes on all inputs
- True TTL input and output compatibility
- Ground bounce controlled outputs
- Reduced output swing of 0 to 3.5V
- Built-in 25Ω series resistor outputs reduce reflection and other system noise
- $I_{OL} = 12\text{mA}$

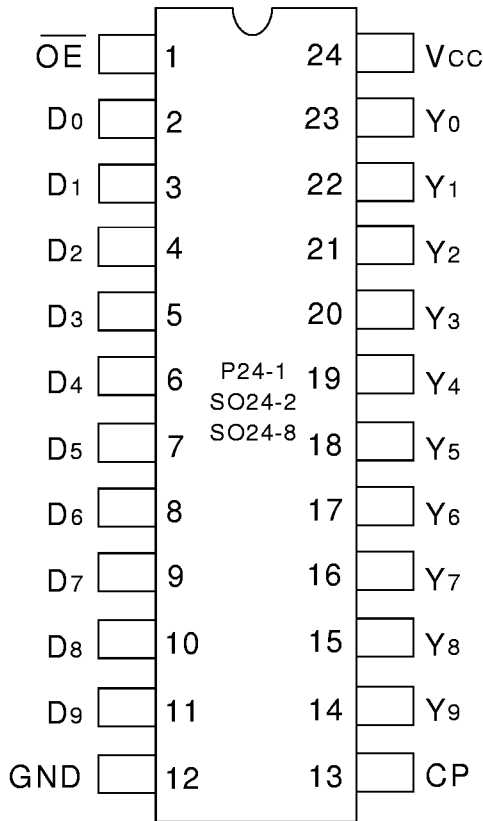
DESCRIPTION:

The IDT74FCTL2821T is a 10-bit high-speed CMOS TTL-compatible buffered register with 3-state outputs, ideal for driving high capacitance loads such as memory address and data buses. The 2821 device is a 25Ω resistor output version, useful for driving transmission lines and reducing system noise. The 2821 series parts can replace the 821 series to reduce noise in an existing design. All inputs have clamp diodes for undershoot noise suppression. All outputs have ground bounce suppression. Outputs will not load an active bus when V_{CC} is removed from the device.

FUNCTIONAL BLOCK DIAGRAM

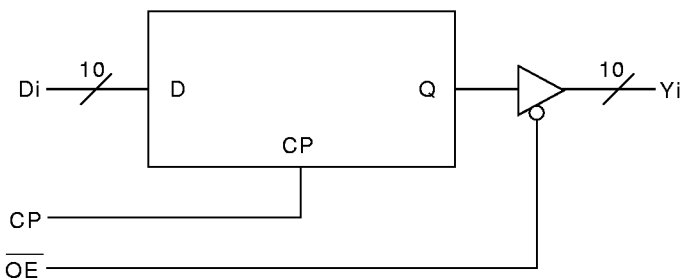


PIN CONFIGURATION



PDIP/ SOIC/ QSOP
TOP VIEW

LOGIC SYMBOL



ABSOLUTE MAXIMUM RATINGS (1)

Symbol	Description	Max.	Unit
VTERM ⁽²⁾	Terminal Voltage with Respect to GND	- 0.5 to +7	V
VTERM ⁽³⁾	Terminal Voltage with Respect to GND	- 0.5 to +7	V
TSTG	Storage Temperature	- 65 to +150	°C
I _{OUT}	DC Output Current	120	mA
I _{IK}	Continuous Clamp Current, Vi < 0 or Vo < 0	- 20	mA
I _{OK}		- 50	mA

NOTES:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- V_{CC} terminals.
- All terminals except V_{CC}.

CAPACITANCE (TA = +25°C, f = 1.0MHz)

Symbol	Parameter ⁽¹⁾	Conditions	Typ.	Max.	Unit
C _{IN}	Input Capacitance	V _{IN} = 0V	6	10	pF
C _{OUT}	Output Capacitance	V _{OUT} = 0V	8	12	pF

NOTE:

- This parameter is measured at characterization but not tested.

PIN DESCRIPTION

Name	I/O	Description
Di	I	The D flip-flop data inputs.
CP	I	Clock Pulse for the Register; enters data into the register on the LOW-to-HIGH transition.
Yi	O	The register three-state outputs.
\overline{OE}	I	Output Control. When the \overline{OE} input is HIGH, the Yi outputs are in the high impedance state. When the \overline{OE} input is LOW, the TRUE register data is present at the Yi outputs.

FUNCTION TABLE (1)

Inputs			Int.	O/P	Function
\overline{OE}	Di	CP	Qi	Yi	
H	L	↑	L	Hi-Z	High Z
H	H	↑	H	Hi-Z	High Z
H	L	↑	L	Hi-Z	Load
H	H	↑	H	Hi-Z	Load
L	L	↑	L	L	Load
L	H	↑	H	H	Load

NOTE:

- H = HIGH
L = LOW
↑ = LOW-to-HIGH Transition
Z = High-Impedance

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Extended Commercial: TA = -40°C to +85°C, Vcc = 5.0V ± 5%

Symbol	Parameter	Test Conditions	Min.	Typ. ⁽¹⁾	Max.	Unit
V _{IH}	Input HIGH Level	Guaranteed Logic HIGH Level	2	—	—	V
V _{IL}	Input LOW Level	Guaranteed Logic LOW Level	—	—	0.8	V
ΔV _T	Input Hysteresis	V _T LH - V _T HL for all inputs	—	0.2	—	V
I _{IH}	Input HIGH Current	V _{CC} = Max. 0 ≤ V _{IN} < V _{CC}	—	—	5	μA
I _{IL}	Input LOW Current					
I _{OZ}	Off-State Output Current (Hi-Z)	V _{CC} = Max. 0 ≤ V _{IN} ≤ V _{CC}	—	—	5	μA
I _{OR}	Current Drive	V _{CC} = Min., V _{OUT} = 2.0V ⁽²⁾	50	—	—	mA
V _{IC}	Input Clamp Voltage	V _{CC} = Min., I _{IN} = -18mA, TA = 25°C	—	-0.7	-1.2	V
V _{OH}	Output HIGH Voltage	V _{CC} = Min. I _{OH} = -24mA	2.4	—	—	V
V _{OL}	Output LOW Voltage - 25Ω	V _{CC} = Min. I _{OL} = 12mA	—	—	0.5	V
R _{OUT}	Output Resistance - 25Ω	V _{CC} = Min. I _{OL} = 12mA	20	28	40	Ω

NOTES:

1. Typical values are at V_{CC} = 5.0V, TA = 25°C.
2. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.

POWER SUPPLY CHARACTERISTICS

Following Conditions Apply Unless Otherwise Specified:

Extended Commercial: TA = -40°C to +85°C, Vcc = 5.0V ± 5%

Symbol	Parameter	Test Conditions ⁽¹⁾	Min.	Max.	Unit
I _{CC}	Quiescent Power Supply Current	V _{CC} = Max. freq = 0 0V ≤ V _{IN} ≤ 0.2V or V _{CC} -0.2V ≤ V _{IN} ≤ V _{CC}	—	1.5	mA
ΔI _{CC}	Supply Current per Input TTL Inputs HIGH	V _{CC} = Max. V _{IN} = 3.4V ⁽²⁾ freq = 0	—	2	mA
I _{CCD}	Supply Current per Input per MHz	V _{CC} = Max. Outputs Open and Enabled One Bit Toggling 50% Duty Cycle Other inputs at GND or V _{CC} ^(3,4)	—	0.25	mA/MHz

FCTL

NOTES:

1. For conditions shown as Min. or Max., use the appropriate values specified under DC Electrical Characteristics.
2. Per TTL driven input (V_{IN} = 3.4V).
3. For flip-flops, I_{CCD} is measured by switching one of the data input pins so that the output changes every clock cycle. This is a measurement of device power consumption only and does not include power to drive load capacitance or tester capacitance.
4. I_{CC} = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}
I_{CC} = I_{CC} + ΔI_{CC} D_{HNT} + I_{CCD} (f_{CP}/2 + f_iN_i)
I_{CC} = Quiescent Current
ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
D_H = Duty Cycle for TTL Inputs High
N_T = Number of TTL Inputs at DH
I_{CCD} = Dynamic Current Caused by an Output Transition Pair (HLH or LHL)
f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
f_i = Input Frequency
N_i = Number of Inputs at f_i
All currents are in milliamps and all frequencies are in megahertz.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE(1)

Following Conditions Apply Unless Otherwise Specified:
 Extended Commercial: TA = -40°C to +85°C, Vcc = 5.0V ± 5%

Symbol	Parameter	74FCTL2821AT		74FCTL2821BT		Unit
		Min.	Max.	Min.	Max.	
tPHL tPLH	Clock to Y Delay OE = LOW	—	10	—	7.5	ns
tPHL tPLH	Clock to Y Delay OE = LOW (2)	—	20	—	15	ns
tsu	Data to CP Setup Time	4	—	3	—	ns
th	Data to CP Hold Time	2	—	1.5	—	ns

NOTES:

1. CLOAD = 50pF, RLOAD = 500Ω unless otherwise noted.
2. CLOAD = 300pF

TIMING REQUIREMENTS OVER OPERATING RANGE(1)

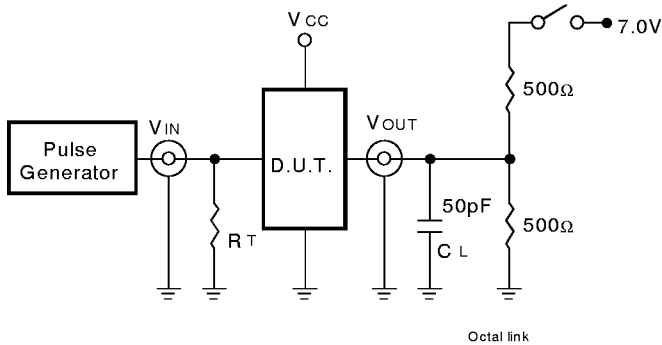
Symbol	Parameter(2)	74FCTL2821AT		74FCTL2821BT		Unit
		Min.	Max.	Min.	Max.	
tPWH tPWL	Clock Pulse Width HIGH or LOW	7	—	6	—	ns
tPZH tPZL	Output Enable Time OE to Yi	—	12	—	8	ns
tPZH tPZL	Output Enable Time(3) OE to Yi	—	23	—	—	ns
tPHZ tPLZ	Output Disable Time(4) OE to Yi	—	7	—	6.5	ns
tPHZ tPLZ	Output Disable Time OE to Yi	—	9	—	7.5	ns

NOTES:

1. CLOAD = 50pF, RLOAD = 500Ω unless otherwise noted.
2. See Test Circuits and Waveforms.
3. CLOAD = 300pF
4. CLOAD = 5pF

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



SWITCH POSITION

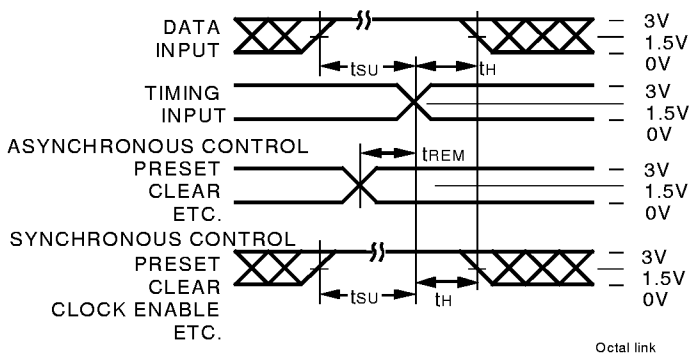
Test	Switch
Open Drain	Closed
Disable Low	
Enable Low	
All Other Tests	Open

DEFINITIONS:

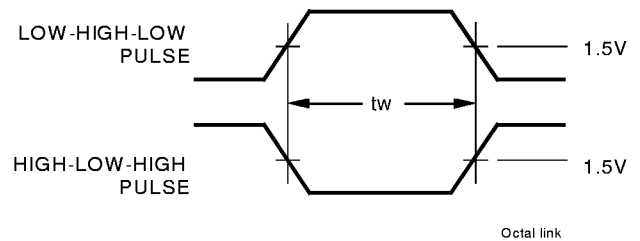
C_L = Load capacitance: includes jig and probe capacitance.

R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

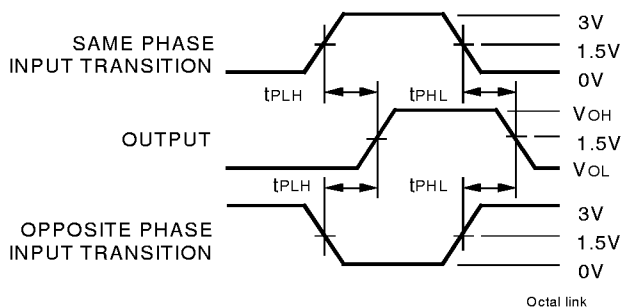
SET-UP, HOLD, AND RELEASE TIMES



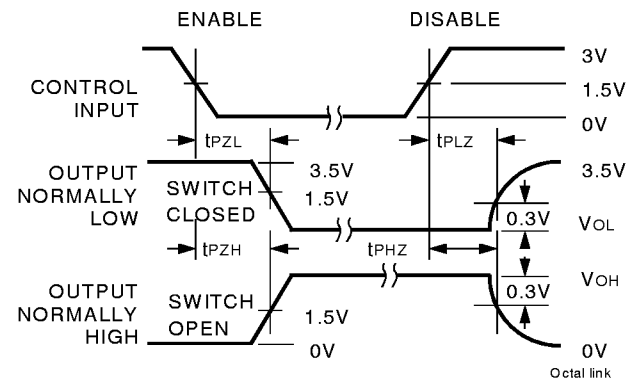
PULSE WIDTH



PROPAGATION DELAY



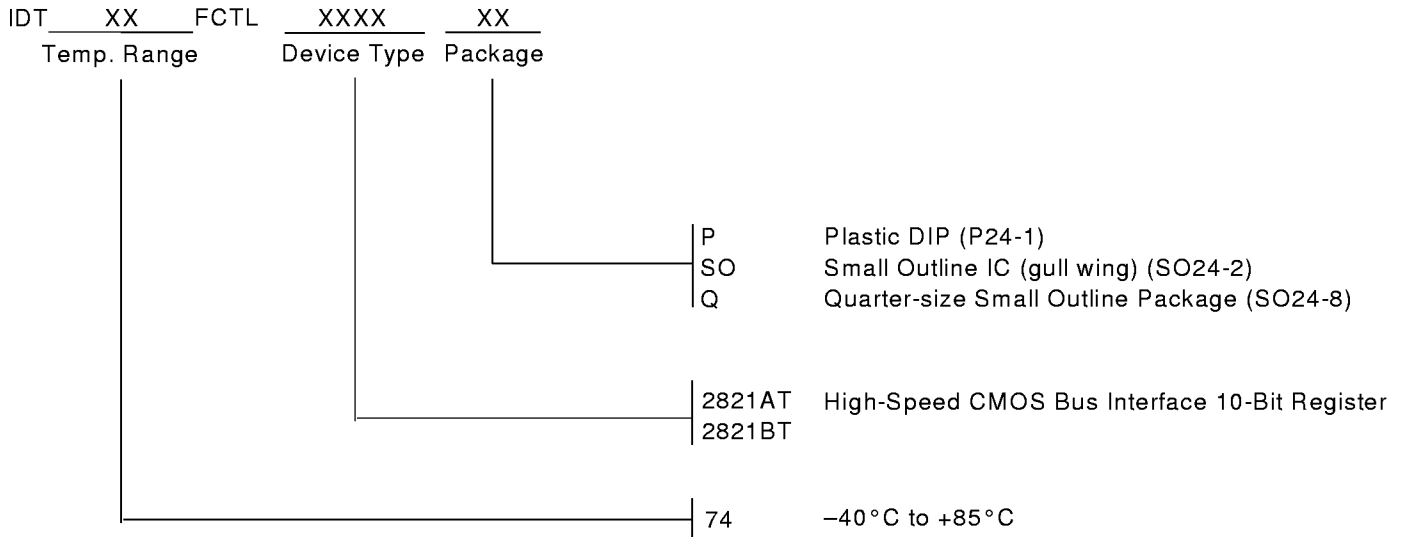
ENABLE AND DISABLE TIMES



NOTES:

- Diagram shown for input Control Enable-LOW and input Control Disable-HIGH
- Pulse Generator for All Pulses: Rate $\leq 1.0\text{MHz}$; $t_f \leq 2.5\text{ns}$; $t_r \leq 2.5\text{ns}$

ORDERING INFORMATION



CORPORATE HEADQUARTERS
2975 Stender Way
Santa Clara, CA 95054

for SALES:
800-345-7015 or 408-727-6116
fax: 408-492-8674
www.idt.com*

**To search for sales office near you, please click the sales button found on our home page or dial the 800# above and press 2.
The IDT logo is a registered trademark of Integrated Device Technology, Inc.*