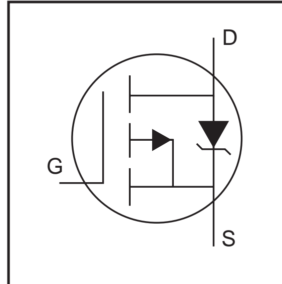
freescale
飞思卡尔(深圳)功率半导体有限公司

IRFR/U5410

HEXFET® Power MOSFET

- Ultra Low On-Resistance
- P-Channel
- Surface Mount (IRFR5410)
- Straight Lead (IRFU5410)
- Advanced Process Technology
- Fast Switching
- Fully Avalanche Rated



V_{DSS} = -100V

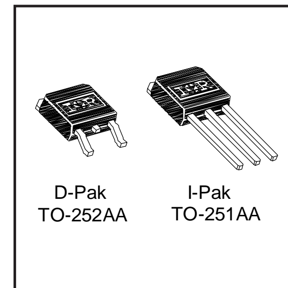
$R_{DS(on)}$ = 0.205Ω

I_D = -13A

Description

Fifth Generation HEXFETs from International Rectifier utilize advanced processing techniques to achieve extremely low on-resistance per silicon area. This benefit, combined with the fast switching speed and ruggedized device design that HEXFET Power MOSFETs are well known for, provides the designer with an extremely efficient and reliable device for use in a wide variety of applications.

The D-Pak is designed for surface mounting using vapor phase, infrared, or wave soldering techniques. The straight lead version (IRFU series) is for through-hole mounting applications. Power dissipation levels up to 1.5 watts are possible in typical surface mount applications.



D-Pak TO-252AA   I-Pak TO-251AA

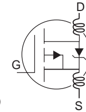
Absolute Maximum Ratings

	Parameter	Max.	Units
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ -10V	-13	A
I_D @ T_C = 100°C	Continuous Drain Current, V_{GS} @ -10V	-8.2	
I_{DM}	Pulsed Drain Current ①	-52	
P_D @T_C = 25°C	Power Dissipation	66	W
	Linear Derating Factor	0.53	W/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
E_{AS}	Single Pulse Avalanche Energy②	194	mJ
I_{AR}	Avalanche Current①	-8.4	A
E_{AR}	Repetitive Avalanche Energy①	6.3	mJ
dv/dt	Peak Diode Recovery dv/dt ③	-5.0	V/ns
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 150	°C
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{θJC}$	Junction-to-Case	----	1.9	°C/W
$R_{θJA}$	Junction-to-Ambient (PCB mount)**	----	50	
$R_{θJA}$	Junction-to-Ambient	----	110	

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	-100	–––	–––	V	V_{GS} = 0V, I_D = -250μA
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	–––	-0.12	–––	V/°C	Reference to 25°C, I_D = -1.0mA
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	–––	–––	0.205	Ω	V_{GS} = -10V, I_D = -7.8A ④
$V_{GS(th)}$	Gate Threshold Voltage	-2.0	–––	-4.0	V	V_{DS} = V_{GS}, I_D = -250μA
g_{fs}	Forward Transconductance	3.2	–––	–––	S	V_{DS} = -50V, I_D = -7.8A
I_{DSS}	Drain-to-Source Leakage Current	–––	–––	-25	μA	V_{DS} = -100V, V_{GS} = 0V
		–––	–––	-250		V_{DS} = -80V, V_{GS} = 0V, T_J = 150°C
I_{GSS}	Gate-to-Source Forward Leakage	–––	–––	100	nA	V_{GS} = 20V
	Gate-to-Source Reverse Leakage	–––	–––	-100		V_{GS} = -20V
Q_g	Total Gate Charge	–––	–––	58	nC	I_D = -8.4A
Q_{gs}	Gate-to-Source Charge	–––	–––	8.3		V_{DS} = -80V
Q_{gd}	Gate-to-Drain ("Miller") Charge	–––	–––	32		V_{GS} = -10V, See Fig. 6 and 13 ④⑥
$t_{d(on)}$	Turn-On Delay Time	–––	15	–––	ns	V_{DD} = 50V
t_r	Rise Time	–––	58	–––		I_D = -8.4A
$t_{d(off)}$	Turn-Off Delay Time	–––	45	–––		R_G = 9.1Ω
t_f	Fall Time	–––	46	–––		R_D =6.2Ω, See Fig. 10 ④⑥
L_D	Internal Drain Inductance	–––	4.5	–––	nH	Between lead, 6mm (0.25in.) from package
L_S	Internal Source Inductance	–––	7.5	–––		and center of die contact⑤ 
C_{iss}	Input Capacitance	–––	760	–––	pF	V_{GS} = 0V
C_{oss}	Output Capacitance	–––	260	–––		V_{DS} = -25V
C_{rss}	Reverse Transfer Capacitance	–––	170	–––		f = 1.0MHz, See Fig. 5⑥

Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	–––	–––	-13	A	MOSFET symbol showing the
I_{SM}	Pulsed Source Current (Body Diode) ①	–––	–––	-52		integral reverse p-n junction diode.
V_{SD}	Diode Forward Voltage	–––	–––	-1.6	V	T_J = 25°C, I_S = -7.8A, V_{GS} = 0V ④
t_{rr}	Reverse Recovery Time	–––	130	190	ns	T_J = 25°C, I_F = -8.4A
Q_{rr}	Reverse Recovery Charge	–––	650	970	nC	di/dt = 100A/μs ④⑥
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L_S+L_D)				

Notes:

① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11)

② Starting T_J = 25°C, L = 6.4mH R_G = 25Ω, I_{AS} = -7.8A. (See Figure 12)

③ $I_{SD} \le$ -7.8A, di/dt $\le$ 200A/μs, $V_{DD} \le V_{(BR)DSS}$, $T_J \le$ 150°C

④ Pulse width $\le$ 300μs; duty cycle $\le$ 2%.

⑤This is applied for I-PAK, L_S of D-PAK is measured between lead and center of die contact

⑥ Uses IRF9530N data and test conditions.

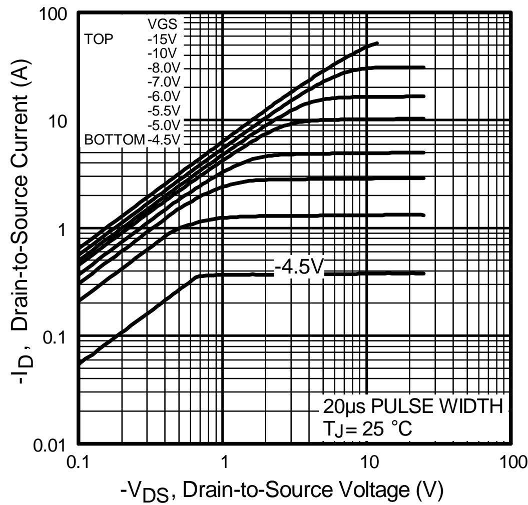


Fig 1. Typical Output Characteristics

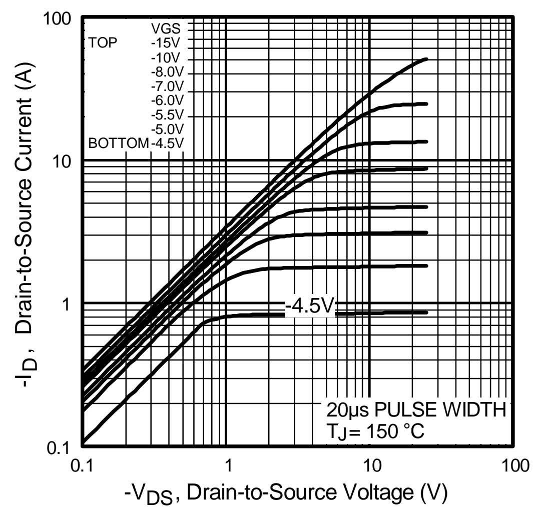


Fig 2. Typical Output Characteristics

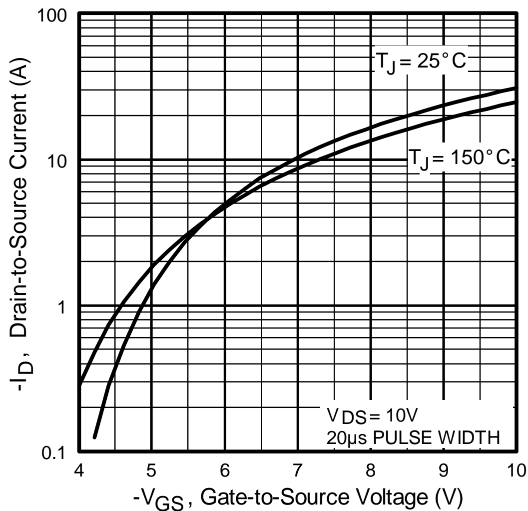


Fig 3. Typical Transfer Characteristics

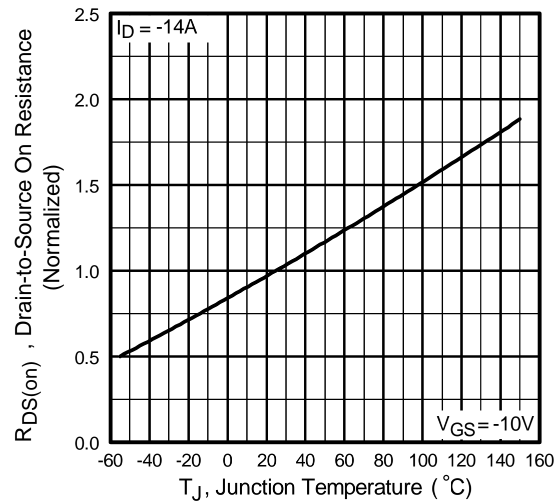


Fig 4. Normalized On-Resistance Vs. Temperature

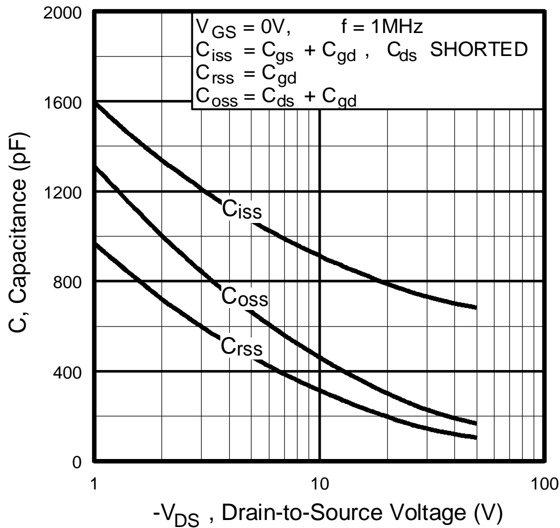


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

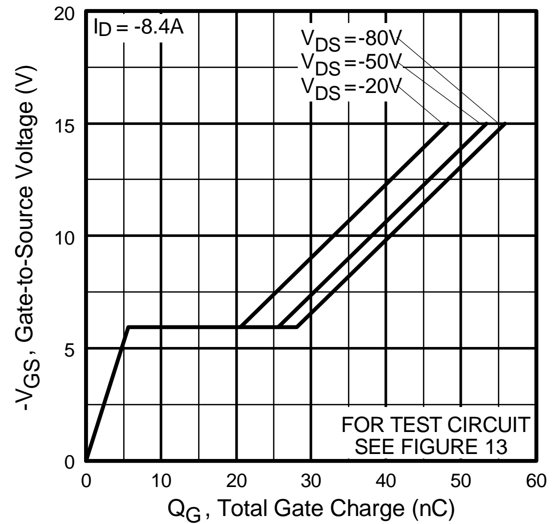


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

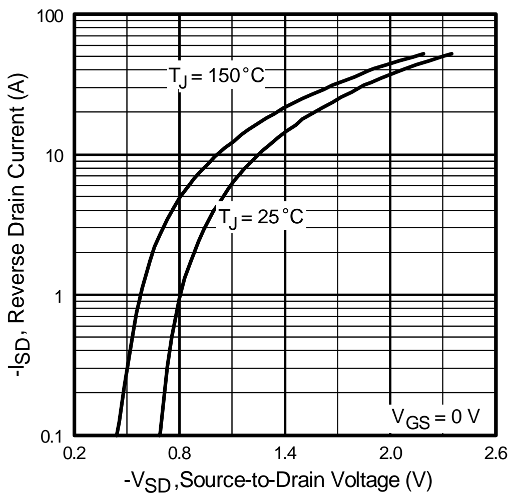


Fig 7. Typical Source-Drain Diode Forward Voltage

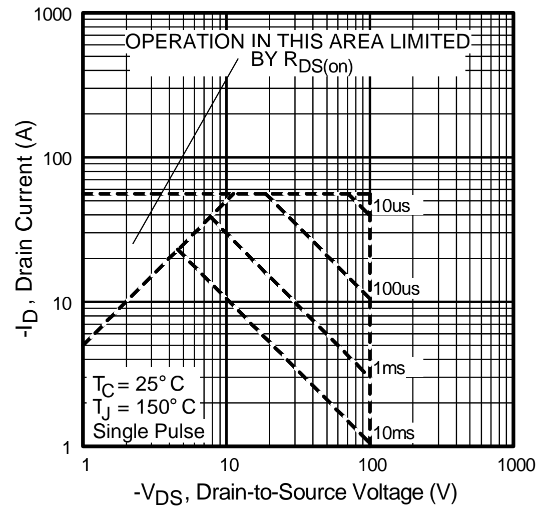


Fig 8. Maximum Safe Operating Area

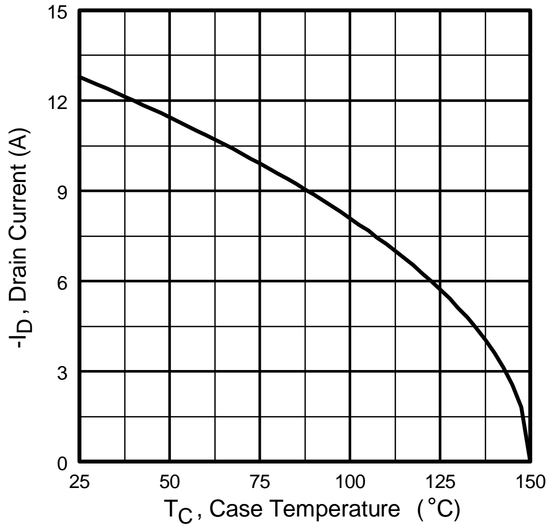


Fig 9. Maximum Drain Current Vs. Case Temperature

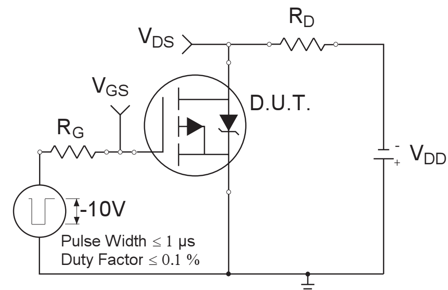


Fig 10a. Switching Time Test Circuit

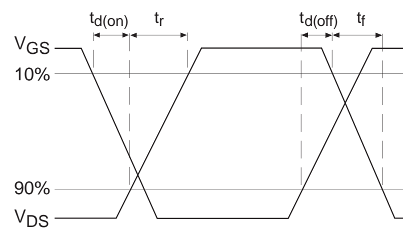


Fig 10b. Switching Time Waveforms

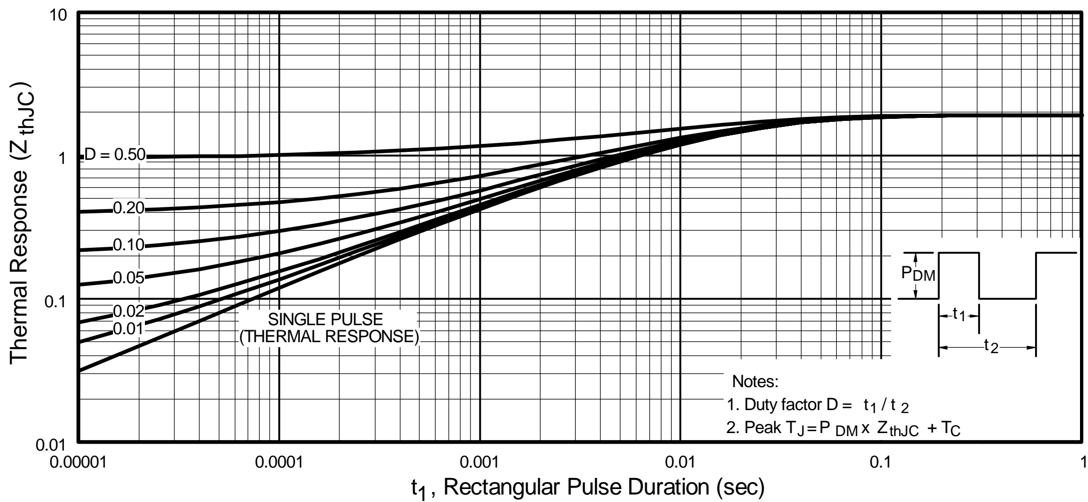


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

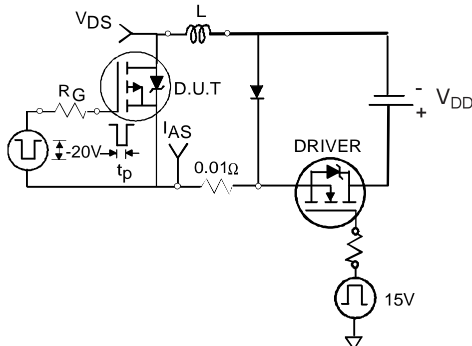
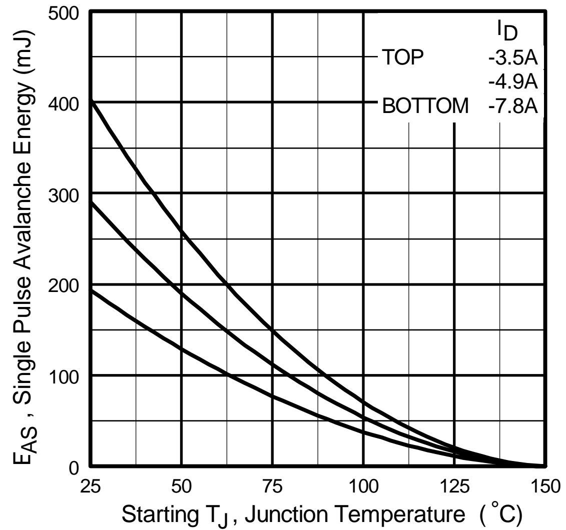


Fig 12a. Unclamped Inductive Test Circuit



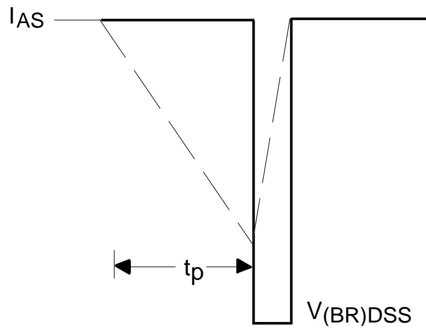


Fig 12b. Unclamped Inductive Waveforms

Fig 12c. Maximum Avalanche Energy Vs. Drain Current

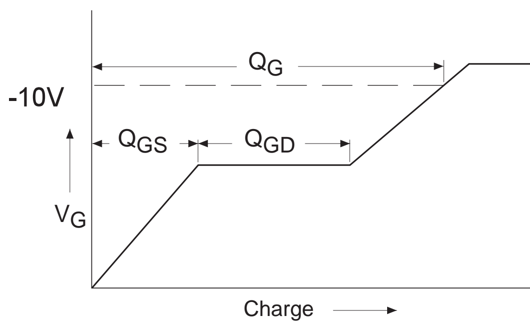


Fig 13a. Basic Gate Charge Waveform

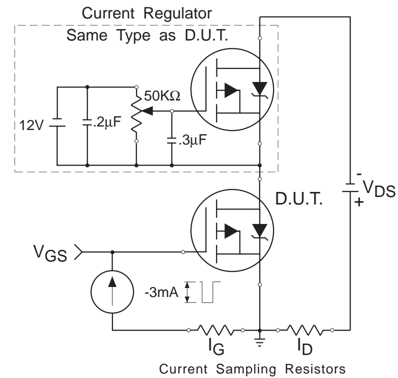
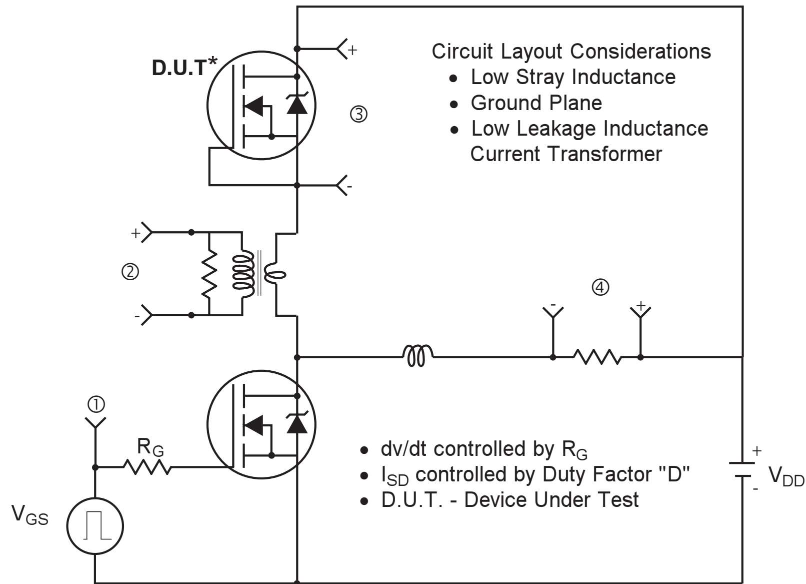


Fig 13b. Gate Charge Test Circuit

Peak Diode Recovery dv/dt Test Circuit



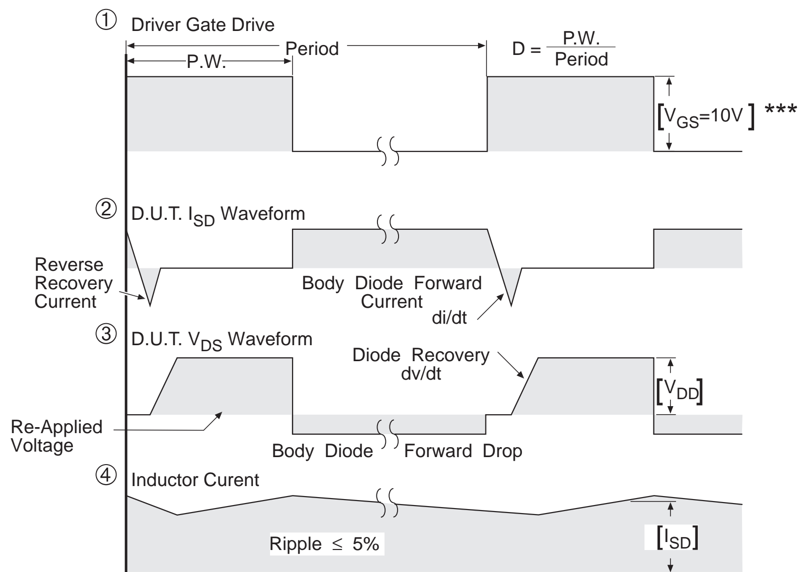
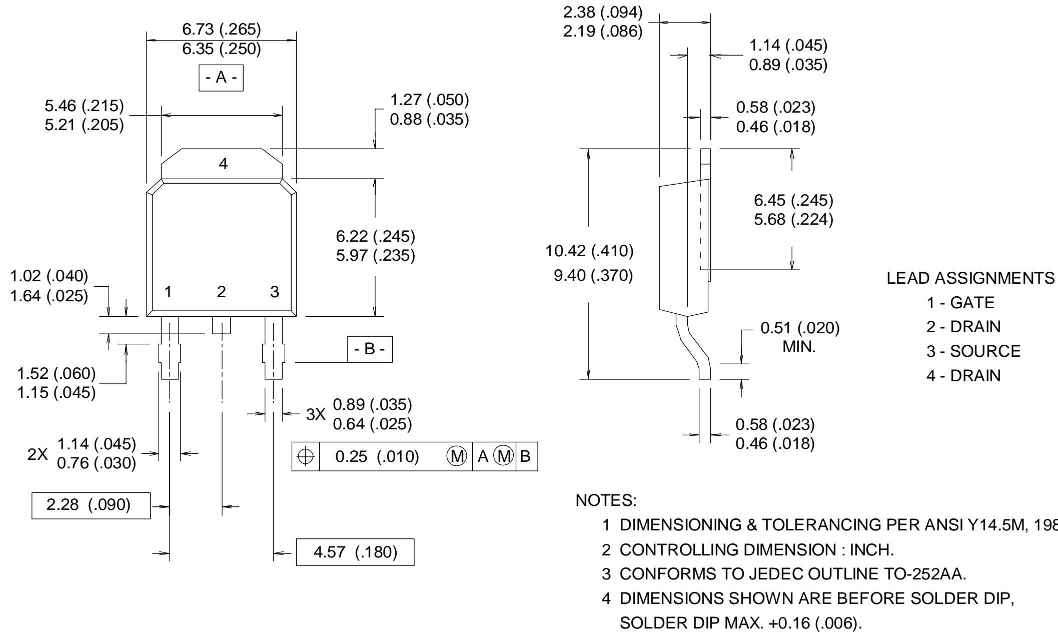


Fig 14. For P-Channel HEXFETS

Package Outline

TO-252AA Outline
Dimensions are shown in millimeters (inches)

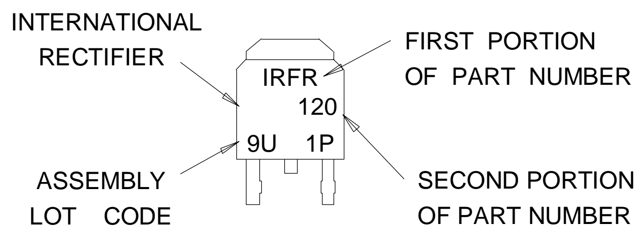


NOTES:
1 DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.
2 CONTROLLING DIMENSION : INCH.
3 CONFORMS TO JEDEC OUTLINE TO-252AA.
4 DIMENSIONS SHOWN ARE BEFORE SOLDER DIP, SOLDER DIP MAX. +0.16 (.006).

Part Marking Information

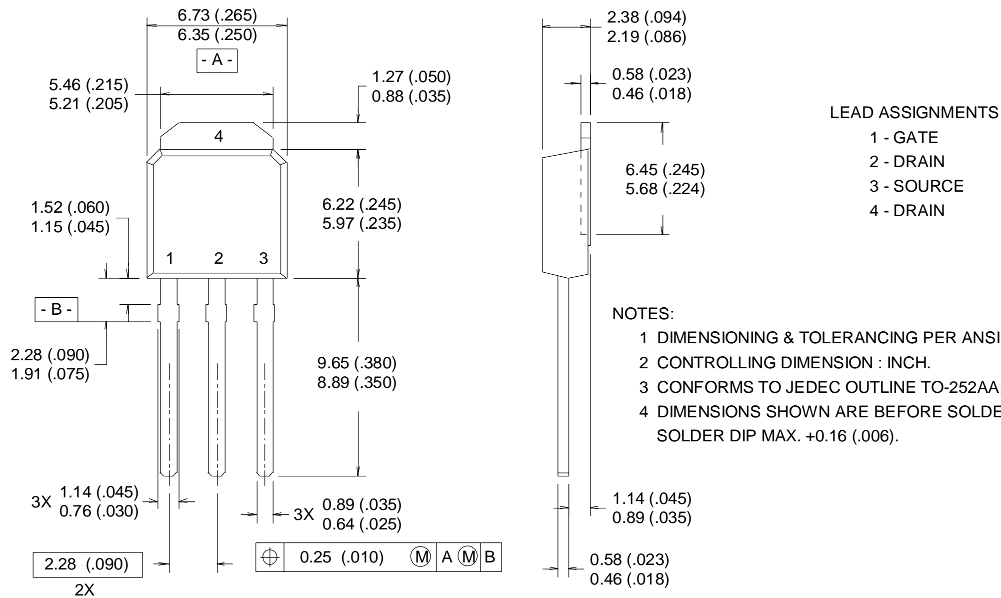
TO-252AA (D-Pak)

EXAMPLE : THIS IS AN IRFR120
WITH ASSEMBLY
LOT CODE 9U1P



Package Outline

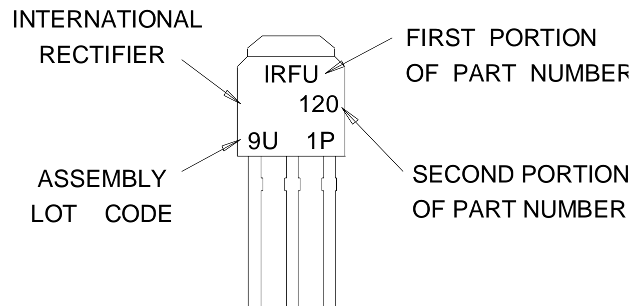
TO-251AA Outline
Dimensions are shown in millimeters (inches)



Part Marking Information

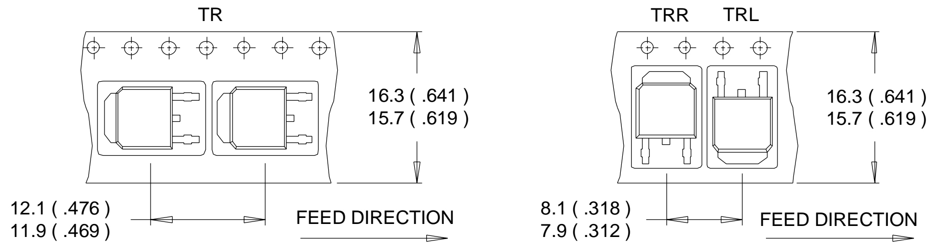
TO-251AA (I-Pak)

EXAMPLE : THIS IS AN IRFU120 WITH ASSEMBLY LOT CODE 9U1P

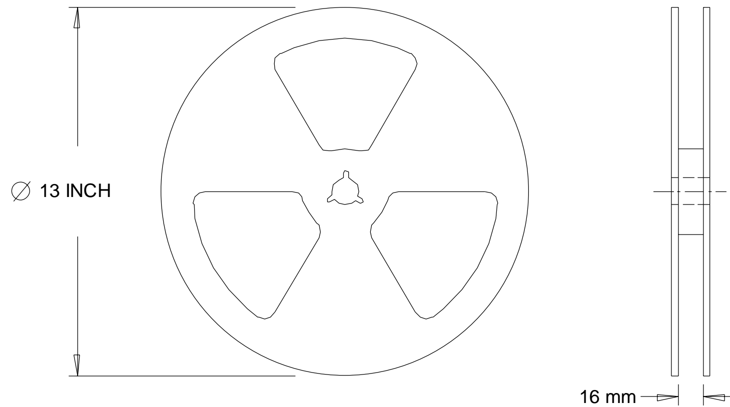


Tape & Reel Information

TO-252AA



NOTES :
1. CONTROLLING DIMENSION : MILLIMETER.
2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES).
3. OUTLINE CONFORMS TO EIA-481 & EIA-541.



NOTES :
1. OUTLINE CONFORMS TO EIA-481.