



SANYO Semiconductors

DATA SHEET

An ON Semiconductor Company

LV58063MC — Bi-CMOS LSI Step-down Switching Regulator

Overview

LV58063MC is a 1ch step-down switching regulator. 0.13Ω FET is incorporated on the upper side to achieve high-efficiency operation for large output current.

Low-heat resistance and compact-package SOP8L (200mil) employed.

Current mode control gives superior load current response with easy phase compensation.

EN pin, allowing the standby mode with the current drain of 70μA.

Pulse-by-pulse over-current protection and overheat protection available for protection of load devices.

Externally adjustable soft start time.

Features

- 3A 1ch step-down switching regulator
- Wide input range (8 to 28V)
- High efficiency (90% I_{OUT}=1A, V_{IN}=12V, V_{OUT}=5V)
- Standby mode
- Over-current protection
- Overshoot control after over-current protection event
- Thermal shutdown
- Reference voltage: 0.8V
- Fixed frequency: 370kHz
- Soft start
- Compact package: SOP8L (200mil) with exposed pad

Application

- LCD/PDP-TV
- STB
- White Goods
- Office equipment
- General consumer electronics

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Specifications

Absolute Maximum Ratings at $T_a = 25^\circ\text{C}$

Parameter	Conditions	Conditions	Ratings	Unit
Maximum input V_{IN} voltage	V_{IN} max		32	V
BOOT pin maximum voltage	V_{BT} max		37	V
SW pin maximum voltage	V_{SW} max		V_{IN} max	V
BOOT pin-SW pin maximum voltage	V_{BS-SW} max		7	V
FB, EN, COMP, SS pin maximum voltage	V_{fs} max		7	V
Allowable power dissipation	P_d max	Mount on a specified board *	2.05	W
Junction temperature	T_j max		150	$^\circ\text{C}$
Operating temperature	T_{opr}		-20 to +80	$^\circ\text{C}$
Storage temperature	T_{stg}		-40 to +150	$^\circ\text{C}$

* Specified board: 46.4mm × 31.8mm × 1.7mm, glass epoxy.

Note: Plan the maximum voltage while including coil and surge voltages, so that the maximum voltage is not exceeded even for an instant.

Recommended Operating Conditions at $T_a = 25^\circ\text{C}$

Parameter	Conditions	Conditions	Ratings	Unit
V_{IN} pin voltage	V_{IN}		8 to 28	V
BOOT pin voltage	V_{BT}		-0.3 to 34	V
SW pin voltage	V_{SW}		-0.4 to V_{IN}	V
BOOT pin-SW pin voltage	V_{BS-SW}		6.5	V
FB, EN, COMP, SS pin voltage	V_{FSO}		6	V

Electrical Characteristics at $T_a = 25^\circ\text{C}$ $V_{IN} = 12\text{V}$, unless otherwise specified.

Parameter	Conditions	Conditions	Ratings			Unit
			min	typ	max	
IC current drain at standby	I_{CC1}	EN=0V		70		μA
IC current drain in operation	I_{CC2}	EN=open, FB=1V		5		mA
Efficiency	Effcy	$V_{IN}=12\text{V}$, $I_{OUT}=1\text{A}$, $V_O=5\text{V}$ Design target: *1		90		%
Reference voltage	V_{ref}	$V_{IN}=8\text{V}$ to 28V ($\pm 2\%$)	-2%	0.8	+2%	V
FB pin bias current	I_{ref}	FB=0.8V application		10	100	nA
High-side ON resistance	R_{onH}	BOOT=5V		0.13		Ω
Low-side ON resistance	R_{onL}			7		Ω
Oscillation frequency	F_{OSC}		296	370	444	kHz
Oscillation frequency during short-circuit protection	F_{OSCS}		30	38	46	kHz
EN high-threshold voltage	V_{enh}				1.9	V
EN low-threshold voltage	V_{enl}		0.8			V
EN pull-up current	I_{en}	EN=0V		16		μA
Maximum ON DUTY	D max			80		%
Current limit peak value 1	I_{cl1}	$V_{IN}=12\text{V}$, $V_{OUT}=5\text{V}$, $L=10\mu\text{H}$	3.8			A
Thermal shutdown temperature	T_{tsd}	*Design guarantee *2		160		$^\circ\text{C}$
Thermal shutdown temperature hysteresis	D_{tsd}	*Design guarantee *2		40		$^\circ\text{C}$
Soft start current	I_{SS}	SS=0V	6	10	14	μA

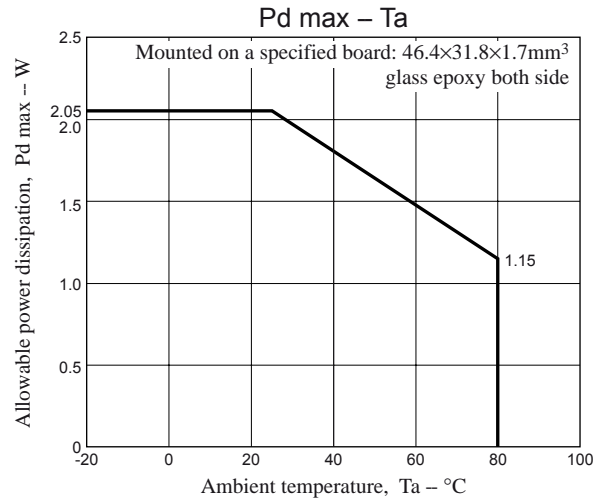
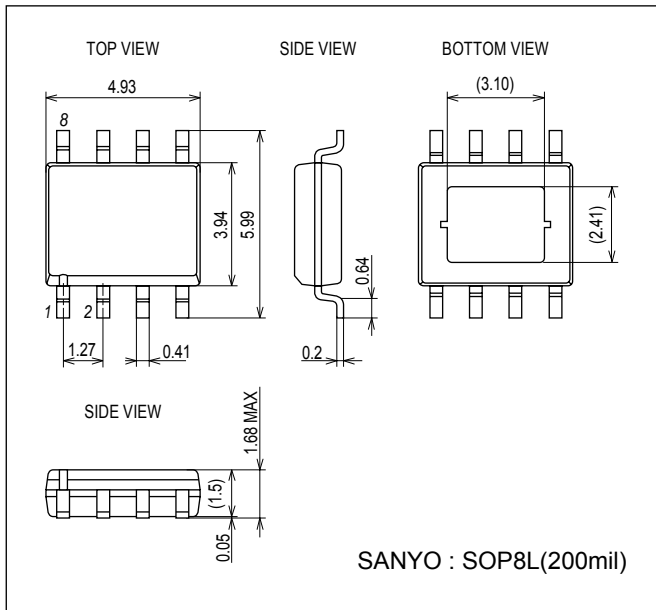
*1: Reference value (not tested before shipment)

*2: Design guarantee (value guaranteed by design and not tested before shipment)

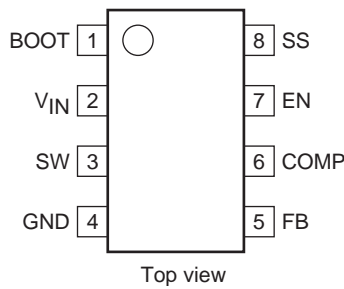
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Package Dimensions

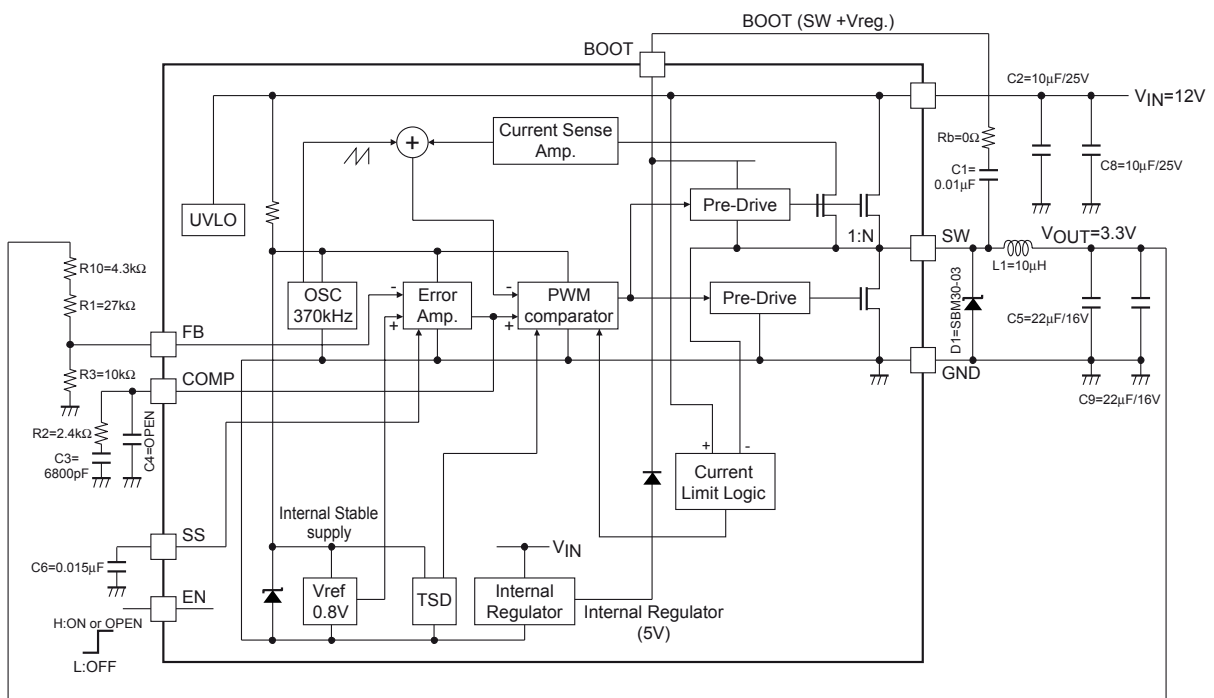
unit : mm (typ)
3439



Pin Assignment



Block Diagram and Sample Application Circuit (3.3V output)



- C1,C8,C5,C9 = Ceramic capacitor
- L1=CDRH105RNP-100NC (sumida)

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Pin Function

Pin No.	Pin name	Description	Equivalent Circuit
1	BOOT	Internal high side nmos fet boot strap capacitor terminal. Connect around 22nF capacitor or greater between SW and BOOT. To operate within absolute maximum rating of SW, to keep stable operation, and to reduce switching noise, please, use a series resistor, Rb (value is around 100Ω) is recommended to use.	
2	V _{IN}	Input Voltage Pin. Large Filter Capacitor (equal or larger than 20μF) should be connected between V _{IN} and GND to eliminate noise on the input and to operate properly.	See BOOT
3	SW	Power Switching Pin. Connect the output LC filter. Connect the above-mentioned capacitor between this pin and BOOT pin.	See BOOT
4	GND	Ground pin.	
5	FB	Feedback pin. Connect a voltage divider resistor across FB to set the regulated output voltage. The output voltage is given by next equation. $V_{OUT} = V_{ref} \times \left\{ 1 + \frac{(R1 + R10)}{R3} \right\}$ V _{ref} = 0.8V Example: 3.3V output voltage (See Block Diagram and Sample Application Circuit) $V_{OUT} = 0.8 \times \left\{ 1 + \frac{(27k + 4.3k)}{10k} \right\}$ =3.304V	
6	COMP	Phase compensation pin. Connect an external capacitor and a resistor for the DC DC converter close loop-phase compensation.	
7	EN	Enable terminal. If applying logically high voltage, or left open, the converter operates. If connected to GND, the converter's operation stops.	

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Pin No.	Pin name	Description	Equivalent Circuit
8	SS	Soft start terminal Internal source current (10μA) and external capacitor will make soft start time. Soft start capacitor, C6 is given by next equation, $C6 = 10\mu A \times \frac{T_{ss}}{V_{ref}}$ Where, Tss : soft start time, Vref : reference voltage Example : soft start time = 1.2ms $C6 = 10\mu A \times \frac{1.2ms}{0.8V} = 0.015\mu F$	See FB

Considerations for the design

- Insertion of serial beads in the Schottky diode for removal of noise may cause generation of the negative voltage on SW pin deviating from the absolute maximum rating at the SW pin, resulting in failure of normal operation. Please, do not insert beads as above described. Instead, remove noise by Rb resistor.
- Exposed pad on the bottom side of the IC should be soldered. We cannot recommend other usages of the exposed pad.

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