

## SWITCHING REGULATOR APPLICATIONS

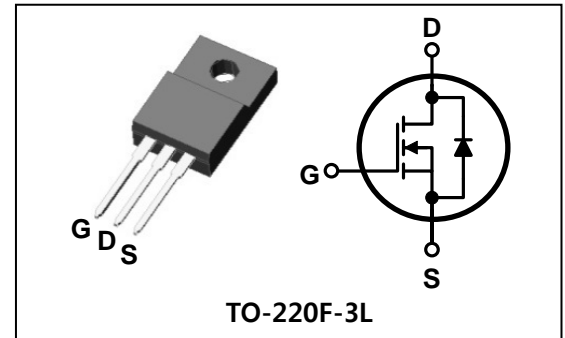
### Features

- High Voltage :  $BV_{DSS}=500V(\text{Min.})$
- Low  $C_{RSS}$  :  $C_{RSS}=33pF(\text{Typ.})$
- Low gate charge :  $Qg=16nC(\text{Typ.})$
- Low  $R_{DS(on)}$  :  $R_{DS(on)}=1.5\Omega(\text{Max.})$

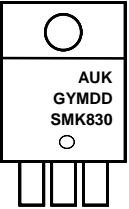
### Ordering Information

Type No.	Marking	Package Code
SMK830FC	SMK830	TO-220F-3L (C Forming)

### PIN Connection



### Marking Diagram

	Column 1 : Manufacturer
	Column 2 : Production Information e.g.) GYMDD -. G : Factory management code -. YMDD : Date Code (year, month, date)
	Column 3 : Device Code

### Absolute maximum ratings ( $T_C=25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Rating	Unit	
Drain-source voltage	$V_{DSS}$	500	V	
Gate-source voltage	$V_{GSS}$	$\pm 30$	V	
Drain current (DC) *	$I_D$	$T_C=25^\circ\text{C}$	4.5	A
		$T_C=100^\circ\text{C}$	2.8	A
Drain current (Pulsed) *	$I_{DM}$	18	A	
Drain power dissipation	$P_D$	30	W	
Avalanche current (Single) ②	$I_{AS}$	4.5	A	
Single pulsed avalanche energy ②	$E_{AS}$	472	mJ	
Avalanche current (Repetitive) ①	$I_{AR}$	4.5	A	
Repetitive avalanche energy ①	$E_{AR}$	5.0	mJ	
Junction temperature	$T_J$	150	$^\circ\text{C}$	
Storage temperature range	$T_{stg}$	-55~150	$^\circ\text{C}$	

\* Limited by maximum junction temperature

Characteristic	Symbol	Typ.	Max.	Unit
Thermal resistance	Junction-case	-	4.16	$^\circ\text{C}/\text{W}$
	Junction-ambient	-	62.5	

## Electrical Characteristics (T<sub>C</sub>=25°C unless otherwise noted)

Characteristic	Symbol	Test Condition	Min.	Typ.	Max.	Unit	
Drain-source breakdown voltage	V <sub>(BR)DSS</sub>	I <sub>D</sub> =250 μA, V <sub>GS</sub> =0V	500	-	-	V	
Gate threshold voltage	V <sub>GS(th)</sub>	I <sub>D</sub> =250 μA, V <sub>DS</sub> =V <sub>GS</sub>	2.0	-	4.0	V	
Drain-source cut-off current	I <sub>DSS</sub>	V <sub>DS</sub> =500V, V <sub>GS</sub> =0V	-	-	1	μA	
Gate leakage current	I <sub>GSS</sub>	V <sub>DS</sub> =0V, V <sub>GS</sub> =±30V	-	-	±100	nA	
Drain-source on-resistance ④	R <sub>DS(on)</sub>	V <sub>GS</sub> =10V, I <sub>D</sub> =2.25A	-	1.2	1.5	Ω	
Forward transfer conductance ④	g <sub>fs</sub>	V <sub>DS</sub> =10V, I <sub>D</sub> =2.25A	-	5.2	-	S	
Input capacitance	C <sub>iss</sub>	V <sub>GS</sub> =0V, V <sub>DS</sub> =25V f=1 MHz	-	745	930	pF	
Output capacitance	C <sub>oss</sub>		-	82	102		
Reverse transfer capacitance	C <sub>rss</sub>		-	33	42		
Turn-on delay time	t <sub>d(on)</sub>	V <sub>DD</sub> =250V, I <sub>D</sub> =4.5A R <sub>G</sub> =12Ω	-	12	-	ns	
Rise time	t <sub>r</sub>		-	46	-		
Turn-off delay time	t <sub>d(off)</sub>		③④	-	50		-
Fall time	t <sub>f</sub>		-	48	-		
Total gate charge	Q <sub>g</sub>	V <sub>DS</sub> =400V, V <sub>GS</sub> =10V I <sub>D</sub> =4.5A	-	16	20	nC	
Gate-source charge	Q <sub>gs</sub>		③④	-	5.5		-
Gate-drain charge	Q <sub>gd</sub>		-	4.0	-		

## Source-Drain Diode Ratings and Characteristics (T<sub>C</sub>=25°C unless otherwise noted)

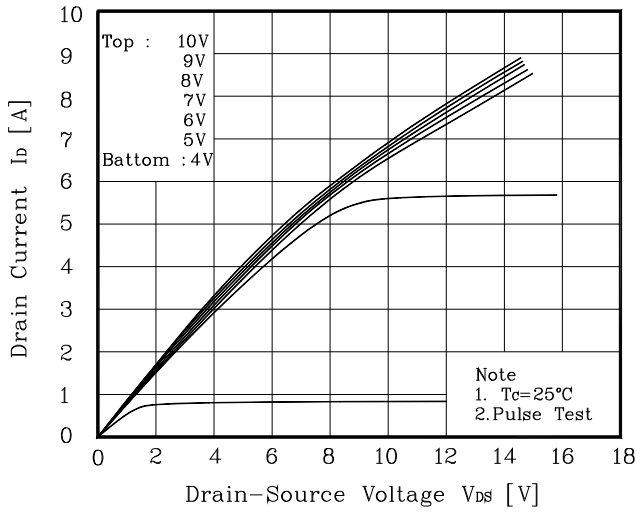
Characteristic	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Source current (DC)	I <sub>S</sub>	Integral reverse diode in the MOSFET	-	-	4.5	A
Source current (Pulsed) ①	I <sub>SP</sub>		-	-	18	
Forward voltage ④	V <sub>SD</sub>	V <sub>GS</sub> =0V, I <sub>S</sub> =4.5A	-	-	1.4	V
Reverse recovery time	t <sub>rr</sub>	I <sub>S</sub> =4.5A, V <sub>GS</sub> =0V dI <sub>S</sub> /dt=100A/μs	-	263	-	ns
Reverse recovery charge	Q <sub>rr</sub>		-	1.9	-	μC

Note ;

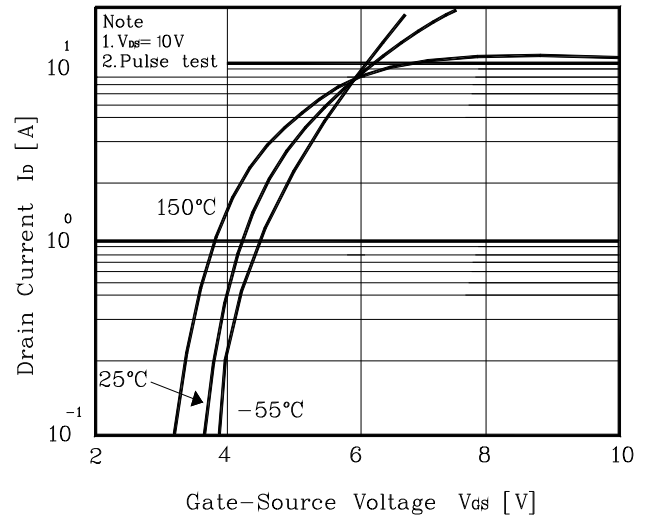
- ① Repetitive rating : Pulse width limited by maximum junction temperature
- ② L=42mH, I<sub>AS</sub>=4.5A, V<sub>DD</sub>=50V, R<sub>G</sub>=27Ω
- ③ Pulse Test : Pulse width≤400 μs, Duty cycle≤2%
- ④ Essentially independent of operating temperature

## Electrical Characteristic Curves

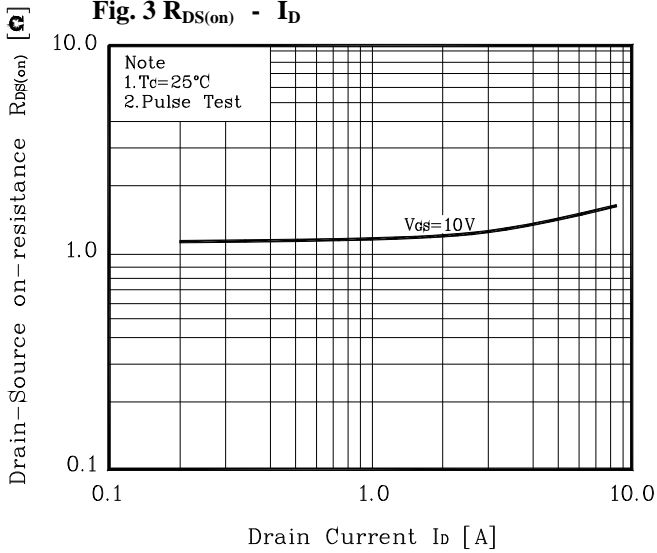
**Fig. 1  $I_D - V_{DS}$**



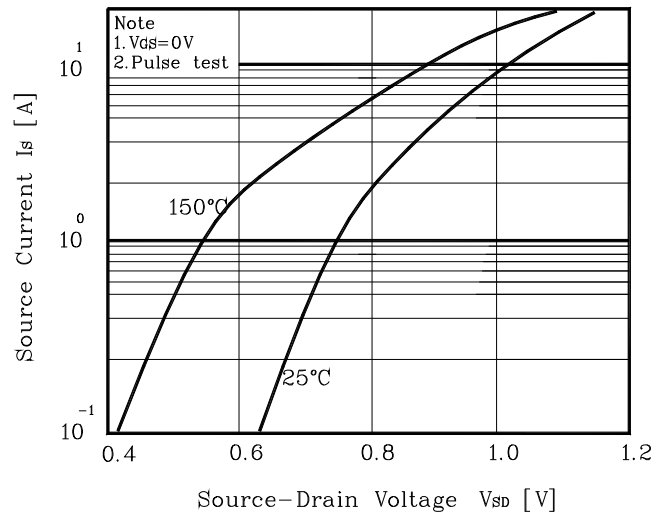
**Fig. 2  $I_D - V_{GS}$**



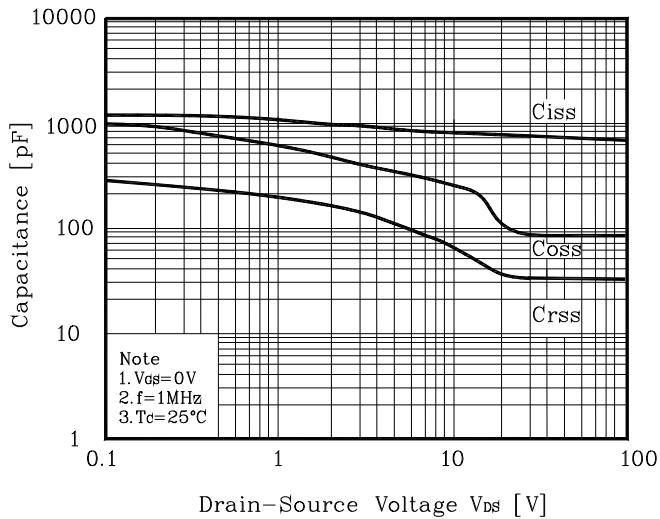
**Fig. 3  $R_{DS(on)} - I_D$**



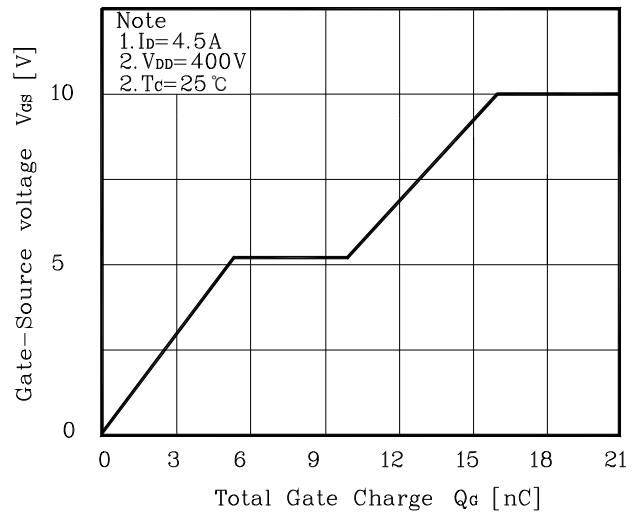
**Fig. 4  $I_S - V_{SD}$**



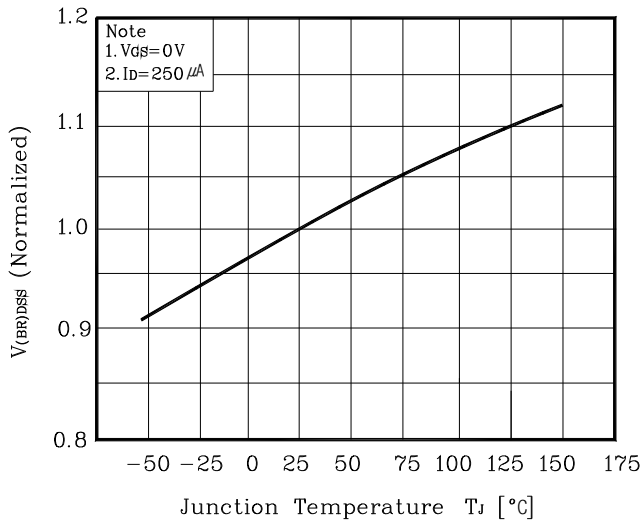
**Fig. 5 Capacitance -  $V_{DS}$**



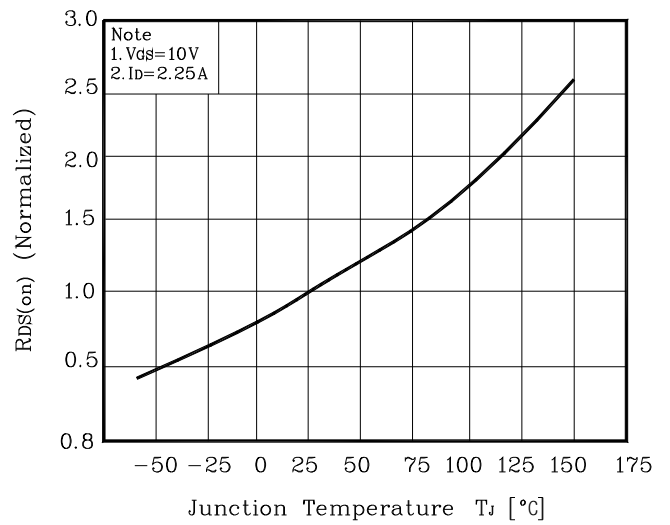
**Fig. 6  $V_{GS} - Q_G$**



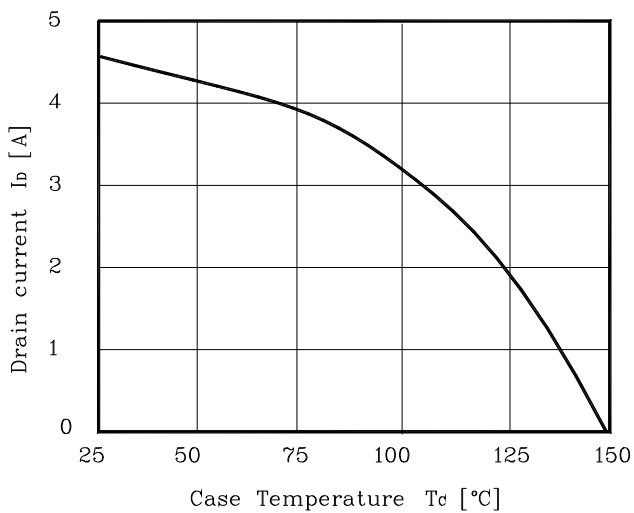
**Fig. 7**  $V_{(BR)DSS} - T_J$



**Fig. 8**  $R_{DS(on)} - T_J$



**Fig. 9**  $I_D - T_C$



**Fig. 10** Safe Operating Area

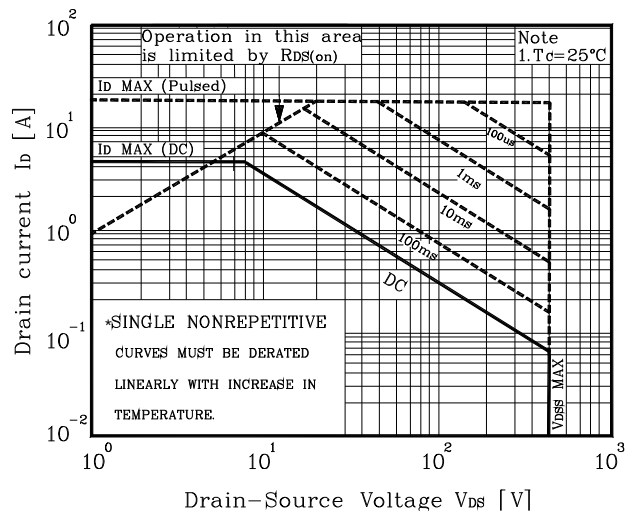


Fig. 11 Gate Charge Test Circuit & Waveform

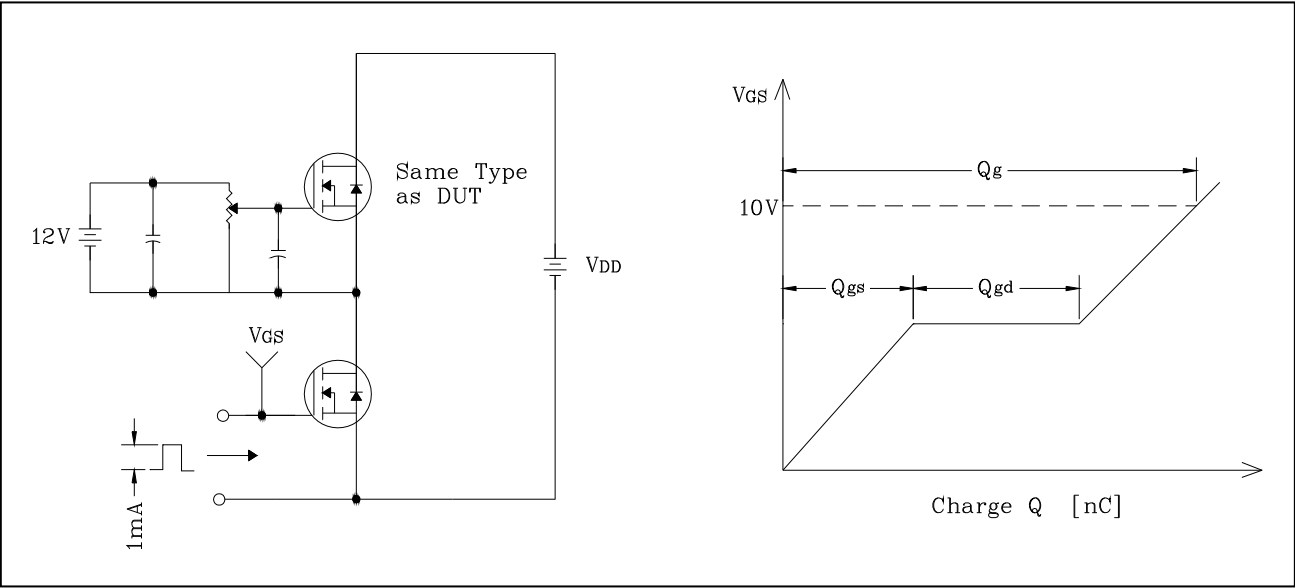


Fig. 12 Switching Time Test Circuit & Waveform

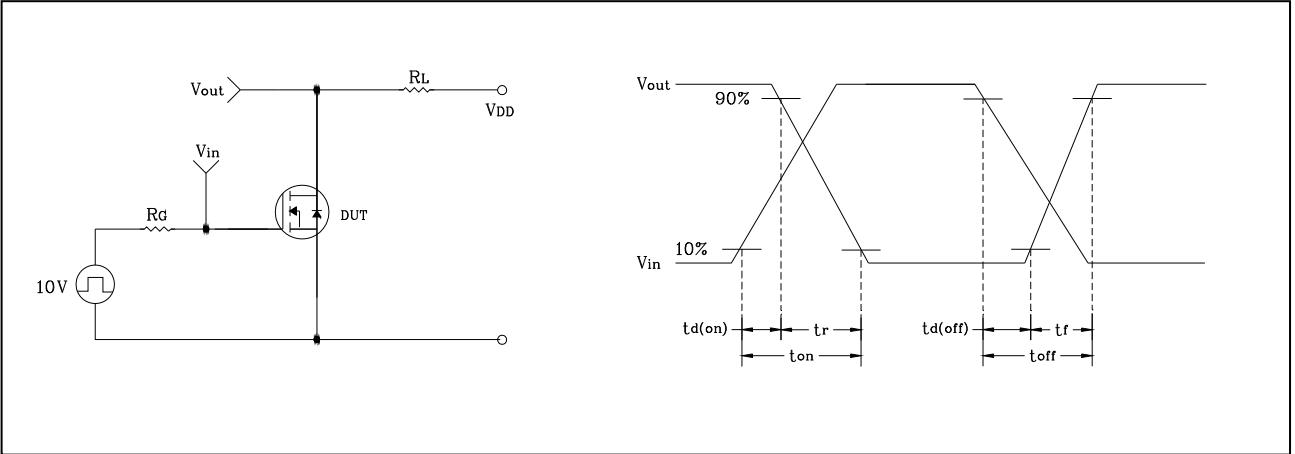


Fig. 13  $E_{AS}$  Test Circuit & Waveform

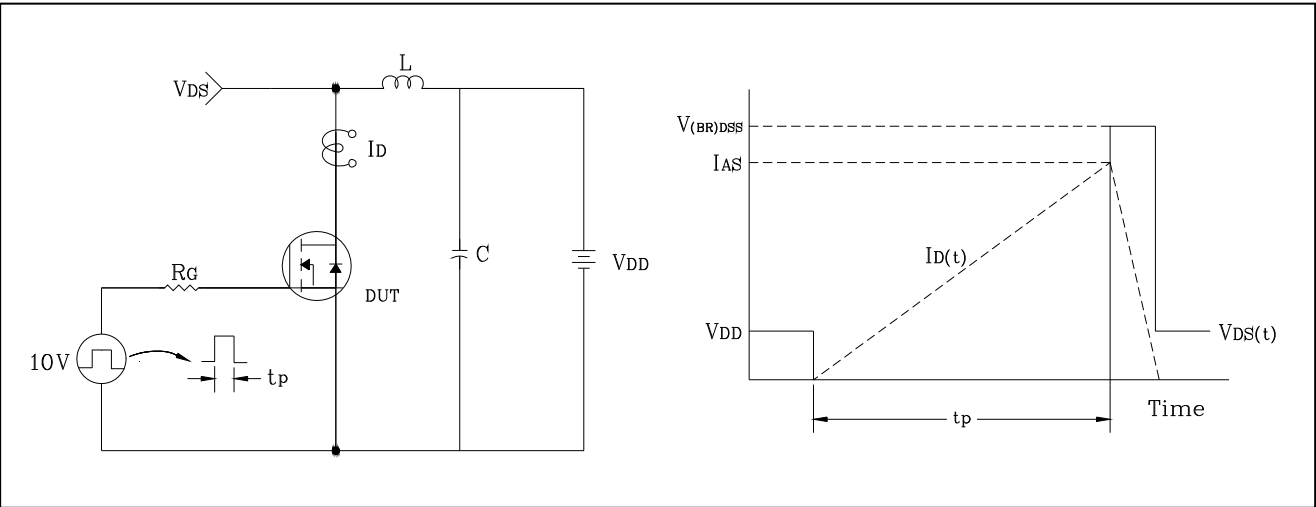
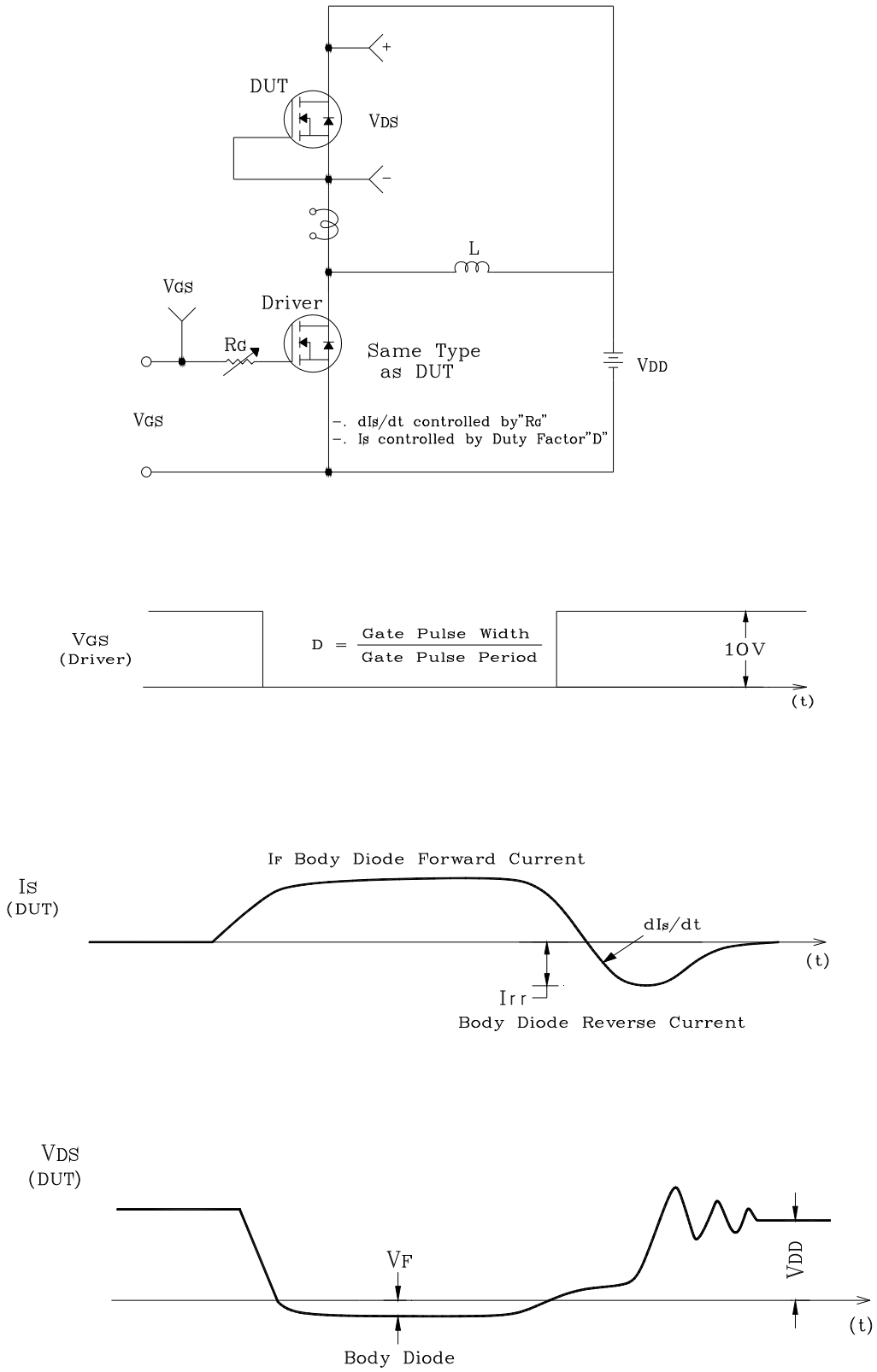
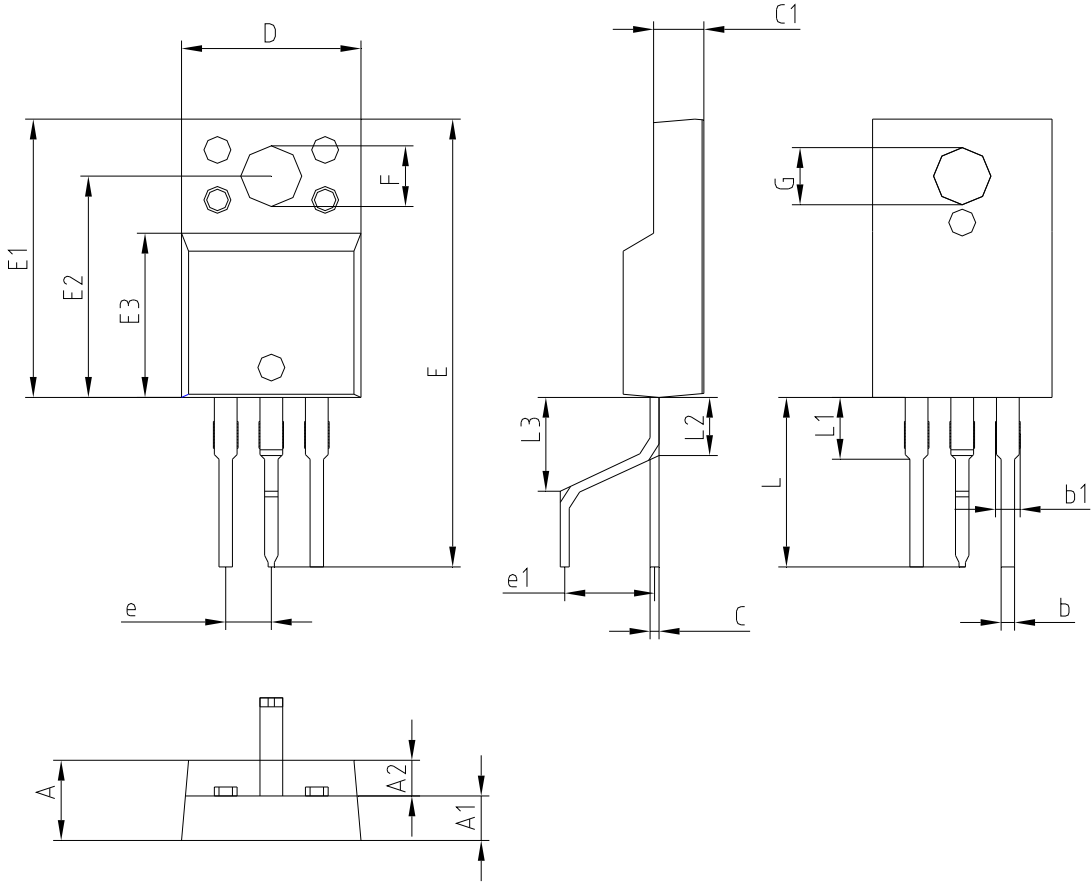


Fig. 14 Peak Diode Recovery dv/dt Test Circuit & Waveform



## Outline Dimension

unit : mm



SYMBOL	MILLIMETERS			NOTE
	MINIMUM	NOMINAL	MAXIMUM	
A	-	-	4.60	
A1	2.45	2.50	2.55	
A2	1.95	2.00	2.05	
b	0.65	0.75	0.85	
b1	1.07	1.27	1.47	
C	0.40	0.50	0.60	
C1	2.70	2.80	2.90	
D	9.90	10.00	10.10	
E	24.61	-	25.61	
E1	15.50	15.60	15.70	
E2	12.30	12.40	12.50	
E3	9.15	9.20	9.25	
F	3.30	3.40	3.50	
G	3.10	3.20	3.30	
e	2.54 BSC			
e1	4.70	5.00	5.30	
L	9.01	-	10.01	
L1	3.46 BSC			
L2	3.26 BSC			
L3	5.26 BSC			

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