TOSHIBA

Toshiba TC86R4400 MIPS RISC High Performance Microprocessor

Toshiba is the leading silicon vendor licensed to develop, manufacture and sell MIPS® Reduced Instruction Set Computing (RISC)-based products. Toshiba's R4400-based systems will run a choice of advanced operating systems, such as UNIX® and Windows NT™ from Microsoft Corporation.

Toshiba is the key supplier of MIPS Reduced Instruction Set Computing (RISC) technology for the computer system and embedded control markets. From the introduction of the R2000™, Toshiba has been a foundry for MIPS RISC-based products. Since then, the R3000, R4000 and R4400 processors have been gaining wide acceptance and have been designed into a variety of products by industry-leading companies.

In 1991, Toshiba delivered one of the first R4000 components, displaying its strength in advanced process technology applied to high-end microprocessors. With a leading combination of highest overall performance, 64-bit architecture and design flexibility, Toshiba's R4400 establishes the standard for RISC microprocessors through the end of this decade.

R4400 Performance

The single-chip R4400 delivers the high performance necessary for a wide range of applications while maintaining full software compatibility with previous generations of MIPS microprocessors. Its scalable performance makes it possible to design the R4400 into applications ranging from embedded controllers, such as those in satellites and telephone switches, to computers ranging from laptops to mainframe-class servers. In designing the R4400, the basic components of the central CPU subsystem, including integer processor, floating point co-processor, memory management unit and primary cache, were integrated onto a single chip. In addition, the R4400 includes full multiprocessing capabilities, superpipelining, and control and management facilities for external secondary cache.

The R4400 is offered in two variants tailored for multiple price/performance points:

- The R4400SC supports high-performance uniprocessor designs with secondary cache
- The R4400MC is the full multiprocessing version of the product and supports both secondary cache and cache coherence mechanisms necessary for synchronizing multiple processors

The R4400 family provides a balanced mix in integer and floating point performance. Through superpipelining, RISC optimization techniques and on-chip integration, high integer performance is achieved for applications such as databases, graphics, spreadsheets and word processing. Superpipelining increases throughput by putting more instructions into the pipeline at the same time. RISC optimization techniques streamline processing operations by minimizing interruptions to the steady progress of the pipeline. In addition, on-chip integration takes more functionality off the board and puts it directly onto the processor to shorten paths and reduce lengthy accesses to main memory.

In the R4400 design, superpipelining requires less circuitry than other multiple-instruction issue techniques, so it leaves more room on the chip for other functions. Further, superpipelining provides greater integer processing than most other techniques whose benefits are confined mainly to floating-point operations. This results in higher overall performance from integer and floating-point units, a desirable characteristic in a microprocessor that is to have broad-based acceptance and applications.

The R4400 takes advantage of optimization techniques built into the MIPS compiler software to run applications faster than other RISC processors at similar or higher clock speeds. With RISC, the microprocessor design is streamlined by eliminating less frequently used instructions and circuitry, shifting the balance of computing from hardware to compiler software. Compilers offered by MIPS have been simultaneously developed and integrated with the R4400 from the start to deliver maximum performance.

Table 1. TC86R4400SC/MC Options

Internal Frequency	External Frequency	Voltage	Temperature	Internal Cache	Package (PGA)
150 MHz	75 MHz	3.3V	70°C	16KI + 16KD	447-pin
175 MHz	87 MHz	3.3V	70°C	16KI + 16 KD	447-pin
200 MHz	100 MHz	3.3V	70°C	16KI + 16 KD	447-pin
200 MHz	100 MHz	3.3V	85°C	16KI + 16 KD	447-pin
200 MHz	100 MHz	3.45V	70°C	16KI + 16 KD	447-pin
250 MHz	125 MHz	3.45V	70°C	16KI + 16 KD	447-pin

R4400SC Microprocessor

Toshiba's R4400SC 64-bit microprocessor and an advanced operating system, like Windows NT™, gives the designer the ability to address new expectations in the mainstream system and high-end server/workstation market at unbeatable price/performance points. R4400SC-based systems can run a choice of advanced operating systems, such as Windows NT and UNIX® which protect end user software investments while also providing an open software environment, are two important achievements for Toshiba in meeting the mainstream and high-end PC market needs. The R4400SC operates from 150MHz (input clock 75 MHz) to 250MHz (input clock 125MHz), and can sustain performance in excess of 175SPECint92.

R4400SC Overview

Toshiba's R4400SC is a highly integrated, single-chip RISC microprocessor designed for high-performance uniprocessor systems with secondary cache support. The R4400SC provides complete application software compatibility with the MIPS R2000, R3000, R4000, and R8000 processors. High integer performance, as well as floating-point performance, has been achieved through a number of techniques such as superpipelining, on-chip data and instruction caches, a pipelined floating point unit, support for two level cache memory and a high-performance on-chip TLB. The R4400SC provides a compatible, timely and necessary path from 32-bit to true 64-bit computing for users and software developers.

R4400SC Features

- True 64-bit microprocessor with 64-bit integer and floating-point operations, registers and virtual addresses
- Fully compatible with earlier 32-bit MIPS microprocessor.
- Dual instruction issue with no restrictions on the type of instruction issued
- On-chip Memory Management Unit (MMU) containing a fully associative TLB whose entries have a variable page size ranging from 4Kbyte to 16Mbyte
- On-chip ANSI/IEEE-754 standard floating-point unit with precise exceptions
- 32 doubleword (64-bit) general-purpose registers and 32 doubleword floating-point registers
- 36-bit physical address accessing 64GB of physical memory
- Built in primary direct mapped caches with parity protection:
  - 16KB instruction cache
  - 16KB data cache
  - Buffered write back with Configurable 4 or 8 word line size
- R4400SC also has built-in direct mapped secondary cache support:
  - The secondary cache can range from 128Kbytes to 4Mbytes
  - 128-bit interface to minimize cache miss latency
  - Timing flexibility for 128-bit secondary cache interface
  - ECC protection
- 64-bit system interface to allow speed matching of logic and memory components
- Dynamically configurable big-endian or little-endian byte ordering

In order to achieve the high performance required in a third generation RISC design, the TC86R4400SC exploits instruction-level parallelism using a superpipelined micro-instruction. The TC86R4400SC implements an 8-stage superpipeline which places no restrictions on instruction issue. Any two instructions can be issued each cycle under normal circumstances. Since the superpipeline places no restrictions on the order of instruction issue, the full benefit of the TC86R4400SC can be realized by existing application programs without any need for recompilation. The internal pipeline of the TC86R4400SC operates at frequency from 150MHz to 200MHz, which is twice the external clock frequency.

R4400MC Microprocessor

TC86R4400MC-based multiprocessor computer systems can run a choice of advanced operating systems, such as Windows NT, UNIX and Univel. Protecting the end user software investments and also providing an open software environment are two important achievements in meeting the high-end market needs. The TC86R4400MC operates at frequencies from 150MHz internal (external clock 75MHz) to 250MHz internal (125MHz external), and can sustain performance in excess of 175SPECint92.

R4400MC Overview

Toshiba R4400MC is a highly integrated, single-chip RISC microprocessor designed for high-performance multiprocessing systems. The R4400MC provides complete application-software compatibility with the MIPS R2000, R3000, R4400 and R8000 processors. High integer performance, as well as floating-point performance, has been achieved through a number of techniques such as superpipelining, on-chip data and instruction caches, a pipelined floating point unit, support for two level cache memory and a high-performance on-chip TLB. The R4400MC provides a compatible, timely and necessary path from 32-bit to true 64-bit computing for users and software developers.

R4400MC Features

- True 64-bit microprocessor with 64-bit integer and floating-point operations, registers and virtual addresses
- Fully compatible with earlier 32-bit MIPS microprocessors
- Dual instruction issue with no restrictions on the type of instruction issued
- Built-in support for multiprocessing
- On-chip Memory Management Unit (MMU) containing a fully associative TLB whose entries have a variable page size ranging from 4KB to 16MB
- On-chip ANSI/IEEE-754 standard floating-point unit with precise exceptions
- 32 doubleword (64-bit) general-purpose registers and 32 doubleword floating-point registers
- 36-bit physical address accessing 64GB of physical memory
- Built-in primary direct mapped caches with parity protection:
  - 16KB instruction cache
  - 16KB data cache
  - Buffered write back with configurable 4 or 8 word line size
- Built-in direct mapped secondary cache support:
  - The secondary cache can range from 128KB to 4MB
  - 128-bit interface to minimize cache miss latency
  - Timing flexibility for 128-bit secondary cache interface
  - 64-bit system interface to allow speed matching of logic and memory components with multiprocessing support
  - ECC protection
- Dynamically configurable big-endian or little-endian byte ordering

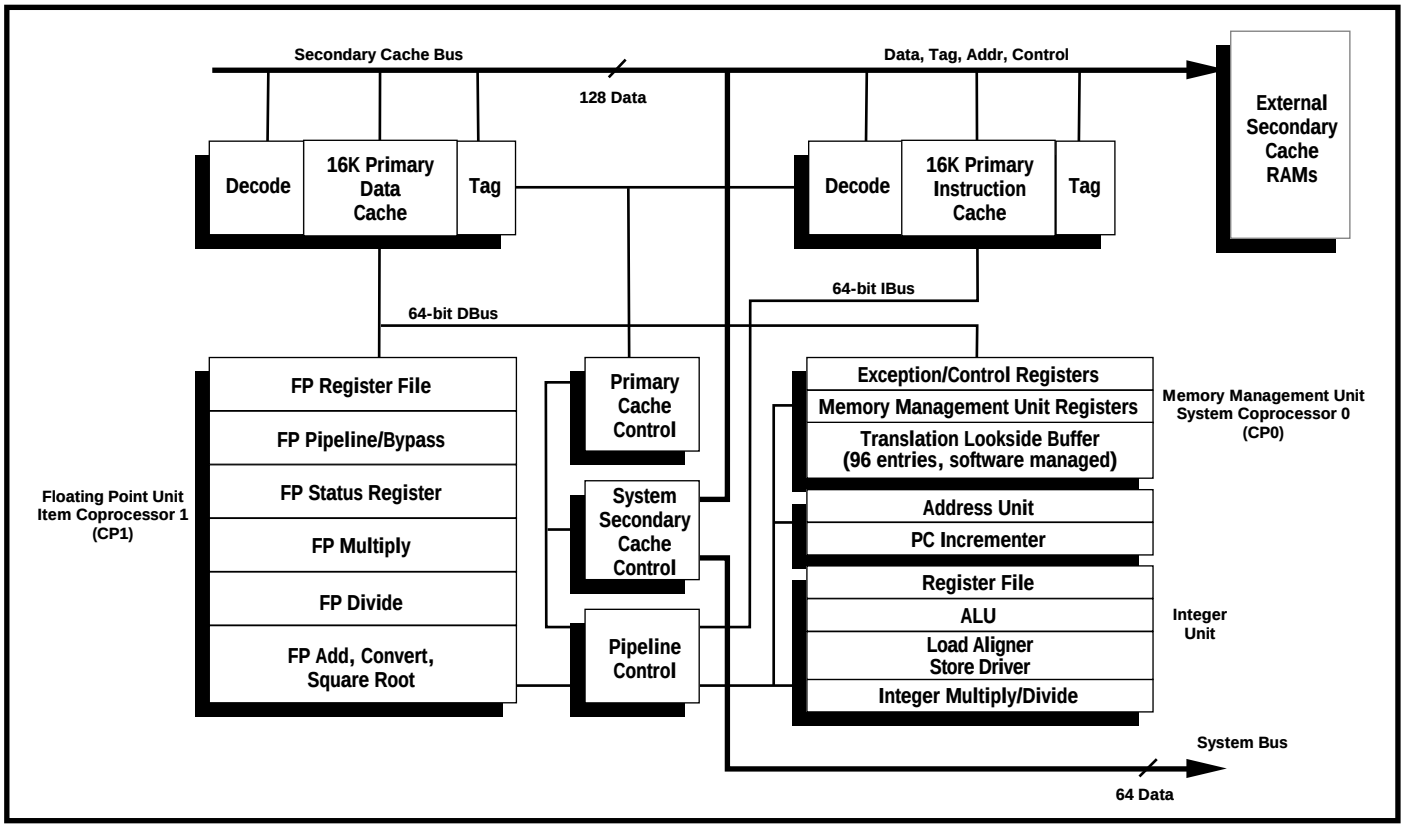
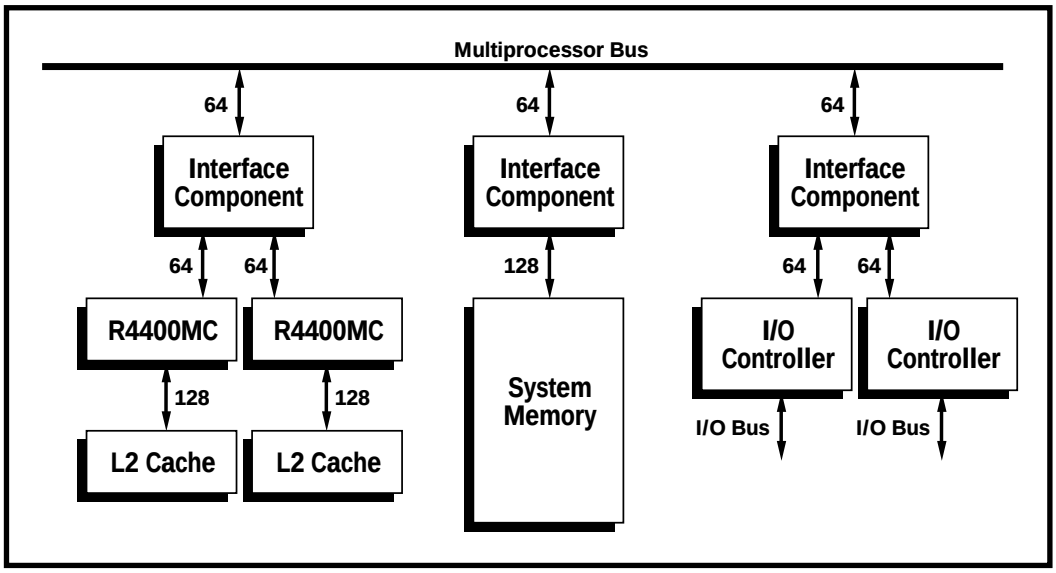


Figure 1. R4400 Block Diagram

Figure 2. R4400MC System Block Diagram



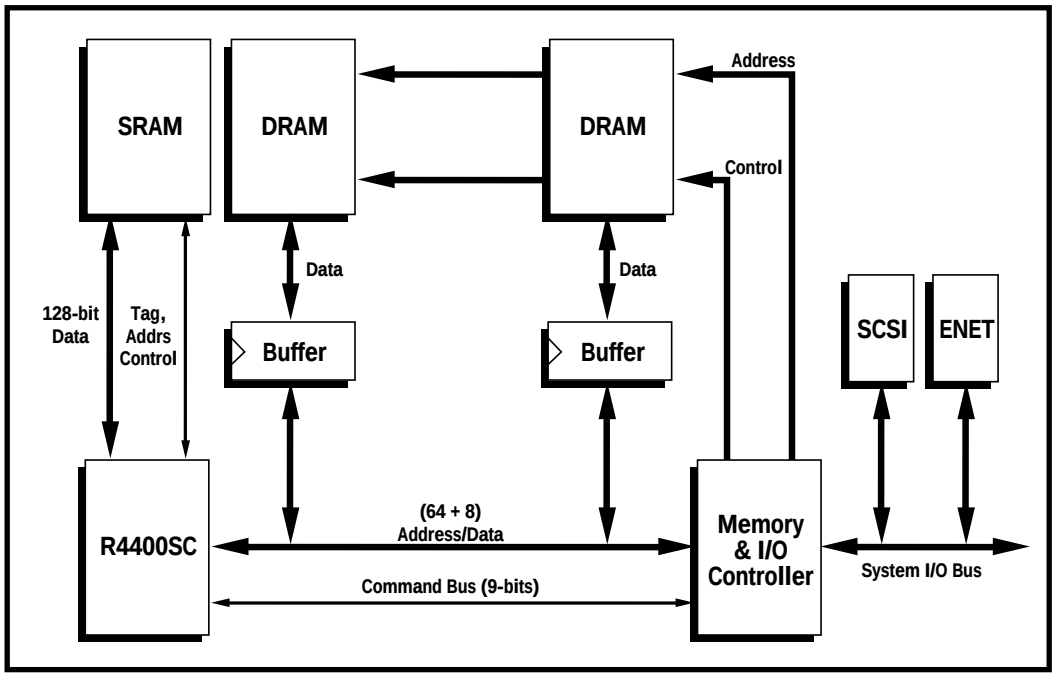


Figure 3. R4400SC System Block Diagram

RSC-1156/8-95

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