1. Functional Description of the AMG-SO204

The AMG-SO204 is a fully integrated optical receiver for optical switch or data transmission applications. It is an integrated light barrier receiver/transmitter front-end IC to be used with external receiving and emitting diodes. The IC consists of a current-to-voltage converter, a variable-gain amplifier, a 10-bit ADC, a logic block, two bandgap reference voltage cells, one 1.8V, two 2.5V, and one 3.3V regulator.

The emitting diode is controlled by the digital block of the IC, its light signal is received by the receiving photo diode. The resulting input current signal of the IC, is converted into a voltage signal by the current to voltage converter and then amplified. The gain of the amplifier can be set to six predefined levels. The IC's ADC samples and converts the gained signal synchronously with the emitting diode's signal. The signal values are processed by the logic block which allows for variable object detection threshold values, adjustable light signal timing, and digital signal filtering.

The digital block can be configured and monitored through an asynchronous interface. An eight digit, 7-segment display can be driven by the AMG-SO204 whose value is set through the UART interface. The IC requires external reset and 20MHz clock signal to operate.

2. Features

- ❑ Specialized photo diode receiver front-end in CMOS technology
- ❑ 4.5V to 6.5V supply voltage range
- ❑ On-chip 3.3V linear voltage regulator supporting off-chip electronics
- ❑ Separate on-chip analog and digital core on-chip 2.5V linear voltage regulators
- ❑ On-chip 1.8V ADC reference voltage regulator
- ❑ Internal current-to-voltage converter with modifiable trans resistance
- ❑ Support of an external current-to-voltage converter by disabling the internal one
- ❑ 6 step variable gain amplifier with matched compensation for increased dynamic range
- ❑ PWM-adjustable transmit-LED signal strength
- ❑ Adjustable transmit-LED timing
- ❑ Adjustable digital signal filtering
- ❑ Integrated 8 digit 7-segment LED driver
- ❑ 625kBit/s UART interface
- ❑ Low power consumption

3. Application

The AMG-SO204 is suitable for optical switch applications (i.e. light barriers) and optical data transmission applications.

3.1. Example Application Drawing

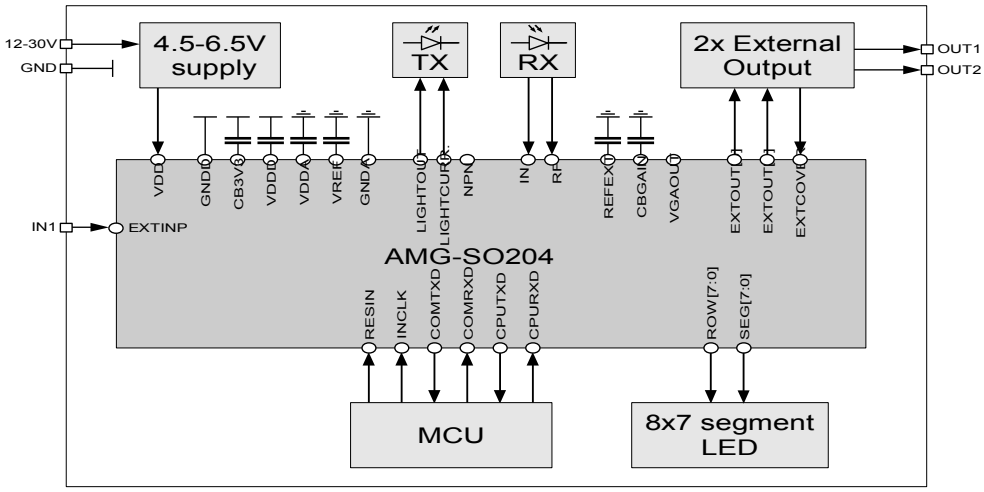

Figure 1: Optical Switch.

3.2. Application Notes

In preparation

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4. Block Diagram

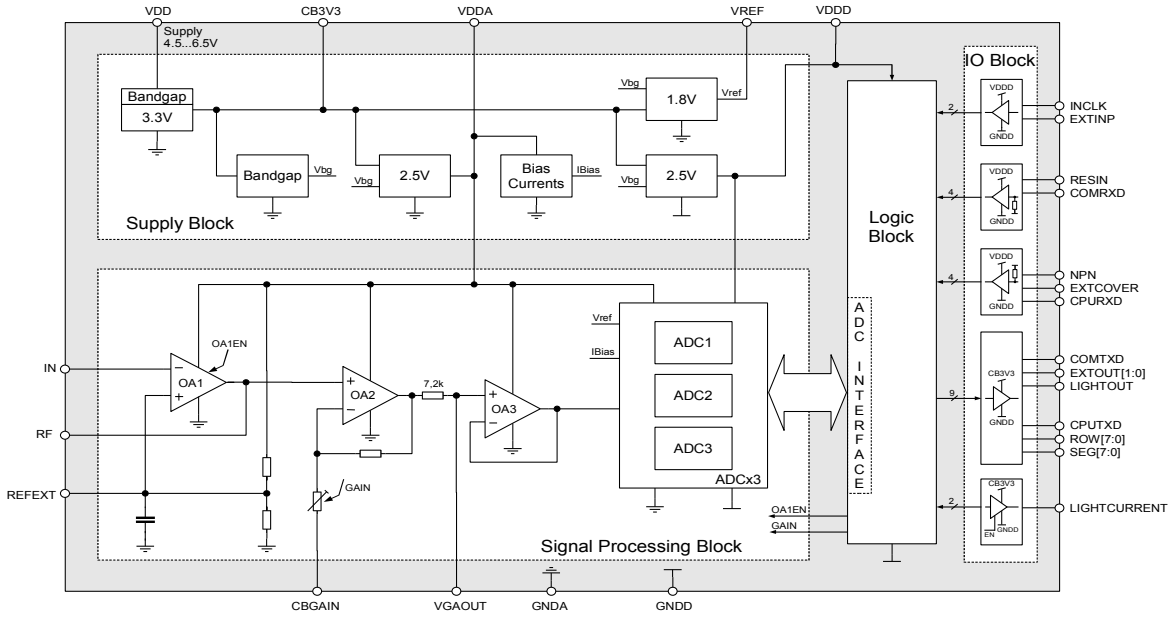


Figure 2: Block Diagram

5. Block Descriptions

5.1. Current-to-Voltage Converter (OA1)

The converter is built around operational amplifier OA1. Its trans resistance is defined by the resistance of an off-chip resistor connected between the pins IN and RF of the IC. The DC voltage applied to the non-inverting input of OA1, which is about 0.5V, defines the average voltage at the output of the converter. This reference voltage is also available at pin REFEXT of the IC.

The current to voltage converter can also be built using an external operational amplifier. In such a case OA1 is disabled by bringing its output to a high-impedance state. This makes it possible for the output of an external operational amplifier to be connected directly to pin RF. It is important to remember that, if an external amplifier is used, the voltage at pin RF must not exceed 2.75V (see Section 6).

5.2. Variable Gain Amplifier (OA2)

The variable gain amplifier is built around operational amplifier OA2. Its gain can be modified using a 3-bit signal GAIN. The gain can be set to one of six predefined values: 9, 17, 33, 65, 129, and 257V/V. The DC gain of the amplifier is always equal to 1V/V, and the low 3-dB frequency is set by an external capacitor connected to pin CBGAIN.

5.3. Unity Gain Buffer (OA3)

The cell OA3 is used as a buffer and provides the separation between the output of the VGA and the input of the ADC block. It ensures short settling times during sampling.

5.4. ADC Block

The ADC block consists of three successive approximation (SAR) analog to digital converters. It requires a reference voltage signal. The reference voltage (VREF) is generated within the IC. To achieve sampling rates of up to 2MS/s three lower throughput ADCs are combined into one virtual ADC. The digital block controls the individual ADCs in such a way that their offsets are compensated for.

5.5. I/O Block

The I/O block provides an interface between the 2.5V logic core and the 3.3V IO voltage.

5.6. Logic Block

The logic block provides digital processing of the sampled signal available at the output of the variable gain amplifier. The built-in logic interface shown in Fig. 5 controls the sampling action and proper data transmission between the ADC's and the logic block.

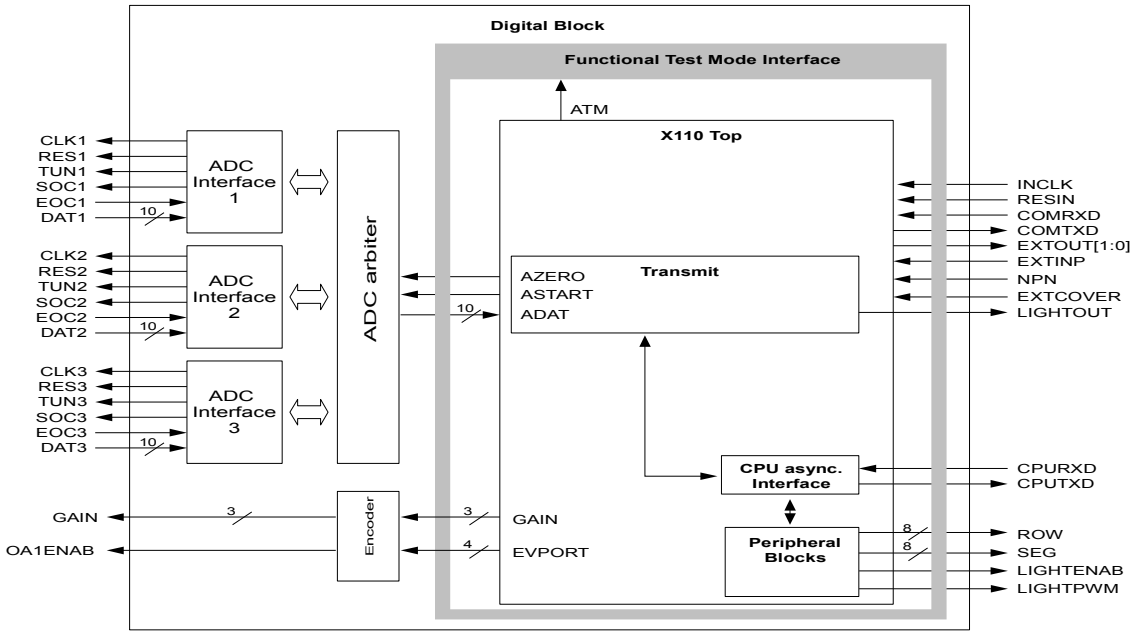


Figure 3 Logic Blocks

6. Pinning / Pad Coordinates

PIN#	Symbol	Description
1	Row 1	Outputs for driving a 7-segment LED display. High level activates a single digit. Connect to an NPN transistor.
2	Row 0	
3	Seg 4	Outputs for driving a 7-segment LED display. High level activates a segment of a digit. Connect to an NPN transistor.
4	Seg 3	
5	Seg 0	
6	Seg 1	
7	Seg 6	
8	Seg 2	
9	EXTOUT[0]	Judgment result output port #1
10	EXTCOVER	Overcurrent detection input of external output port, internally pulled-up to 3.3V
11	NC	Leave unconnected
12	NC	Leave unconnected
13	NC	Leave unconnected
14	NC	Leave unconnected
15	NC	Leave unconnected
16	NC	Leave unconnected
17	NPN	NPN/PNP select, internally pulled-up to 3.3V
18	INCLK	20MHz clock input
19	COMRXD	Microcontroller receive port for intermodule communication, internally pulled-down to GND
20	COMTXD	Microcontroller transmit port for intermodule communication
21	CPURXD	Microcontroller receive port for reading registers, internally pulled-down to GND
22	CPUTXD	Microcontroller transmit port for setting registers
23	EXTOUT[1]	Judgment result output port #2
24	EXTINP	General input port
25	RESETINB	System reset input port, internally pulled-down to GND
26	LIGHTCURRENT	LED intensity control
27	LIGHTOUT	LED ON/OFF control
28	VDD	6V supply pin
29	CB3V3	Output of the 3.3V regulator/3.3V decoupling capacitor pin
30	VDDD	Decoupling capacitor pin for the 2.5V regulator (digital)
31	GNDD	Digital ground pin
32	NC	Leave unconnected
33	GNDA	Analog ground pin

PIN#	Symbol	Description
34	VDDA	Decoupling capacitor pin for the 2.5V regulator (analog)
35	VREF	Decoupling capacitor pin for the 1.8V reference voltage regulator
36	VGAOUT	VGA output (test and debug pin)
37	CBGAIN	VGA decoupling capacitor pin
38	IN	Current-to-voltage converter input
39	RF	Current-to-voltage converter output
40	REFEXT	0.5V bias pin for an external CVC / 0.5V bias blocking capacitor
41	ROW[5]	Outputs for driving a 7-segment LED display. High level activates a single digit. Connect to an NPN transistor.
42	ROW[3]	
43	ROW[4]	
44	ROW[7	
45	ROW[6]	
46	ROW[2]	
47	SEG[5]	Outputs for driving a 7-segment LED display. High level activates a segment of a digit. Connect to an NPN transistor.
48	SEG[7]	

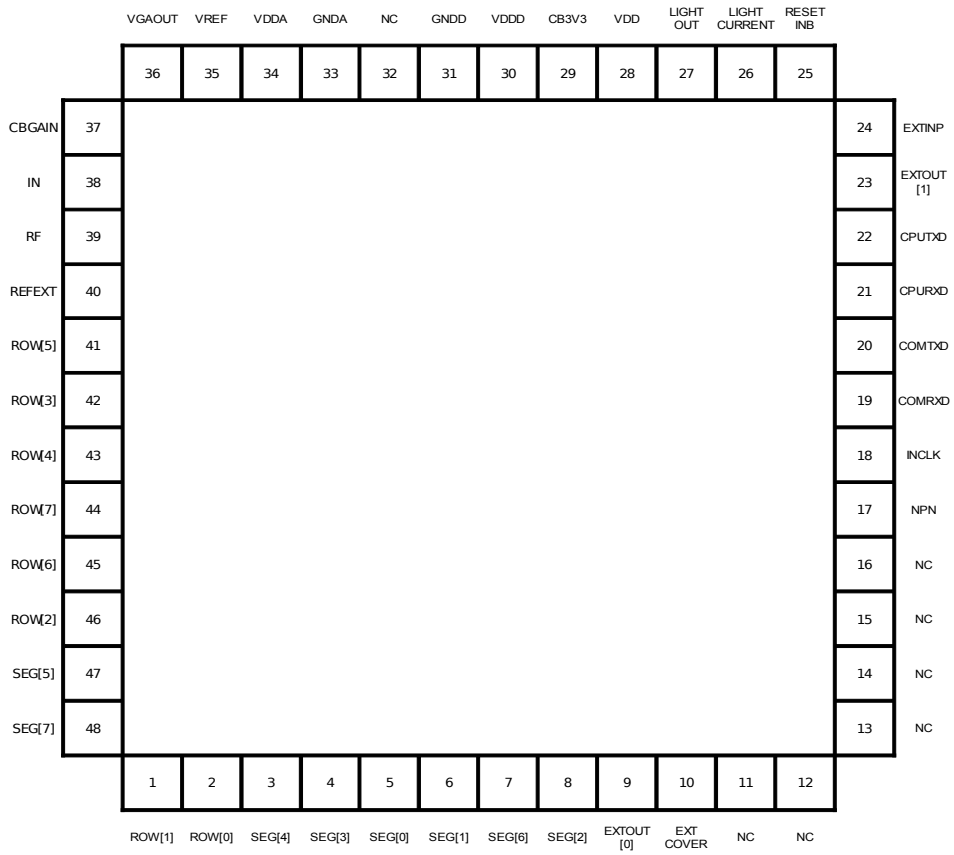


Figure 4: AMG-SO204 pin diagram

7. Absolute Maximum Ratings

The Absolute Maximum Ratings may not be exceeded under any circumstances.

#	Symbol	Parameter	Min	Max	Unit
1	V_{VDD}	Supply Voltage	-0.3	18	V
2	V_{RF}	Voltage at Pin R_F	-0.3	2.75	V
3	V_{CLK}	Voltage at Pin CLK	-0.3	5.5	V
4	$V_{I/O}$	Input Voltages at I/O Ports	-0.3	5.5	V
5	V_{ESD}	ESD Test Voltage (Human Body Model)	-2	2	kV
6	T_{STG}	Storage Temperature	-55	150	°C

Note:

8. Electrical Characteristics

8.1. Operational Range

#	Symbol	Parameter	Min	Max	Unit
1	V_{VDD}	Supply Voltage	4.5	6.5	V
2	T_{AMB}	Ambient Temperature	-25	90	°C

Note:

8.2. DC Characteristics

#	Symbol	Parameter	Min	Typ	Max	Unit
1	I_{VDD}	Total Current Consumption	5	6,5	8	mA
2	$T_{STARTUP}$*	Startup time		150		ms

Note: *Startup time is defined as the time between applying supply voltage and photo diode current and readiness of the IC for proper operation (exempt reset).

8.3. AC Characteristics

a) Operational Amplifier OA1

#	Symbol	Parameter	Min	Typ	Max	Unit
1	$A_{V,0}$	Differential DC Gain	-	110	-	dB
2	$\|V_{O,I}\|$	Input Offset Voltage	-	5	-	mV
3	$\|I_B\|$	Input Bias Current	-	<1	-	nA
4	V_{CM}	Common Mode Input Voltage	0	-	1.5	V
5	SR	Slew Rate (C_L=5pF)	-	0,25	-	V/µs
6	GBW	Gain-Bandwidth Product (C_L=5pF)	-	60	-	MHz
7	PM	Phase Margin (C_L=5pF)	-	65	-	°
8	e_n	Input-referred noise voltage		3		nV/√Hz
9	i_n	Input-referred noise current		1,2		pA/√Hz

Note:

b) Variable Gain Amplifier (built on OA2)

All values are given for Cbgain=2.2uF

#	Symbol	Parameter	Gain	Min	Typ	Max	Unit
1	$A_{V,0}$	DC Voltage Gain	0		9		V/V
2			1		17		
3			2		33		
4			3		65		
5			4		129		
6			5		257		
7	$\lvert V_{O,I} \rvert$	Input Offset Voltage	-	-	5	-	mV
8	$f_{L,3dB}$	Lower 3-dB Frequency	0		10		Hz
9			1		20		
10			2		40		
11			3		80		
12			4		160		
13			5		320		
14	$f_{H,3dB}$	Upper 3-dB Frequency	0		4,5		MHz
15			1		4,5		
16			2		4,5		
17			3		4,5		
18			4		6		
19			5		6		

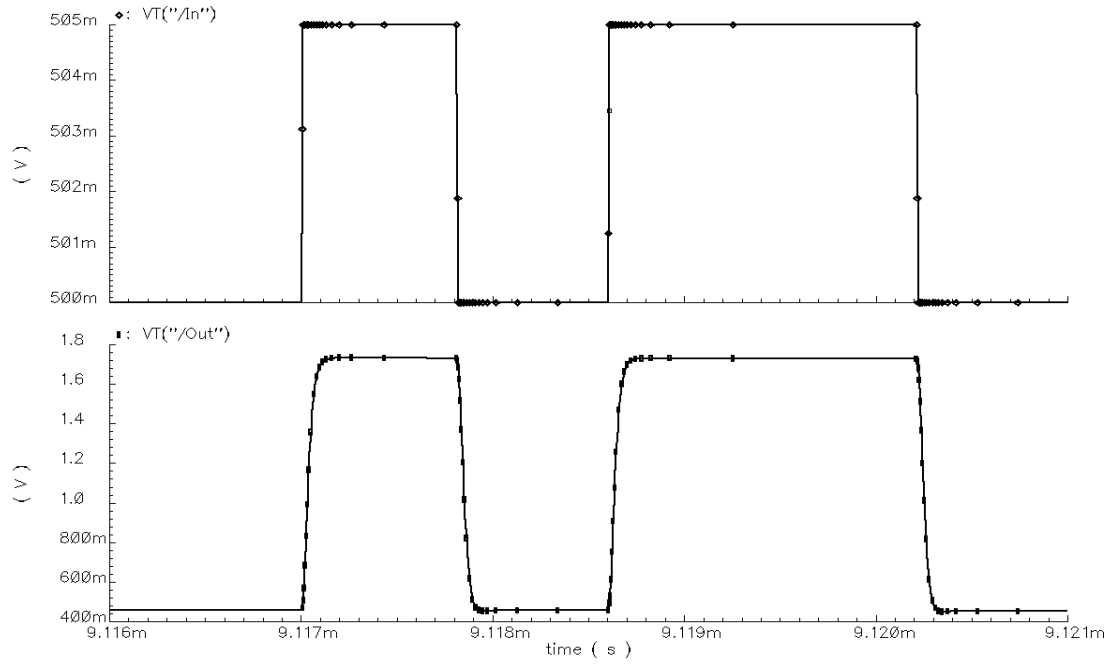


Figure 3: Steady-state time response of the VGA for a typical signal: GAIN=257V/V, Vin=5mV, Vref=0.5V, and Ton=800ns (typical simulation results)

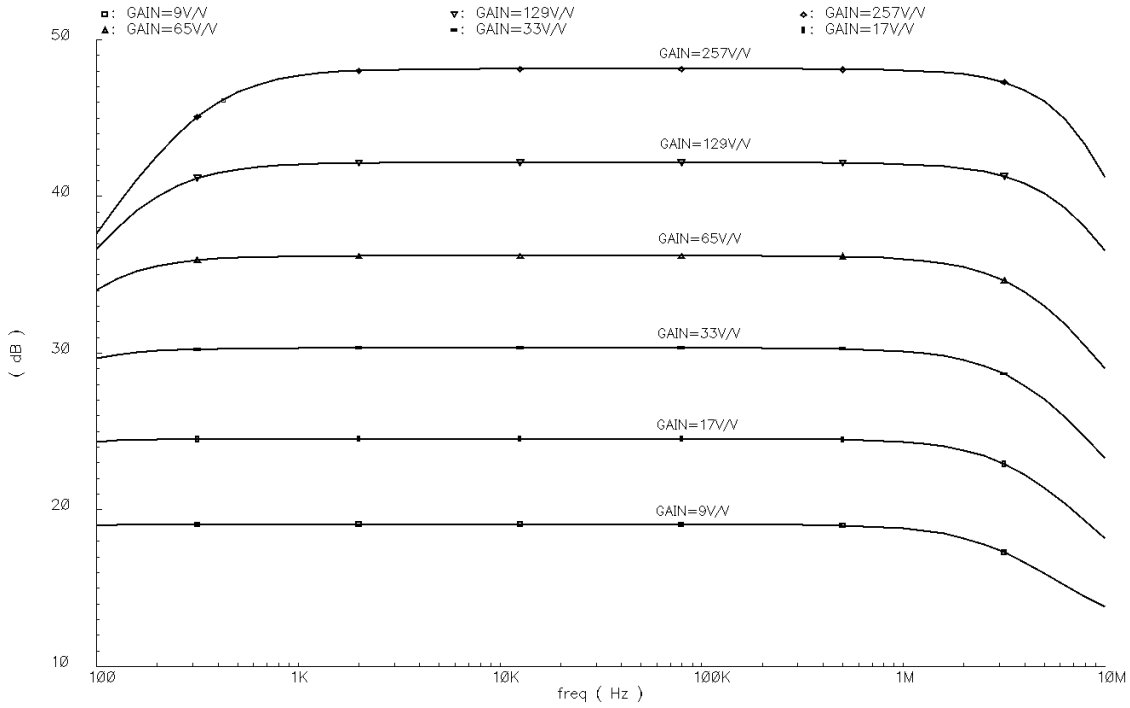


Figure 4: Frequency response of the VGA for different gain levels (typical simulation results,CB,GAIN=2.2uF)

c) ADC

#	Symbol	Parameter	Min	Typ	Max	Unit
1	N	Resolution	-	10	-	bits
2	F_S	Sampling Rate	0.1	-	2	MS/s
3	$V_{O,I}$	Input Offset Voltage	-	-	50	mV
4	DNL	Differential nonlinearity	-0.75	-	0.75	LSB
5	INL	Integral nonlinearity	-2.5	-	2.5	LSB
6	f_{CLK}	Master Clock Frequency	-	$32*F_S$	-	MHz
7	V_{VREF}	Reference Voltage	-	1.8	-	V
8	Vin_{MAX}	Input Voltage Range	0	-	V_{VREF}	V

d) Reference and Supply Voltages

#	Symbol	Parameter	Min	Typ	Max	Unit
1	V_{VREF}	1.8V Reference Voltage	1.70	1.80	1.90	V
2	V_{VDDA}	2.5V Analog Supply Voltage	2.35	2.50	2.65	V
3	V_{VDDD}	2.5V Digital Supply Voltage	2.35	2.50	2.65	V
4	V_{CB3V3}	3.3V Supply Voltage	3.00	3.30	3.60	V

9. Application

The figure below shows the general circuitry. The light line is between RX-Diode (see fig. 6) and the TX-Diode (see fig. 7). The AMG-SO204 needs an external 20MHz clock to connect at Pin INCLK (see fig. 8)

9.1. Example Application Circuit(s)

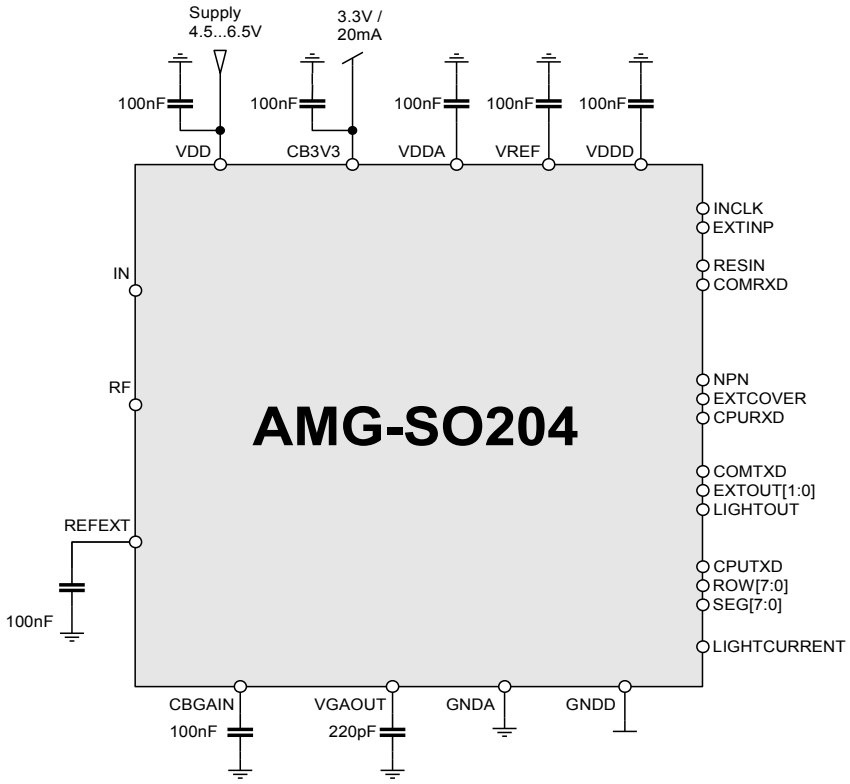


Figure 5: Example Application Circuit

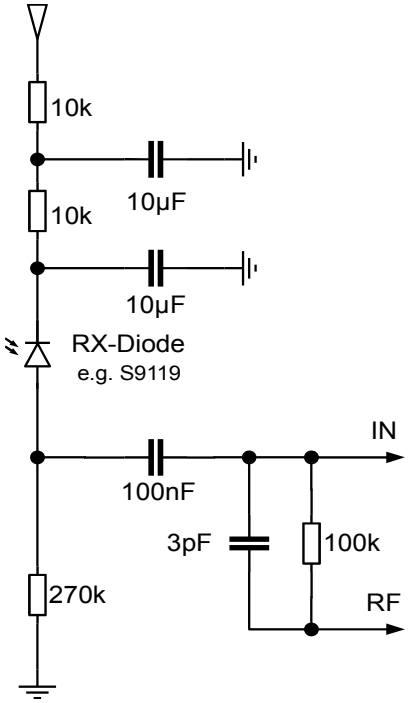


Figure 6: 'Rx circuitry

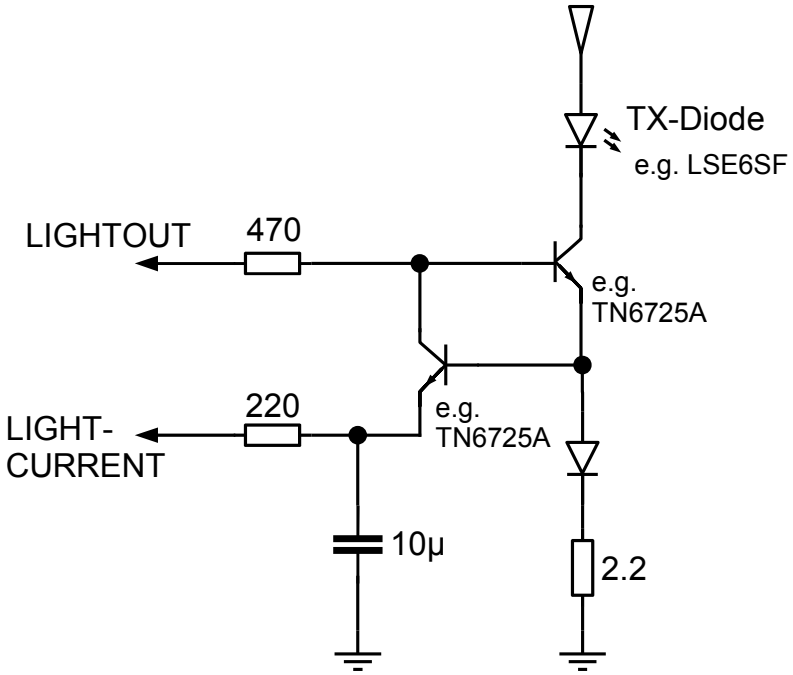


Figure 7: 'Tx circuitry

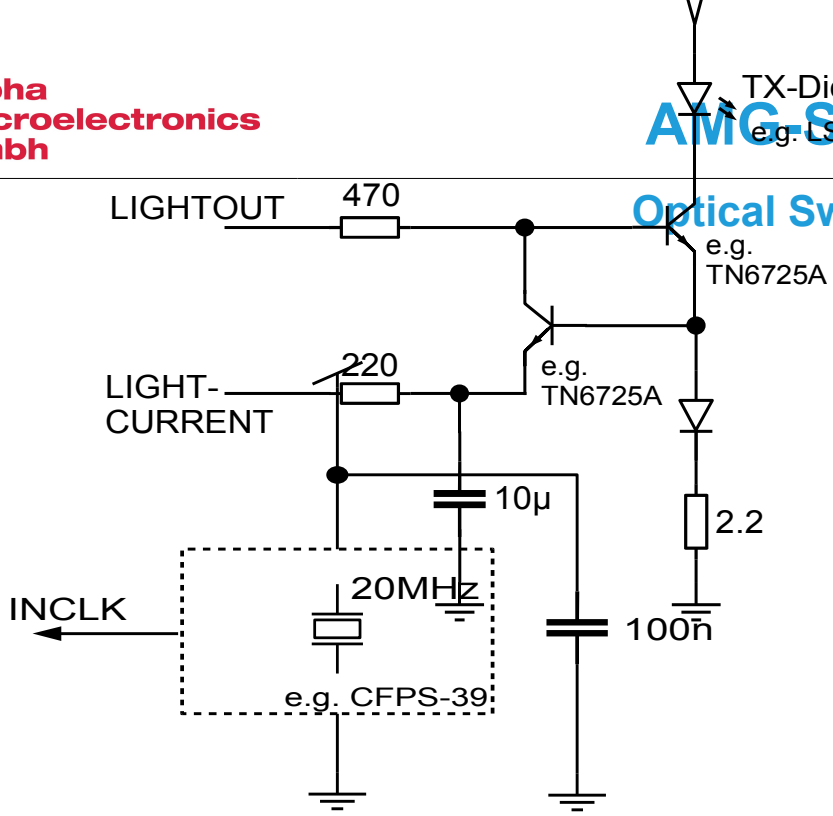


Figure 8: External Oscillator

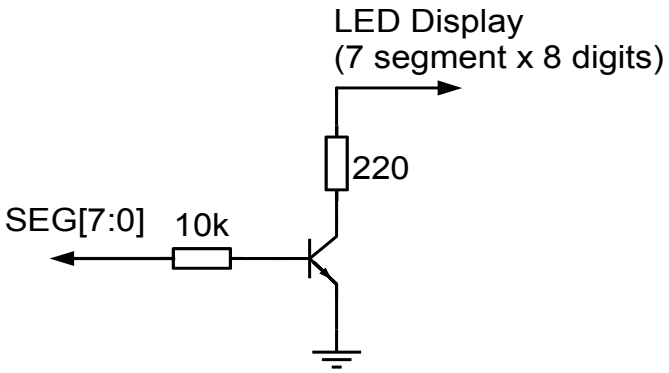


Figure 9: Segment driver circuitry for LED Display

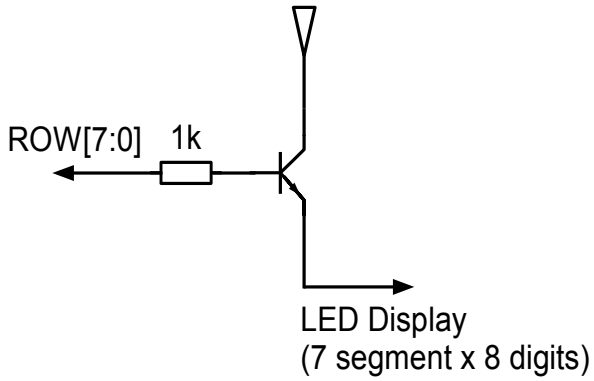


Figure 10: Row driver circuitry for LED Display

If the internal OA1 is disabled (see chapter 5.1), an external OA can be connected to RF and REFEXT as shown in fig. 11.

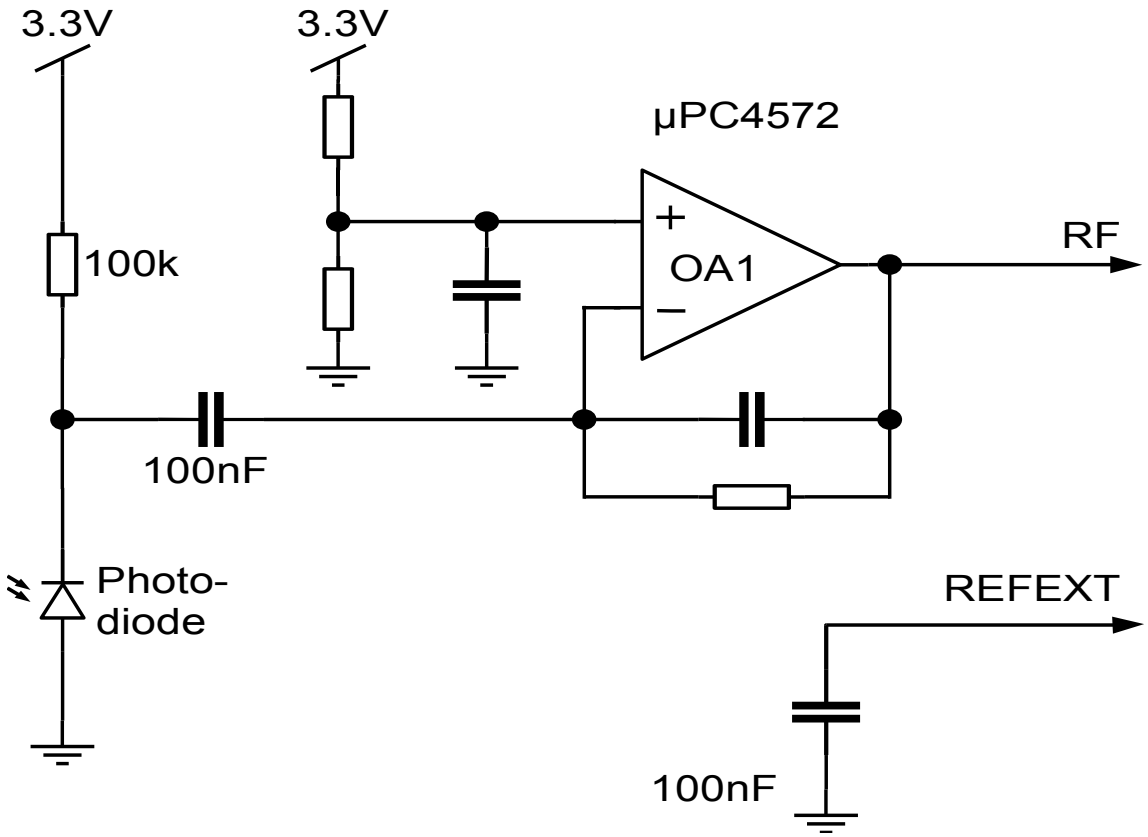


Figure 11: external Current-to-Voltage Converter OA1 (intern OA1 is inactive)

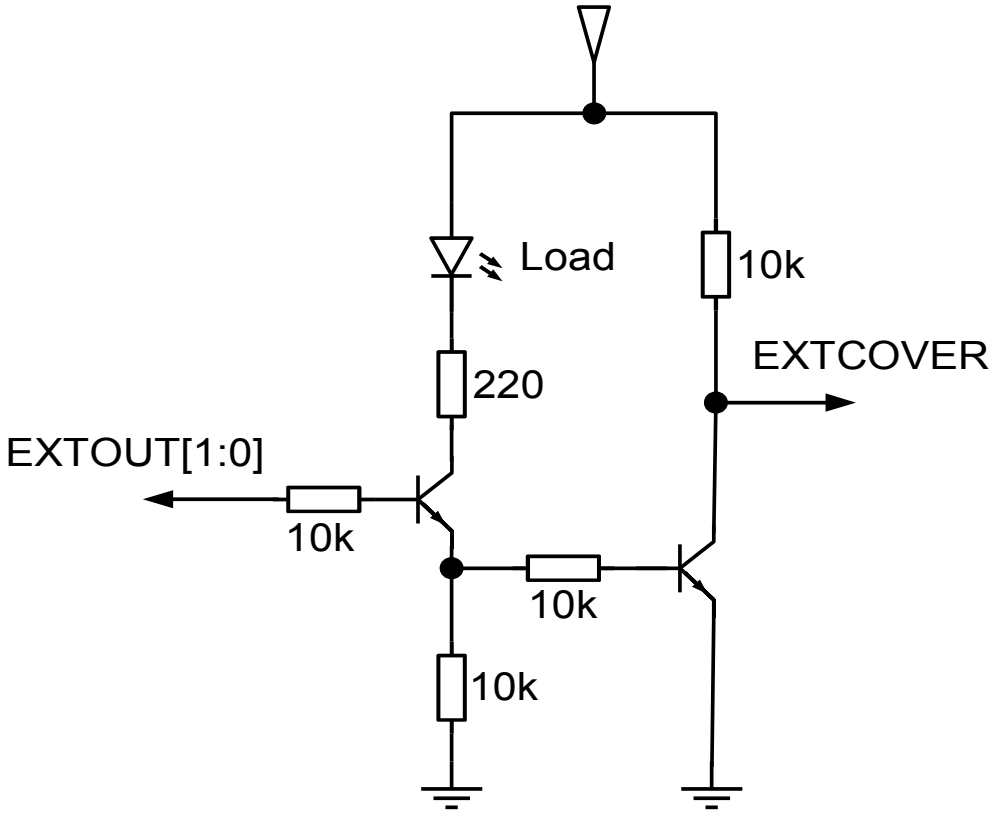


Figure 12: external threshold control

10. Register Description

10.1. Write Registers

Address	Bit	Name	Value	Reset Value*	Detail
0	0	CLM	0	n/a	n/a
			1		Update RECMAX and RECMIN with present received value
	1	CLC	0	n/a	n/a
			1		Clear COUNTVAL
1	0	ETG	0	0	Update EXTOUT on every emitting cycle
			1		Update EXTOUT at the external trigger input is active
	2...1	For future use	0	0	Open for future use
			1		Open for future use

Address	Bit	Name	Value	Reset Value*	Detail
			2		Select trigger input source as the expansion input #1 on the comparator unit
			3		Select trigger input source as the expansion input #2 on the comparator unit
	3	FILT	0	0	Disable the received light filter
			1		Enable the received light filter
	5...4	FILTE	0	0	Set 1 to the number of eliminating maximum and minimum value in the received light filter
			1		Set 2 to above
			2		Set 3 to above
			3		Set 4 to above
	7...6	FILTA	0	0	Set 6 to the number of received light values in the received light filter. The result of received light filter is sum of ((FILTA - FILTE)*2+4) times of received data
			1		Set 8 to above
			2		Set 10 to above
			3		Set 12 to above
	10..8	GAIN	0...5	0	Set the gain of operational amplifier #2
	11	For future use	0	0	Open for future use
			1		Open for future use
	12	DRK	0	0	Turns on EXTOUT when the received light value is the inside of between THREnLR and THREnHR
			1		Turns on EXTOUT when the received light value is the outside of between THREnLR and THREnHR
	13	DEMT	0	0	Enable LIGHTOUT
			1		Disable LIGHTOUT
	14	For future use	0	0	Open for future use
			1		Open for future use
	15	AVG	0	0	Open for future use
			1		Open for future use
2	8...0	EMITW	0...511	511	Specify the emitter light pulse width. Time period is 50ns*(EMITW+1). It should be set greater than 15
	15...9	ECYCLE	0...127	127	Specify the emitter light cycle. Time period is the emitter pulse width×(ECYCLE+1). It should be set greater than 4. Display switching noise may affect on the setting value is 5,37,69, or 101
3	8...0	EMITS	0...511	7	Put forward the emitter light pulse. Set value that is calculated (EMITW-[time period].
4	13...0	THRE1LR	0…16383	1000	Lower and Upper threshold levels of EXTOUT[0]. Turn ON when

Address	Bit	Name	Value	Reset Value*	Detail
5	13...0	THRE1HR	0…16383	8192	the received light value is equal
6	13...0	THRE2LR	0…16383	1000	Lower and Upper threshold levels of EXTOUT[1]. Turn ON when the received light value is equal or greater than THRE2LR and equal or less than THRE2HR
7	13...0	THRE2HR	0…16383	8192	
8	13...0	THRE1LF	0…16383	1000	Lower and Upper threshold levels of EXTOUT[0]. Turn OFF when the received light value is less than THRE1LF or greater than THRE1HF
9	13...0	THRE1HF	0…16383	8192	
10	13...0	THRE2LF	0…16383	1000	Lower and Upper threshold levels of EXTOUT[1]. Turn OFF when the received light value is less than THRE2LF or greater than THRE2HF
11	13...0	THRE2HF	0…16383	8192	
12	13...0	ONDLY	0…16383	0	On-delay timer value for EXTOUT. Time unit is specified by ONDBS
	15...14	ONDBS	0	0	Set 1 microsecond to the on-delay timer unit for EXTOUT
			1		Set 10 microsecond to the on-delay timer unit for EXTOUT
			2		Set 100 microsecond to the on-delay timer unit for EXTOUT
			3		Set 1 millisecond to the on-delay timer unit for EXTOUT
13	13...0	OFFDLY1	0…16383	0	Off-delay timer value for EXTOUT[0]. Time unit is specified by OFFDBS1
	15...14	OFFDBS1	0	0	Set 1 microsecond to the off-delay timer unit for EXTOUT[0]
			1		Set 10 microsecond to the off-delay timer unit for EXTOUT[0]
			2		Set 100 microsecond to the off-delay timer unit for EXTOUT[0]
			3		Set 1 millisecond to the off-delay timer unit for EXTOUT[0]
14	13...0	OFFDLY2	0…16383	0	Off-delay timer value for EXTOUT[1]. Time unit is specified by OFFDBS2
	15...14	OFFDBS2	0	0	Set 1 microsecond to the off-delay timer unit for EXTOUT[1]
			1		Set 10 microsecond to the off-delay timer unit for EXTOUT[1]
			2		Set 100 microsecond to the off-delay timer unit for EXTOUT[1]
			3		Set 1 millisecond to the off-delay timer unit for EXTOUT[1]
15	0	CNM	0	0	Disable the automatic counter clear mode
			1		Enable the automatic counter clear mode. Clear COUNTVAL when COUNTVAL is equal or greater than COUNTMCH
	2...1	CNS	0	0	Select counter clear source as the external input
			1		Select counter clear source as the external input on the master unit
			2		Select counter clear source as the expansion input #1 on the comparator unit
			3		Select counter clear source as the expansion input #2 on the comparator unit
	4...3	ONESHT	bit3=0	0	Disable one-shot mode on EXTOUT[0]

Address	Bit	Name	Value	Reset Value*	Detail
			bit3=1		Enable one-shot mode on EXTOUT[0]
			bit4=0	0	Disable one-shot mode on EXTOUT[1]
			bit4=1		Enable one-shot mode on EXTOUT[1]
	6...5	O2M	0	0	Select EXTOUT[1] control to the threshold level mode
			1		Select EXTOUT[1] control to the counter compared output mode
			2		Select EXTOUT[1] control to the inverted output of EXTOUT[0]
	7	CCEN	0	0	Disable the external counter clear input
			1		Enable the external counter clear input
	8	OIH1	0	0	Enable the on-delay timer of EXTOUT[0]
			1		Disable the on-delay timer of EXTOUT[0] whatever ONDLY is set
	9	OIH2	0	0	Enable the on-delay timer of EXTOUT[1]
			1		Disable the on-delay timer of EXTOUT[1] whatever ONDLY is set
	10	DIM	0	0	Set 7/8 duty ratio to ROW[3…0] and 2/8 duty ratio to ROW[7…4]
			1		Set 1/8 duty ratio to ROW[7…0]
	12...11	ONENA	bit11=0	0	Set the continuous one-shot mode for EXTOUT[0]
			bit11=1		Set the triggered one-shot mode for EXTOUT[0]
			bit12=0	0	Set the continuous one-shot mode for EXTOUT[1]
			bit12=1		Set the triggered one-shot mode for EXTOUT[1]
16	6...0	DISPO	0	0	Turn off the segments of the rightmost column in the 8-digit LED display
			1		Turn on the rightmost column in the 8-digit LED display
	7	EVF	0	0	Open for future use
			1		Open for future use
	14...8	DISP1	0	0	Turn off the 7th column in the 8-digit LED display
			1		Turn on the 7th column in the 8-digit LED display
17	6...0	DISP2	0	0	Turn off the 6th column in the 8-digit LED display
			1		Turn on the 6th column in the 8-digit LED display
	14...8	DISP3	0	0	Turn off the 5th column in the 8-digit LED display
			1		Turn on the 5th column in the 8-digit LED display
18	6...0	DISP4	0	0	Turn off the 4th column in the 8-digit LED display
			1		Turn on the 4th column in the 8-digit LED display
	7	D80	0	0	Turn off the dot segment of row 2
			1		Turn on the dot segment of row 2

Address	Bit	Name	Value	Reset Value*	Detail
	14...8	DISP5	0	0	Turn off the 3rd column in the 8-digit LED display
			1		Turn on the 3rd column in the 8-digit LED display
	15	D81	0	0	Turn off the dot segment of row 3
			1		Turn on the dot segment of row 3
19	6...0	DISP6	0	0	Turn off the 2nd column in the 8-digit LED display
			1		Turn on the 2nd column in the 8-digit LED display
	7	D82	0	0	Turn off the dot segment of row 4
			1		Turn on the dot segment of row 4
	14...8	DISP7	0	0	Turn off the leftmost column in the 8-digit LED display
			1		Turn on the leftmost column in the 8-digit LED display
	15	D83	0	0	Turn off the dot segment of row 5
			1		Turn on the dot segment of row 5
20	7...0	PWM	0...255	0	The PWM duty ratio of LIGHT_CURRENT output
	14...13	ATM	bit13=0	0	Turn off Analog-Test-Mode
			bit13=1		Turn on Analog-Test-Mode
			bit14=1	0	Trigger Digital-Test-Mode (reset to disable)
21	15...0	COUNTMCH	0...65535	65535	Set value for comparison with the counter

** values after POR or Reset by Reset-Pin*

10.2. Read Registers

Address	Bit	Name	Value	Reset Value*	Detail
0	13…0	REC DATA	0…16383	n/a	Latest value of the received light
1	13…0	REC MAX	0…16383	n/a	Maximum value of the received light
2	13…0	REC MIN	0…16383	n/a	Minimum value of the received light
3	3…0	For future use	0...15	n/a	Open for future use
	4	For future use	0	n/a	Open for future use
			1		Open for future use
	5	For future use	0	n/a	Open for future use
			1		Open for future use
	8...6	For future use	0	n/a	Open for future use
			1		Open for future use
			0		Open for future use
			1		Open for future use
			0		Open for future use
			1		Open for future use
	9	EIN	0	n/a	The external input is inactive (NPN = L), active (NPN = H)
			1		The external input is active (NPN = L), inactive (NPN = H)
	10	NPN	0	n/a	NPN input port is inactive
			1		NPN input port is active
	11	COV	0	n/a	EXTCOVER input port is inactive
			1		EXTCOVER input port is active
	13...12	JDGSTS	bit12=0	n/a	RECDATA is the outside of THRE1LR and THRE1HR
			bit12=1		RECDATA is the inside of THRE1LR and THRE1HR
			bit13=0		RECDATA is the outside of THRE2LR and THRE2HR
			bit13=1		RECDATA is the inside of THRE2LR and THRE2HR
4	15...0	COUNTVAL	0…65535	n/a	Latest value of the counter

** values after POR or Reset by Reset-Pin*

11. Serial Interface

All registers are either read-only or write-only (see register map in chapter10). Data is received via the pin CPURX and sent via the pin CPUTX using a 625kbit/s UART, shown in Fig. 13 for write and Fig. 14 for read. Data is sent byte-wise, framed by one start bit and one stop bit.

Each transfer consists of one address byte followed by two data bytes, the low byte is sent before the high byte. The 7 bit address is contained in the 7 least significant bits of the address byte. For writes the MSB is set to 0 for reads to 1.

Symbol	Parameter Name	Min	Typ	Max	Unit
t_{Bit}	Bit length	-5,00%	1/625	5,00%	1/kHz

Table 1: UART parameters

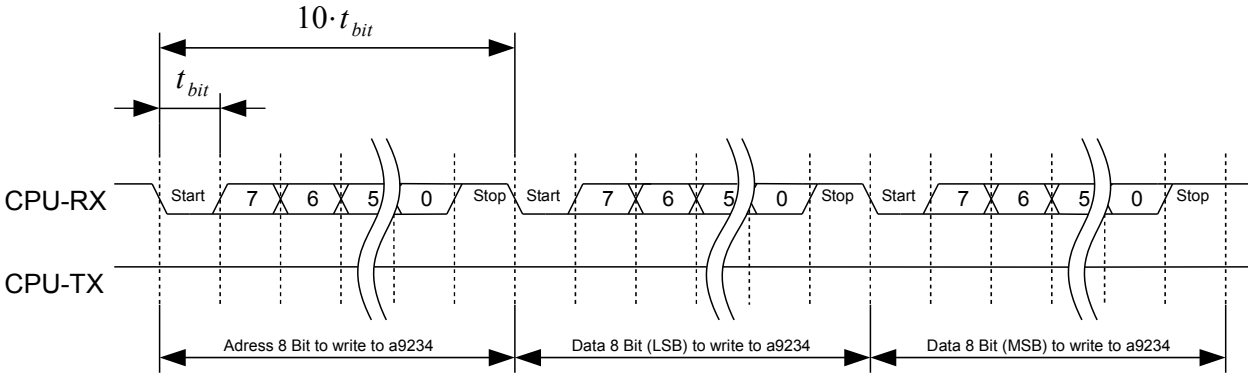


Figure 13: write to SO204

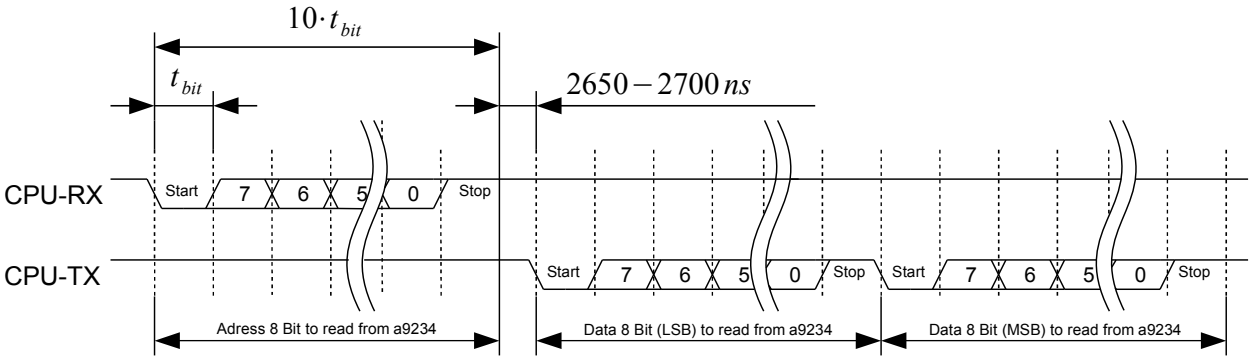
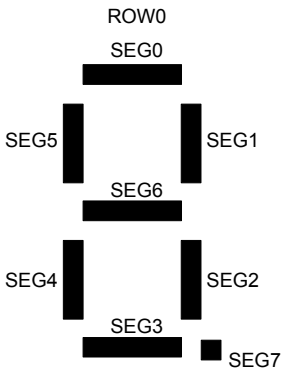


Figure 14: read from SO204

12. LED Display Driver

An 8 digit 7-segment LED display can be connected to the IC via ROW[7:0], and SEG[7:0]. It is controlled via registers 16, 17, 18, 19 (see register map in chapter 10). The relationship between segment number and register bit is shown in the figure below. When a segment bit is set the related SEG[7:0] pin is set to logic high. One line out of ROW [7:0] is set to high sequentially to display the value of SEG[7:0] for each digit, see fig. 16 for the signal's timing.

Note: Only the dot segments of row 2 through 5 can be set. It must be observed that the flag must be set in the registers normally associated with row 4 through 7.



SEG0 => BIT 0 / 8
SEG1 => BIT 1 / 9
SEG2 => BIT 2 / 10
SEG3 => BIT 3 / 11
SEG4 => BIT 4 / 12
SEG5 => BIT 5 / 13
SEG6 => BIT 6 / 14

Only the dot segments of ROW2 – 5 can be set:
SEG7 => ROW2 / 3 => BIT 7 / 15 (Adresse 18)
=> ROW4 / 5 => BIT 7 / 15 (Adresse 19)

Figure 15: schematic drawing of numeric 7-segment LED

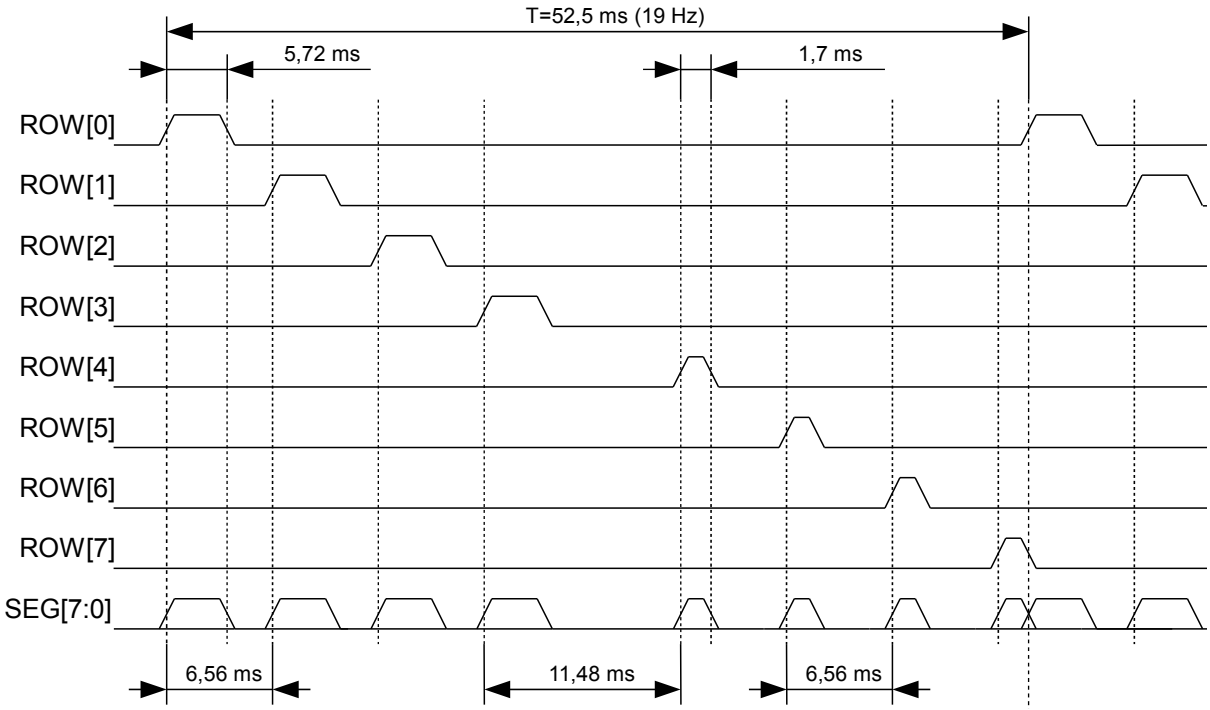


Figure 16: timings of 7-Segment LED control

13. Supply Block

The supply block consists of 2 bandgap cells, 4 low-drop voltage regulators and 1 bias current generator. It provides the voltages as shown in the table below.

Name	Value
Bandgap	1,24 V
CB3V3	3,3 V
VDDA	2,5 V
VDDD	2,5 V
VREF	1,8 V

Table 2: provided voltages

The bandgap cells are responsible for delivering temperature- and process-independent reference voltages used for biasing other blocks of the AMG-SO204. These voltages are only

internal. The use of two bandgaps has been dictated by precision and voltage considerations: the high-voltage bandgap is less precise but can operate under a relatively wide range of supply voltages (4.5V...6.5V), whereas the low-voltage bandgap is more precise but requires an accurate supply voltage of 3.3V. The high voltage bandgap provides the reference voltage for the 3.3V voltage regulator and the low voltage bandgap the reference for the 2.5V and 1.8V voltage regulators.

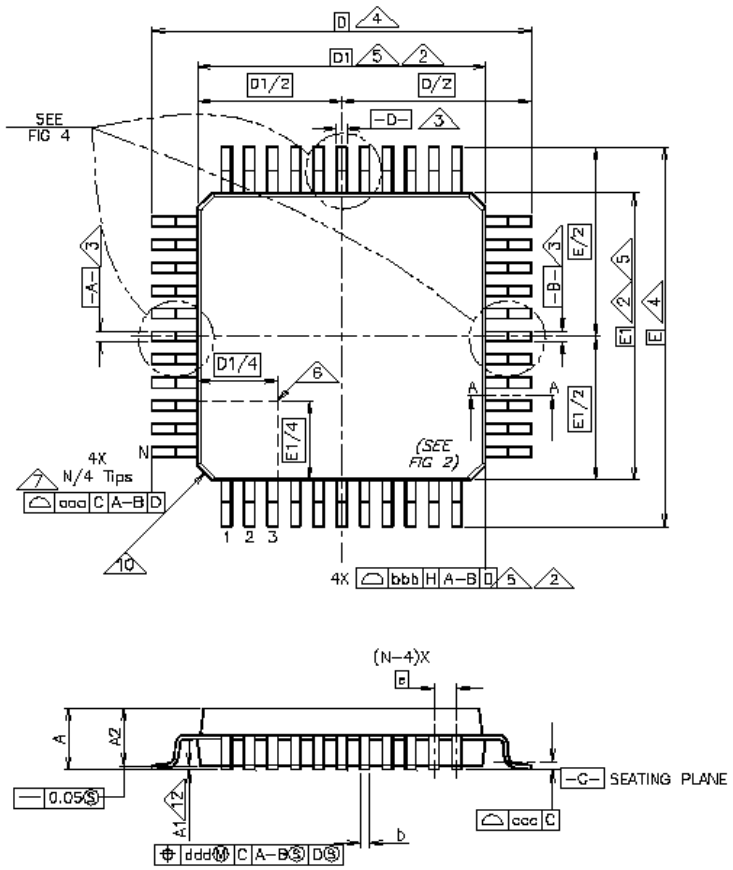
The IC includes four low-drop voltage regulators. The 3.3V regulator lowers the supply voltage to about 3.3V. This regulated voltage is used to supply two on-chip 2.5V regulators, the low-voltage voltage bandgap, the on-chip 1.8V regulator, and any off-chip 3.3V electronics. The two 2.5V regulators supply, independently, the analog and the digital part of the IC and the bias current generator. The use of two virtually identical 2.5V regulators was dictated by the desire to achieve high separation between the (quiet) analog and the (noisy) digital part of the IC. The 1.8V regulator is used to provide the reference voltage for the ADC. The voltage regulators whose output voltage are extern available at the pins CB3V3, VDDA, VDDD and VREF and the supply pin VDD needs to be decoupled.

The cell bias currents provides a current of about 15uA to each ADC.

14. IC-Package

TQFP 48

Package: TQFP 7x7 48L



SYMBOL	MS-026			NOTE
	ABC			
	SQUARE			
	MIN	NOM	MAX	
A	1.00	1.10	1.20	
A1	0.05	0.10	0.15	
A2	0.95	1.00	1.05	
D		9.00 BSC		
D1		7.00 BSC		
E		9.00 BSC		
E1		7.00 BSC		
N		*48*		
e		0.50 BSC		
b	0.17	0.22	0.27	
b1	0.17	0.20	0.23	
Tolerance of form and position				
ccc		0.08		
ddd		0.08		

Figure 17: Package

15. IC-Marking

αSO204

4 digits date code = 2 digits year + 2 digits work week

8 digits lot number = 2 digits fab process + 4 digits lot number + 1 digit sub lot

16. Ordering Information

AMG-SO204-ILQ48T (LQFP48, Tube)

17. Notes and Cautions

17.1. ESD Protection

The Requirements for Handling Electrostatic Discharge Sensitive Devices are described in the JEDEC standard JESD625-A. Please note the following recommendations:

- When handling the device, operators must be grounded by wearing a for the purpose designed grounded wrist strap with at least 1MΩ resistance and direct skin contact.
- Operators must at all times wear ESD protective shoes or the area should be surrounded by for ESD protection intended floor mats.
- Opening of the protective ESD package that the device is delivered in must only occur at a properly equipped ESD workbench. The tape with which the package is held together must be cut with a sharp cutting tool, never pulled or ripped off.
- Any unnecessary contact with the device or any unprotected conductive points should be avoided.
- Work only with qualified and grounded tools, measuring equipment, casing and workbenches.
- Outside properly protected ESD-areas the device or any electronic assembly that it may be part of should always be transported in EGB/ESD shielded packaging.

17.2. Storage conditions

The AMG-SO204 corresponds to moisture sensitivity classification **ML2** , according to JEDEC standard J-STD-020, and should be handled and stored according to J-STD-033.

18. Disclaimer

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