Fibre Channel GBaud Optical Link Module

Technical Data

HGLM-1063

Features

- **ANSI X3.230-1994 Fibre Channel Standard Compatible (FC-0)**
- **FCSI-301-Rev 1.0 "GBaud Link Module Specification" Compatible**
- **Standard 20 Bit (1063 MBd), TTL Interface**
- **Class I Laser Safety Certified**
- **Single +5.0 V Power Supply**

Applications

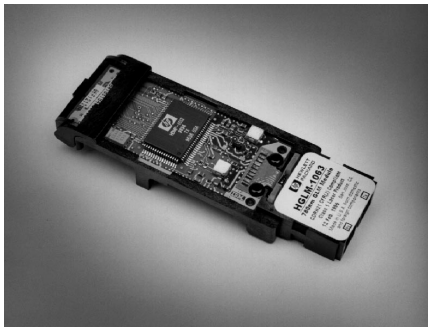
- **Mass Storage System I/O Channel**
- **Computer System I/O Channel**
- **High Speed Peripheral Interface**

Description

The HGLM-1063 Gigabaud Optical Link Module, provides a complete Fibre Channel FC-0 layer solution. The module meets the requirements of the **100-M5-SL-I** physical link as defined by the American National Standards Institute (ANSI) X3.230-1994 Fibre Channel standard. The HGLM-1063 is also compatible with the Fibre Channel Systems Initiative (FCSI) document #FCSI-301-Rev 1.0 "Gigabaud Optical Link Module" specification.

The HGLM-1063 transmits and receives 8b/10b encoded, parallel, data in the 20 bit wide format defined by the FCSI-301 document. The 20 bit wide data is transmitted at 100MB/sec over a serial fiber link and has the capability to receive data at 100 MB/sec simultaneously. With overhead, this translates to a serial line rate of 1062.5 MBaud transmitting and 1062.5 MBaud receiving. The serial data link uses a 780 nm laser transmitter and photodiode. The optimum fiber is 50/125 μm multimode fiber (62.5/125 μm multimode fiber can be used with degraded performance) and attaches to the HGLM-1063 via a duplex SC connector.

As specified in the Fibre Channel Standard, the HGLM-1063 is a Class 1 laser safe device; the transmitted optical signal shuts down in the case of an open fiber condition after a specific time interval. The HGLM-1063 accomplishes this by monitoring the transmitted optical power levels, and the received optical signal.



The HGLM-1063 is intended for use in building adapter cards (or equivalent devices) as shown in Figure 1. The HGLM-1063 provides complete FC-0 functionality. The HPFC-5000 provides the FC-1 through FC-4 functions and interfaces directly to the HGLM-1063. Finally, a bus gasket is used to connect the HPFC-5000 to the specific system bus in use. This block diagram is meant only to illustrate the basic Fibre Channel functionality.

For proper operation, it is necessary to connect the HGLM-1063 to another HGLM-1063 (or equivalent) in a full duplex configuration as depicted in Figure 3. This ensures proper operation of the Open Fiber Control circuitry and allows proper link startup and synchronization.

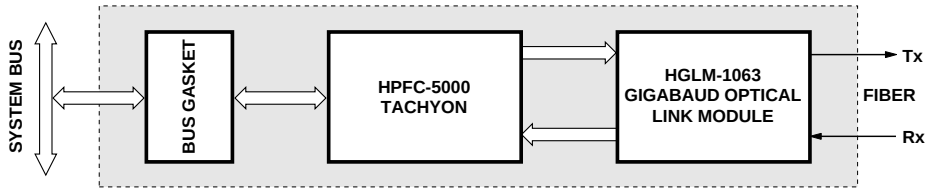


Figure 1. Example System Adapter Card, Block Diagram (Simplified).

Functional Description

A simplified block diagram of the HGLM-1063 module is shown in Figure 2. This block diagram shows the 5 key elements of the module. These are the Transmitter I.C., the Laser Diode Assembly, the Receiver I.C., the photodiode assembly, and the Open Fiber Control circuit. The high level of integration on the HGLM-1063 is apparent from this block diagram. Pin assignments and signal definitions are given on pages 6 and 7.

In general, the HGLM-1063 utilizes a user provided Transmit Byte Clock (TBC) of 53.125 MHz to transmit two 8b/10b encoded data bytes, simultaneously, by creating a serial data stream of 1062.5 MBd and modulating a 780 nm laser diode with it. The 20 bit wide (two encoded bytes) data input is provided to the module through the 80 pin connector in standard TTL format. Similarly, the HGLM-1063 receives 780 nm optical signals at a data rate of 1062.5 MBd, deserializes this data stream to recover the two encoded data bytes and provides this 20 bit wide standard TTL data to the receiving system via the 80 pin connector. The receiver also recovers the byte rate clock for use in clocking the received 20 bit wide parallel data.

Link Acquisition and Power Up

The following discussion assumes the HGLM-1063 is connected in a full duplex point to point link as shown in Figure 3. When initially applying power to the HGLM-1063, the Transmit Byte Clock must start no later than 5 msec after the +5 volt supply reaches the +4 volt level. If this requirement is not met, the Open Fiber Control (OFC) circuit may stick in a nonfunctional state. If this should happen, the OFC can be put into a functional state by holding the Enable Wrap (EWRAP) line high for 10.5 seconds. Once the TBC is running, and the module is properly powered up, the following sequence should be followed to bring the link into full synchronization and ready to transmit data:

1. Both Link Unusable lines will be driven high, by the OFC, indicating neither receiver is detecting a signal from the link.

2. Drive the Transmit Data lines, Tx[00:19] to a 01010101010101010101.

3. Drive the input control lines as follows:
- Enable Wrap: **low**
- Tx_SI: **low**
- Enable Comma Detect: **high**
- -Lock to Reference: **high**

4. Assuming the link is properly connected, and both link ends are in the same state of readiness, the lasers will turn on in 10.1 seconds. This will be indicated by the Link Unusable lines going low. This transition indicates the OFC is operational and in control.

5. Once the lasers have come on, and Link Unusable is observed to transition low, bring -Lock to Reference low for at least 500 µsec. This forces the module to frequency lock to the Transmit Byte Clock.

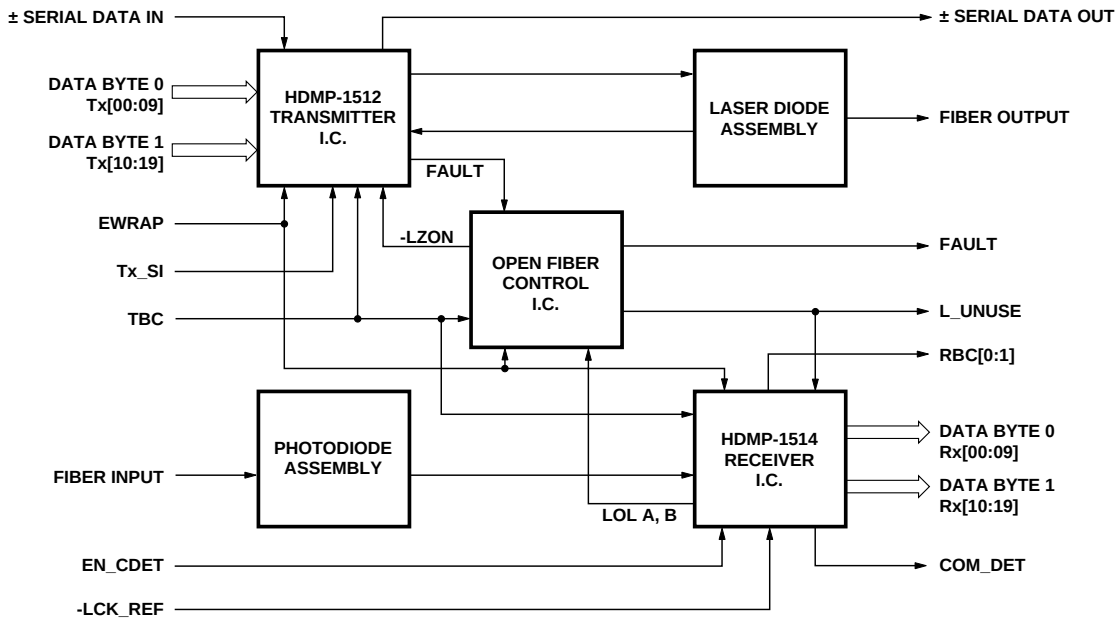


Figure 2. HGLM-1063 Functional Block Diagram.

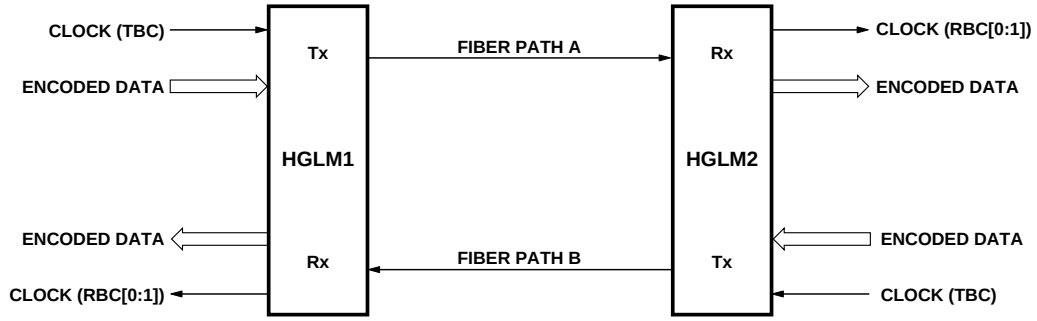


Figure 3. Full Duplex Point to Point Link.

Figure 4. Typical HGLM-1063 Label.

6. After holding -Lock to Reference low for 500 µsec it should then be driven high. This causes the module to phase and frequency lock onto the incoming data stream within 2500 bit times (2.4 µsec).

7. After 2500 bit times, the modules should be in bit synchronization, but not yet byte synchronization. The Receive Byte Clock (RBC0) should be running at 53.125 MHz.

8. Finally, drive the data lines Tx[00:19] with a K28.5 (comma or byte sync) character. Upon detection of this character, the receiver will drive the Comma Detect line high, the clocks will align to the byte boundary, and the receive data lines (Rx[00:19]) will have valid data. The link is now ready for data transmission.

TX_SI Operation

In normal operation, pin Tx_SI should be held low. In this mode, the data at Tx[00:19] is serialized and driven over the fiber optic link. With pin Tx_SI driven high, however, the data at Tx[00:19] is serialized and driven out the ± Serial Data Out lines and the data applied to the ± Serial Data In lines are driven over the fiber optic link.

EWRAP Operation

To aid in link diagnostics, the modules have the capability of wrapping the local transmit data electrically back to the local deserializer. This feature is enabled by driving the EWRAP pin high. When enabled, EWRAP causes the laser to turn off within 20 µsec. The OFC circuit goes into its low duty cycle "on-off-on" handshake mode. The link will need to be stepped through the synchronization procedure outlined above to return to normal operation after EWRAP is brought low.

Enable Comma Detect

In the synchronization procedure above, the Enable Comma Detect (EN_CDET) signal is driven high to allow the receiver to reset and align its boundaries properly when a K28.5 character is transmitted. This line can be kept in a high state and the receiver will reset on every K28.5 character it detects. This feature can be disabled, after initial synchronization, by driving Enable Comma Detect to a low state.

Open Fiber Control

The purpose of the Open Fiber Control (OFC) integrated circuit is to ensure user safety. This circuit uses the dual loss of light signals from the receiver I.C. and the laser Fault detection signal from the transmitter I.C. to determine if the laser and the fiber link are properly connected and functioning normally. Should a Fault condition be determined, all laser transmission is shut down.

A safety interlock is provided by the HGLM-1063 module. HGLM-1063 modules (or equivalent) must be connected in full point-to-point configuration as shown in Figure 3 for proper operation. The Open Fiber Control System (OFCS) of the HGLM-1063 deactivates the laser signal whenever there is an interruption or loss of signal of either laser drive circuit.

For example, in Figure 3, if Path A is opened through a cut or other physical damage to the fiber, or if the fiber is disconnected at either the transmitting port of HGLM1 or the receiving port of HGLM2, the OFCS detects the loss of signal. The Link Unusable line of HGLM2 goes high, signaling the system of an open fiber condition. The OFCS then shuts down the laser of HGLM2. HGLM1 in turn detects this loss of signal, raises its Link Unusable line, and shuts down its laser. The OFC pulses the laser of HGLM2 at a very low duty cycle. Simultaneously, the OFCS of HGLM1 detects the low duty cycle operation of HGLM2 and places its laser in the same low duty cycle pulsing mode. It takes less than 2 msec to shut down all laser transmission and results in a safe (Class I) laser emission level in Path A, the open path.

While Path A is still open, HGLM1 launches a pulse synchronously with the pulse it receives on Path B from HGLM2. However, HGLM2 receives no pulse (because Path A is open) and continues in an inactive mode. HGLM2 will continue launching "inquiry" pulses once approximately every 10.1 seconds along Path B.

After Path A is restored, HGLM2 will receive pulses along Path A, synchronous with its transmit pulses along Path B. A completed link of Path A and Path B is verified by both HGLM1 and HGLM2. HGLM2 will verify its link by deactivating its laser and confirm that its receive signal disappears. HGLM1 also performs the same verification check, deactivating its laser. Once both HGLM modules have

deactivated their lasers, HGLM2 then activates its laser, sends a signal to HGLM1 (which activates its laser), which in turn sends a confirming signal back to HGLM2. This on-off-on handshake confirms that the first synchronous pulse came from another HGLM-1063, or equivalent module, with an OFC safety system. Once this sequence is complete, the link between HGLM1 and HGLM2 returns to normal operation, with both in the active mode. The on-off-on timing is compatible with the timing requirements of the ANSI FC-PH specification for Open Fibre Control timing of 100-M5-SL-I links. These timings are defined as Decode 1, 2, and 3 and are given in the Timing Specifications table later in this document.

Laser Safety Compliance

The HGLM-1063 is designed and certified as a Class 1 laser product per 21 CFR (U.S. Code of Federal Regulations), Subchapter J. A Class 1 laser product is safe for use and does not pose a biological hazard if used in accordance within the data sheet limits and instructions.

CAUTION:

There are no user serviceable parts nor any maintenance required for the HGLM-1063. All adjustments are made at the factory before shipment to our customers. Tampering with, modifying or breaking the preset trim pot seals will result in voided product warranty. It may also result in improper operation of the HGLM-1063 circuitry, and possible overstress of the laser source. Device degradation or product failure may result.

Connection of the HGLM-1063 to a non-approved optical source, operating above the recommended absolute maximum conditions (especially power supply) or operating the HGLM-1063 in a manner inconsistent with its design and function may result in hazardous radiation exposure and may be considered an act of modifying or manufacturing a laser product. The person(s) performing such an act is required by law to recertify and reidentify the laser product under the provisions of 21 CFR(Subchapter J).

Labeling

Each HGLM-1063 module is labeled per 21 CFR (Subchapter J), including the actual date of manufacture (Figure 4).

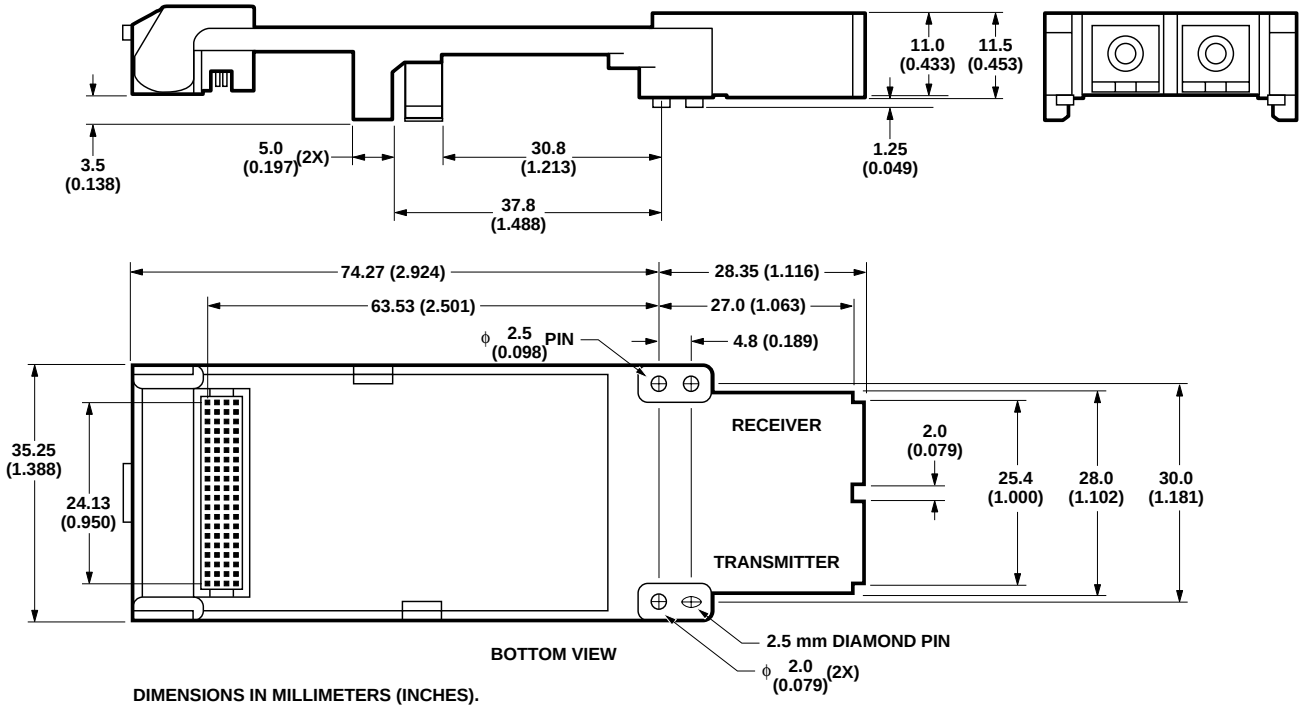


Figure 5. HGLM-1063 Outline Drawing.

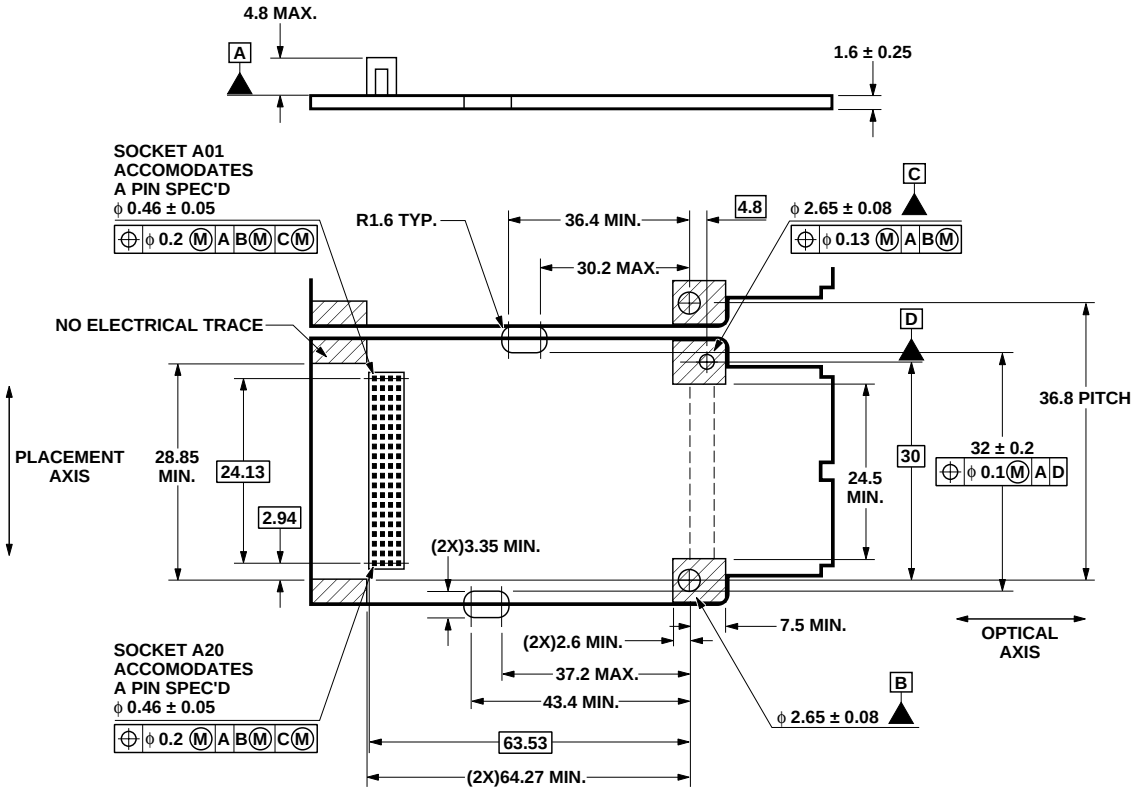


Figure 6. Host PCB Layout for Mounting the HGLM-1063.

HGLM-1063 Pin Assignments

Pin	Name	Pin	Name	Pin	Name	Pin	Name
A01	+SO	B01	-SO	C01	gnd	D01	+SI
A02	gnd	B02	gnd	C02	gnd	D02	-SI
A03	V_{CC}	B03	TX[10]	C03	TX[00]	D03	V_{CC}
A04	TX[12]	B04	TX[11]	C04	TX[02]	D04	TX[01]
A05	TX[14]	B05	TX[13]	C05	TX[04]	D05	TX[03]
A06	TX[16]	B06	TX[15]	C06	TX[06]	D06	TX[05]
A07	TX[18]	B07	TX[17]	C07	TX[08]	D07	TX[07]
A08	gnd	B08	TX[19]	C08	TX[09]	D08	gnd
A09	STROB_ID	B09	gnd	C09	gnd	D09	V_{CC}
A10	V_{CC}	B10	L_UNUSE	C10	FAULT	D10	TBC
A11	PAR_ID[1]	B11	rsv	C11	TX_SI	D11	PAR_ID[0]
A12	RBC[0]	B12	EWRAP	C12	COM_DET	D12	V_{CC}
A13	V_{CC}	B13	gnd	C13	rsv	D13	RBC[1]
A14	gnd	B14	RX[10]	C14	RX[00]	D14	gnd
A15	RX[12]	B15	RX[11]	C15	RX[02]	D15	RX[01]
A16	RX[14]	B16	RX[13]	C16	RX[04]	D16	RX[03]
A17	RX[16]	B17	RX[15]	C17	RX[06]	D17	RX[05]
A18	RX[18]	B18	RX[17]	C18	RX[08]	D18	RX[07]
A19	V_{CC}	B19	RX[19]	C19	RX[09]	D19	V_{CC}
A20	EN_CDET	B20	gnd	C20	gnd	D20	-LCK_REF

HGLM-1063 Signal Definitions

Symbol	Signal Name	I/O	Logic Level	Description
TX[00:19]	Transmit Data	Input	TTL	The 20-bit parallel transmit data to be serialized and sent to the transmitter.
TBC	Transmit Byte Clock	Input	TTL	Used to operate the state machines, derive the 20X serial clocks, and latch TX[00:19].
EWRAP	Enable Wrap/Enable STROP_ID	Input	TTL	Causes the serialized transmit data to electrically wrap back to the deserializer and disables the laser output.
-LCKREF	Lock to Reference	Input	TTL	Causes the PLL to lock to TBC.
TX_SI	Transmit SI	Input	TTL	Selects the serial data mode.
EN_CDET	Enable Comma Detect/STROB_ID clock	Input	TTL	Enables the comma detection circuitry to establish byte synchronization on the next comma that is received.
± SI	Serial Data In	Input	PECL	A pair of differential signals for transmission of serial data.
RX[00:19]	Receive Data	Output	TTL	The 20 bit decoded received data from the receiver.
RBC[0]	Receive Byte Clock 0	Output	TTL	Used by the system to latch RX[00:19].
RBC[1]	Receive Byte Clock 1	Output	TTL	Not normally used.
COM_DET	Comma Detect	Output	TTL	Indicates byte synchronization has occurred.
L_UNUSE	Link Unusable	Output	TTL	Indicates the link is currently not usable.
FAULT	Fault	Output	TTL	Indicates an electrical fault has been detected and turns the laser output off.
± SO	Serial Data Out	Output	PECL	A pair of high speed differential signals representing the serialized data.
PAR_ID	Parallel ID	Output	TTL	A 2 bit identification of the link rate.
STROB_ID	Strobed ID	Output	TTL	Optional output used to access the serial Strobed ID information. Not active.
rsv	Reserved			Reserved for future use.

Absolute Maximum Ratings

T_C = 25°C, except as specified. Operation in excess of any one of these conditions may result in permanent damage to this device.

Symbol	Parameter	Units	Min.	Max.
V_{CC}	Supply Voltage	V	-0.5	6.0
$V_{IN,TTL}$	TTL Data Input Voltage	V	-0.7	V_{CC} + 0.7
$I_{O,TTL}$	TTL Output Source Current	mA		13
T_{stg}	Storage Temperature	°C	-40	+75
T_{OP}	Ambient Operating Temperature	°C	0	+60
RHop	Relative Humidity Operating	%	8	80
RHst	Relative Humidity Storage	%	5	95

Transmit Byte Clock Requirements

T_A = 10°C to +50°C, V_{CC} = 4.5 V to 5.5 V

Symbol	Parameter	Unit	Min.	Typ.	Max.
f	Nominal Frequency	MHz	53.119	53.125	53.131
F_{tol}	Frequency Tolerance (for Fibre Channel Compliance)	ppm	-100		+100
Symm	Symmetry (Duty Cycle)	%	40		60
Jpe	Positive Edge Jitter	ns			0.5
t_r	Rise Time, 20% to 80%	nsec			4
t_f	Fall Time, 20% to 80%	nsec			4

DC Electrical Specifications

T_A = 10°C to +50°C, V_{CC} = 4.5 V to 5.5 V

Symbol	Parameter	Unit	Min.	Typ.	Max.
$V_{IH,TTL}$	TTL Input High Voltage Level, Guaranteed High Signal for All Inputs, I_{IH} = 100 µA	V	2		5
$V_{IL,TTL}$	TTL Input Low Voltage Level, Guaranteed Low Signal for All Inputs, I_{IL} = -1 mA	V	0		0.8
$V_{OH,TTL}$	TTL Output High Voltage Level, I_{OH} = 1 mA	V	2.4		5
$V_{OL,TTL}$	TTL Output Low Voltage Level, I_{OL} = -1 mA	V	0		0.6
I_{CC}	V_{CC} Supply Current	mA			1200
$V_{CC,noise}$	Peak to Peak Noise and Ripple Allowed on the V_{CC} Input	mV			100

AC Electrical Specifications

T_A = 10°C to +50°C, V_{CC} = 4.5 V to 5.5 V

Symbol	Parameter	Units	Min.	Typ.	Max.
$t_{r,TTLin}$	Input TTL Rise Time, 20% to 80%	nsec		2	
$t_{f,TTLin}$	Input TTL Fall Time, 20% to 80%	nsec		2	
$t_{r,TTLout}$	Output TTL Rise Time, 20% to 80%, 15 pF Load	nsec		2	4
$t_{f,TTLout}$	Output TTL Fall Time, 20% to 80%, 15 pF Load	nsec		2	4
$t_{r,RBC}$	Receive Byte Clock Rise Time, 0.8 V to 2.0 V, 15 pF Load	nsec		1.5	3.0
$t_{f,RBC}$	Receive Byte Clock Fall Time, 2.0 V to 0.8 V, 15 pF Load	nsec		1.5	2.4
$t_{r,\ BLL}$	BLL Rise Time, AC Coupled, 25 Ω Source and Load, 20% to 80%	psec		150	350
$t_{f,BLL}$	BLL Fall Time, AC Coupled, 25 Ω Source and Load, 20% to 80%	psec		150	350
$VSWR_{i,H50}$	H50 Input VSWR, AC Coupled, 50 Ω Source and Load			2.0	
$VSWR_{o,BLL}$	BLL Output VSWR, AC Coupled, 50 Ω Source and Load			2.0	
$V_{IP,H50}$	Input Peak-To-Peak Differential Voltage, AC Coupled, 50 Ω Load	mV	50	1200	2000
$V_{OP,BLL}$	BLL Output Peak-To-Peak Differential Voltage, AC Coupled, 50 Ω Load	mV	1200	1400	2000

Timing Specifications

T_A = 10°C to +50°C, V_{CC} = 4.5 V to 5.5 V

Symbol	Parameter	Units	Min.	Typ.	Max.
t_{Dcd_1}	Decode 1 Time	µsec		154	
t_{Dcd_2}	Decode 2 Time	µsec		617	
t_{Dcd_3}	Decode 3 Time	µsec		154	
Transmitter					
t_s	Transmit Data Setup Time	nsec	2.0		
t_h	Transmit Data Hold Time	nsec	3.3		
Receiver					
t_s	Receive Data Setup Time	nsec	2.5		
t_h	Receive Data Hold Time	nsec	6.0		

Optical Specifications

T_A = 10°C to +50°C, V_{CC} = 4.5 V to 5.5 V

Symbol	Parameter	Units	Min.	Typ.	Max.
f_{op}	Serial Baud Rate	Mbaud	1062.38	1062.5	1062.62
OPB	Optical Power Budget	dB	6	8	
	Optical Extinction Ratio	dB	6		
PT	Transmitter Launched Optical Power, Average	dBm	-5.0	-2.5	1.3
P_{Rx}	Receiver Input Power, Average, BER = 10^{-12}	dBm	-13.0		1.3
RL	Receiver Return Loss	dB	12		
λ	Receiver Operating Wavelength	nm	770	780	850
λ_C	Transmitter Spectral Center Wavelength	nm	770	790	795
$\Delta\lambda$	Transmitter Spectral Width, RMS	nm			4
RIN_{12}	Transmitter Relative Intensity Noise	dB/Hz			-116
DJ	Transmitter Deterministic Jitter, peak-peak	%			20
	Transmitter Eye Opening, peak-peak, BER = 1E-12	%	57		

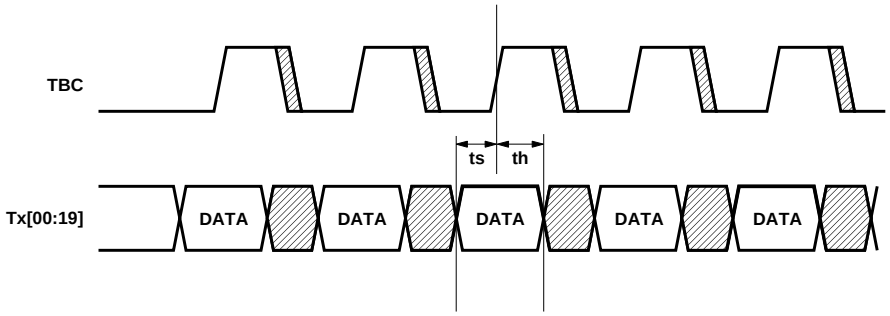


Figure 7. Transmit Byte Clock and Data Timing Relationships.

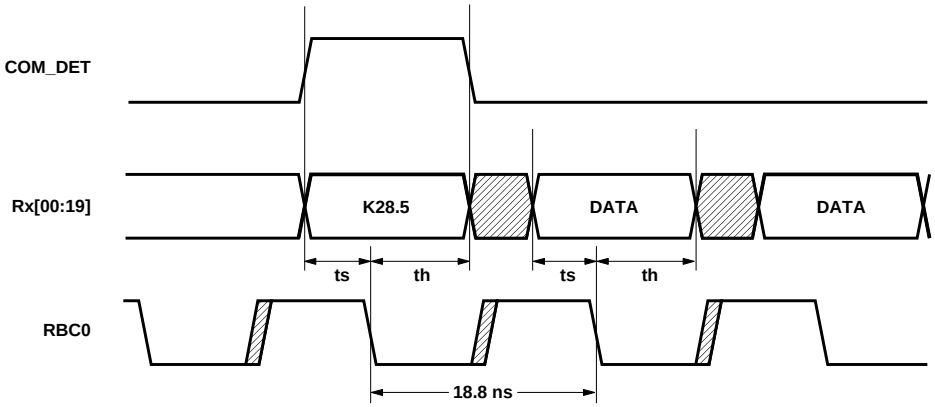


Figure 8. Receive Timing Relationships.