AON3402
20V N-Channel MOSFET

General Description

The AON3402 uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge and operation with gate voltages as low as 1.8V while retaining a 12V $V_{GS(MAX)}$ rating.This device is suitable for use as load switch and general purpose FET application.

Product Summary

V_{DS} (V) = 20V

I_D = 12.6A (V_{GS} = 4.5V)

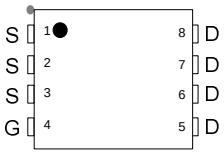
$R_{DS(ON)}$ < 13mΩ (V_{GS} = 4.5V)

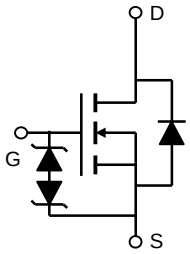
$R_{DS(ON)}$ < 17mΩ (V_{GS} = 2.5V)

$R_{DS(ON)}$ < 26mΩ (V_{GS} = 1.8V)

Green Product

Top View





Absolute Maximum Ratings T_A=25℃ unless otherwise noted				
Parameter		**Symbol**	**Maximum**	**Units**
Drain-Source Voltage		V_{DS}	20	V
Gate-Source Voltage		V_{GS}	±12	V
Continuous Drain Current [A]	T_A=25℃	I_D	12.6	A
	T_A=70℃		10	
Pulsed Drain Current [B]		I_{DM}	40	
Power Dissipation [A]	T_A=25℃	P_D	3.1	W
	T_A=70℃		2	
Junction and Storage Temperature Range		T_J, T_{STG}	-55 to 150	℃

Thermal Characteristics					
Parameter		**Symbol**	**Typ**	**Max**	**Units**
Maximum Junction-to-Ambient [A]	t ≤ 10s	$R_{\theta JA}$	30	40	℃/W
Maximum Junction-to-Ambient [A]	Steady-State		65	80	℃/W
Maximum Junction-to-Lead [C]	Steady-State	$R_{\theta JL}$	20	25	℃/W

Electrical Characteristics (T_J=25℃ unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV_{DSS}	Drain-Source Breakdown Voltage	I_D=250μA, V_{GS}=0V	20			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=16V, V_{GS}=0V			10	μA
		T_J=55℃			25	
I_{GSS}	Gate-Body leakage current	V_{DS}=0V, V_{GS}=±10V			10	μA
BV_{GSO}	Gate-Source Breakdown Voltage	V_{DS}=0V, I_G=±250uA	±12			V
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS} I_D=250μA	0.5	0.78	1	V
$I_{D(ON)}$	On state drain current	V_{GS}=4.5V, V_{DS}=5V	40			A
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS}=4.5V, I_D=12A		10.3	13	mΩ
		T_J=125℃		14.4	18	
		V_{GS}=2.5V, I_D=10.5A		14.3	17	mΩ
		V_{GS}=1.8V, I_D=8.5A		21.7	26	mΩ
g_{FS}	Forward Transconductance	V_{DS}=5V, I_D=12A		37		S
V_{SD}	Diode Forward Voltage	I_S=1A,V_{GS}=0V		0.73	1	V
I_S	Maximum Body-Diode Continuous Current				4.8	A
DYNAMIC PARAMETERS						
C_{iss}	Input Capacitance	V_{GS}=0V, V_{DS}=10V, f=1MHz		1810		pF
C_{oss}	Output Capacitance			232		pF
C_{rss}	Reverse Transfer Capacitance			200		pF
R_g	Gate resistance	V_{GS}=0V, V_{DS}=0V, f=1MHz		1.6		Ω
SWITCHING PARAMETERS						
Q_g	Total Gate Charge	V_{GS}=4.5V, V_{DS}=10V, I_D=12A		17.9		nC
Q_{gs}	Gate Source Charge			1.5		nC
Q_{gd}	Gate Drain Charge			4.7		nC
$t_{D(on)}$	Turn-On DelayTime	V_{GS}=10V, V_{DS}=10V, R_L=1.0Ω, R_{GEN}=3Ω		2.5		ns
t_r	Turn-On Rise Time			7.2		ns
$t_{D(off)}$	Turn-Off DelayTime			49		ns
t_f	Turn-Off Fall Time			10.8		ns
t_{rr}	Body Diode Reverse Recovery Time	I_F=12A, dI/dt=100A/μs		20.2		ns
Q_{rr}	Body Diode Reverse Recovery Charge	I_F=12A, dI/dt=100A/μs		8		nC

A: The value of $R_{\theta JA}$ is measured with the device mounted on 1in^2 FR-4 board with 2oz. Copper, in a still air environment with T_A=25℃. The value in any given application depends on the user's specific board design. The current rating is based on the t ≤ 10s thermal resistance rating.

B: Repetitive rating, pulse width limited by junction temperature.

C. The $R_{\theta JA}$ is the sum of the thermal impedence from junction to lead $R_{\theta JL}$ and lead to ambient.

D. The static characteristics in Figures 1 to 6 are obtained using 300 μs pulses, duty cycle 0.5% max.

E. These tests are performed with the device mounted on 1 in^2 FR-4 board with 2oz. Copper, in a still air environment with T_A=25℃. The SOA curve provides a single pulse rating.

Rev2: Nov. 2010

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

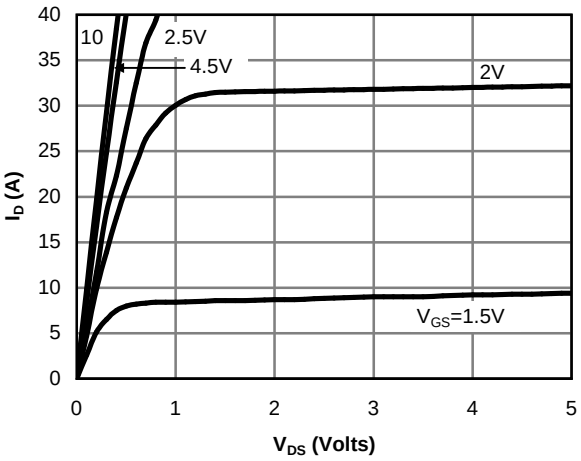


Fig 1: On-Region Characteristics

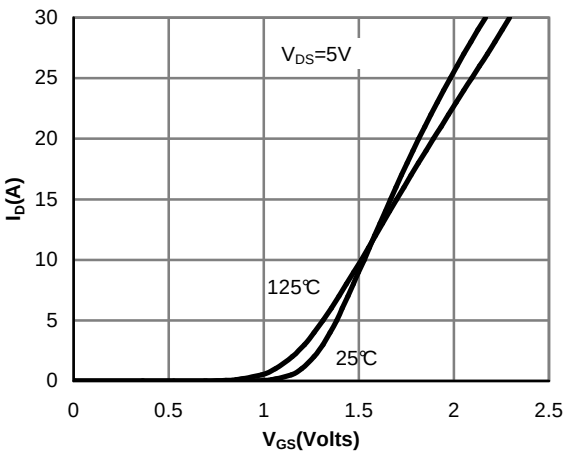


Figure 2: Transfer Characteristics

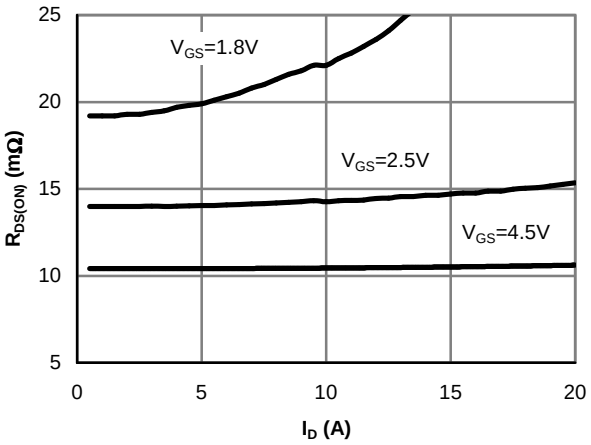


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

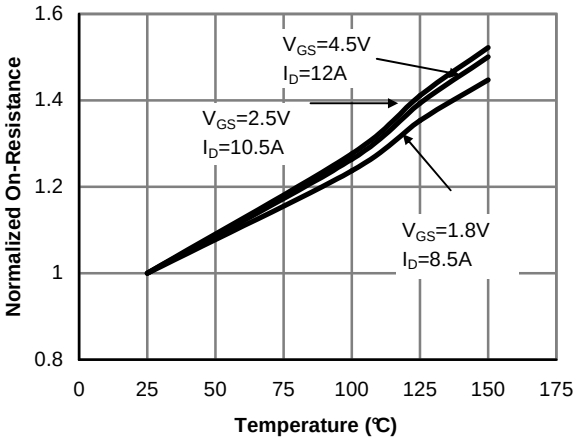


Figure 4: On-Resistance vs. Junction Temperature

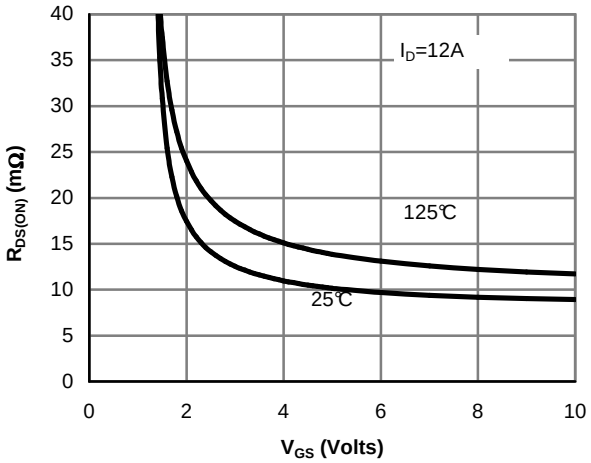


Figure 5: On-Resistance vs. Gate-Source Voltage

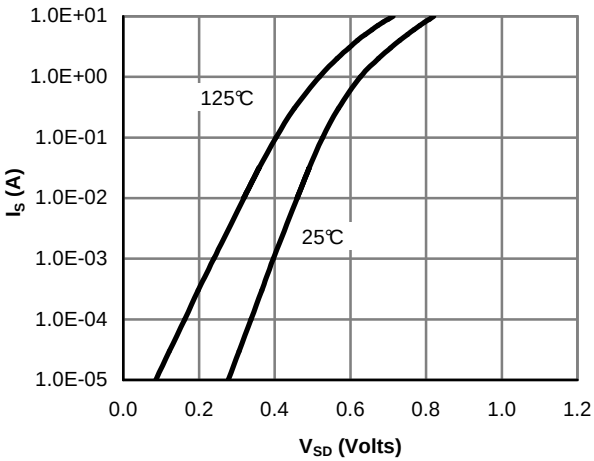


Figure 6: Body-Diode Characteristics

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

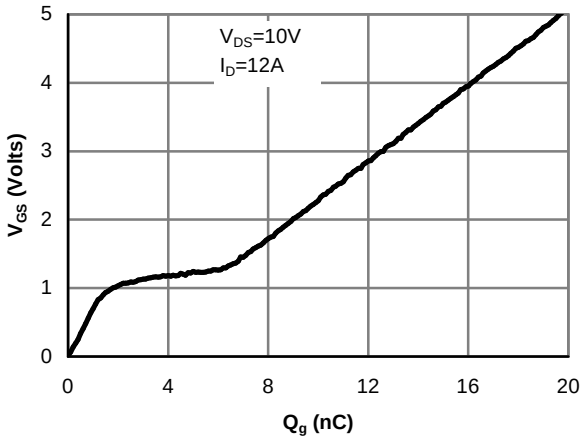


Figure 7: Gate-Charge Characteristics

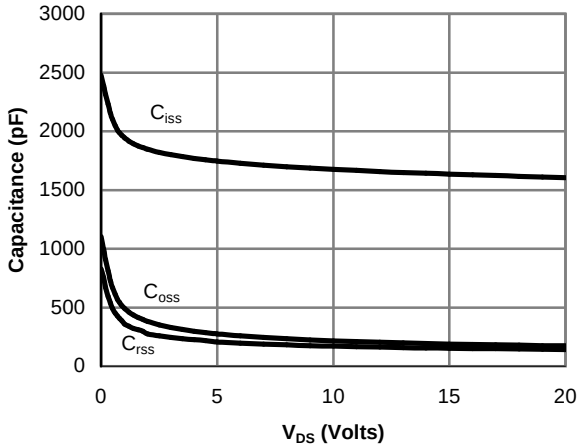


Figure 8: Capacitance Characteristics

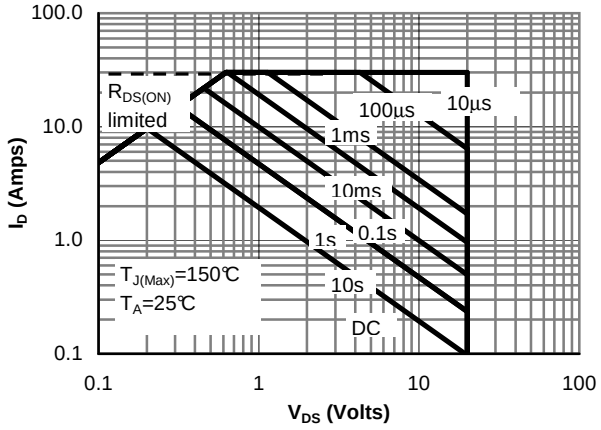


Figure 9: Maximum Forward Biased Safe Operating Area (Note E)

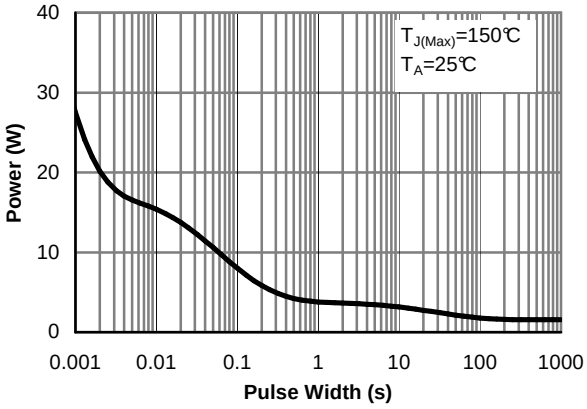


Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note E)

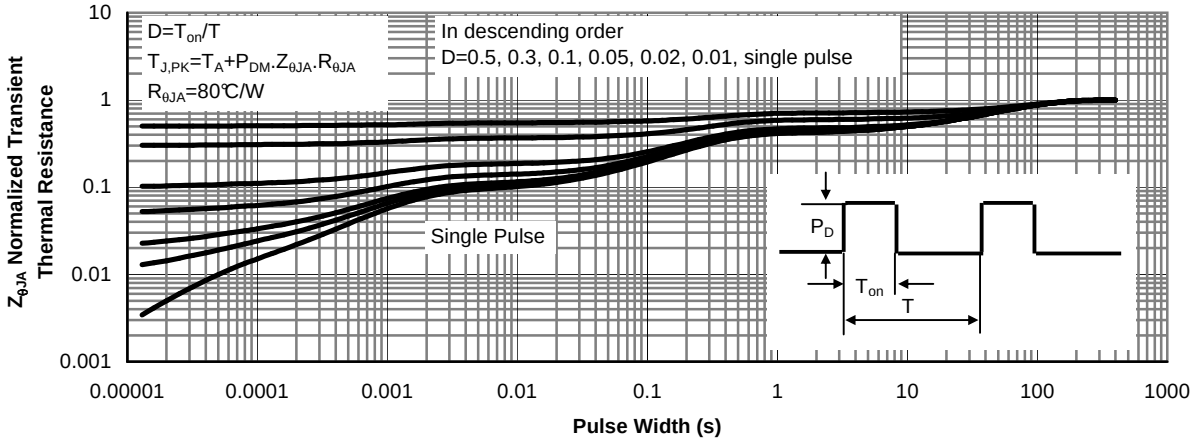


Figure 11: Normalized Maximum Transient Thermal Impedance