

# IP4352CX24

9-channel SD-memory card interface filter with ESD protection to IEC 61000-4-2 level 4

Rev. 01 — 13 August 2009

Product data sheet

## 1. Product profile

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### 1.1 General description

The IP4352CX24 is a diode array for protecting downstream components from ElectroStatic Discharge (ESD) voltages up to 8 kV.

The IP4352CX24 is fabricated using monolithic silicon semiconductor technology integrating 9 pairs of rail-to-rail diodes, 15 resistors and 12 Zener diodes in a single Wafer-Level Chip-Scale Package (WLCSP). These features make the IP4352CX24 ideal for applications requiring miniaturized components, such as mobile phone handsets, cordless telephones and personal digital devices.

### 1.2 Features

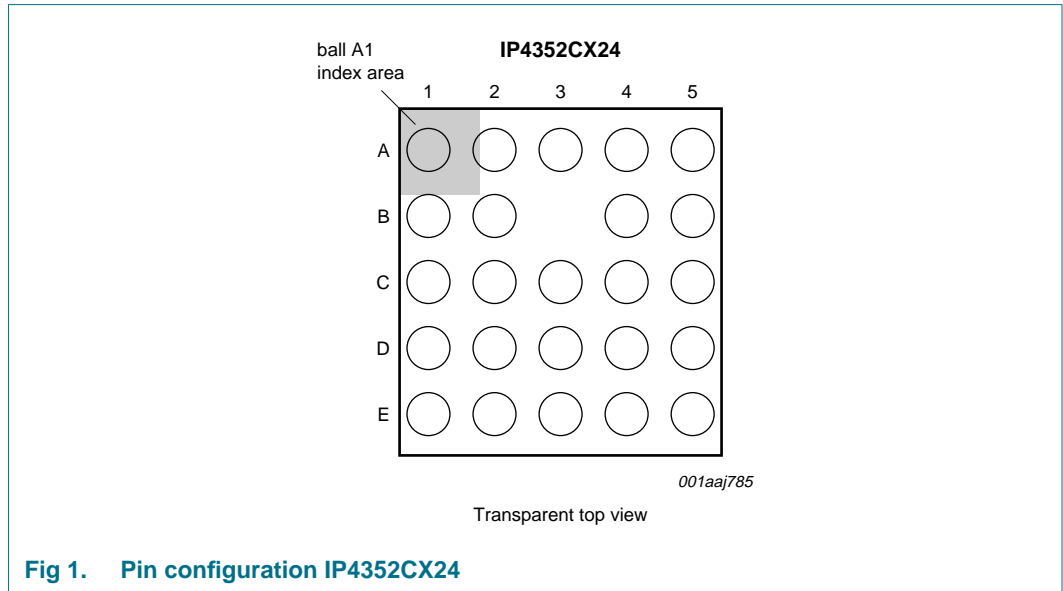
- Pb-free, RoHS compliant, free of halogen and antimony (Dark Green compliant)
- All SD-memory card channels have integrated ESD protection and EMI/RF filters
- 9 channels with > 8 kV ESD protection at output terminals
- 5 channels with integrated EMI/RF filters and pull-up resistors
- 4 channels with integrated EMI/RF filters
- Additional SD-card power supply protection
- WLCSP with 0.4 mm pitch

### 1.3 Applications

- SD-memory card interfaces in cellular and PCS mobile handsets
- Cordless telephones
- PDAs

## 2. Pinning information

### 2.1 Pinning



**Fig 1. Pin configuration IP4352CX24**

**Table 1. Pinning**

Pin	Description
A1	DATA2: data line 2
A2	DATA3: data line 3
A3	GND1: ground 1
A4	SDDATA2: secure digital data 2
A5	SDDATA3: secure digital data 3
B1	CD: card detect
B2	CMD: command
B3	not connected
B4	SDCD: secure digital card detect
B5	SDCMD: secure digital command
C1	DAT3_PD: data 3 pull-down
C2	WP: write protect
C3	DAT3_PU: data 3 pull-up
C4	SDWP: secure digital write protect
C5	VSD: supply voltage
D1	WP+CD: write protect and card detect
D2	CLK: clock
D3	GND2: ground 2
D4	SDWP+CD: secure digital write protect and card detect
D5	SDCLK: secure digital clock
E1	DATA1: data line 1

Table 1. Pinning ...continued

Pin	Description
E2	DATA0: data line 0
E3	GND3: ground 3
E4	SDDATA1: secure digital data 1
E5	SDDATA0: secure digital data 0

### 3. Ordering information

Table 2. Ordering information

Type number	Package		Version
	Name	Description	
IP4352CX24	WLCSP24	wafer level chip-size package; 24 bumps; 2.01 × 2.02 × 0.61 mm	IP4352CX24

### 4. Functional diagram

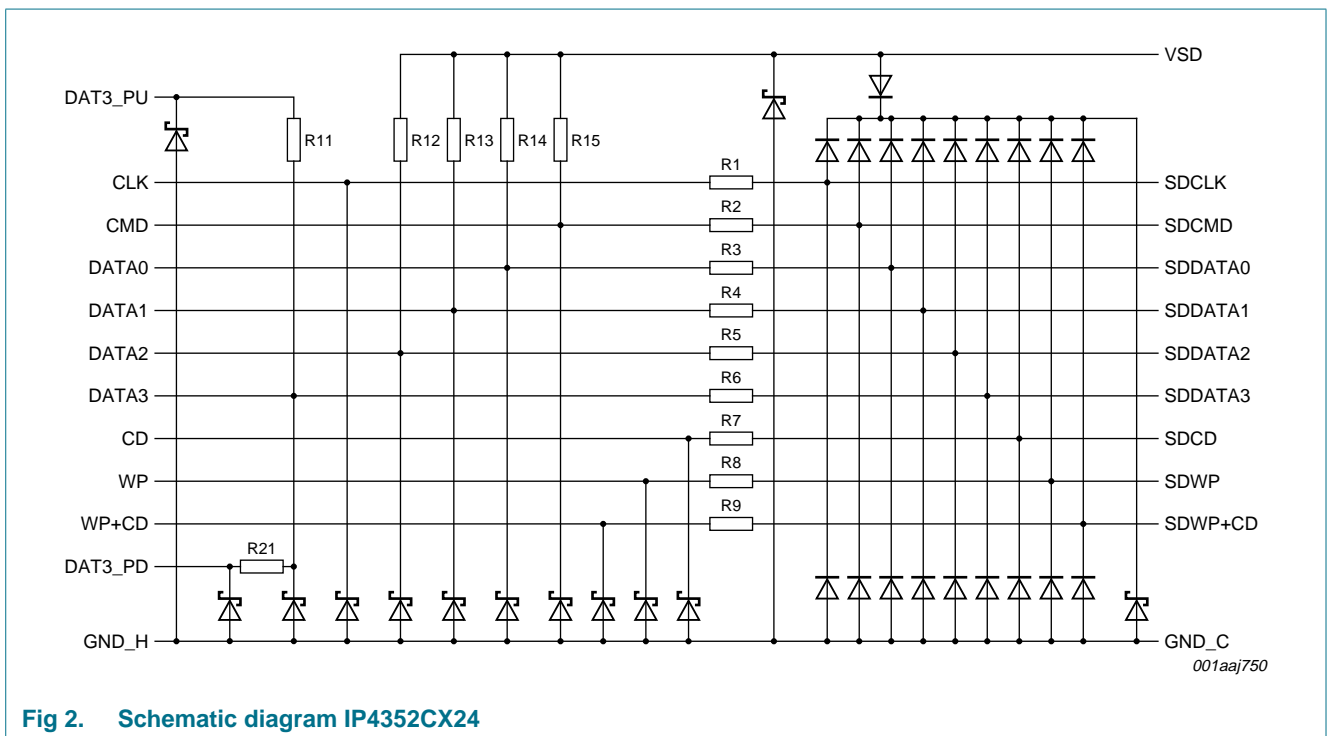


Fig 2. Schematic diagram IP4352CX24

## 5. Limiting values

**Table 3. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_I$	input voltage		-0.5	+5.0	V
$V_{ESD}$	electrostatic discharge voltage	IEC 61000-4-2, level 4; output pins A4, A5, B4, B5, C4, C5, D4, D5, E4, E5; pins A3, D3 and E3 connected to ground			
		contact discharge	[1] -8	+8	kV
		air discharge	-15	+15	kV
		IEC 61000-4-2, level 1; all other pins; pins A3, D3 and E3 connected to ground			
		contact discharge	-2	+2	kV
		air discharge	-2	+2	kV
$P_{ch}$	channel power dissipation	continuous power; $T_{amb} = 70\text{ °C}$	-	25	mW
$P_{tot}$	total power dissipation	$T_{amb} = 70\text{ °C}$	-	100	mW
$T_{stg}$	storage temperature		-55	+150	°C
$T_{reflow(peak)}$	peak reflow temperature	10 s maximum	-	260	°C
$T_{amb}$	ambient temperature		-30	+85	°C

[1] Device is tested with 1000 pulses of  $\pm 15\text{ kV}$  contact discharges, each according to the IEC 61000-4-2 model, and far exceeds specified level 4 (8 kV contact discharge).

## 6. Characteristics

**Table 4. Channel characteristics**

$T_{amb} = 25\text{ °C}$ ; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{s(ch)}$	channel series resistance	R1 to R9 $\pm 20\%$	32	40	48	$\Omega$
		R11 to R14 $\pm 30\%$	35	50	65	k $\Omega$
		R15 $\pm 30\%$	10.5	15	19.5	k $\Omega$
		R21 $\pm 30\%$	329	470	611	k $\Omega$
$C_{ch}$	channel capacitance	$V_{bias(DC)} = 0\text{ V}$ ; $f = 1\text{ MHz}$ ; pin DAT3_PU = 0 V; pin DAT3_PD = 0 V; pin VSD = 0 V				
		SD-card to I/O interface:	[1] -	-	20	pF
		pins DAT3_PD, DAT3_PU and VSD	[1] -	30	-	pF
$V_{BR}$	breakdown voltage	$I_{test} = 1\text{ mA}$	6.0	-	-	V
$I_{LR}$	reverse leakage current	per channel; $V_I = 3.0\text{ V}$	-	-	100	nA

[1] Guaranteed by design.

**Table 5. Frequency characteristics**

$T_{amb} = 25\text{ }^{\circ}\text{C}$ ; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$\alpha_{ij}$	insertion loss	all channels; $R_{gen} = 50\ \Omega$ ; $R_L = 50\ \Omega$				
		$f < 400\text{ MHz}$	-	-	9	dB
		$400\text{ MHz} < f < 800\text{ MHz}$	9	-	-	dB
		$800\text{ MHz} < f < 2.5\text{ GHz}$	13	-	-	dB
		$2.5\text{ GHz} < f < 6\text{ GHz}$	28	32	-	dB

**Table 6. Time domain characteristics**

$R_{gen} = 50\ \Omega$ ;  $R_s$  per channel =  $15\ \Omega$ ; generator  $t_r = t_f = 2\text{ ns}$ ;  $T_{amb} = 25\text{ }^{\circ}\text{C}$ ; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_r$	rise time	$R_L = 20\text{ pF} \parallel 100\text{ k}\Omega$	-	3.2	3.7	ns
		$R_L = 40\text{ pF} \parallel 100\text{ k}\Omega$	-	4.4	6	ns
$t_f$	fall time	$R_L = 20\text{ pF} \parallel 100\text{ k}\Omega$	-	3.3	4.3	ns
		$R_L = 40\text{ pF} \parallel 100\text{ k}\Omega$	-	5.5	7.5	ns

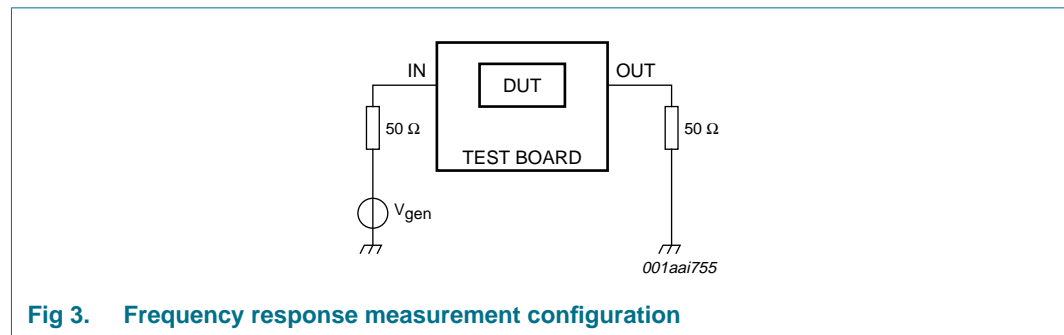
[1] Measured using source generator with 0 V to 3 V steps and 20 % to 70 % LOW-to-HIGH limits.

## 7. Application information

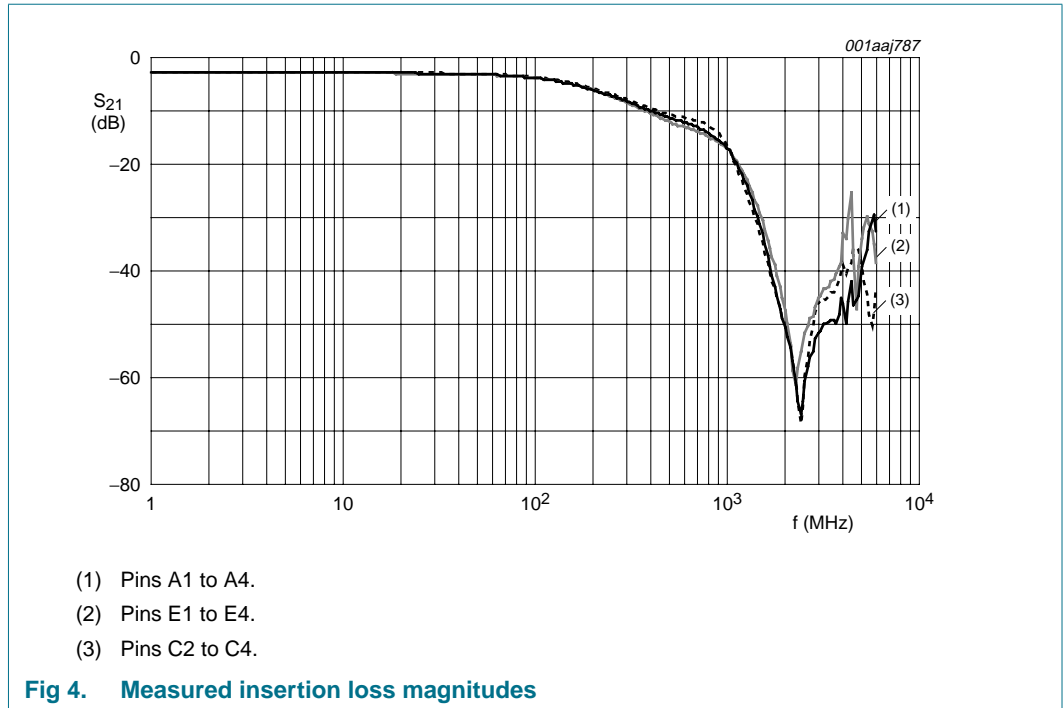
### 7.1 Insertion loss

The insertion loss was measured with a test PCB utilizing laser-drilled micro-via holes which connect the PCB ground plane to the ground pins.

The configuration for measuring insertion loss in a  $50\ \Omega$  system is shown in [Figure 3](#).



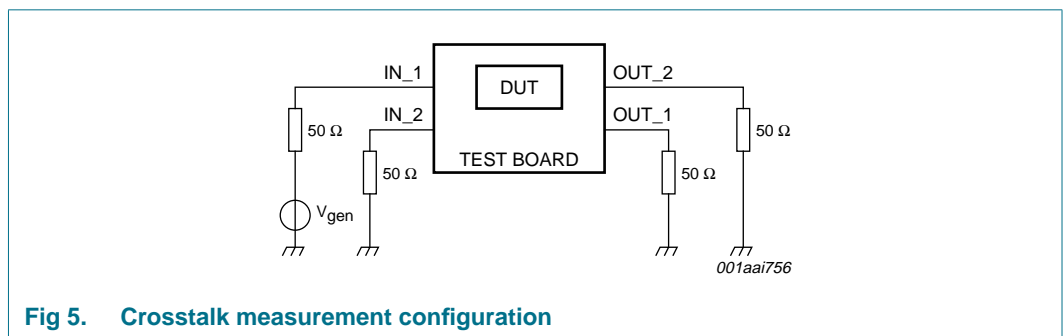
The frequency response curves measured on pins A1 and A4, E1 and E4 and C2 and C4 at frequencies up to 3 GHz is shown in [Figure 4](#).



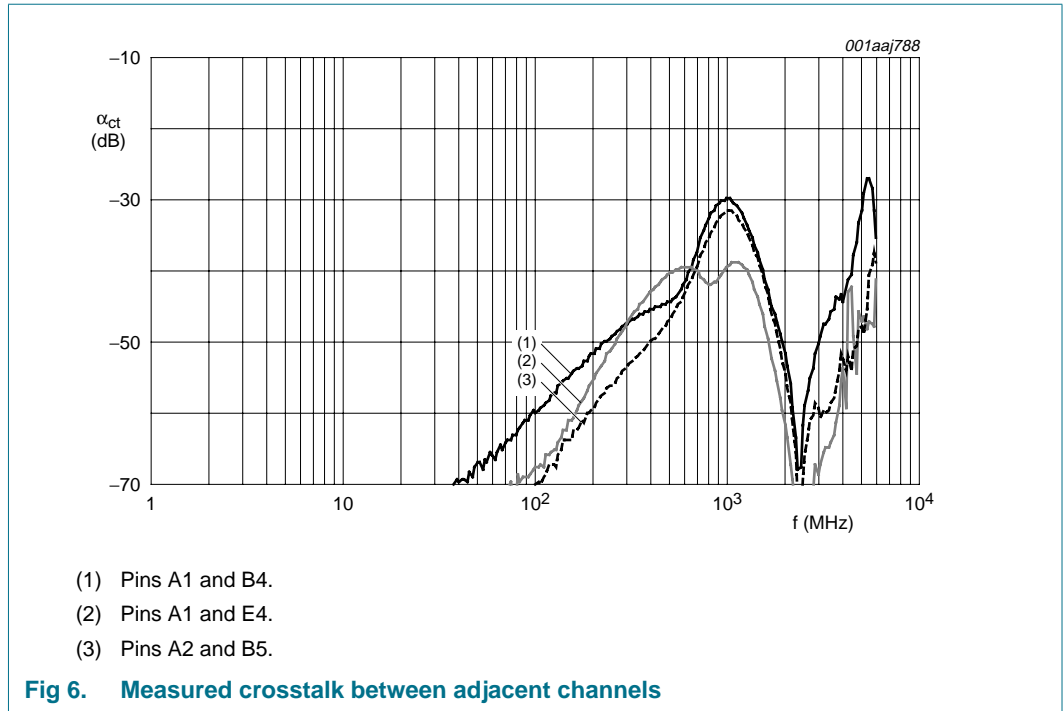
**7.2 Crosstalk**

The crosstalk between adjacent channels within the IP4352CX24 for different channel pairs was measured in a 50 Ω NetWork Analyzer (NWA) system.

The configuration for measuring crosstalk in a 50 Ω system is shown in [Figure 5](#).



The crosstalk measured for five different pairs of channels is shown in [Figure 6](#). In all cases, all unused connections are terminated with 50 Ω to ground.



8. Package outline

WLCSP24: wafer level chip-size package; 24 bumps; 2.01 x 2.02 x 0.61 mm

IP4352CX24

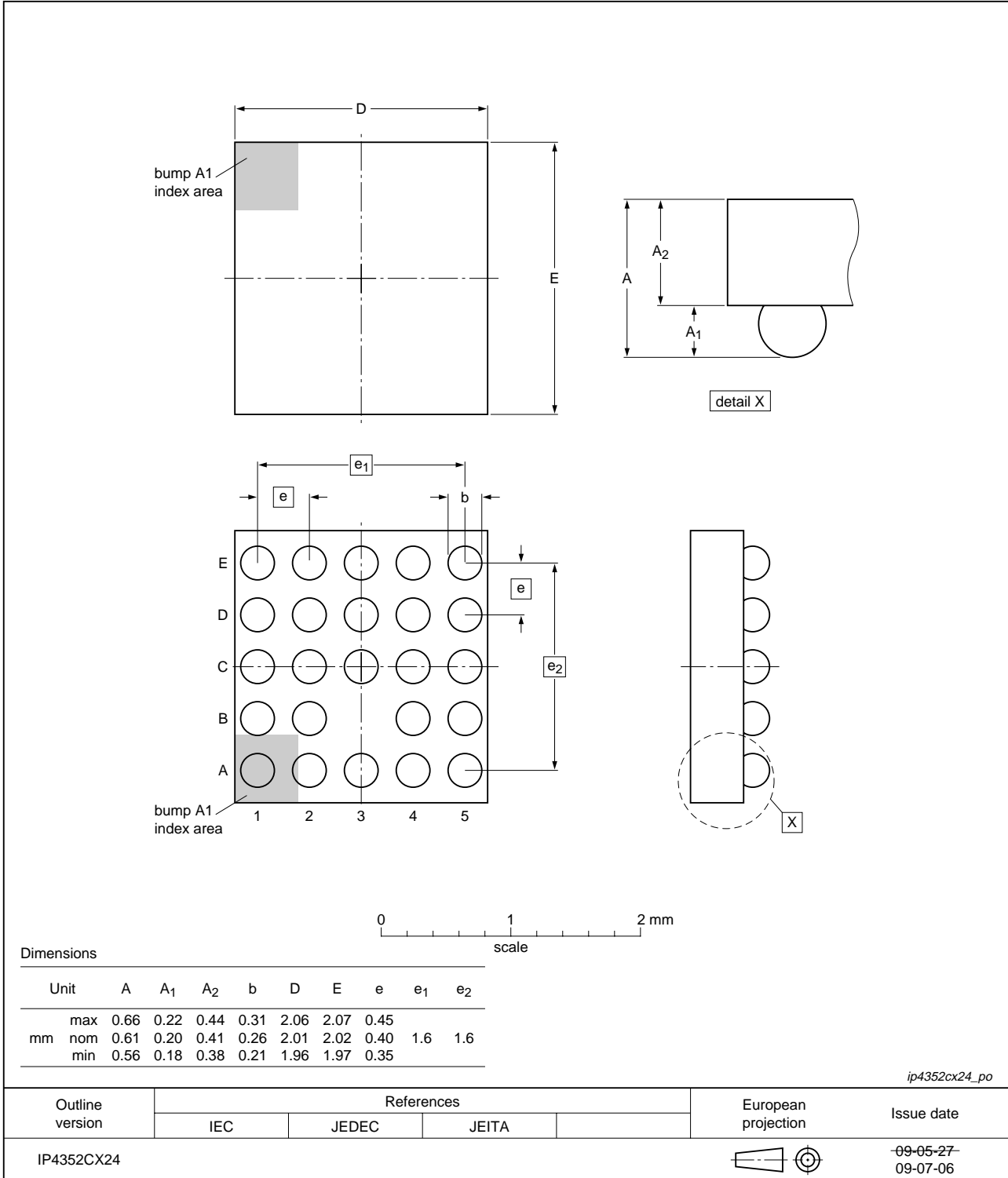


Fig 7. Package outline IP4352CX24 (WLCSP24)



## 9. Soldering of WLCSP packages

### 9.1 Introduction to soldering WLCSP packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering WLCSP (Wafer Level Chip-Size Packages) can be found in application note AN10439 "Wafer Level Chip Scale Package" and in application note AN10365 "Surface mount reflow soldering description".

Wave soldering is not suitable for this package.

All NXP WLCSP packages are lead-free.

### 9.2 Board mounting

Board mounting of a WLCSP requires several steps:

1. Solder paste printing on the PCB
2. Component placement with a pick and place machine
3. The reflow soldering itself

### 9.3 Reflow soldering

Key characteristics in reflow soldering are:

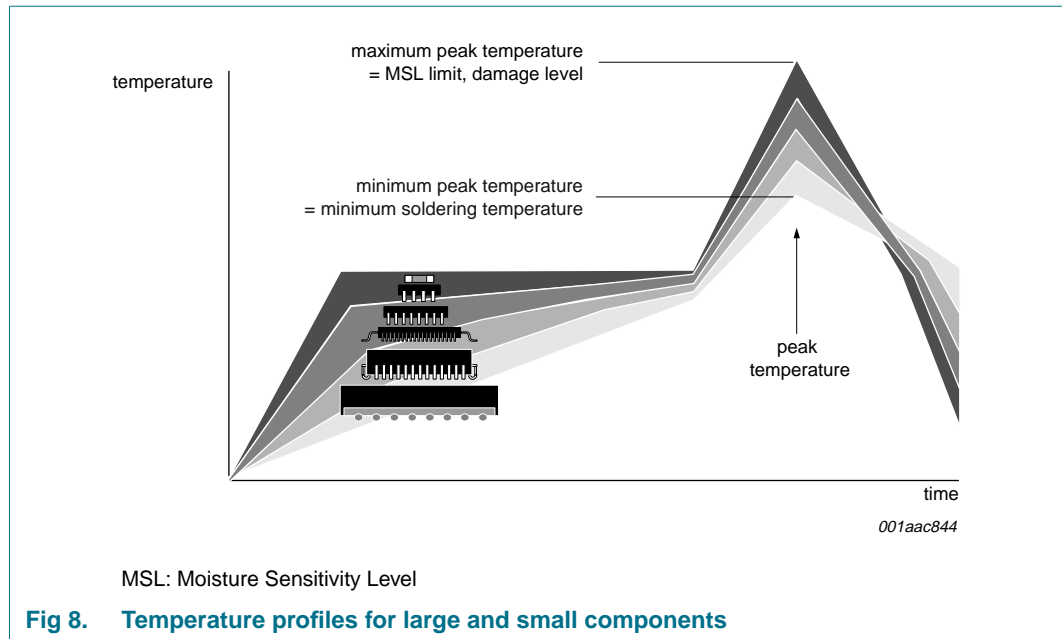
- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see [Figure 8](#)) than a PbSn process, thus reducing the process window
- Solder paste printing issues, such as smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature), and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic) while being low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with [Table 7](#).

**Table 7. Lead-free process (from J-STD-020C)**

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm <sup>3</sup> )		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see [Figure 8](#).



For further information on temperature profiles, refer to application note *AN10365 "Surface mount reflow soldering description"*.

### 9.3.1 Stand off

The stand off between the substrate and the chip is determined by:

- The amount of printed solder on the substrate
- The size of the solder land on the substrate
- The bump height on the chip

The higher the stand off, the better the stresses are released due to TEC (Thermal Expansion Coefficient) differences between substrate and chip.

### 9.3.2 Quality of solder joint

A flip-chip joint is considered to be a good joint when the entire solder land has been wetted by the solder from the bump. The surface of the joint should be smooth and the shape symmetrical. The soldered joints on a chip should be uniform. Voids in the bumps after reflow can occur during the reflow process in bumps with high ratio of bump diameter to bump height, i.e. low bumps with large diameter. No failures have been found to be related to these voids. Solder joint inspection after reflow can be done with X-ray to monitor defects such as bridging, open circuits and voids.

### 9.3.3 Rework

In general, rework is not recommended. By rework we mean the process of removing the chip from the substrate and replacing it with a new chip. If a chip is removed from the substrate, most solder balls of the chip will be damaged. In that case it is recommended not to re-use the chip again.

Device removal can be done when the substrate is heated until it is certain that all solder joints are molten. The chip can then be carefully removed from the substrate without damaging the tracks and solder lands on the substrate. Removing the device must be done using plastic tweezers, because metal tweezers can damage the silicon. The surface of the substrate should be carefully cleaned and all solder and flux residues and/or underfill removed. When a new chip is placed on the substrate, use the flux process instead of solder on the solder lands. Apply flux on the bumps at the chip side as well as on the solder pads on the substrate. Place and align the new chip while viewing with a microscope. To reflow the solder, use the solder profile shown in application note AN10365 "Surface mount reflow soldering description".

### 9.3.4 Cleaning

Cleaning can be done after reflow soldering.

## 10. Abbreviations

**Table 8. Abbreviations**

Acronym	Description
DUT	Device Under Test
EMI	ElectroMagnetic Interference
ESD	ElectroStatic Discharge
FR4	Flame Retard 4
LAN	Local Area Network
NSMD	Non-Solder Mask Design
OSP	Organic Solderability Preservative
PCB	Printed-Circuit Board
PCS	Personal Communication System
PDA	Personal Digital Assistant
PSU	Power Supply Unit
RoHS	Restriction of Hazardous Substances
WAN	Wide Area Network
WLCSP	Wafer-Level Chip-Scale Package

## 11. Revision history

**Table 9. Revision history**

Document ID	Release date	Data sheet status	Change notice	Supersedes
IP4352CX24_1	20090813	Product data sheet	-	-

## 12. Legal information

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Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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