FUJITSU SEMICONDUCTOR
DATA SHEET

DS05–30335–1E

MEMORY

FLASH MEMORY CARD

MB98A808Ax-/809Ax-/810Ax-/811Ax-20

FLASH ERASABLE AND PROGRAMMABLE MEMORY CARD
256K / 512K / 1M / 2M-BYTE

■ DESCRIPTION

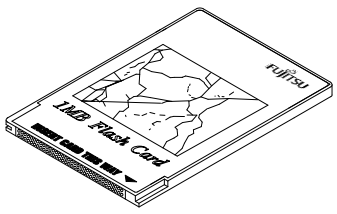
The Fujitsu MB98A808Ax, MB98A809Ax, MB98A810Ax and MB98A811Ax are Flash electrically erasable and programmable (Flash) memory cards capable of storing and retrieving large amounts of data. The memory circuits are housed in a credit-card sized 68-pin package. Internal circuit is protected by two metal panels, one at the top and bottom of the card, that help to reduce chip damage from electrostatic discharge.

A unique feature of the Fujitsu memory cards allows the user to organize the card into either an 8-bit or a 16-bit bus configuration. All cards are portable and operate on low power at high speed.

In accordance with the Personal Computer Memory Card International Association (PCMCIA) and Japan Electrical Industry Development Association (JEIDA) industry standard specification, Flash memory cards offer additional EEPROM memory that is used to store attribute data. The attribute memory is a Flash memory card option. (See page 2 for description of the three available options.)

- Conformed to PCMCIA and JEIDA industry standards.
- Credit card size : 85.6mm (length) × 54.0mm (width) × 3.3mm (thick)
- PCMCIA / JEIDA conformed two-piece 68-pin connector (with a two-row built-in receptacle)
- Single +5.0 V±5% power supply (+12.0 V±5%VPP)
- Command control for Write / Erase operation
- Write protect function

■ PACKAGE



CRD-68P-M17

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

■ ABSOLUTE MAXIMUM RATINGS (see WARNING)

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC}	–0.5 to +6.0	V
Input Voltage	V_{IN}	–0.5 to V_{CC}+0.5	V
Output Voltage	V_{OUT}	–0.5 to V_{CC}+0.5	V
Programming Voltage *1	V_{PP1}, V_{PP2}	–2.0 to +14.0	V
Storage Temperature at turning on the power	T_{BIAS}	–10 to 70	°C
Ambient Temperature	T_A	0 to +60	°C
Storage Temperature	T_{STG}	–30 to +70	°C

Note: *1 Minimum DC input voltage is –0.5 V.

WARNING: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ATTRIBUTE MEMORY OPTIONS

PCMCIA and JEIDA standard memory cards from Fujitsu provide a separate EEPROM memory address space for recording fundamental card information. It is used by the card manufacturers to record basic configuration information such as device type, size, speed, etc.

The attribute memory is selected by asserting the $\overline{REG}$ pin on the card interface. Option descriptions as follows:

OPTION 1: Attribute memory is not supported. $\overline{REG}$ Pin : Not Contacted

Part Number	Main Memory		Attribute Memory		Memory Organization *
	Memory Device	Access Time	Memory Device	Access Time	
MB98A808A1	1M Flash Memory × 2pcs	200 ns	N / A	N / A	256K × 8 bits/ 128K × 16 bits
MB98A809A1	1M Flash Memory × 4pcs	200 ns	N / A	N / A	512K × 8 bits/ 256K × 16 bits
MB98A810A1	1M Flash Memory × 8pcs	200 ns	N / A	N / A	1M × 8 bits/ 512K × 16 bits
MB98A811A1	1M Flash Memory × 16pcs	200 ns	N / A	N / A	2M × 8 bits/ 1M × 16 bits

OPTION 2: Attribute memory in a separate location is not supported.

When $\overline{REG}$ line is asserted, "FF" is output to the data bus to indicate that attribute data may be stored in main memory.

Part Number	Main Memory		Attribute Memory		Memory Organization *
	Memory Device	Access Time	Memory Device	Access Time	
MB98A808A2	1M Flash Memory × 2pcs	200 ns	N / A	N / A	256K × 8 bits/ 128K × 16 bits
MB98A809A2	1M Flash Memory × 4pcs	200 ns	N / A	N / A	512K × 8 bits/ 256K × 16 bits
MB98A810A2	1M Flash Memory × 8pcs	200 ns	N / A	N / A	1M × 8 bits/ 512K × 16 bits
MB98A811A2	1M Flash Memory × 16pcs	200 ns	N / A	N / A	2M × 8 bits/ 1M × 16 bits

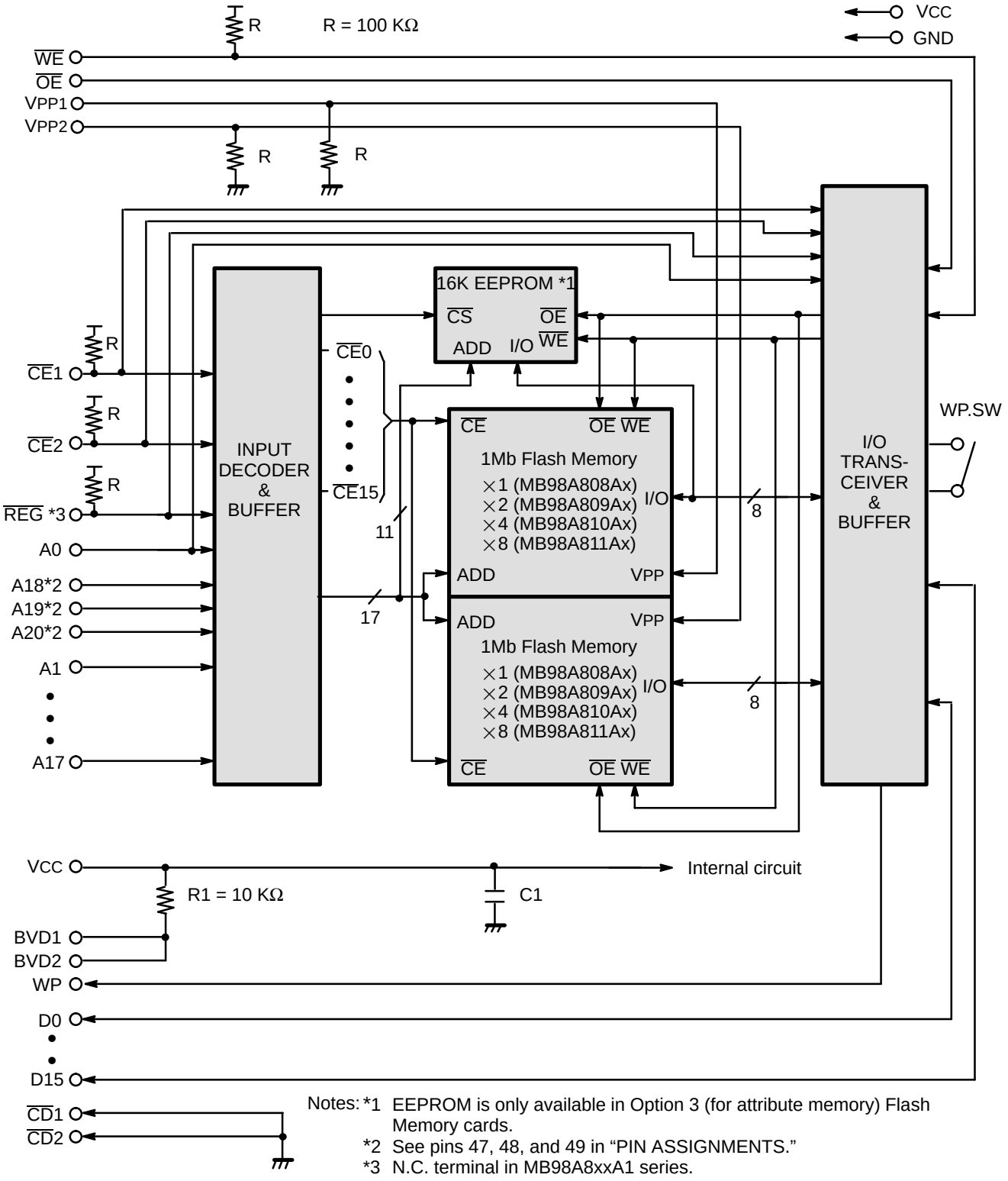
OPTION 3: Attribute memory is supported. The data is stored in 16K-bit EEPROM.

When the $\overline{REG}$ line is asserted, data stored in EEPROM is output to the data bus.

Part Number	Main Memory		Attribute Memory		Memory Organization *
	Memory Device	Access Time	Memory Device	Access Time	
MB98A808A3	1M Flash Memory × 2pcs	200 ns	EEPROM × 1pcs	300 ns	256K × 8 bits/ 128K × 16 bits
MB98A809A3	1M Flash Memory × 4pcs	200 ns	EEPROM × 1pcs	300 ns	512K × 8 bits/ 256K × 16 bits
MB98A810A3	1M Flash Memory × 8pcs	200 ns	EEPROM × 1pcs	300 ns	1M × 8 bits/ 512K × 16 bits
MB98A811A3	1M Flash Memory × 16pcs	200 ns	EEPROM × 1pcs	300 ns	2M × 8 bits/ 1M × 16 bits

Note: * To be configured by user.

Fig. 1 – MB98A808Ax, 809Ax, 810Ax, and 811Ax BLOCK DIAGRAM



Notes: *1 EEPROM is only available in Option 3 (for attribute memory) Flash Memory cards.
*2 See pins 47, 48, and 49 in “PIN ASSIGNMENTS.”
*3 N.C. terminal in MB98A8xxA1 series.

PIN ASSIGNMENTS

MB98A808Ax	MB98A809Ax	MB98A810Ax	MB98A811Ax	Pin No.		MB98A808Ax	MB98A809Ax	MB98A810Ax	MB98A811Ax
GND	GND	GND	GND	1	35	GND	GND	GND	GND
D3	D3	D3	D3	2	36	$\overline{CD}$1	$\overline{CD}$1	$\overline{CD}$1	$\overline{CD}$1
D4	D4	D4	D4	3	37	D11	D11	D11	D11
D5	D5	D5	D5	4	38	D12	D12	D12	D12
D6	D6	D6	D6	5	39	D13	D13	D13	D13
D7	D7	D7	D7	6	40	D14	D14	D14	D14
$\overline{CE}$1	$\overline{CE}$1	$\overline{CE}$1	$\overline{CE}$1	7	41	D15	D15	D15	D15
A10	A10	A10	A10	8	42	$\overline{CE}$2	$\overline{CE}$2	$\overline{CE}$2	$\overline{CE}$2
$\overline{OE}$	$\overline{OE}$	$\overline{OE}$	$\overline{OE}$	9	43	N.C.	N.C.	N.C.	N.C.
A11	A11	A11	A11	10	44	N.C.	N.C.	N.C.	N.C.
A9	A9	A9	A9	11	45	N.C.	N.C.	N.C.	N.C.
A8	A8	A8	A8	12	46	A17	A17	A17	A17
A13	A13	A13	A13	13	47	A18 *1	A18	A18	A18
A14	A14	A14	A14	14	48	N.C.	N.C.	A19	A19
$\overline{WE}$	$\overline{WE}$	$\overline{WE}$	$\overline{WE}$	15	49	N.C.	N.C.	N.C.	A20
N.C.	N.C.	N.C.	N.C.	16	50	N.C.	N.C.	N.C.	N.C.
V_{CC}	V_{CC}	V_{CC}	V_{CC}	17	51	V_{CC}	V_{CC}	V_{CC}	V_{CC}
V_{PP1}	V_{PP1}	V_{PP1}	V_{PP1}	18	52	V_{PP2}	V_{PP2}	V_{PP2}	V_{PP2}
A16	A16	A16	A16	19	53	N.C.	N.C.	N.C.	N.C.
A15	A15	A15	A15	20	54	N.C.	N.C.	N.C.	N.C.
A12	A12	A12	A12	21	55	N.C.	N.C.	N.C.	N.C.
A7	A7	A7	A7	22	56	N.C.	N.C.	N.C.	N.C.
A6	A6	A6	A6	23	57	N.C.	N.C.	N.C.	N.C.
A5	A5	A5	A5	24	58	N.C.	N.C.	N.C.	N.C.
A4	A4	A4	A4	25	59	N.C.	N.C.	N.C.	N.C.
A3	A3	A3	A3	26	60	N.C.	N.C.	N.C.	N.C.
A2	A2	A2	A2	27	61	$\overline{REG}$/N.C. *2	$\overline{REG}$/N.C. *2	$\overline{REG}$/N.C. *2	$\overline{REG}$/N.C. *2
A1	A1	A1	A1	28	62	BVD2	BVD2	BVD2	BVD2
A0	A0	A0	A0	29	63	BVD1	BVD1	BVD1	BVD1
D0	D0	D0	D0	30	64	D8	D8	D8	D8
D1	D1	D1	D1	31	65	D9	D9	D9	D9
D2	D2	D2	D2	32	66	D10	D10	D10	D10
WP	WP	WP	WP	33	67	$\overline{CD}$2	$\overline{CD}$2	$\overline{CD}$2	$\overline{CD}$2
GND	GND	GND	GND	34	68	GND	GND	GND	GND

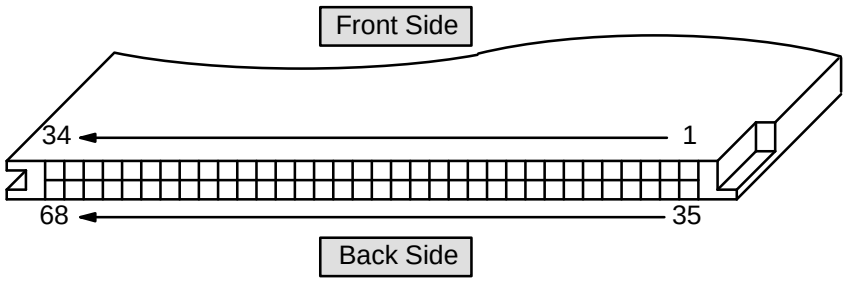
*1: A18 doesn't relate with "H" and "L" level.
*2: N.C. terminal in MB98A8xxA1 series.

PIN DESCRIPTIONS

Symbol	Pin Name	Input/Output	Function
A0 to A20	Address Input	Input	Address Inputs, A0 to A20.
D0 to D15	Data Input/Output	Input/Output	Data Inputs/Outputs. This data bus size (8-bit or 16-bit) is selected with $\overline{CE}1$ and $\overline{CE}2$.
$\overline{CE}1$	Card Enable for Lower Byte	Input	Active Low. –Lower byte (D0 to D7) is selected for read / write / erase function of flash memory cards.
$\overline{CE}2$	Card Enable for Upper Byte	Input	Active Low. –Upper byte (D8 to D15) is selected for read / write / erase function of flash memory cards.
$\overline{REG}$	Attribute Memory Select	Input	Active Low. –Attribute memory is selected for read / write function of identification data of flash memory cards. (N.C. or “FF” data or attribute data.)
$\overline{OE}$	Output Enable	Input	Active Low. –Output enable for flash memory cards.
$\overline{WE}$	Write Enable	Input	Active Low. –Write enable for flash memory cards.
$V_{PP}1$	Programming Voltage 1	Input	Programming voltage for lower byte.
$V_{PP}2$	Programming Voltage 2	Input	Programming voltage for upper byte.
$\overline{CD}1$, $\overline{CD}2$	Card Detect	Output	These pins detect if the card has been correctly inserted. Both pins are tied to GND internally.
WP	Write Protect	Output	Write controller for flash memory cards. This pin outputs the Protect / Non Protect status of “WP Switch”.
BVD1, BVD2	Battery Voltage Detect	Output	Both pins are tied to V_{CC} internally.
V_{CC}	Power Supply	–	Power Supply Voltage. (+5.0 V ±5%)
GND	Ground	–	System Ground.
N.C.	Non Connection	–	

PIN LOCATIONS

Fig. 2 – BOTTOM VIEW (CONNECTOR SIDE)



FUNCTION TRUTH TABLE

MAIN MEMORY FUNCTION *1

Read Function ($\overline{REG}$=VIH)

$\overline{CE}$2	$\overline{CE}$1	A0	$\overline{OE}$	$\overline{WE}$	WP*2	VPP2	VPP1	Mode	Data Input / Output		WP SW
									D8 to D15	D0 to D7	
H	H	X	X	X	X	VPPL	VPPL	Standby	High-Z		P or NP
H	L	L	L	H	X	VPPL	VPPL	Read (×8)	High-Z	DOUT (Lower Byte)	P or NP
H	L	H	L	H	X	VPPL	VPPL	Read (×8)	High-Z	DOUT (Upper Byte)	P or NP
L	H	X	L	H	X	VPPL	VPPL	Read (×8)	DOUT (Upper Byte)	High-Z	P or NP
L	L	X	L	H	X	VPPL	VPPL	Read (×16)	DOUT		P or NP
X	X	X	H	H	X	VPPL	VPPL	Output Disable	High-Z		P or NP

Erase / Write / Verify Function ($\overline{REG}$=VIH)

$\overline{CE}$2	$\overline{CE}$1	A0	$\overline{OE}$	$\overline{WE}$	WP*2	VPP2	VPP1	Mode	Data Input / Output		WP SW
									D8 to D15	D0 to D7	
H	H	X	X	X	X	VPPH	VPPH	Standby	High-Z		P or NP
H	L	L	L	H	L	VPPL*3	VPPH	Read (×8)	High-Z	DOUT	NP
H	L	H	L	H	L	VPPH	VPPL*3	Read (×8)	High-Z	DOUT	NP
H	L	L	H	L	L	VPPL*3	VPPH	Write (×8)	High-Z	DIN	NP
H	L	H	H	L	L	VPPH	VPPL*3	Write (×8)	High-Z	DIN	NP
L	H	X	L	H	L	VPPH	VPPL*3	Read (×8)	DOUT	High-Z	NP
L	H	X	H	L	L	VPPH	VPPL*3	Write (×8)	DIN	High-Z	NP
L	L	X	L	H	L	VPPH	VPPH	Read (×16)	DOUT		NP
L	L	X	H	L	L	VPPH	VPPH	Write (×16)	DIN		NP
X	X	X	H	H	L	VPPH	VPPH	Output Disable	High-Z		NP

Notes: *1 H = VIH, L = VIL, X = Either VIL or VIH, WP SW = Write Protect Switch, P = Protect , NP = Non Protect
*2 L-level is output when WPSW=NP. H-level is output when WPSW=P.
*3 VPPL is recommended though it is functionable at VPPH.

FUNCTION TRUTH TABLE (Continued)

ATTRIBUTE MEMORY FUNCTION *1 ($\overline{REG}$ = VIL) *2

$\overline{CE2}$	$\overline{CE1}$	A0	$\overline{OE}$	$\overline{WE}$	WP	Mode	Data Input/Output		WP SW.
							D15 to D8	D7 to D0	
H	H	X	X	X	L	Standby	High-Z		NP
H	L	L	L	H	L	Read (×8)	High-Z	DOUT *3 (Lower Byte)	NP
H	L	H	L	H	L	Read (×8)	High-Z	H	NP
H	L	L	H	L	L	Write (×8)	High-Z	DIN (Lower Byte)	NP
H	L	H	H	L	L	Write (×8)	High-Z	X	NP
L	H	X	L	H	L	Read (×8)	H	High-Z	NP
L	H	X	H	L	L	Write (×8)	High-Z	High-Z	NP
L	L	X	L	H	L	Read (×16)	H	DOUT *3 (Lower Byte)	NP
L	L	X	H	L	L	Write (×16)	X	DIN (Lower Byte)	NP
X	X	X	H	H	L	Output Disable	High-Z		NP
H	H	X	X	X	H	Standby	High-Z		P
H	L	L	L	H	H	Read (×8)	High-Z	DOUT *3 (Lower Byte)	P
H	L	H	L	H	H	Read (×8)	High-Z	H	P
H	L	L	H	L	H	Output Disable	High-Z		P
H	L	H	H	L	H	Output Disable	High-Z		P
L	H	X	L	H	H	Read (×8)	H	High-Z	P
L	H	X	H	L	H	Output Disable	High-Z		P
L	L	X	L	H	H	Read (×16)	H	DOUT *3 (Lower Byte)	P
L	L	X	H	L	H	Output Disable	High-Z		P
X	X	X	H	H	H	Output Disable	High-Z		P

Notes: *1 H = VIH, L = VIL, X = Either VIL or VIH, WP SW = Write Protect Switch, P = Protect , NP = Non Protect
*2 N.C. for MB98A808A1, 809A1, 810A1, and 811A1.
*3 H-level is output for MB98A808A2, 809A2, 810A2, and 811A2.

WRITE / ERASE CHIP DECODING INFORMATION

Bus Organization	$\overline{CE}2$	$\overline{CE}1$	A23	A22	A21	A0	Decode Chips
8-bit Bus	H	L	L	L	L	L	Chip 0
						H	Chip 1
					H	L	Chip 2
						H	Chip 3
				H	L	L	Chip 4
						H	Chip 5
					H	L	Chip 6
						H	Chip 7
			H	L	L	L	Chip 8
						H	Chip 9
					H	L	Chip 10
						H	Chip 11
				H	L	L	Chip 12
						H	Chip 13
					H	L	Chip 14
						H	Chip 15
	L	H	L	L	L	X	Chip 1
					H		Chip 3
				H	L		Chip 5
					H		Chip 7
			H	L	L		Chip 9
					H		Chip 11
				H	L		Chip 13
					H		Chip 15
16-bit Bus	L	L	L	L	L	X	Chip 0, Chip 1
					H		Chip 2, Chip 3
				H	L		Chip 4, Chip 5
					H		Chip 6, Chip 7
			H	L	L		Chip 8, Chip 9
					H		Chip 10, Chip 11
				H	L		Chip 12, Chip 13
					H		Chip 14, Chip 15

Note: H=V_{IH}, L=V_{IL}, X=Either V_{IH} or V_{IL}

COMMAND DEFINITION TABLE

Command Table for 8-bit Mode

Command	Bus Cycle Required	First Bus Cycle			Second Bus Cycle		
		Operation *1	Address *2	Data *3	Operation *1	Address *2	Data *3
Read Memory	1	Write	RA	00H	—	—	—
Read Intelligent ID Codes *4	3	Write	IA	90H	Read	IA	ID
Set Up Erase / Erase *5	2	Write	ZA	20H	Write	ZA	20H
Erase Verify *5	2	Write	EA	A0H	Read	EA	EVD
Set Up Write / Write *6	2	Write	WA	40H	Write	WA	WD
Write Verify *6	2	Write	WA	CH	Read	WA	WVD
Reset *7 *8	2	Write	ZA	FFH	Write	ZA	FFH

Command Table for 16-bit Mode

Command	Bus Cycle Required	First Bus Cycle			Second Bus Cycle		
		Operation *1	Address *2	Data *3	Operation *1	Address *2	Data *3
Read Memory	1	Write	RA	0000H	—	—	—
Read Intelligent ID Codes *4	3	Write	IA	9090H	Read	IA	ID
Set Up Erase / Erase *5	2	Write	ZA	2020H	Write	ZA	2020H
Erase Verify *5	2	Write	EA	A0A0H	Read	EA	EVD
Set Up Write / Write *6	2	Write	WA	4040H	Write	WA	WD
Write Verify *6	2	Write	WA	C0C0H	Read	WA	WVD
Reset *7 *8	2	Write	ZA	FFFFH	Write	ZA	FFFFH

Notes: *1 Bus operations are defined in “FUNCTION TRUTH TABLE”.
*2 IA = Identifier address: 00H for manufacturer code, 01H for device code.
EA = Address of memory location to be read during erase verify.
RA = Read Address
WA = Address of memory location to be written.
ZA = Address of 128K-Byte zones involved in erase operation.
Addresses are latched on the falling edge of the Write Enable pulse.
*3 ID = Data read from location IA during device identification.
Manufacturer = 31H for 8-bit, 3131H for 16-bit / Device = B4H for 8-bit, B4B4H for 16-bit
EVD = Data read from location EA during erase verify.
WD = Data to be programmed at location WA. Data is latched on the rising edge of Write Enable.
WVD = Data read from location WA during write verify. WA is latched on the Write command.
*4 Following the Read Intelligent ID command, two read operations access manufacturer and device codes.
*5 “ERASE FLOWCHART” in Fig.6, Fig.7 and Fig.8 illustrate the Erase Algorithm.
*6 “WRITE FLOWCHART” in Fig.4 and Fig.5 illustrate the Write Algorithm.
*7 The second bus cycle must be followed by the desired command register write.
*8 The Reset command operates on a zone basis. To reset the entire card requires reset write cycles to each zone.

ADDRESS CONFIGURATIONS *1 (MAIN MEMORY)

8-BIT BUS ORGANIZATION ($\overline{CE}1$ = VIL, $\overline{CE}2$ = VIH)

A20 to A0						$\overline{CE}2$	$\overline{CE}1$	D15 to D8	D7 to D0
0	0000	0000	0000	0000	0000	H	L	– – – – –	0 Add.
0	0000	0000	0000	0000	0001	H	L	– – – – –	1 Add.
0	0000	0000	0000	0000	0010	H	L	– – – – –	2 Add.
0	0000	0000	0000	0000	0011	H	L	– – – – –	3 Add.
↓	↓	↓	↓	↓	↓	↓	↓	↓ ↓	↓ ↓
1	1111	1111	1111	1111	1100	H	L	– – – – –	2,097,148 Add.
1	1111	1111	1111	1111	1101	H	L	– – – – –	2,097,149 Add.
1	1111	1111	1111	1111	1110	H	L	– – – – –	2,097,150 Add.
1	1111	1111	1111	1111	1111	H	L	– – – – –	2,097,151 Add.

8-BIT BUS ORGANIZATION ($\overline{CE}1$ = VIH, $\overline{CE}2$ = VIL) *2

A20 to A0						$\overline{CE}2$	$\overline{CE}1$	D15 to D8	D7 to D0
0	0000	0000	0000	0000	000X	L	H	1 Add.	– – – – –
0	0000	0000	0000	0000	001X	L	H	3 Add.	– – – – –
0	0000	0000	0000	0000	010X	L	H	5 Add.	– – – – –
0	0000	0000	0000	0000	011X	L	H	7 Add.	– – – – –
↓	↓	↓	↓	↓	↓	↓	↓	↓ ↓	↓ ↓
1	1111	1111	1111	1111	100X	L	H	2,097,145 Add.	– – – – –
1	1111	1111	1111	1111	101X	L	H	2,097,147 Add.	– – – – –
1	1111	1111	1111	1111	110X	L	H	2,097,149 Add.	– – – – –
1	1111	1111	1111	1111	111X	L	H	2,097,151 Add.	– – – – –

16-BIT BUS ORGANIZATION ($\overline{CE}1$ = VIL, $\overline{CE}2$ = VIL)

A20 to A0						$\overline{CE}2$	$\overline{CE}1$	D15 to D8	D7 to D0
0	0000	0000	0000	0000	000X	L	L	1 Add.	0 Add.
0	0000	0000	0000	0000	001X	L	L	3 Add.	2 Add.
0	0000	0000	0000	0000	010X	L	L	5 Add.	4 Add.
0	0000	0000	0000	0000	011X	L	L	7 Add.	6 Add.
↓	↓	↓	↓	↓	↓	↓	↓	↓ ↓	↓ ↓
1	1111	1111	1111	1111	100X	L	L	2,097,145 Add.	2,097,144 Add.
1	1111	1111	1111	1111	101X	L	L	2,097,147 Add.	2,097,146 Add.
1	1111	1111	1111	1111	110X	L	L	2,097,149 Add.	2,097,148 Add.
1	1111	1111	1111	1111	111X	L	L	2,097,151 Add.	2,097,150 Add.

Notes: *1 H = VIH, L = VIL, X = Either 0 or 1.
*2 Even addresses are not available in this mode.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ.	Max	Unit
V_{CC} Supply Voltage	V_{CC}	4.75	5.0	5.25	V
Ground	GND	—	0	—	V
Ambient Temperature	T_A	0	—	+55	°C

DC CHARACTERISTICS

Parameter	Test Condition	Symbol	Value			Unit
			Min	Typ	Max	
Input Leakage Current *1	V_{CC}=V_{CC} max V_{IN}=0 V or V_{CC}	I_{LI}	—	±1.0	±20	µA
Output Leakage Current *2	V_{CC}=V_{CC} max V_{IN}=0 V or V_{CC}	I_{LO}	—	±1.0	±20	µA
V_{CC} Standby Current	V_{CC}=V_{CC} max $\overline{CE}1$=$\overline{CE}2$=V_{CC}–0.2 V	I_{SB1}	—	0.9	1.7	mA
	V_{CC}=V_{CC} max $\overline{CE}1$=$\overline{CE}2$=V_{IH}	I_{SB2}	—	7.0	14.0	mA
V_{CC} Active Read Current	V_{CC}=V_{CC} max $\overline{CE}1$=$\overline{CE}2$=V_{IL} cyc. =200 ns, I_{OUT}=0 mA	I_{CC1}	—	85	125	mA
V_{CC} Write Current	Write in progress	I_{CC2}	—	2.0	20	mA
V_{CC} Erase Current	Erase in progress	I_{CC3}	—	10	30	mA
V_{PP} Leakage Current *3	V_{PP}≤V_{CC}	I_{PPS}	—	—	250	µA
V_{PP} Read Current or *3 Standby Current	V_{PP}>V_{CC}	I_{PP1}	—	0.9	1.8	mA
	V_{PP}≤V_{CC}		—	—	250	mA
V_{PP} Write Current *3	V_{PP}=V_{PPH} Write in progress	I_{PP2}	—	9	30	mA
V_{PP} Erase Current *3	V_{PP}=V_{PPH} Erase in progress	I_{PP3}	—	7	30	mA
Input Low Voltage	—	V_{IL}	–0.3	—	0.8	V
Input High Voltage	—	V_{IH}	2.4	—	V_{CC}+0.3	V
Output Low Voltage	I_{OL}=3.2 mA, V_{CC}=V_{CC} min	V_{OL}	—	—	0.4	V
Output High Voltage *4	I_{OH}=–2.0 mA, V_{CC}=V_{CC} min	V_{OH}	3.8	—	—	V
V_{PP} during Read-Only Operation	Note: *5	V_{PPL}	0	—	6.5	V
V_{PP} during Write/Erase Operation	—	V_{PPH}	11.4	—	12.6	V

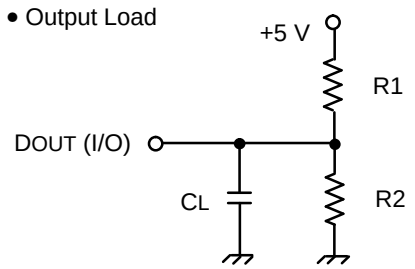
Notes: *1 This value does not apply to $\overline{CE}1$, $\overline{CE}2$, $\overline{WE}$ and $\overline{REG}$.
*2 This value does not apply to BVD1, BVD2, $\overline{CD}1$ and $\overline{CD}2$.
*3 This value apply to V_{PP1} and V_{PP2}.
*4 This value does not apply to BVD1 and BVD2.
*5 Write / Erase are inhibited when V_{PP}=V_{PPL}.

CAPACITANCE (T_A=25°C, f=1MHz, V_{IN}=$V_{I/O}$=GND)

Parameter	Symbol	Min	Max	Unit
Input Capacitance *1	C_{IN}	—	50	pF
I/O Capacitance *2	$C_{I/O}$	—	50	pF

Notes: *1 This value does not apply to $\overline{CE}1$, $\overline{CE}2$, $\overline{WE}$ and $\overline{REG}$.
*2 This value does not apply to $\overline{CE}1$, $\overline{CE}2$, BVD1 and BVD2.

Fig. 3 – AC TEST CONDITIONS



- Input Pulse Levels: 0.6 V to 2.6 V
- Input Pulse Rise and Fall Times: 5 ns (Transient between 0.8 V and 2.4 V)
- Timing Reference Levels

  Input: V_{IL} = 0.8 V, V_{IH} = 2.4 V
  Output: V_{OL} = 0.8 V, V_{OH} = 2.0 V

* Including jig and stray capacitance

	R1	R2	C_L	Parameter Measured
Load I	1.8 kΩ	990 Ω	100 pF	All parameters except t_{CLZ}, t_{OLZ}, t_{EHQZ}, t_{DF}, t_{RCLZ}, t_{ROLZ}, t_{RCHZ} and t_{ROHZ}
Load II	1.8 kΩ	990 Ω	5 pF	t_{CLZ}, t_{OLZ}, t_{EHQZ}, t_{DF}, t_{RCLZ}, t_{ROLZ}, t_{RCHZ} and t_{ROHZ}

AC CHARACTERISTICS

(At recommended operating conditions unless otherwise noted.)

MAIN MEMORY READ CYCLE *1

Parameter	Symbol	Min	Max	Unit
Read Cycle Time	tRC	200	—	ns
Card Enable Access Time	tCE	—	200	ns
Address Access Time	tACC	—	200	ns
Output Enable Access Time	tOE	—	100	ns
Card Enable to Output in Low-Z *2	tCLZ	5	—	ns
Card Disable to Output in High-Z *2	tEHQZ	—	60	ns
Output Enable to Output in Low-Z *2	tOLZ	5	—	ns
Output Disable to Output in High-Z *2	tDF	—	60	ns
Output Hold from Address, $\overline{CE}$, or $\overline{OE}$ Change *3	tOH	5	—	ns

ATTRIBUTE MEMORY READ CYCLE *1*4

Parameter	Symbol	Min	Max	Unit
Read Cycle Time	tRRC	300	—	ns
Address Access Time	tRAA	—	300	ns
Card Enable Access Time	tRCE	—	300	ns
Output Enable Access Time	tROE	—	150	ns
Output Hold from Address Change	tROH	5	—	ns
Card Enable to Output Low-Z *2	tRCLZ	5	—	ns
Output Enable to Output Low-Z *2	tROLZ	5	—	ns
Card Enable to Output High-Z *2	tRCHZ	—	60	ns
Output Enable to Output High-Z *2	tROHZ	—	60	ns

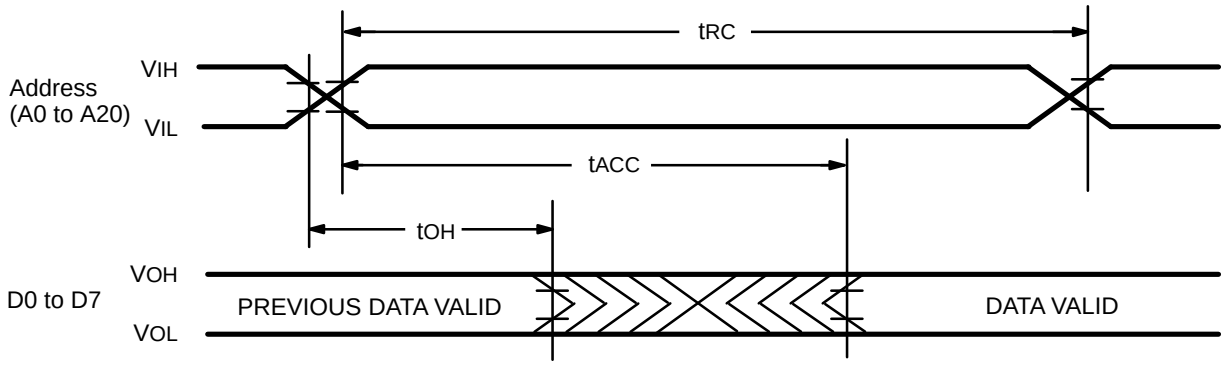
Notes: *1 Rise / Fall time < 5 ns.
*2 Transition is measured at the point of ±500 mV from steady state voltage. This parameter is specified using Load II in Fig.3.
*3 This parameter is specified from the rising edge of $\overline{OE}$, $\overline{CE}$1 and $\overline{CE}$2, whichever occurs first.
*4 This parameter is for MB98A808A3, 809A3, 810A3, and 811A3.

AC CHARACTERISTICS (Continued)

(At recommended operating conditions unless otherwise noted.)

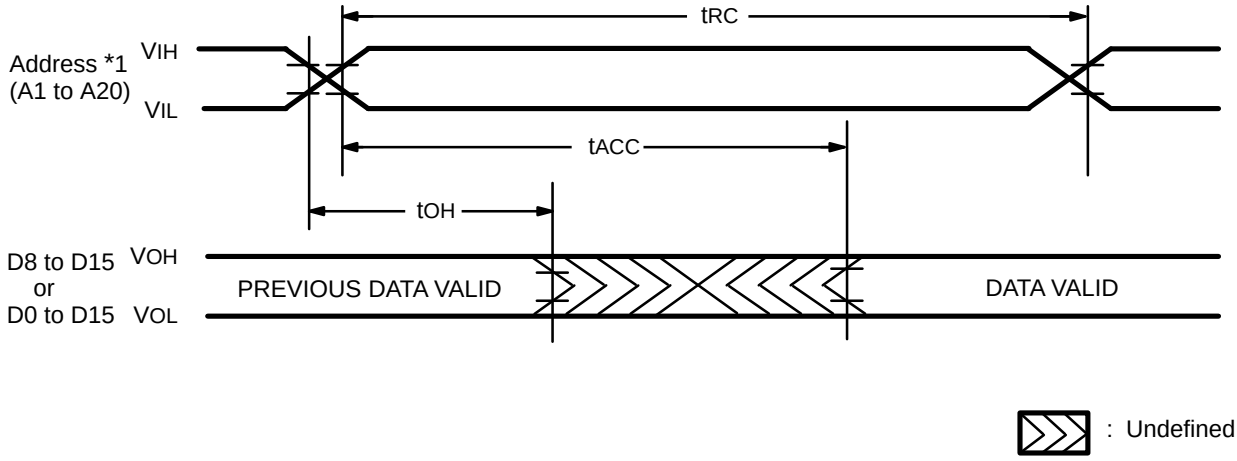
MAIN MEMORY READ CYCLE TIMING DIAGRAM ($\overline{WE}$ = V_{IH}, $\overline{REG}$ = V_{IH})

READ CYCLE 1: $\overline{CE}1$ = $\overline{OE}$ = V_{IL}, $\overline{CE}2$ = V_{IH}: ×8-bit Bus Organization



READ CYCLE 2: $\overline{CE}1$ = V_{IH}, $\overline{CE}2$ = $\overline{OE}$ = V_{IL}: ×8-bit Bus Organization

$\overline{CE}1$ = $\overline{CE}2$ = $\overline{OE}$ = V_{IL}: ×16-bit Bus Organization



: Undefined

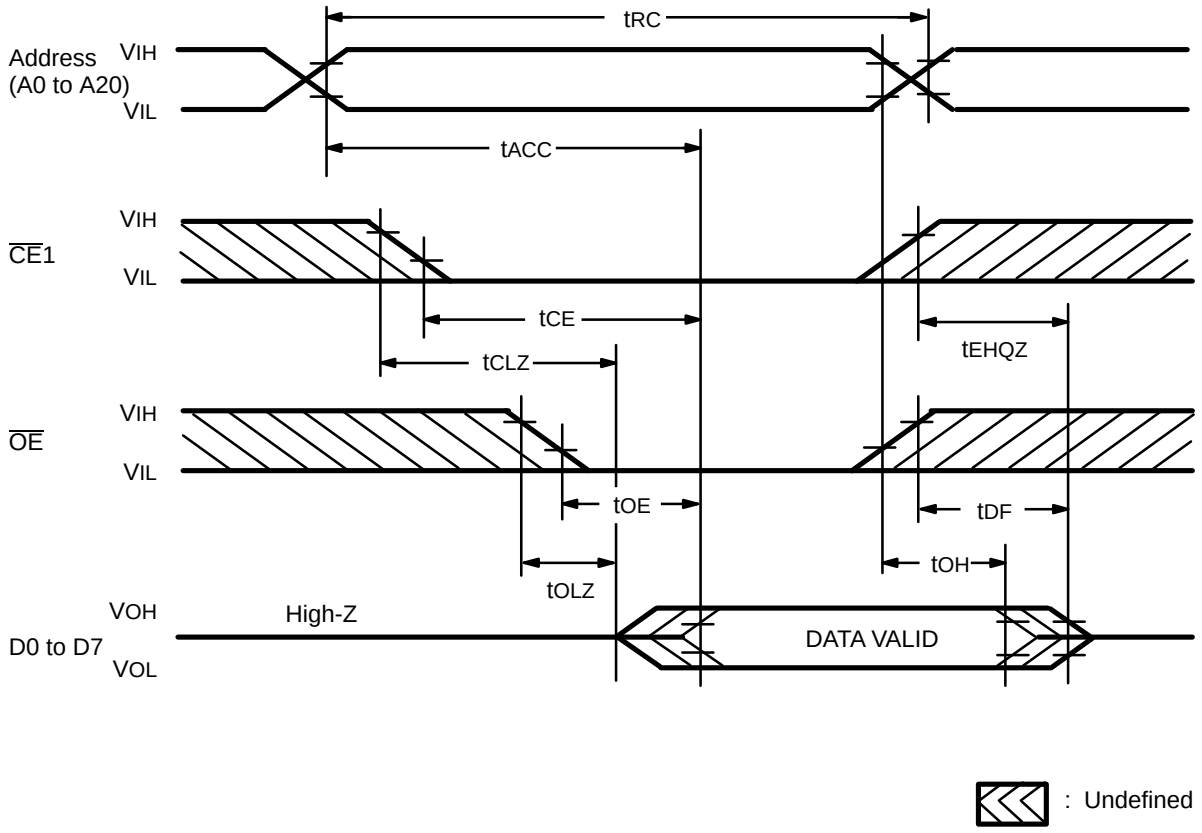
Note: *1 A0 = Either V_{IH} or V_{IL}.

AC CHARACTERISTICS (Continued)

(At recommended operating conditions unless otherwise noted.)

MAIN MEMORY READ CYCLE TIMING DIAGRAM ($\overline{WE}$ = V_{IH}, $\overline{REG}$ = V_{IH})

READ CYCLE 3: $\overline{CE}2$ = V_{IH}: ×8-bit Bus Organization

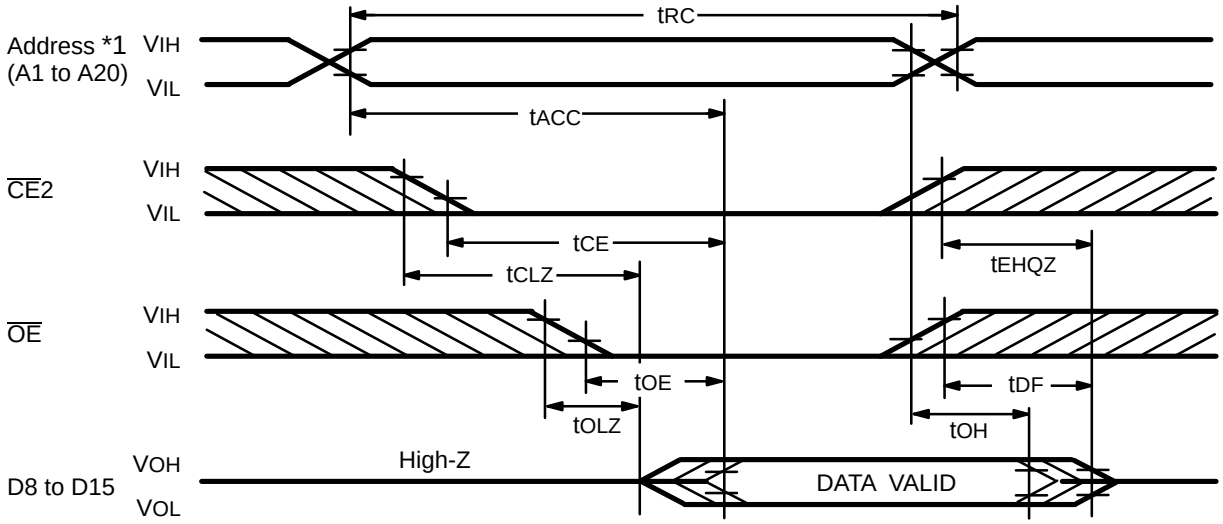


AC CHARACTERISTICS (Continued)

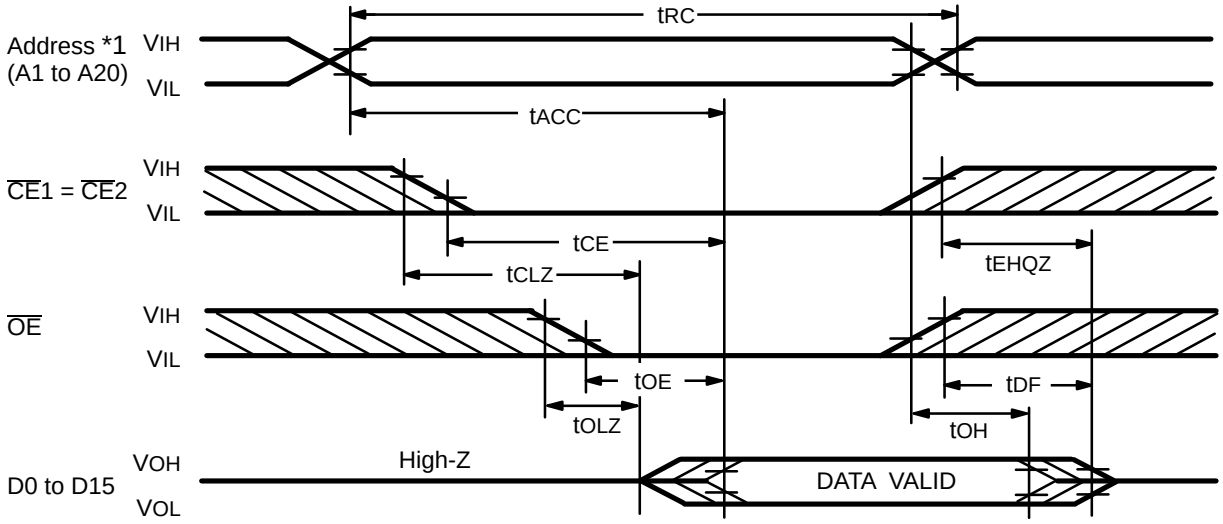
(At recommended operating conditions unless otherwise noted.)

MAIN MEMORY READ CYCLE TIMING DIAGRAM ($\overline{WE}$ = VIH, $\overline{REG}$ = VIH)

READ CYCLE 4: $\overline{CE}1$ = VIH: ×8-bit Bus Organization



READ CYCLE 5: $\overline{CE}1$ = $\overline{CE}2$ = VIL: ×16-bit Bus Organization



: Undefined

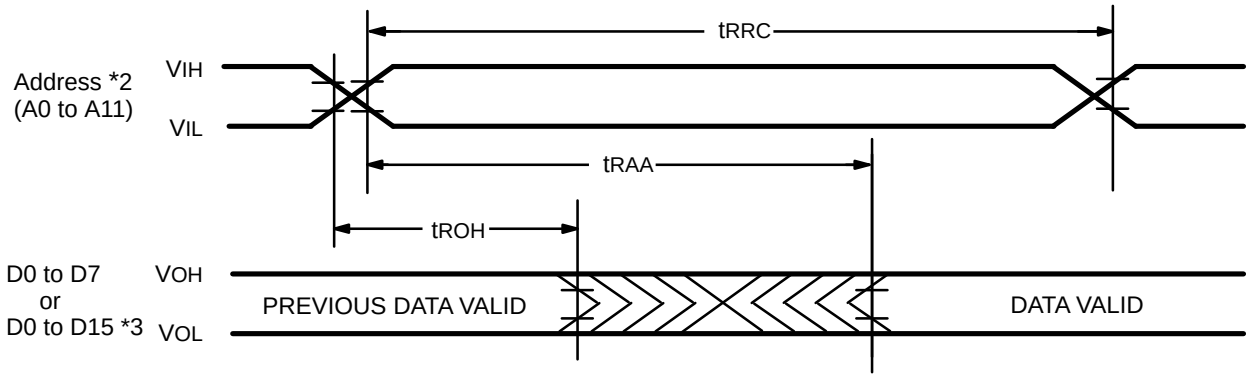
Note: *1 A0 = Either VIL or VIH.

AC CHARACTERISTICS (Continued)

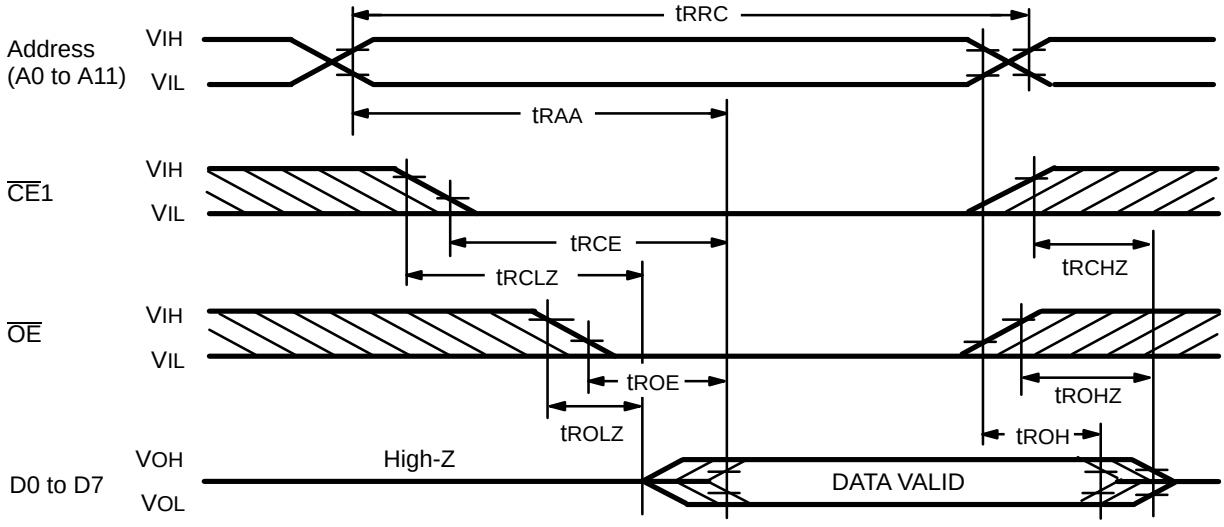
(At recommended operating conditions unless otherwise noted.)

ATTRIBUTE MEMORY READ CYCLE TIMING DIAGRAM ($\overline{WE}$ = VIH, $\overline{REG}$ = VIL) *1

READ CYCLE 1: $\overline{CE}1$ = $\overline{OE}$ = VIL, $\overline{CE}2$ = VIH: ×8-bit Bus Organization
$\overline{CE}1$ = $\overline{CE}2$ = $\overline{OE}$ = VIL: ×16-bit Bus Organization



READ CYCLE 2: $\overline{CE}2$ = VIH: ×8-bit Bus Organization



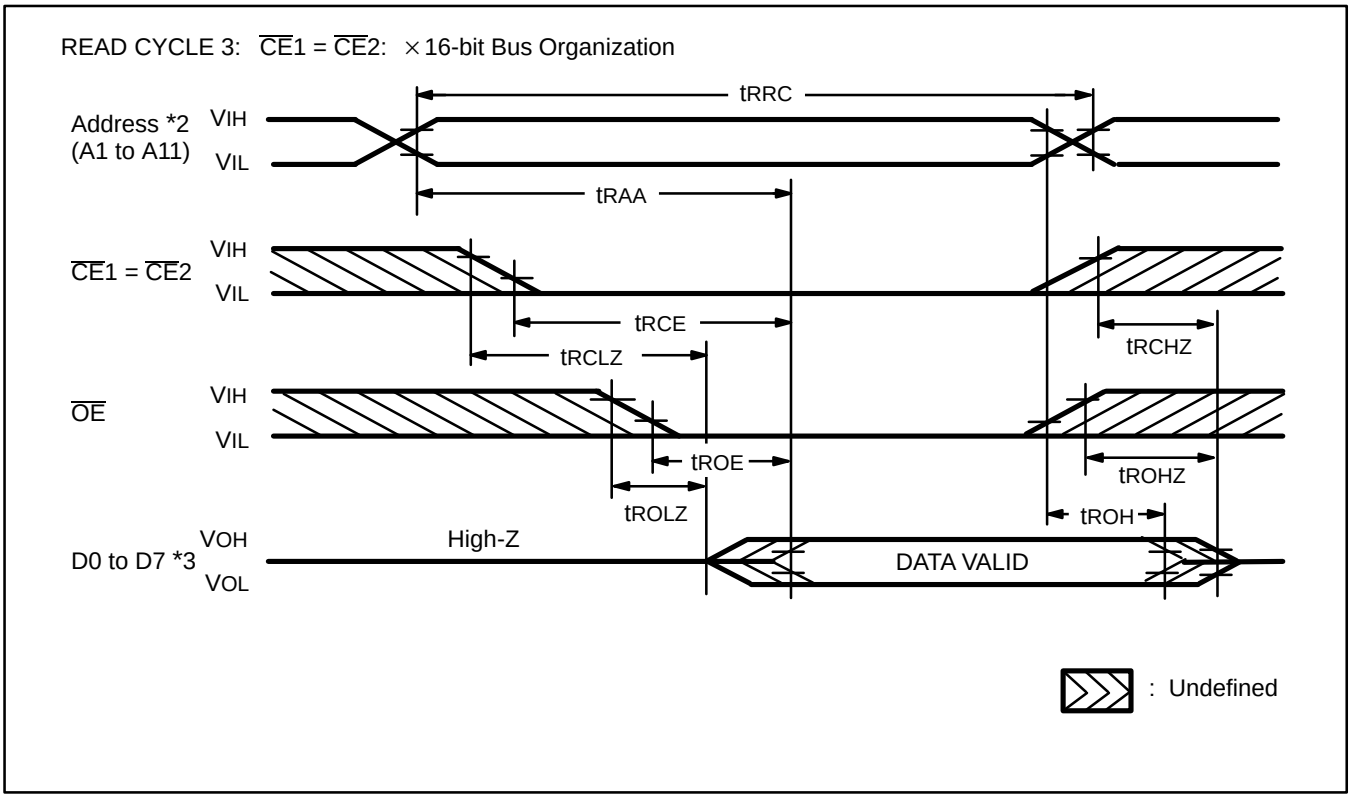
: Undefined

Notes: *1 This timing diagram is for MB98A808A3, 809A3, 810A3, and 811A3. “FF” data is available on MB98A808A2, 809A2, 810A2, and 811A2 only.
*2 A0 = Either VIH or VIL during 16 bits bus organization.
*3 H-level is output from D8 to D15.

AC CHARACTERISTICS (Continued)

(At recommended operating conditions unless otherwise noted.)

ATTRIBUTE MEMORY READ CYCLE TIMING DIAGRAM ($\overline{WE}$ = VIH, $\overline{REG}$ = VIL) *1



Notes: *1 This timing diagram is for MB98A808A3, 809A3, 810A3, and 811A3. “FF” data is available on MB98A808A2, 809A2, 810A2, and 811A2 only.
*2 A0 = Either VIH or VIL.
*3 H-level is output from D8 to D15.

AC CHARACTERISTICS (Continued)

(At recommended operating conditions unless otherwise noted.)

MAIN MEMORY WRITE / ERASE CYCLE *1 *2

Parameter	Symbol	Min	Max	Unit
Write Cycle Time	tWC	200	—	ns
Address Set Up Time	tAS	0	—	ns
Address Hold Time	tAH	100	—	ns
Data Set Up Time	tDS	80	—	ns
Data Hold Time	tDH	30	—	ns
Write Recovery Time before Read	tWHGL	6	—	µs
Read Recovery Time before Write	tGHWL	0	—	µs
Card Enable Set Up Time before Write	tCS	40	—	ns
Card Enable Hold Time	tCH	0	—	ns
Write Enable Pulse Width	tWP	100	—	ns
Write Enable Pulse Width High	tWPH	60	—	ns
Write Enable Set Up Time	tWS	0	—	ns
Write Enable Hold Time	tWH	0	—	ns
Card Enable Pulse Width	tCP	140	—	ns
Card Enable Pulse Width High	tCPH	60	—	ns
Duration of Write Operation *3	tWHWH1	10	—	µs
Duration of Erase Operation *3	tWHWH2	9.5	—	ms
V_{PP} Set Up Time to Chip Enable Low	tGHWL	1.0	—	µs

Notes: *1 Read timing parameters during Write / Erase operations are the same as during read only operations. Refer to AC characteristics for Main Memory Read Cycle.
*2 Rise/Fall time ≤ 5 ns.
*3 The integrated stop timer terminates the Write / Erase operations, thereby eliminating the need for a maximum specification.

AC CHARACTERISTICS (Continued)

(At recommended operating conditions unless otherwise noted.)

MAIN MEMORY WRITE / ERASE PERFORMANCE *1

Rating	Min	Typ	Max	Unit
Chip Erase Time *1	—	1.0 *2	10	Sec.
Chip Write Time	—	2.0 *2	12.5 *3	Sec.
Write / Erase Cycle	100,000	—	—	Cycle

Notes: *1 Excludes 00H writing prior to Erasure.
*2 T_A = 25°C, V_{PP} = 12 V, 100,000 Cycles.
*3 Minimum byte writing time excluding system overhead is 16 µs (10 µs program + 6 µs write recovery), while maximum is 400 µs/byte. (16 µs × 25 loops allowed by algorithm).

ATTRIBUTE MEMORY WRITE CYCLE *1

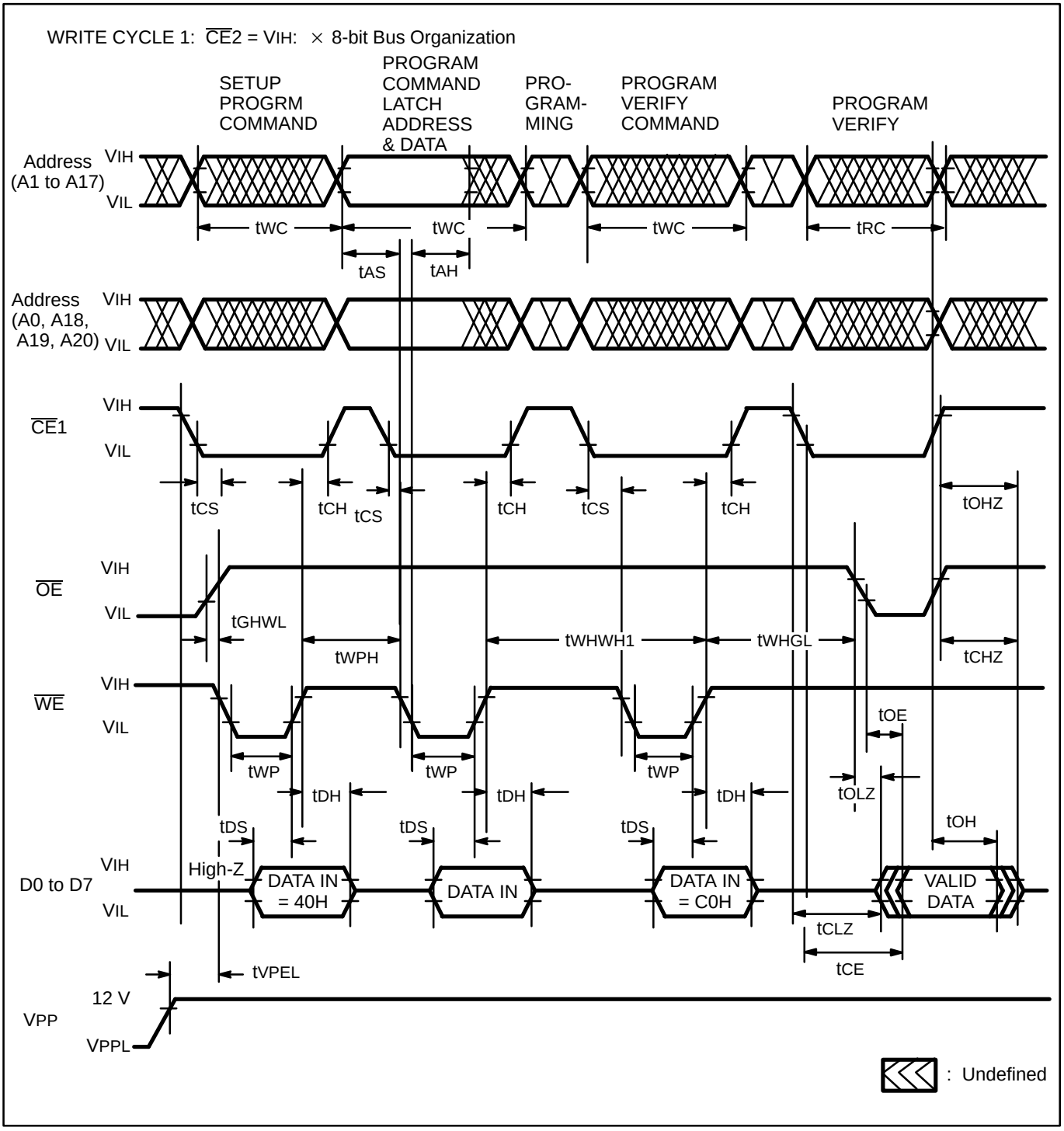
Parameter	Symbol	Min	Max	Unit
Write Cycle Time	t_{RWR}	—	10	ms
Address Set Up Time	t_{RAS}	20	—	ns
Card Enable Set Up Time	t_{RCS}	0	—	ns
Output Enable Set Up Time	t_{ROES}	20	—	ns
Write Pulse Width	t_{RWP}	100	—	ns
Address Hold Time	t_{RAH}	50	—	ns
Data Set Up Time	t_{RDS}	50	—	ns
Data Hold Time	t_{RDH}	20	—	ns
Card Enable Hold Time	t_{RCH}	0	—	ns
Output Enable Hold Time	t_{ROEH}	20	—	ns
Write Recovery Time	t_{RRE}	50	—	ns
End of Write to Output Time	t_{RRBO}	—	100	ns
Number of Write per Byte	N	10000	—	Times
Write Enable Hold Time	t_{RWEH}	10	—	ns

Note: *1 This parameter is for MB98A808A3, 809A3, 810A3, and 811A3.

AC CHARACTERISTICS (Continued)

(At recommended operating conditions unless otherwise noted.)

MAIN MEMORY WRITE CYCLE TIMING DIAGRAM ($\overline{WE}$ = CONTROLLED) *1

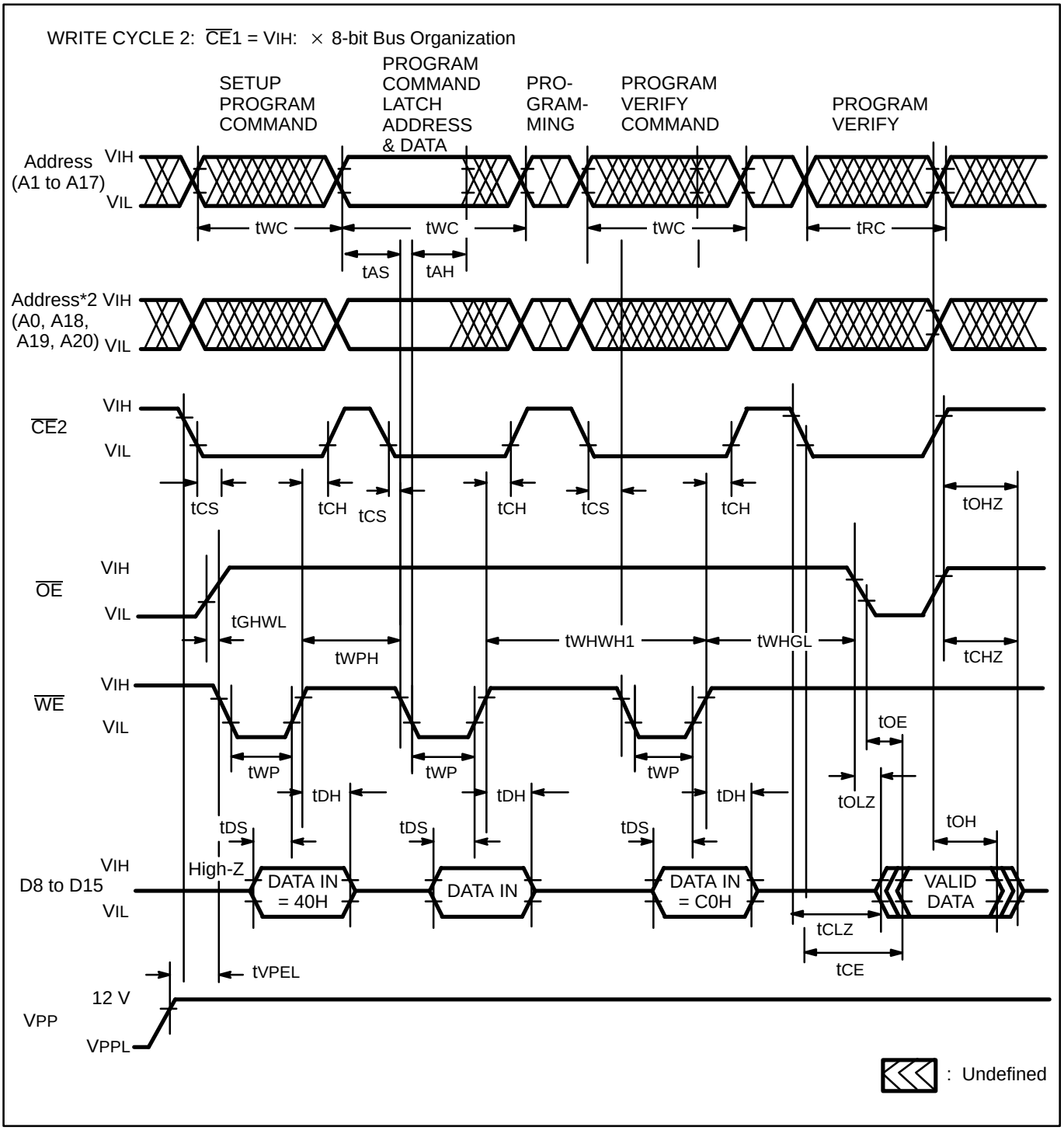


Note: *1 A0, A18, A19 and A20 have to be fixed during programming command input because these addresses are chip decoding addresses. Refer to the WRITE/ERASE CHIP DECODING INFORMATION.

AC CHARACTERISTICS (Continued)

(At recommended operating conditions unless otherwise noted.)

MAIN MEMORY WRITE CYCLE TIMING DIAGRAM ($\overline{WE}$ = CONTROLLED) *1



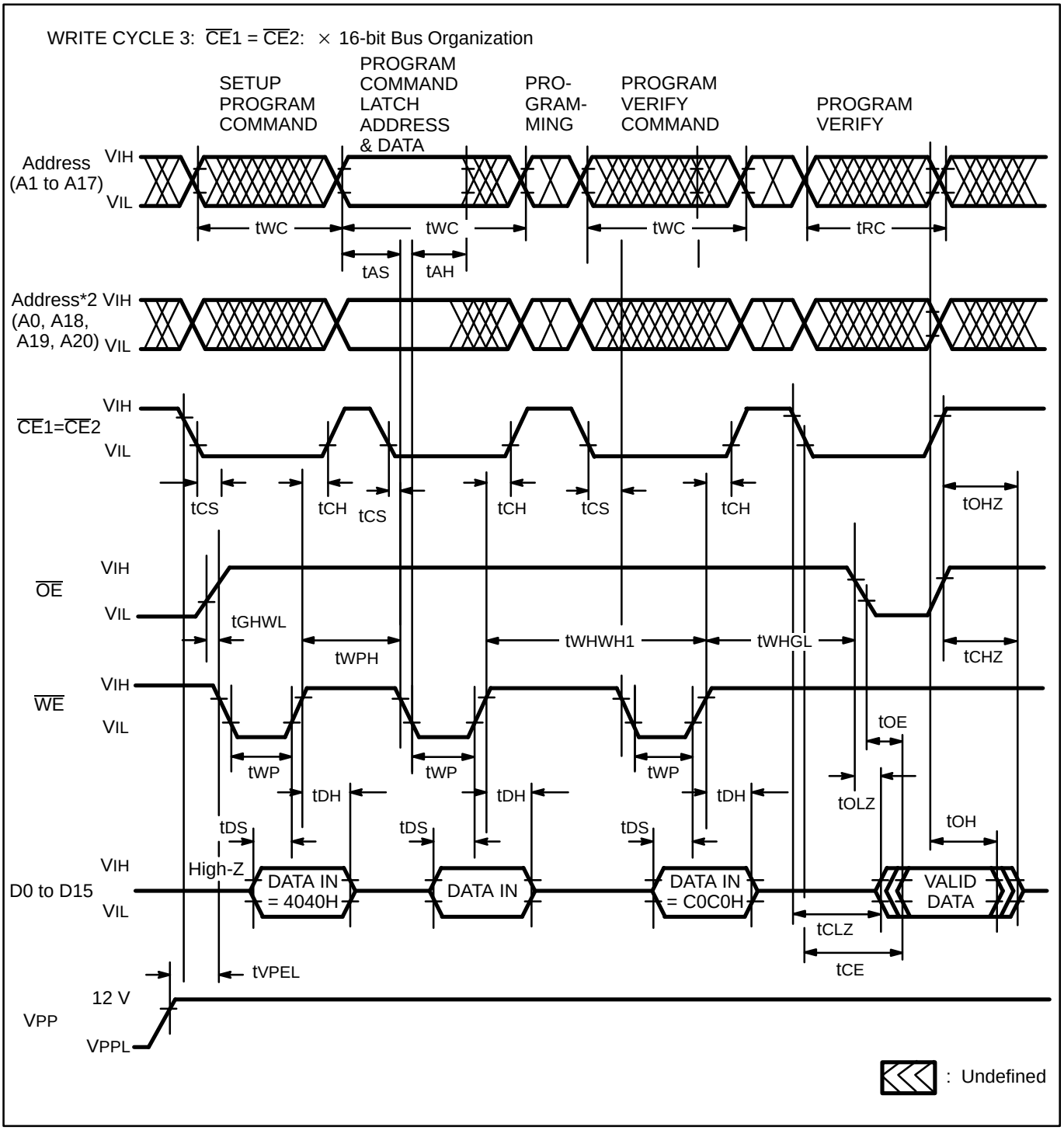
Notes: *1 A0, A18, A19 and A20 have to be fixed during programming command input because these addresses are chip decoding addresses. Refer to the WRITE/ERASE CHIP DECODING INFORMATION.

*2 A0 = Either VIL or VIH.

AC CHARACTERISTICS (Continued)

(At recommended operating conditions unless otherwise noted.)

MAIN MEMORY WRITE CYCLE TIMING DIAGRAM ($\overline{WE}$ = CONTROLLED) *1



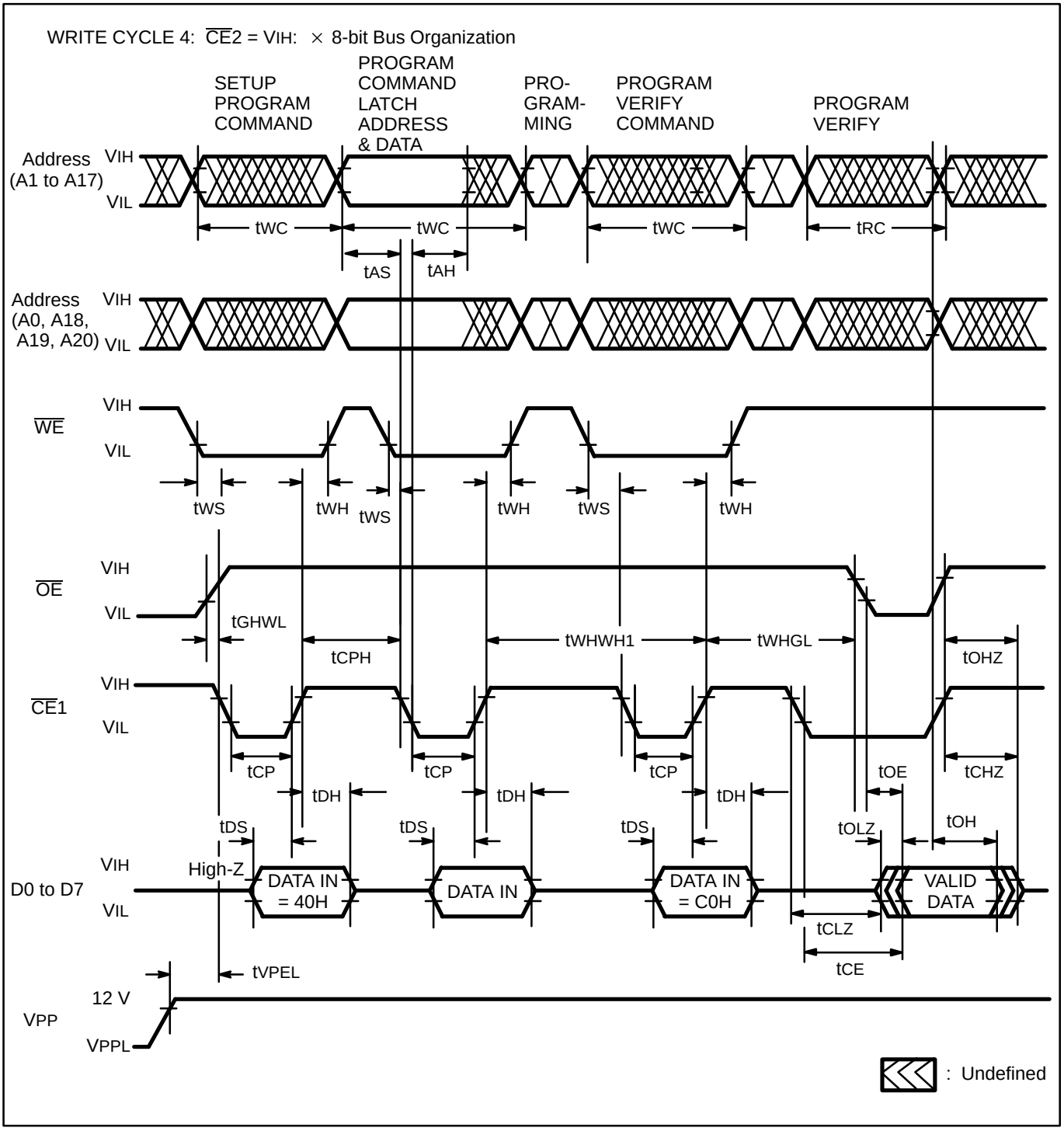
Notes: *1 A0, A18, A19 and A20 have to be fixed during programming command input because these addresses are chip decoding addresses. Refer to the WRITE/ERASE CHIP DECODING INFORMATION.

*2 A0 = Either V_{IL} or V_{IH}.

AC CHARACTERISTICS (Continued)

(At recommended operating conditions unless otherwise noted.)

MAIN MEMORY WRITE CYCLE TIMING DIAGRAM ($\overline{CE}$ = CONTROLLED) *1

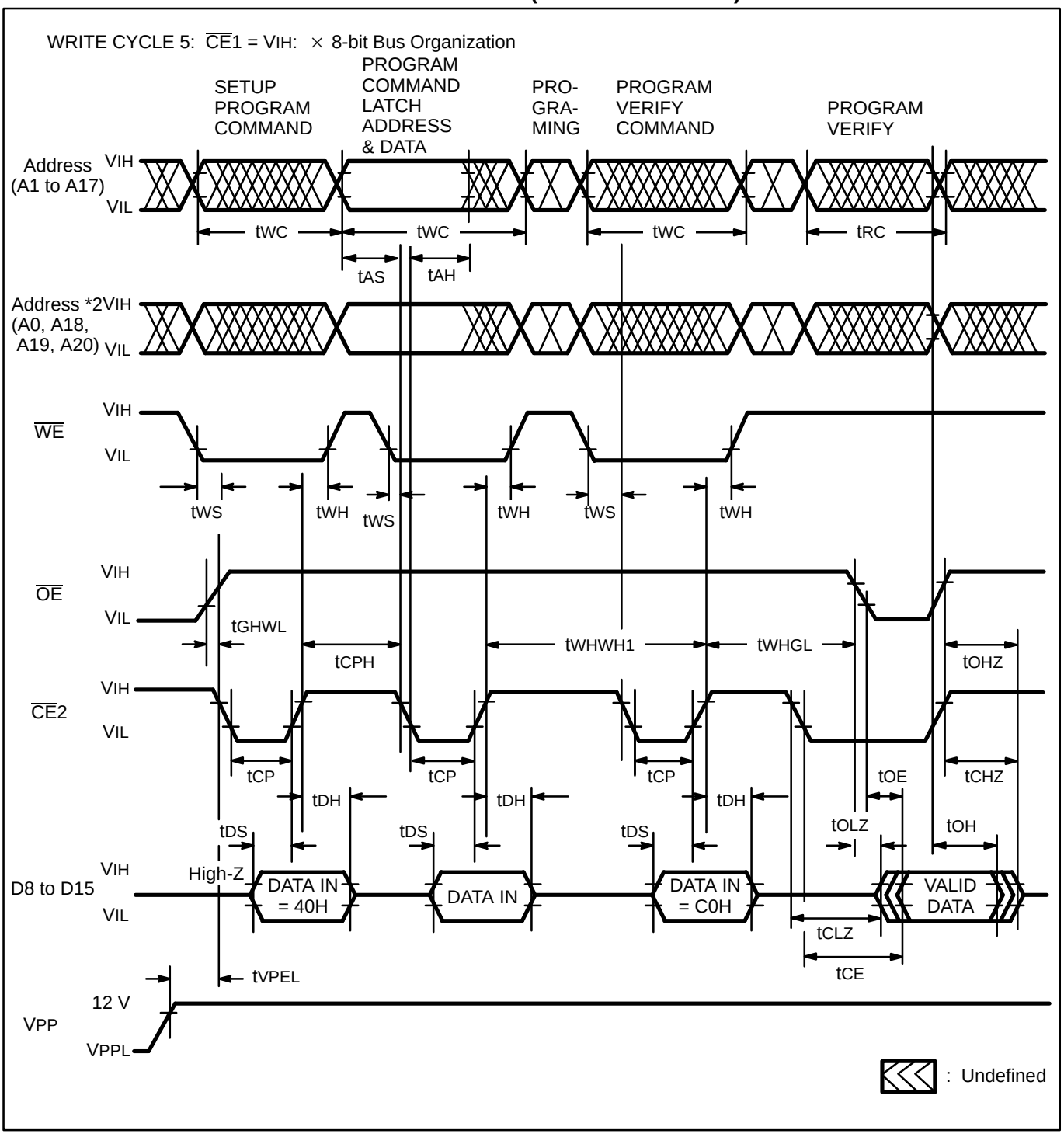


Note: *1 A0, A18, A19 and A20 have to be fixed during programming command input because these addresses are chip decoding addresses. Refer to the WRITE/ERASE CHIP DECODING INFORMATION.

AC CHARACTERISTICS (Continued)

(At recommended operating conditions unless otherwise noted.)

MAIN MEMORY WRITE CYCLE TIMING DIAGRAM ($\overline{CE}$ = CONTROLLED) *1



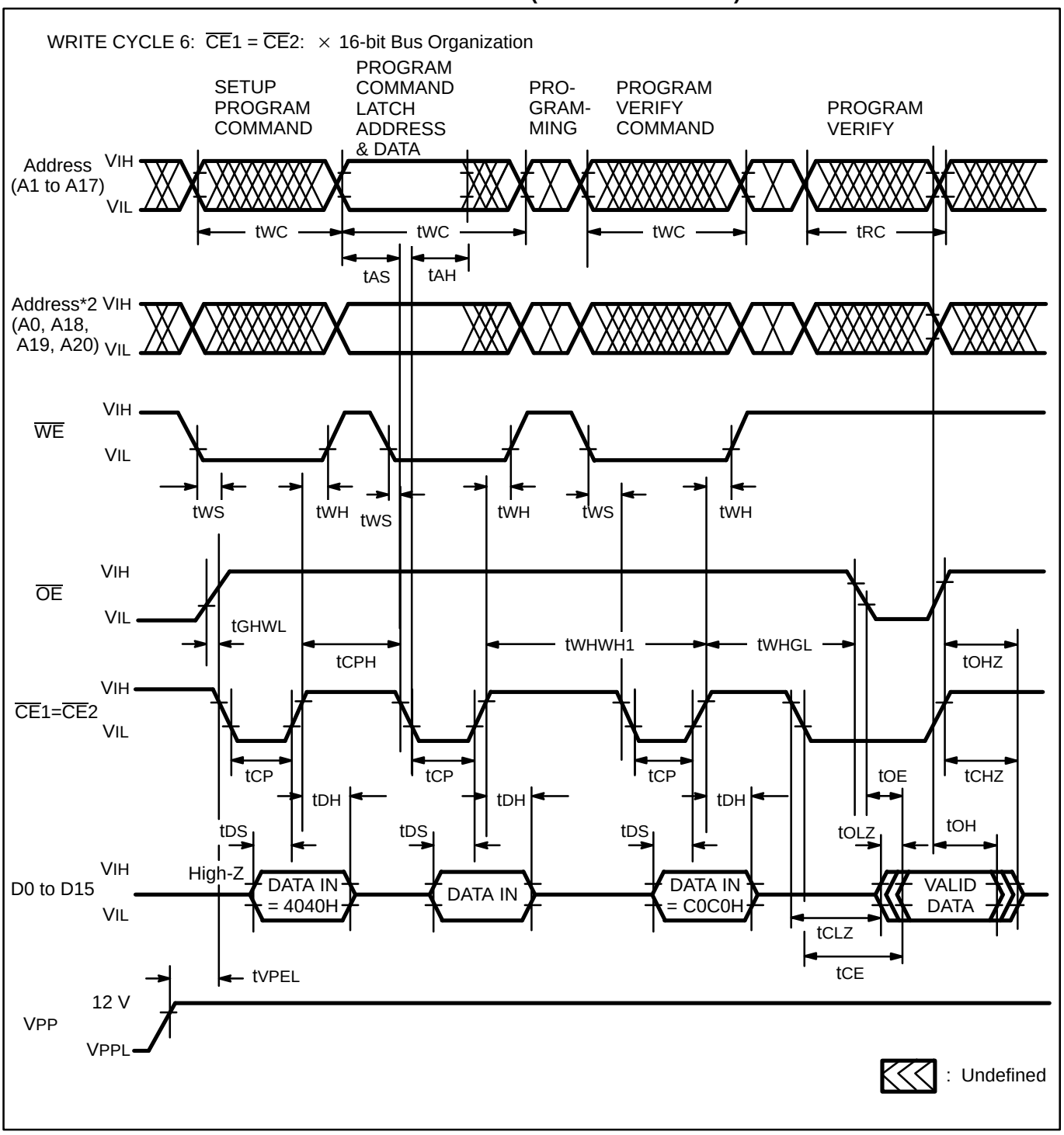
Notes: *1 A0, A18, A19 and A20 have to be fixed during programming command input because these addresses are chip decoding addresses. Refer to the WRITE/ERASE CHIP DECODING INFORMATION.

*2 A0 = Either VIL or VIH.

AC CHARACTERISTICS (Continued)

(At recommended operating conditions unless otherwise noted.)

MAIN MEMORY WRITE CYCLE TIMING DIAGRAM ($\overline{CE}$ = CONTROLLED) *1



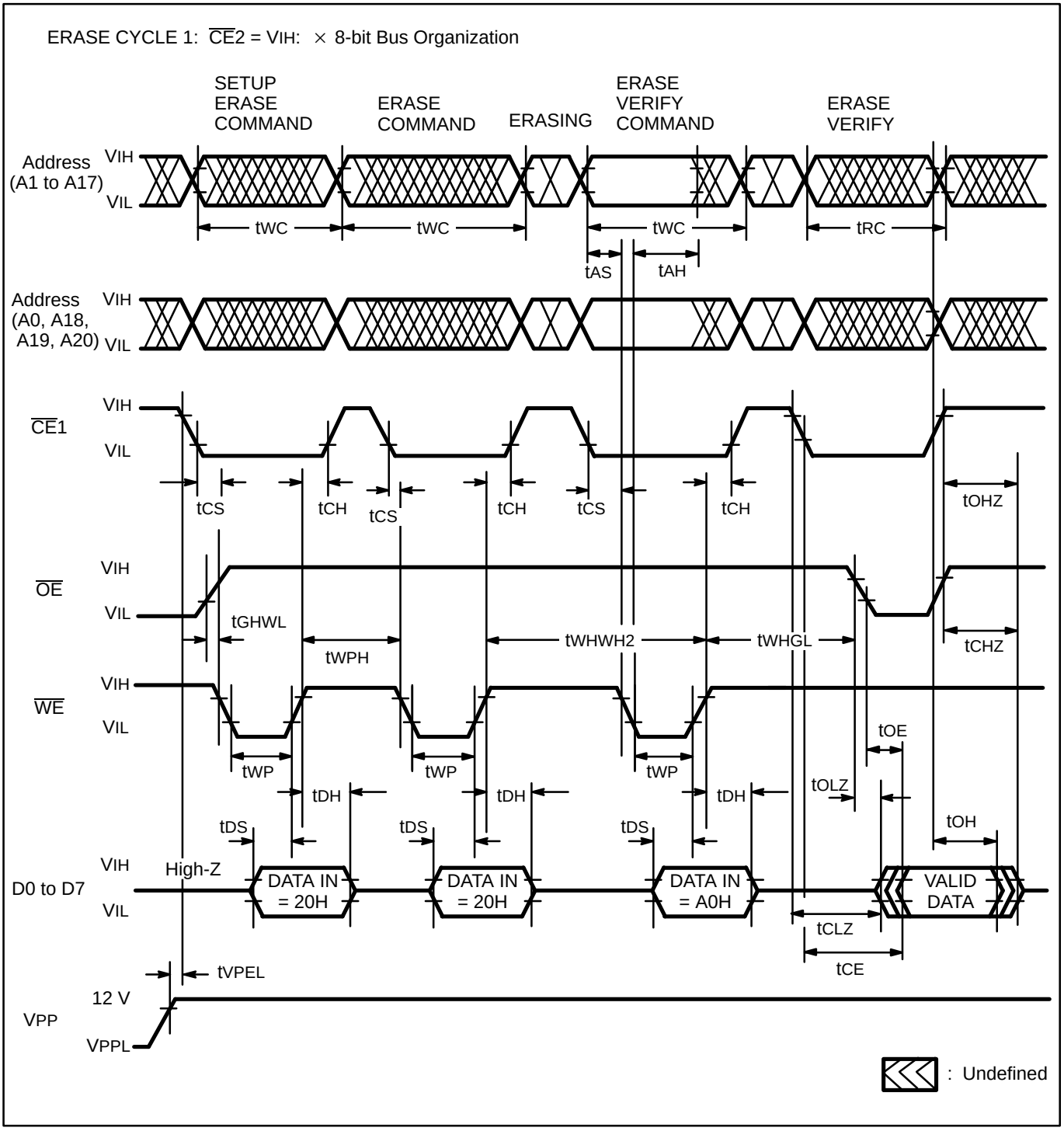
Notes: *1 A0, A18, A19 and A20 have to be fixed during programming command input because these addresses are chip decoding addresses. Refer to the WRITE/ERASE CHIP DECODING INFORMATION.

*2 A0 = Either V_{IL} or V_{IH}.

AC CHARACTERISTICS (Continued)

(At recommended operating conditions unless otherwise noted.)

MAIN MEMORY ERASE CYCLE TIMING DIAGRAM ($\overline{WE}$ = CONTROLLED) *1

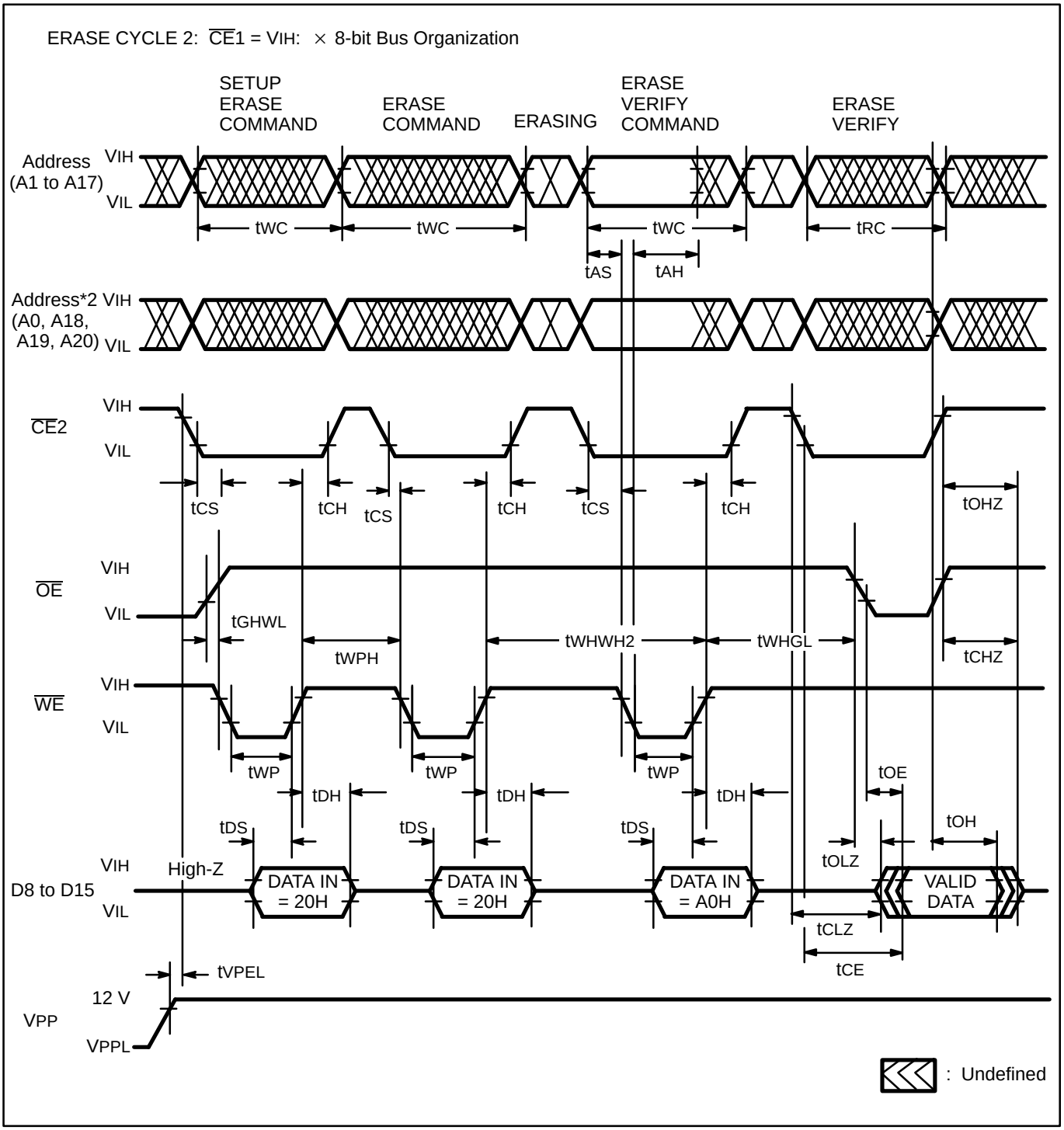


Note: *1 A0, A18, A19 and A20 have to be fixed during erase command input because these addresses are chip decoding addresses. Refer to the WRITE/ERASE CHIP DECODING INFORMATION.

AC CHARACTERISTICS (Continued)

(At recommended operating conditions unless otherwise noted.)

MAIN MEMORY ERASE CYCLE TIMING DIAGRAM ($\overline{WE}$ = CONTROLLED) *1



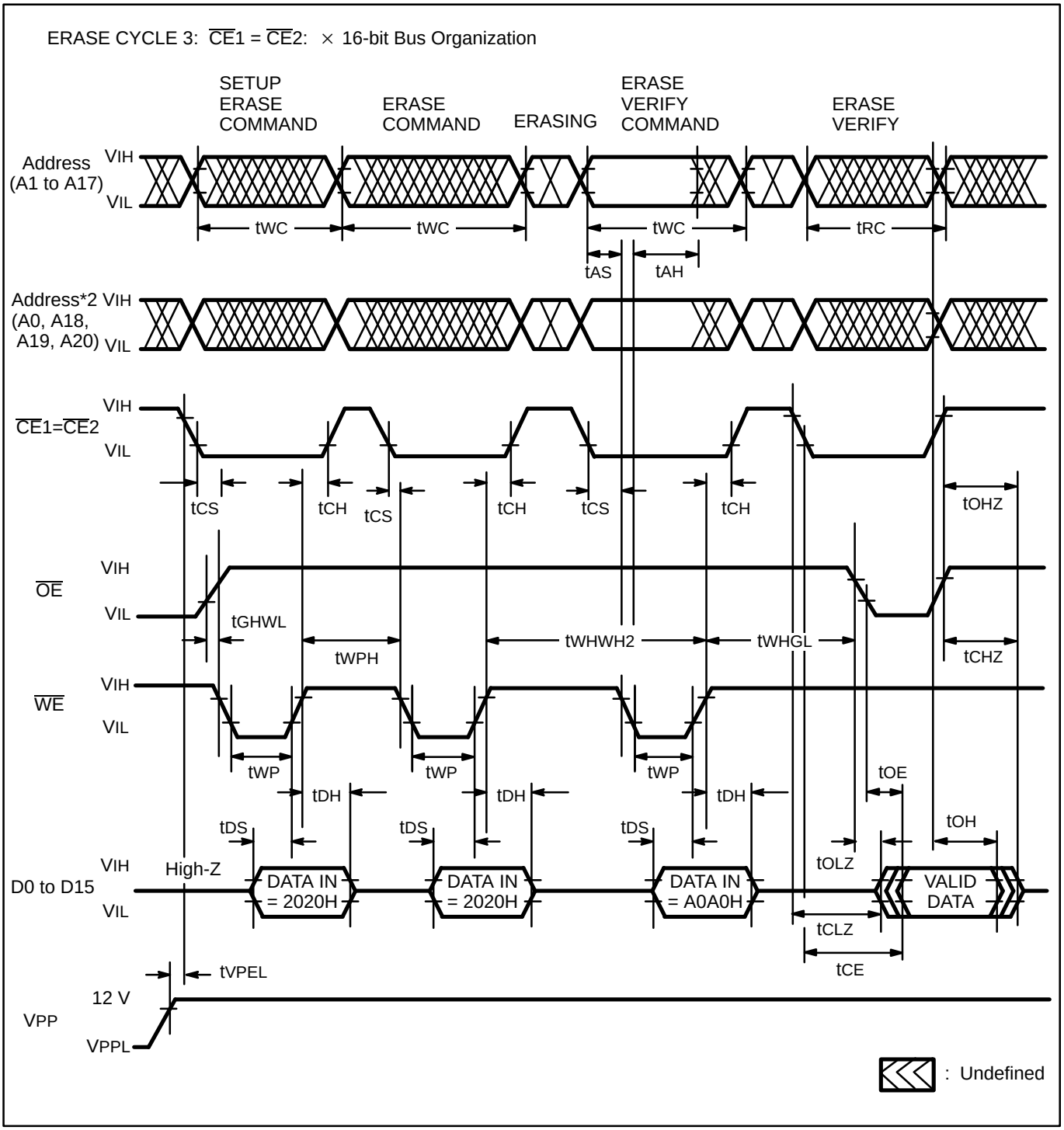
Notes: *1 A0, A18, A19 and A20 have to be fixed during erase command input because these addresses are chip decoding addresses. Refer to the WRITE/ERASE CHIP DECODING INFORMATION.

*2 A0 = Either VIL or VIH.

AC CHARACTERISTICS (Continued)

(At recommended operating conditions unless otherwise noted.)

MAIN MEMORY ERASE CYCLE TIMING DIAGRAM ($\overline{WE}$ = CONTROLLED) *1



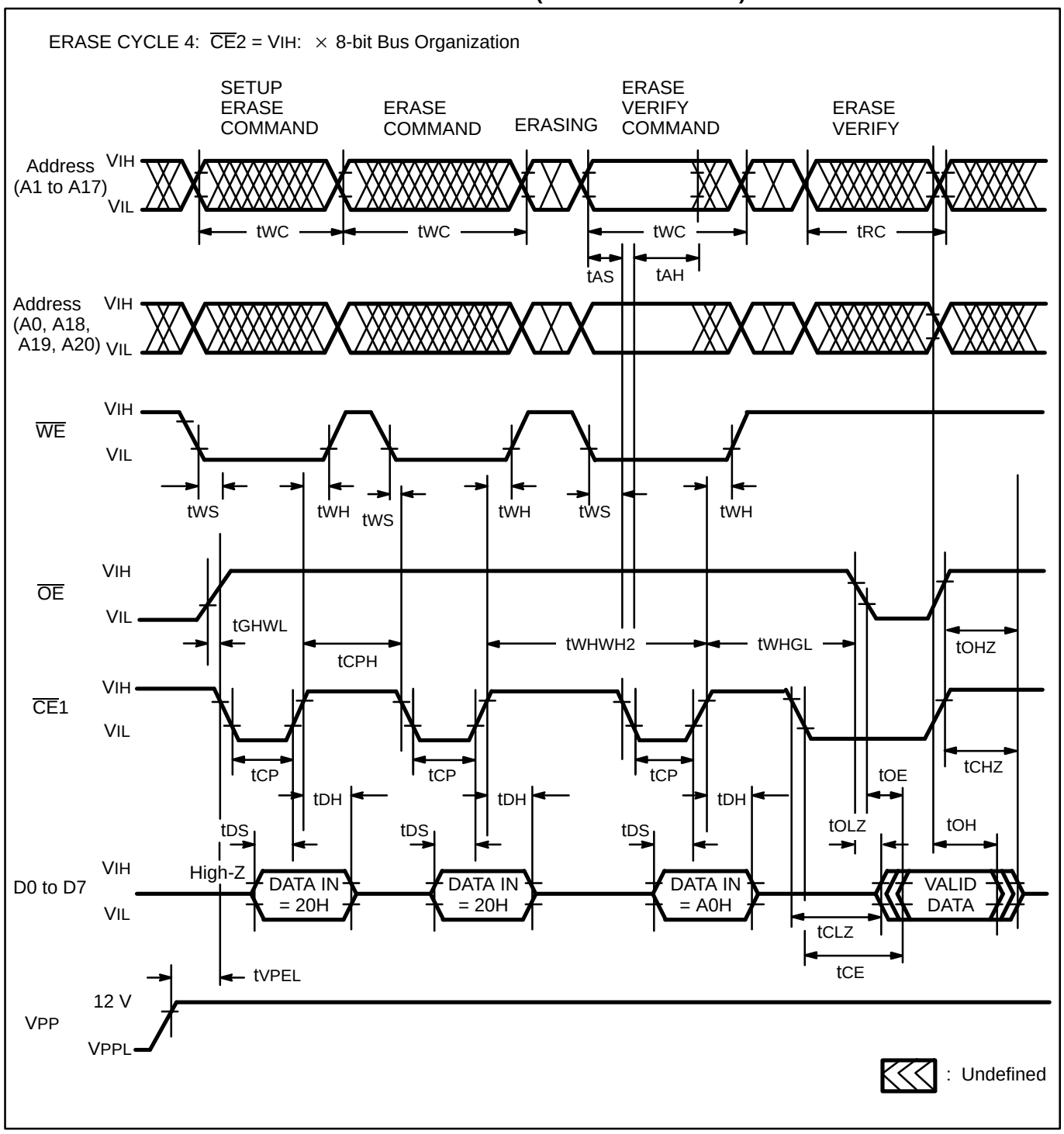
Notes: *1 A0, A18, A19 and A20 have to be fixed during erase command input because these addresses are chip decoding addresses. Refer to the WRITE/ERASE CHIP DECODING INFORMATION.

*2 A0 = Either V_{IL} or V_{IH}.

AC CHARACTERISTICS (Continued)

(At recommended operating conditions unless otherwise noted.)

MAIN MEMORY ERASE CYCLE TIMING DIAGRAM ($\overline{CE}$ = CONTROLLED) *1

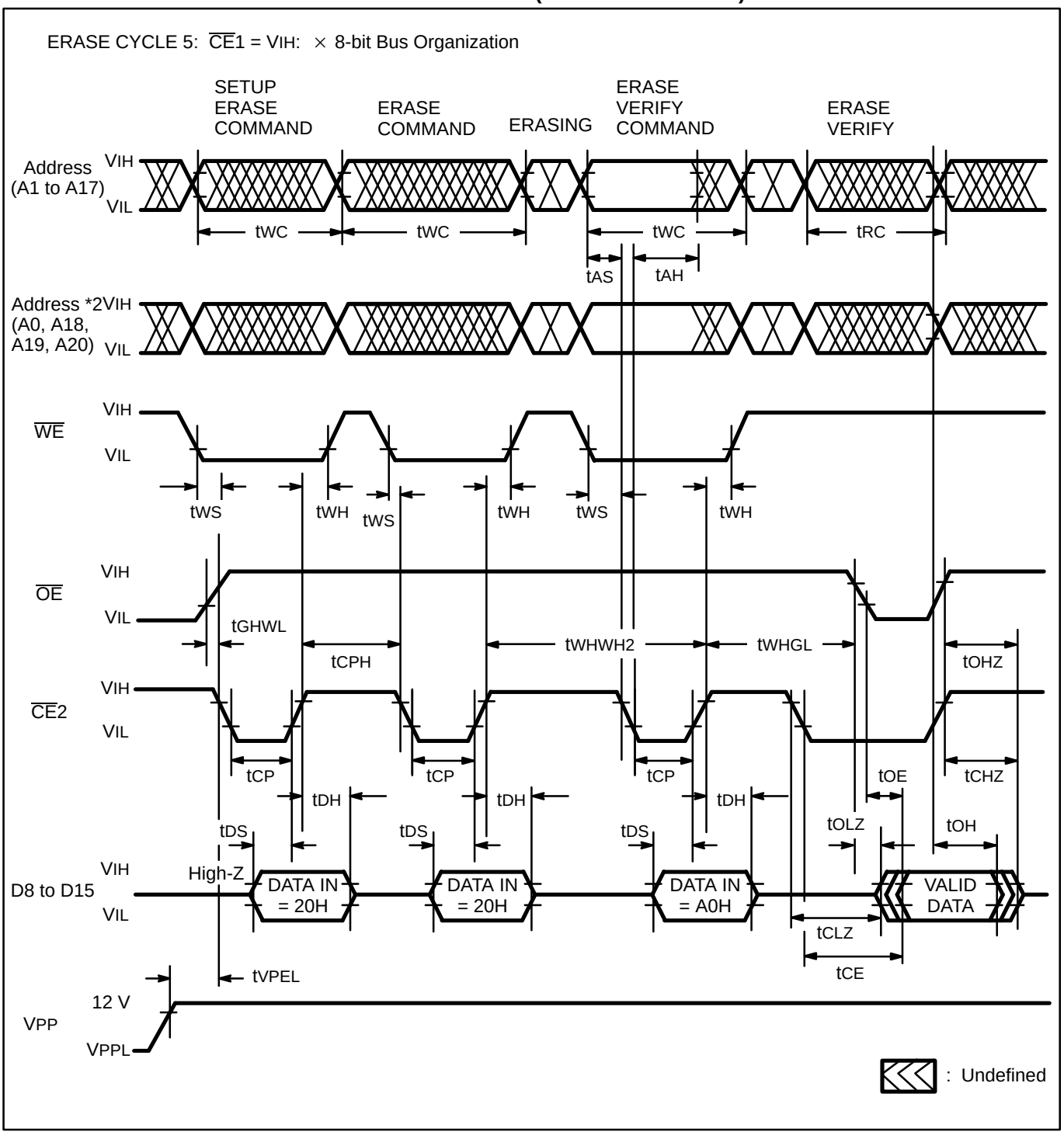


Note: *1 A0, A18, A19 and A20 have to be fixed during erase command input because these addresses are chip decoding addresses. Refer to the WRITE/ERASE CHIP DECODING INFORMATION.

AC CHARACTERISTICS (Continued)

(At recommended operating conditions unless otherwise noted.)

MAIN MEMORY ERASE CYCLE TIMING DIAGRAM ($\overline{CE}$ = CONTROLLED) *1



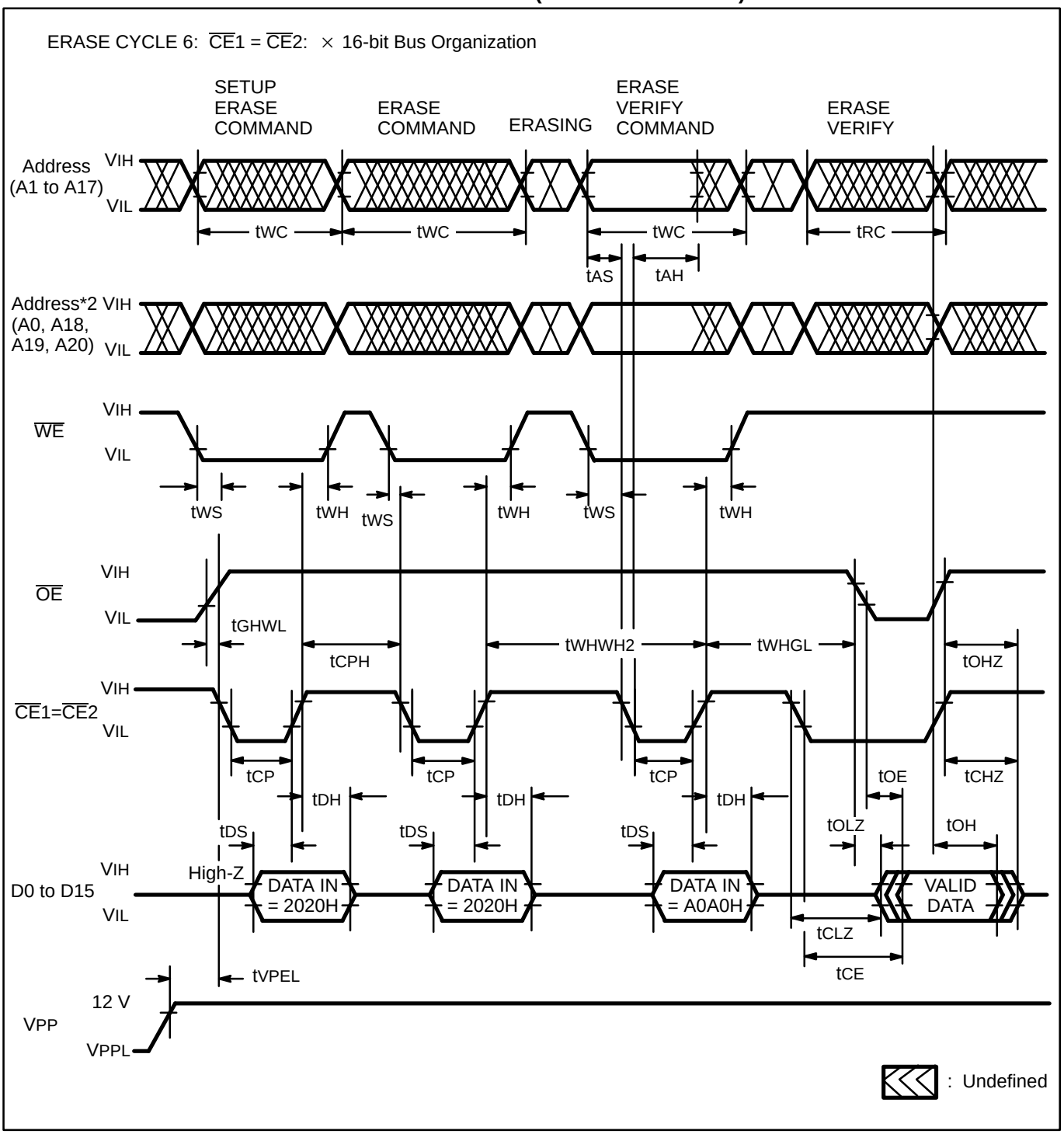
Notes: *1 A0, A18, A19 and A20 have to be fixed during erase command input because these addresses are chip decoding addresses. Refer to the WRITE/ERASE CHIP DECODING INFORMATION.

*2 A0 = Either VIL or VIH.

AC CHARACTERISTICS (Continued)

(At recommended operating conditions unless otherwise noted.)

MAIN MEMORY ERASE CYCLE TIMING DIAGRAM ($\overline{CE}$ = CONTROLLED) *1



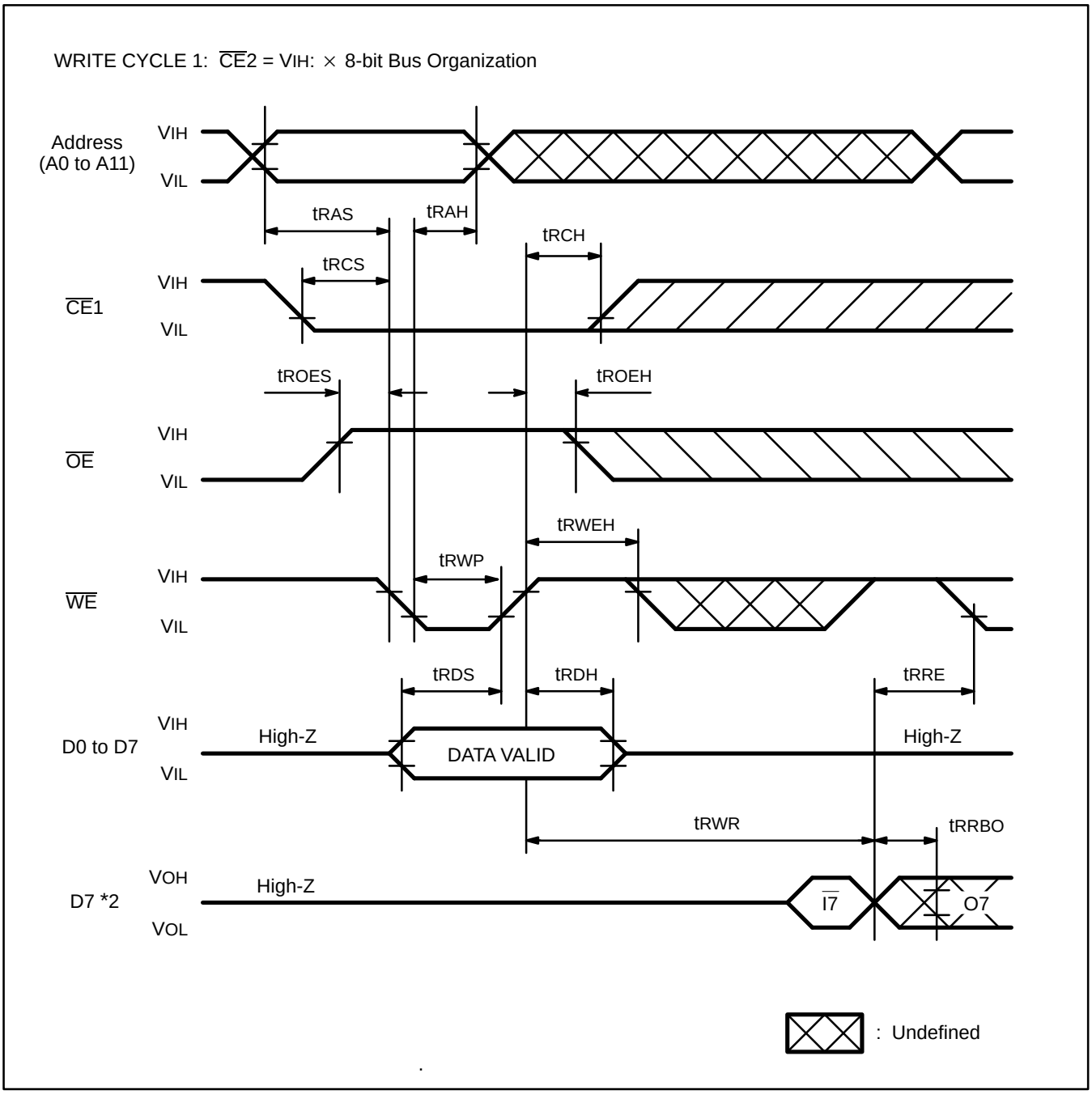
Notes: *1 A0, A18, A19 and A20 have to be fixed during erase command input because these addresses are chip decoding addresses. Refer to the WRITE/ERASE CHIP DECODING INFORMATION.

*2 A0 = Either V_{IL} or V_{IH}.

AC CHARACTERISTICS (Continued)

(At recommended operating conditions unless otherwise noted.)

ATTRIBUTE MEMORY WRITE CYCLE TIMING DIAGRAM ($\overline{WE}$ = CONTROLLED, $\overline{REG}$ = V_{IL}) *1

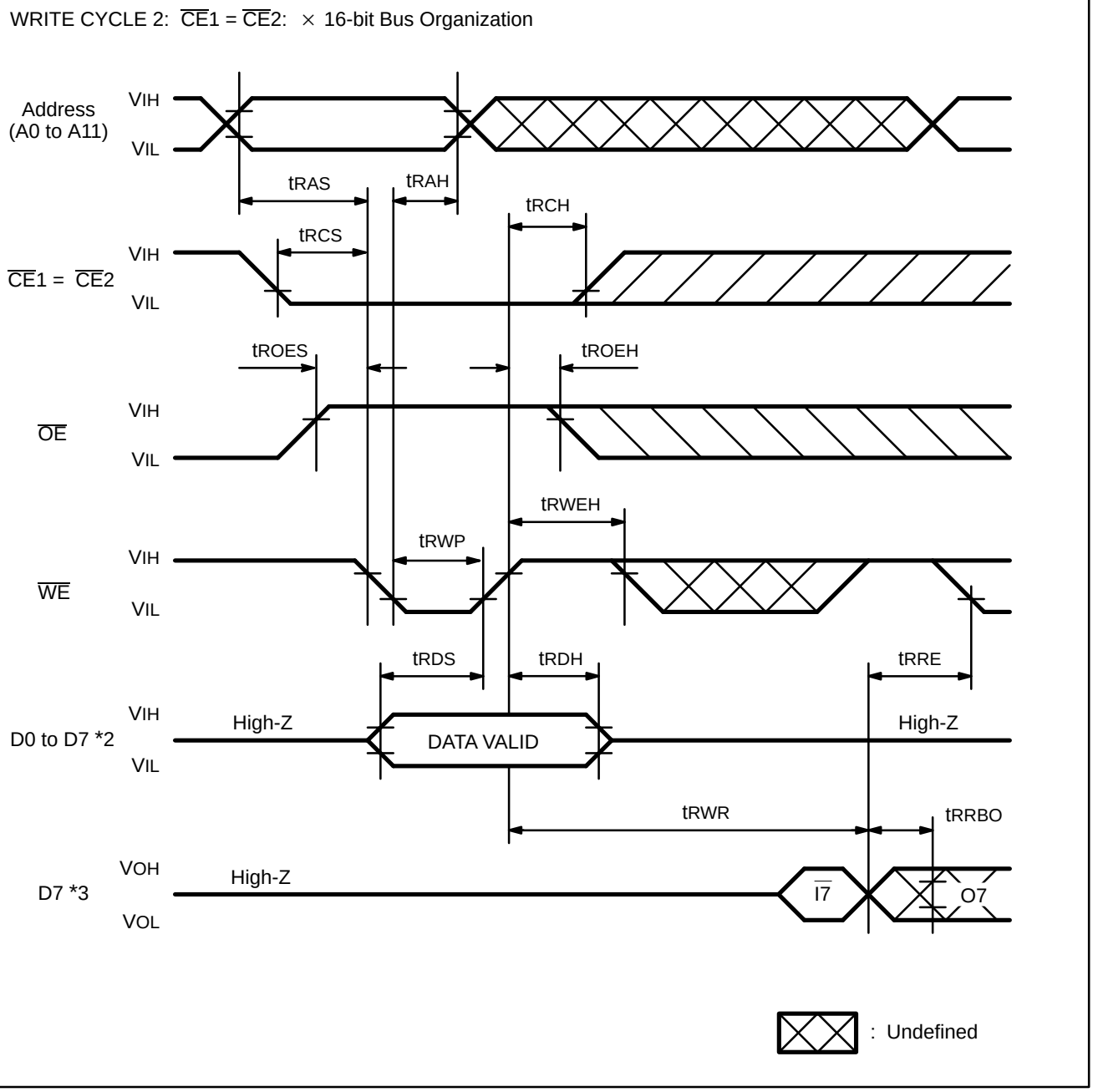


Notes: *1 This timing diagram is for MB98A808A3, 809A3, 810A3, and 811A3. “FF” data is available on MB98A808A2, 809A2, 810A2, and 811A2 only.
*2 Data polling operation.

AC CHARACTERISTICS (Continued)

(At recommended operating conditions unless otherwise noted.)

ATTRIBUTE MEMORY WRITE CYCLE TIMING DIAGRAM ($\overline{WE}$ = CONTROLLED, $\overline{REG}$ = V_{IL}) *1

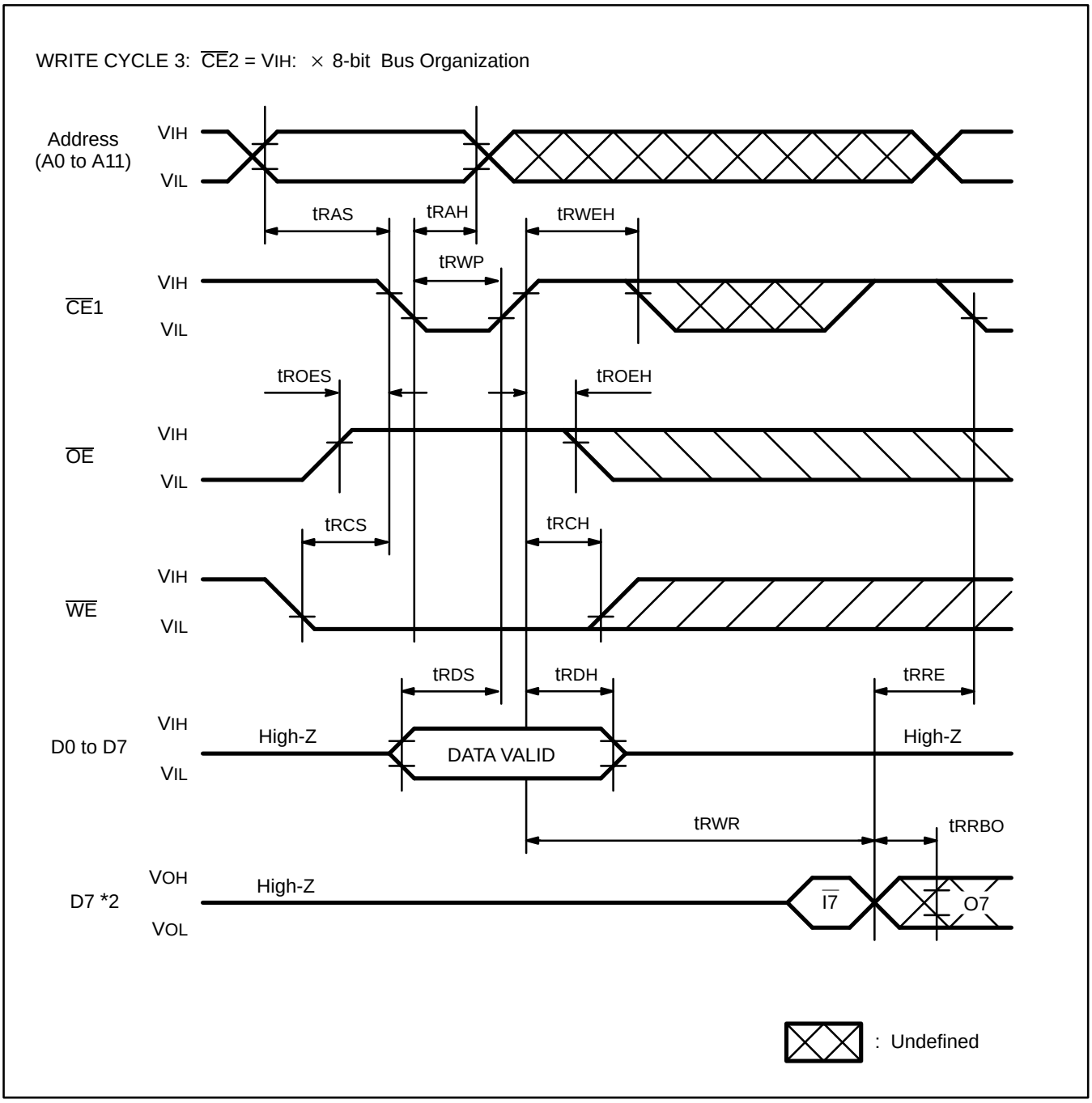


Notes: *1 This timing diagram is for MB98A808A3, 809A3, 810A3, and 811A3. “FF” data is available on MB98A808A2, 809A2, 810A2, and 811A2 only.
*2 H-level or L-level is output from D8 to D15.
*3 Data polling operation.

AC CHARACTERISTICS (Continued)

(At recommended operating conditions unless otherwise noted.)

ATTRIBUTE MEMORY WRITE CYCLE TIMING DIAGRAM ($\overline{CE}$ = CONTROLLED, $\overline{REG}$ = V_{IL}) *1

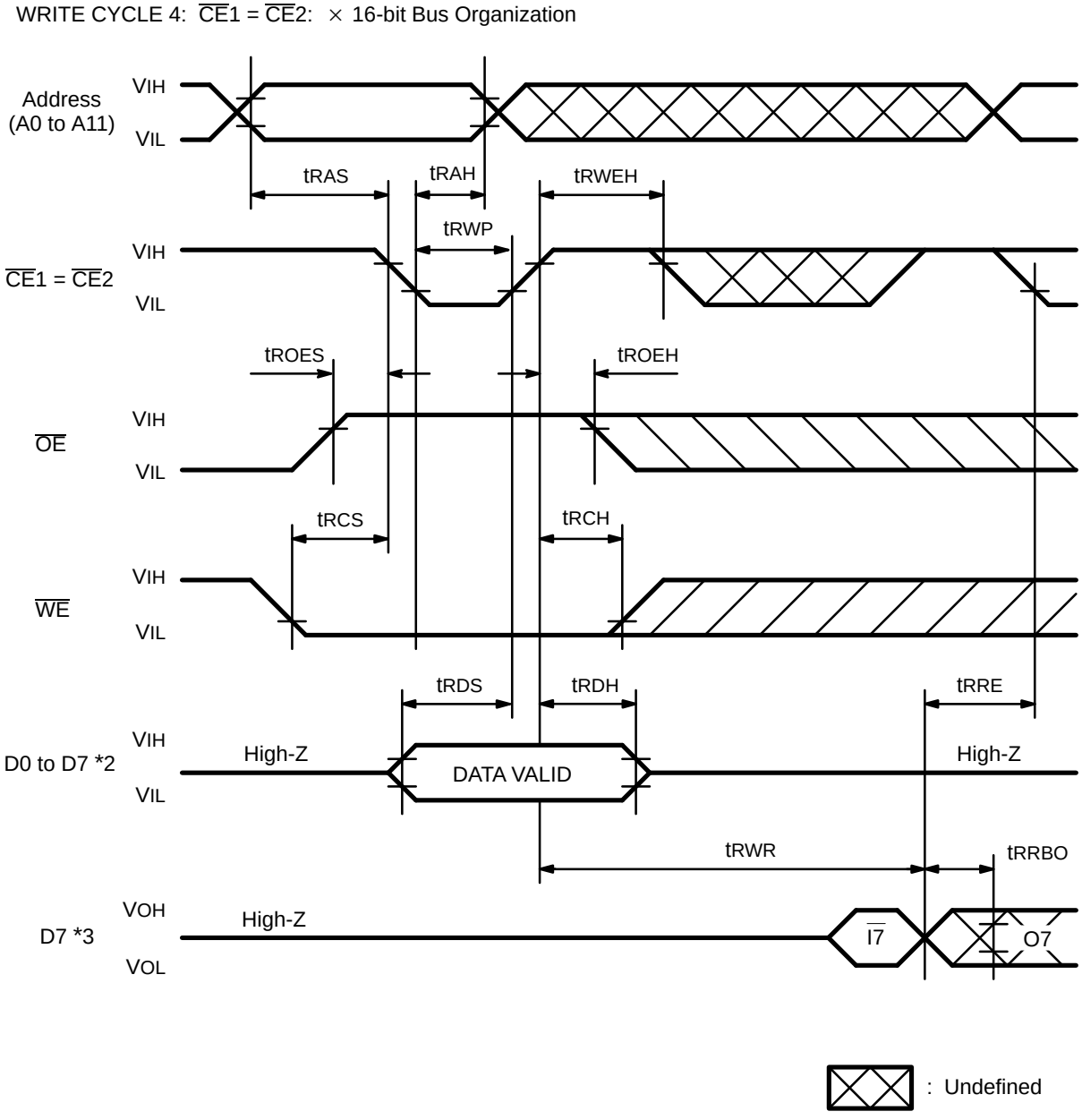


Notes: *1 This timing diagram is for MB98A808A3, 809A3, 810A3 and 811A3. “FF” data is available on MB98A808A2, 809A2, 810A2, and 811A2 only.
*2 Data polling operation.

AC CHARACTERISTICS (Continued)

(At recommended operating conditions unless otherwise noted.)

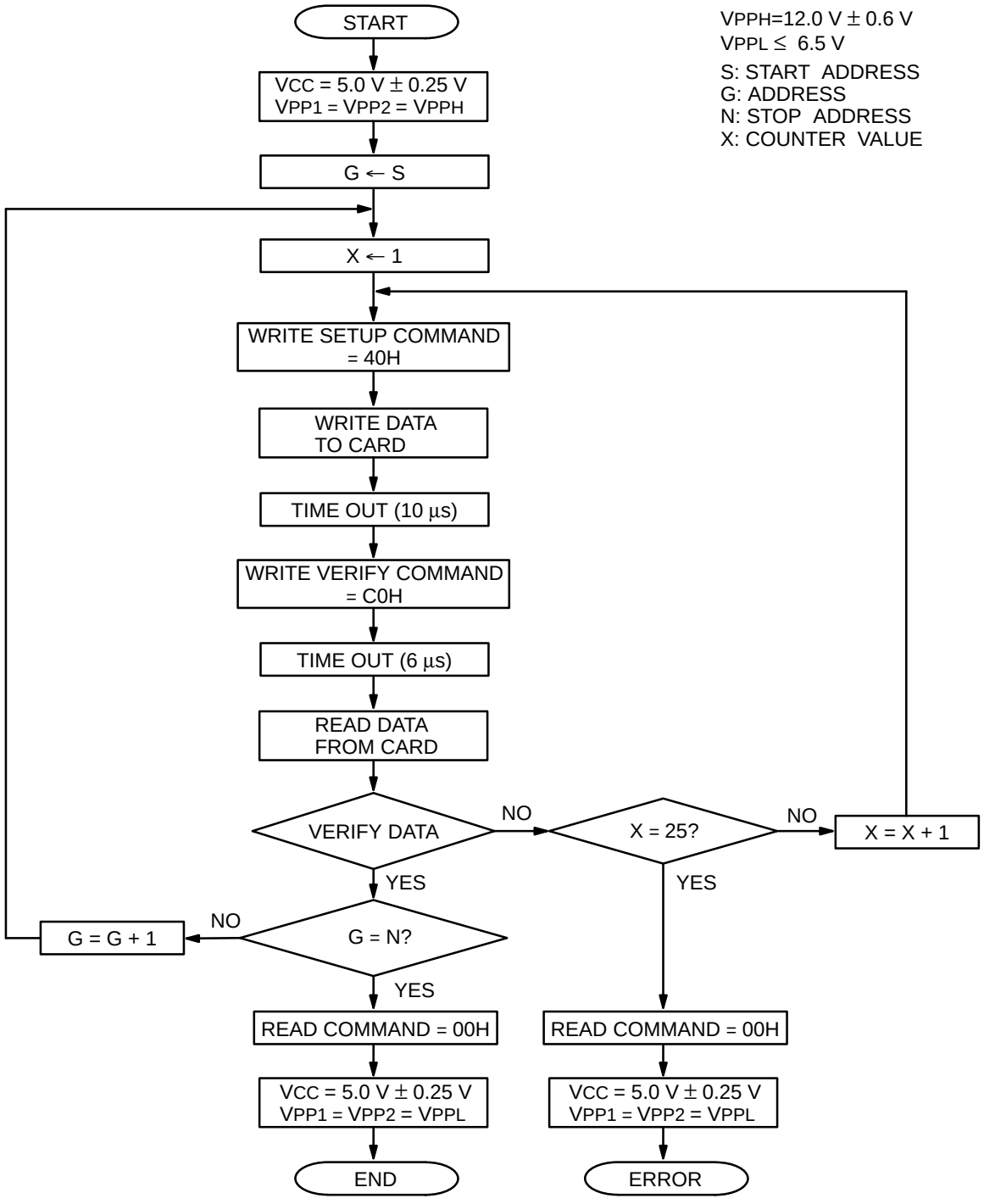
ATTRIBUTE MEMORY WRITE CYCLE TIMING DIAGRAM ($\overline{CE}$ = CONTROLLED, $\overline{REG}$ = V_{IL}) *1



Notes: *1 This timing diagram is for MB98A808A3, 809A3, 810A3, and 811A3. “FF” data is available on MB98A808A2, 809A2, 810A2, and 811A2 only.
*2 H-level or L-level is output from D8 to D15.
*3 Data polling operation.

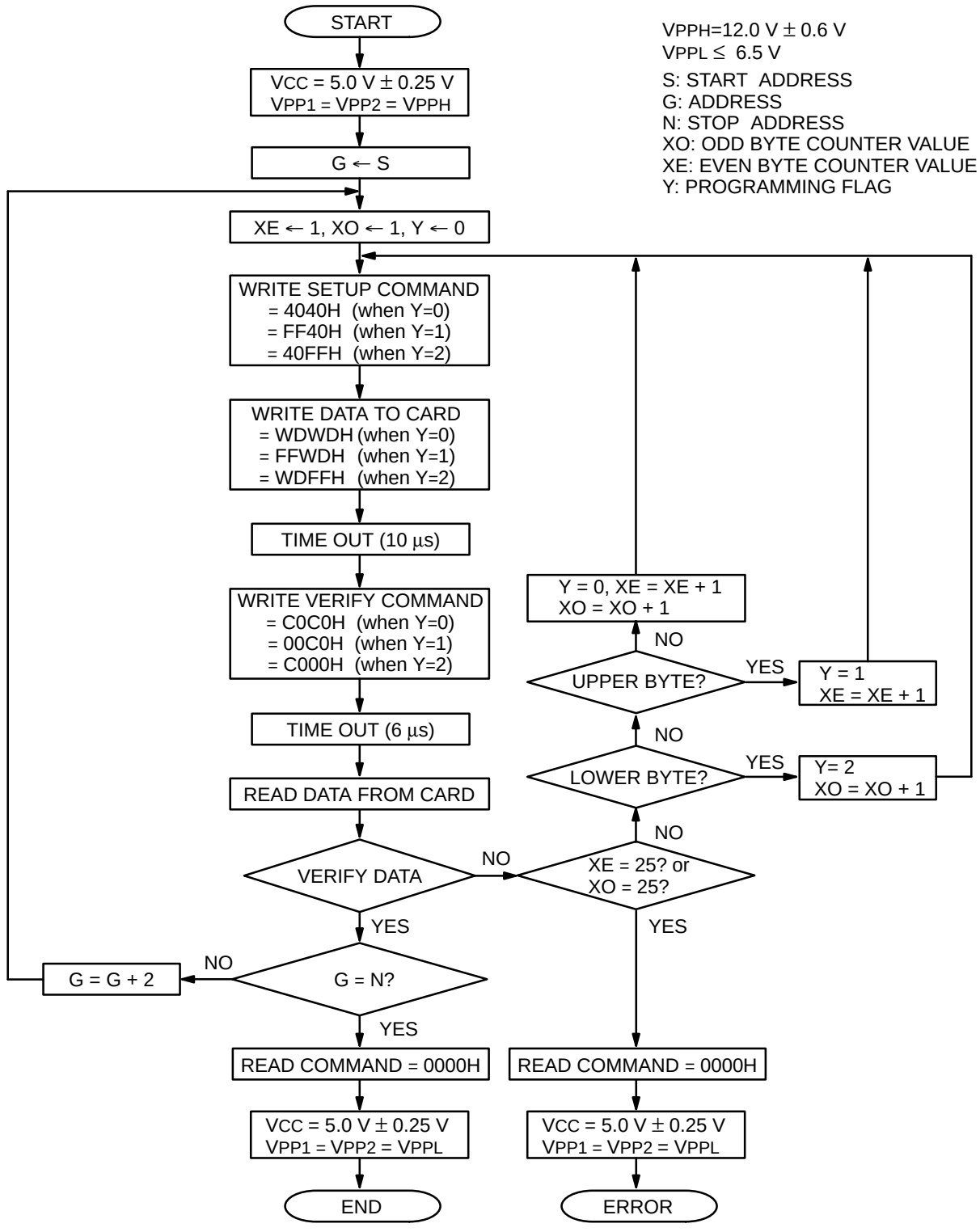
WRITE / ERASE INFORMATION

Fig. 4 – WRITE FLOWCHART FOR 8-BIT ORGANIZATION



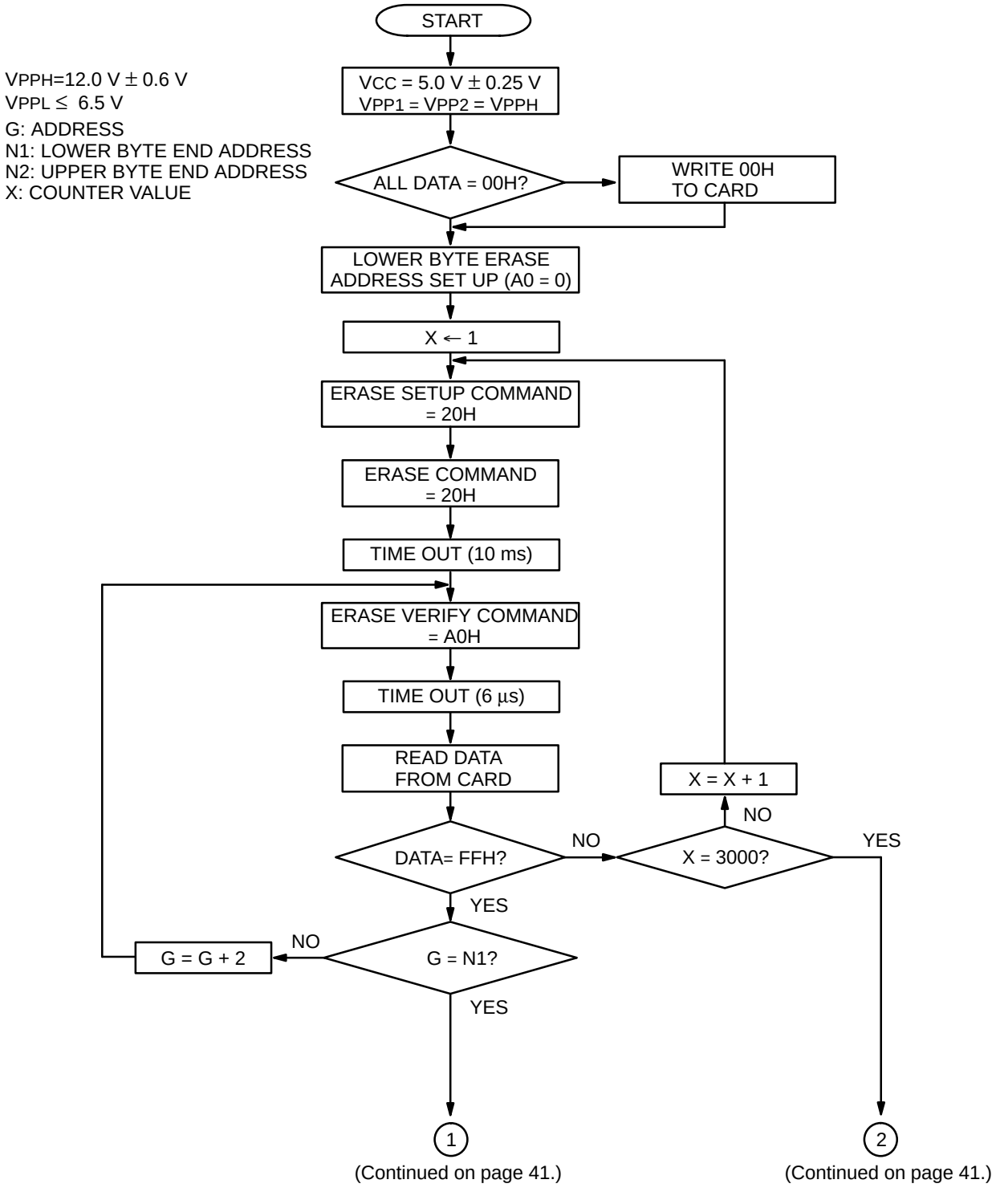
WRITE / ERASE INFORMATION (Continued)

Fig. 5 – WRITE FLOWCHART FOR 16-BIT ORGANIZATION



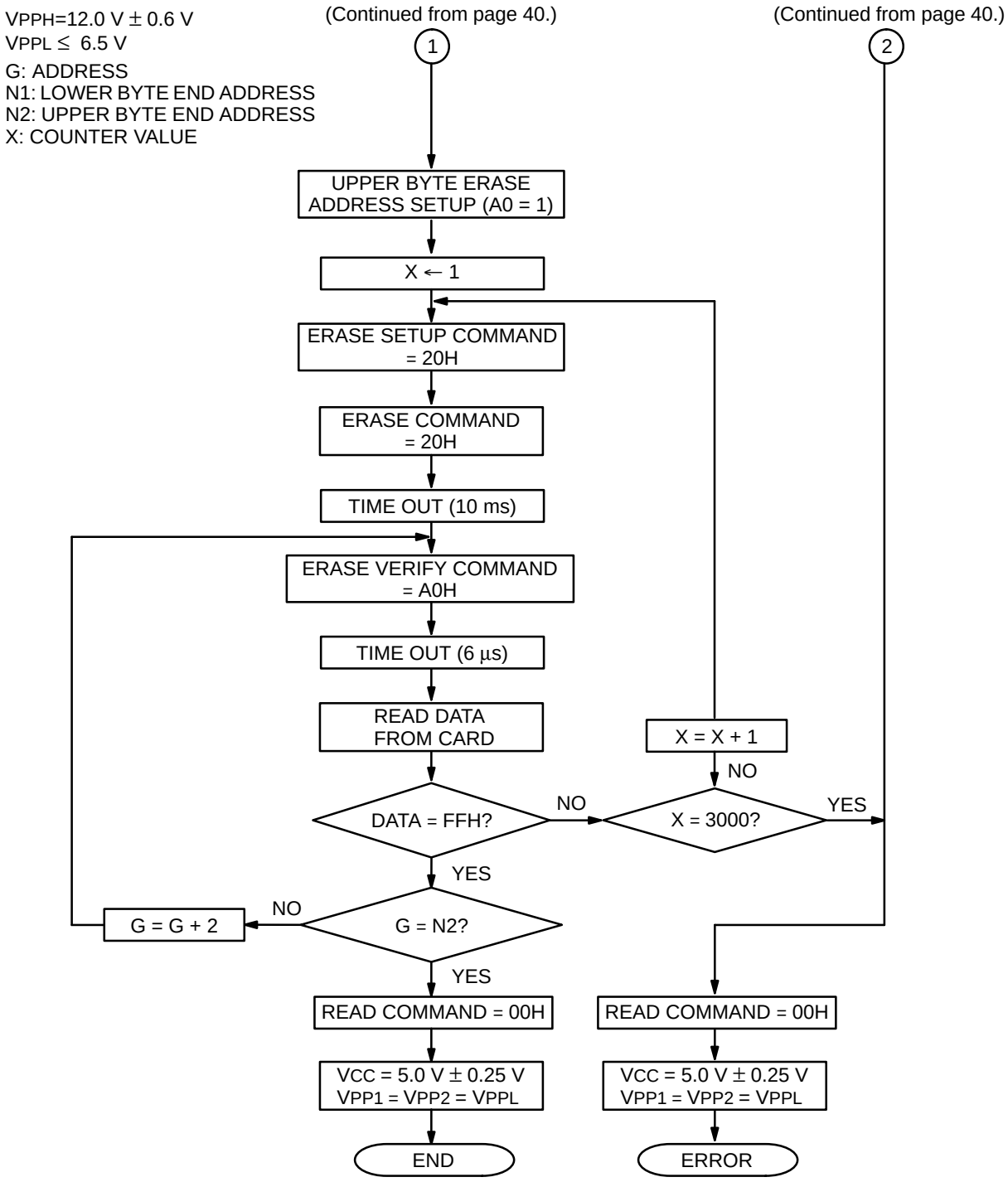
WRITE / ERASE INFORMATION (Continued)

Fig. 6 – ERASE FLOWCHART FOR 8-BIT ORGANIZATION



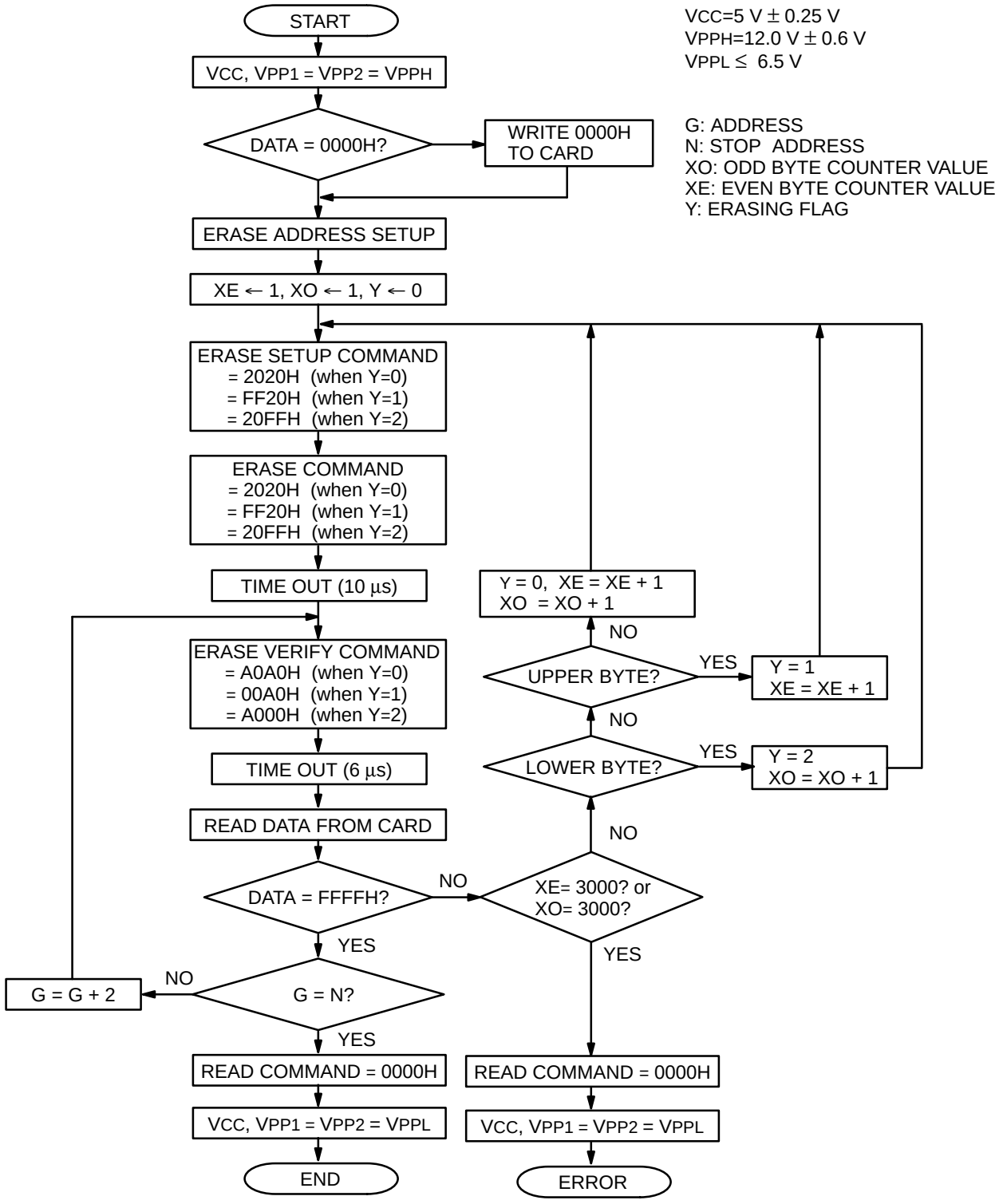
WRITE / ERASE INFORMATION (Continued)

Fig. 7 – ERASE FLOWCHART FOR 8-BIT ORGANIZATION (Continued)



WRITE / ERASE INFORMATION (Continued)

Fig. 8 – ERASE FLOWCHART FOR 16-BIT ORGANIZATION

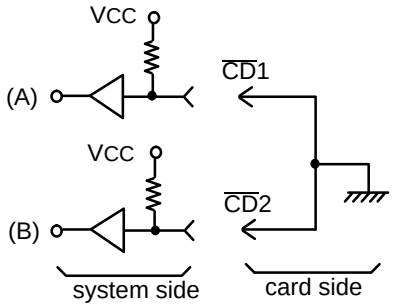


UNIQUE FEATURES FOR FLASH MEMORY CARD

1. SPECIAL MONITORING PINS

1.1 $\overline{CD}$1, $\overline{CD}$2: Card Detection Pins

These pins detect the insertion of the card into the system. (See Fig. 9.)
When the memory card has been correctly inserted, $\overline{CD}$1 and $\overline{CD}$2 are detected by the system. $\overline{CD}$1, $\overline{CD}$2 are tied to ground on the card side as shown in Fig. 9.



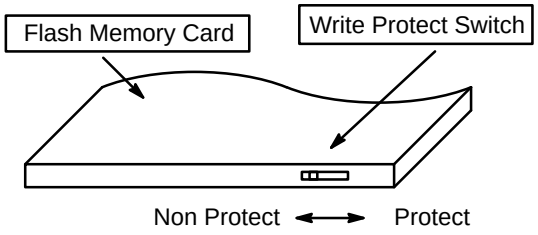
– Fig. 9 –

1.2 WP: Write Protect Pins

This pin monitors the position of the Write Protect switch. As shown in Fig. 10, the Flash memory card has a Write Protect switch at the top of the card.

To write to the card, the switch must be turned to the "Non Protect" position and the $\overline{WE}$ pin low. L-level is output on the WP pin.

To prevent writing to the card, the switch must be turned to the "Protect" position. H-level is output on the WP pin.



– Fig. 10 –

WP Switch	WP (output)
Protect	H
Non Protect	L

■ DEVICE HANDLING PRECAUTIONS

This device in composed of fine electronic parts, so take care in handling or keeping it as below.

- The card is made fine, so do not keep it in the high temperature nor high humiditly, place like in the direct sun-shine nor near the heater.
- The card should not be bent, scratched, dropped nor be shocked violently.
- This device should never be taken a part. It could destroy the card or your personal computer hardware.
- To help you handle this device safely, request us the device specifications when purchasing this device.

PACKAGE DIMENSIONS

68-PIN MEMORY CARD
(CASE No.: CRD-68P-M17)

Note: Dimensions comform with PC CARD standard 95

MEMO

MEMO

MEMO

FUJITSU LIMITED

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