Order this document
by EB166/D

MOTOROLA
SEMICONDUCTOR
ENGINEERING BULLETIN

EB166

System Design Considerations: Converting from the MC68HC805B6 to the MC68HC705B16 Microcontroller

INTRODUCTION

During the past several years, Motorola has been reviewing all processing and manufacturing methods to determine ways to reduce the impact of these methods on the environment. One of the major results of this study was the decision to eliminate the use of chlorofluorocarbons (CFCs) by Motorola. Unfortunately, CFCs were used in the processing of the Motorola MC68HC805B6 microcontroller unit (MCU). In compliance with this new corporate policy, Motorola has discontinued the production of the MC68HC805B6. The recommended replacement for this device is the MC68HC705B16.

The MC68HC705B16 is pin-compatible and supports all resources found on the MC68HC805B6; however, **the MC68HC705B16 is not a drop-in replacement**. There are many considerations when converting from the electrically erasable programmable read-only memory (EEPROM)-based MC68HC805B6 to the erasable programmable read-only memory (EPROM)-based MC68HC705B16. Careful attention must be paid to all of the differences to ensure successful migration to the MC68HC705B16.

In cases where the byte-programmable EEPROM is not required, or if the target MCU is the MC68HC05B4, the MC68HC705B5 provides a virtually transparent replacement for the MC68HC805B6. This EPROM-based device is also pin-compatible, and provides a subset of the resources found on the MC68HC805B6. The only differences are replacement of the user-program memory and the byte-programmable EEPROM with EPROM, and changing the address of the Option Register (OPTR) from $0100 to $1EFE. The OPTR and the EEPROM Control/E-Clock Register ($0007) have been changed to support EPROM programming instead of EEPROM. The watchdog timer has been changed to include some additional options.

Many resources on the MC68HC705B16 have been implemented exactly as on the MC68HC806B6. Some resources have been changed, and several new features have been added that are not found on the MC68HC805B6. The following is a detailed comparison of the two devices, with a specific emphasis on those subsystems that are different. In addition, any considerations that apply to converting from the MC68HC705B16 to a mask ROM (MROM) device, such as the MC68HC05B6, will be addressed.

SYSTEM OVERVIEW

The MC68HC805B6 is a high-density complementary metal-oxide semiconductor (HCMOS), single-chip, 8-bit microcontroller based on the Motorola M68HC05 CPU. The on-chip resources of this part include:

- Fully static operation
- On-chip oscillator
- Power-saving modes: STOP, WAIT, and SLOW
- 176 bytes of random access memory (RAM)
- 5952 bytes of EEPROM for user program
- 256 bytes of byte-erasable EEPROM
  - — Internal charge pump
  - — Write/erase protect bit for 224 of these bytes
- 24 bidirectional Input/Output (I/O) lines
- 16-bit free-running counter
  - — Two input capture systems
  - — Two output compare systems
  - — Software force compare
  - — Software reset of main counter
- 8-channel, 8-bit analog to digital (A/D) converter
- Two pulse length modulation (PLM) digital to analog (D/A) converters
- Asynchronous serial communications interface (SCI)
  - — Programmable prescaler
  - — Transmitter clock output for synchronous transmissions
- External, timer, and SCI interrupts
- E-Clock output option
- Power-on reset (POR) bit to determine reset source

The MC68HC705B16 is actually an MC68HC705X16 device packaged to be compatible with the MC68HC(8)05Bx family of MCUs. This device is normally packaged in a 64-pin plastic-leaded chip carrier (PLCC) or ceramic-leaded chip carrier (CLCC) package, and contains a controller area network (CAN) interface. The CAN interface is not bonded out when the MC68HC705X16 is assembled as an MC68HC705B16.

The MC68HC705X16 supports all resources listed above, but there are several changes that must be noted, as well as additional resources not found on the MC68HC805B6. Please note that the CAN interface is not available for use in the MC68HC705B16, but must be considered in the design migration.

The MC68HC705B16 has 352 bytes of RAM, instead of the 176 bytes found in the MC68HC805B6. The 6-Kbyte EEPROM user memory space has been replaced with a 16-Kbyte EPROM array. Ports B and C have programmable pull-down resistor options. Port B can also be configured as a wired-OR interrupt (WOI) source. These additional resources are certainly available for use, but if the ultimate goal is to use an MROM device, care must be taken ensure that only those resources that are found on the target device are used.

CPU-RELATED CONSIDERATIONS

The resources provided by the MC68HC805B6 and the MC68HC705B16 must be carefully compared to determine what changes must be made to ensure that the system will function as desired. The first resource to consider is the MC68HC705B16 CPU. In the MC68HC805B6, the address space is limited to an 8-Kbyte range. Only 12 internal address lines were implemented, and the upper 3 bits of the 16-bit program counter (PC) were always read as "0". The address space in the MC68HC705B16 has been increased to 16 Kbytes. An additional address line was required, and the PC now has 13 active bits. The result of this change is that the MC68HC705B16 User Vector Table is located from **$3FF2 to $3FFF.** (See **User Vector Table** subheading.) **The increased memory space also has another significant effect. The development tools used to support the MC68HC805B6 do not support development of the MC68HC705B16.** (See **Emulation Concerns** subheading.)

Most of the differences between the MC68HC805B6 and the MC68HC705B16 are enhancements. Other differences include changes required by the conversion from EEPROM-based user memory to EPROM-based. The on-chip resources and the changes will now be discussed in a memory map sequence, beginning at $0000.

PARALLEL I/O

The I/O port data registers (PORTx) and the port data direction registers (DDRx) are at the same address locations ($0000–$0006) and serve the same functions. What has changed is added flexibility to Port B and Port C. These ports, when configured as inputs, now have a selectable pull-down feature. These pull-downs are selected by programming bits 0 and 1 in the Mask Option Register (MOR) located at $3DFE. When enabled, a resistive pull-down is applied to any selected port pins that are configured as inputs. The pull-downs provide a sink capability of about 80 μA (62.5 kΩ), compared to the normal port input current of 1.0 μA (5 MΩ). Port B also has been enhanced with the capability to interrupt the CPU. This port now can be configured as a WOI source. This feature is also selected by programming bit 7 (WOI) in the MOR, and enabled by bit 7 (wired-OR interrupt enable (WOIE)) of the EPROM/EEPROM/ECLK Control Register located at $0007.

EEPROM/E-CLOCK CONTROL REGISTER

The EEPROM/ECLK Control Register is still located at $0007, but has been renamed the EPROM/ EEPROM/ECLK Control Register. The bits formerly associated with control and programming of the user EEPROM space in the MC68HC805B6 now have new functions. Bit 7 was E6BW, and is now WOIE as noted above. Bit 6, which was E6ERA, is currently not activated and is always read as "0".

A/D, PLM, SCI, AND TIMERS

The control, data, and status registers for the A/D converter, PLM D/A converter, SCI, and timer systems on the MC68HC705B16 are identical to those found on the MC68HC805B6, and do not require any changes in the system design. Additionally, there are no changes in the Miscellaneous Register. Addresses for these registers are $0008 to $001F.

PAGE 0 USER EEPROM 6

The Page 0 user EEPROM from $0020 to $004F has been replaced with EPROM. There should be no changes required in the system design.

RANDOM ACCESS MEMORY (RAM)

The RAM area from $0050 to $00FF has been renamed RAM1. There should be no changes required in the system design.

OPTION REGISTER

The Option register (OPTR) at $0100 has been renamed EEPROM Options register. There should be no changes required in the system design.

EEPROM 1

The EEPROM 1 area from $0101 to $01FF has been renamed EEPROM. There should be no changes required in the system design.

BOOTSTRAP ROM I

The Bootstrap ROM I area from $0200 to $027F has been reduced to 80 bytes ($0200 to $024F). There should be no changes required in the system design.

UNUSED

The Unused area from $0280 to $07FF has been replaced with RAM II from $0250 to $02FF. This area is available for use; however, care must be taken to exclude this area when an MROM device is planned. There should be no other changes required in the system design.

USER EEPROM 6

The EEPROM 6 area from $0800 to $1EFF has been replaced with EPROM from $0300 to $3DFD. The additional user memory space is available for use; however, care must be taken to use only valid memory space when an MROM device is planned. There should be no other changes required in the system design.

BOOTSTRAP ROM II

The Bootstrap ROM II area from $1F00 to $1FEF has been moved, and is now located from $3E00 to $3FEF. There should be no changes required in the system design.

USER VECTOR TABLE

The User Vector Table from $1FF2 to $1FFF has been moved, and is now located from $3FF2 to $3FFF. One simple solution is to place the User Vector Table in **both** locations. If the goal is a reduced user memory space MROM device, the User Vector Table for the MC68HC705B16 should be removed in the final version of the code.

ADDITIONAL CONSIDERATIONS

The MC68HC705B16 has an additional control register, the Mask Option Register (MOR). The MOR is used to select options that are available in the MROM devices. This register is located at $3DFE. Bit 7 (WOI) is used to control the wired-OR feature of Port B. Bits 6 and 5 are not used. Bit 4 (RTIM) is used to control the reset start-up time for the oscillator, either 16 or 4096 clock cycles. Bit 3 (RWAT) controls the function of the watchdog timer after reset. The COP can be set to be enabled immediately out of reset, or to be enabled under program control. Bit 2 (WWAT) controls the function of the watchdog timer during wait mode. The timer can be disabled or enabled during wait by this bit. Bits 1 and 0 control the pull-down option for Ports B and C.

As stated earlier, the MC68HC705B16 contains a CAN interface. There is a problem with the existing versions of this device that occasionally allows the CAN module to be enabled after reset. Although this event is rare, it is advisable to compensate for this problem by including a CAN interrupt service routine in the user software. The CAN interrupt vector is located from $3FF0 to $3FF1. The suggested method is to cause a watchdog reset after a CAN interrupt occurs. The system will then restart, and the CAN module should now be disabled. For example:

```
        ORG  $2000
CANIRQ      BSET 0,$0C  Enable Watchdog
            STOP        Cause Watchdog reset to occur
        ORG  $3FF0
        FDB  CANIRQ
```

This code stub should probably be placed in the upper part of the user program space, above the $1FFF location, making it easier to remove for migration back to an MROM device. Also, the CANIRQ vector should be removed at this time.

EMULATION CONCERNS

Another major issue when migrating to the MC68HC705B16 is in development system requirements. The M68HC05EVM and the M68CDS8HC05 that currently support the MC68HC805B6 do not readily support development of the MC68HC705B16. This includes programming functions as well as in-circuit emulation. It is necessary to use an M68HC05X16EVS, or an M68MMDS05 with an M68HC05X16EM installed, to support the changes in the memory map and resource set. Cables currently used with the M68HC05EVM to support the MC68HC805B6FN can be used with the M68HC05X16EVS or the M68MMDS05. Cables used with the M68CDS8HC05 cannot be used. Neither the M68HC05X16EVS nor the M68MMDS05 support device programming. Programming the MC68HC705B16 is only supported on the M68HC05BPGMR. The M68HC05BPGMR supports both parallel and serial programming modes. The current versions of the MC68HC705B16 require +15.5 volts for programming. Attempts to use any other programming solutions previously used with the MC68HC805B6 will be unsuccessful. However, accidentally attempting to do so will not damage the devices. The V_{PP6} pin is a "no connect" on the MC68HC705B16, so application of the normal programming voltage used with the MC68HC805B6 has no effect on the MC68HC705B16.

EMC AND THERMAL PERFORMANCE

The technology used in the production of the MC68HC805B6 is significantly different than that used in the MC68HC705B16. The device geometries used in the MC68HC705B16 are much smaller than those used in the MC68HC806B6. The EPROM with EEPROM manufacturing process required for the MC68HC705B16 is also very different from the EEPROM-only process used for the MC68HC805B6. The MC68HC705B16 exhibits much faster switching times, and responds to faster input signals. There is a significant difference in system radio frequency (RF) performance when using the MC68HC705B16. The user must take appropriate steps to compensate for the faster MC68HC705B16 in systems where electromagnetic compatibility (EMC) is required. However, the MC68HC705B16 performs more like an MROM device than the MC68HC805B6.

The die size of the MC68HC705B16 is different than that of the MC68HC805B6. The difference in die size and the change from EEPROM to EPROM causes different thermal performance between the MC68HC705B16 and the MC68HC805B6. There should be a net improvement in overall thermal performance with the MC68HC705B16.

SUMMARY

Applications currently using the MC68HC805B6 can also take advantage of the additional resources found on the MC68HC705B16. The only current drawback is the availability of window EPROM devices, which would allow reprogramming. At this time, only one-time programmable (OTP) devices are available. Window EPROM devices should be available later this year (1993). The MC68HC705B16FN devices should be available at the same or lower cost as the MC68HC805B6FN.

Applications that will eventually migrate to MROM devices can be successfully developed on the MC68HC705B16. Care must be taken to limit the resource usage to those actually found on the desired MROM device (i.e.: MC68HC05B4, MC68HC05B6, MC68HC05B8, etc.). Final versions of the user code must be changed to ramp the user reset vectors and remove the CAN interrupt support.

Migration from the MC68HC805B6 to the MC68HC705B16 can be a very simple operation. The only changes that are absolutely necessary in the user software are to define the values needed to program the MOR correctly, duplicate the User Vector Table from $3FF2 to $3FFF, and add the CAN interrupt service routine. Making these additions exactly as recommended allows the user to program either the previously used MC68HC805B6 devices or the new MC68HC705B16 devices.

Literature Distribution Centers:
USA: Motorola Literature Distribution; P.O. Box 20912; Phoenix, Arizona 85036.
EUROPE: Motorola Ltd.; European Literature Centre; 88 Tanners Drive, Blakelands, Milton Keynes, MK14 5BP, England.
JAPAN: Nippon Motorola Ltd.; 4-32-1, Nishi-Gotanda, Shinagawa-ku, Tokyo 141, Japan.
ASIA PACIFIC: Motorola Semiconductors H.K. Ltd.; Silicon Harbour Center, No. 2 Dai King Street, Tai Po Industrial Estate, Tai Po, N.T., Hong Kong.

MOTOROLA

1ATX31468-0 PRINTED IN USA (12/93) MPS 68131 2000 MUC YGACAA

EB166/D