

## TOSHIBA MOS DIGITAL INTEGRATED CIRCUIT SILICON GATE CMOS

### 262,144-WORD BY 16-BIT STATIC RAM DESCRIPTION

The TC554161AFTI is a 4,194,304-bit static random access memory (SRAM) organized as 262,144 words by 16 bits. Fabricated using Toshiba's CMOS Silicon gate process technology, this device operates from a single 5 V  $\pm$  10% power supply. Advanced circuit technology provides both high speed and low power at an operating current of 10 mA/MHz (typ) and a minimum cycle time of 70 ns. It is automatically placed in low-power mode at 2  $\mu$ A standby current (typ) when chip enable ( $\overline{CE}$ ) is asserted high. There are two control inputs.  $\overline{CE}$  is used to select the device and for data retention control, and output enable ( $\overline{OE}$ ) provides fast memory access. Data byte control pin ( $\overline{LB}$ ,  $\overline{UB}$ ) provides lower and upper byte access. This device is well suited to various microprocessor system applications where high speed, low power and battery backup are required. And, with a guaranteed operating extreme temperature range of  $-40^{\circ}$  to  $85^{\circ}$ C, the TC554161AFTI can be used in environments exhibiting extreme temperature conditions. The TC554161AFTI is available in a plastic 54-pin thin-small-outline package (TSOP).

### FEATURES

- Low-power dissipation  
Operating: 55 mW/MHz (typical)
- Single power supply voltage of 5 V  $\pm$  10%
- Power down features using  $\overline{CE}$ .
- Data retention supply voltage of 2 to 5.5 V
- Direct TTL compatibility for all inputs and outputs
- Wide operating temperature range of  $-40^{\circ}$  to  $85^{\circ}$ C
- Standby Current (maximum) :

	TC554161AFTI	
	-70,-85,-10	-70L,-85L,-10L
5.5V	200 $\mu$ A	100 $\mu$ A
3.0V	100 $\mu$ A	50 $\mu$ A

- Access Times (maximum):

	TC554161AFTI		
	-70,-70L	-85,-85L	-10,-10L
Access Time	70 ns	85 ns	100 ns
$\overline{CE}$ Access Time	70 ns	85 ns	100 ns
$\overline{OE}$ Access Time	35 ns	45 ns	50 ns

- Package:  
TSOP II 54-P-400-0.80 (AFTI) (Weight: 0.57 g typ)

### PIN ASSIGNMENT (TOP VIEW)

NC	1	54	A4
A3	2	53	A5
A2	3	52	A6
A1	4	51	A7
A0	5	50	NC
I/O16	6	49	I/O1
I/O15	7	48	I/O2
V <sub>DD</sub>	8	47	V <sub>DD</sub>
GND	9	46	GND
I/O14	10	45	I/O3
I/O13	11	44	I/O4
$\overline{UB}$	12	43	$\overline{LB}$
$\overline{CE}$	13	42	$\overline{OE}$
OP	14	41	OP
R/W	15	40	NC
I/O12	16	39	I/O5
I/O11	17	38	I/O6
GND	18	37	GND
V <sub>DD</sub>	19	36	V <sub>DD</sub>
I/O10	20	35	I/O7
I/O9	21	34	I/O8
NC	22	33	A8
A17	23	32	A9
A16	24	31	A10
A15	25	30	A11
A14	26	29	A12
A13	27	28	NC

(Normal pinout)

### PIN NAMES

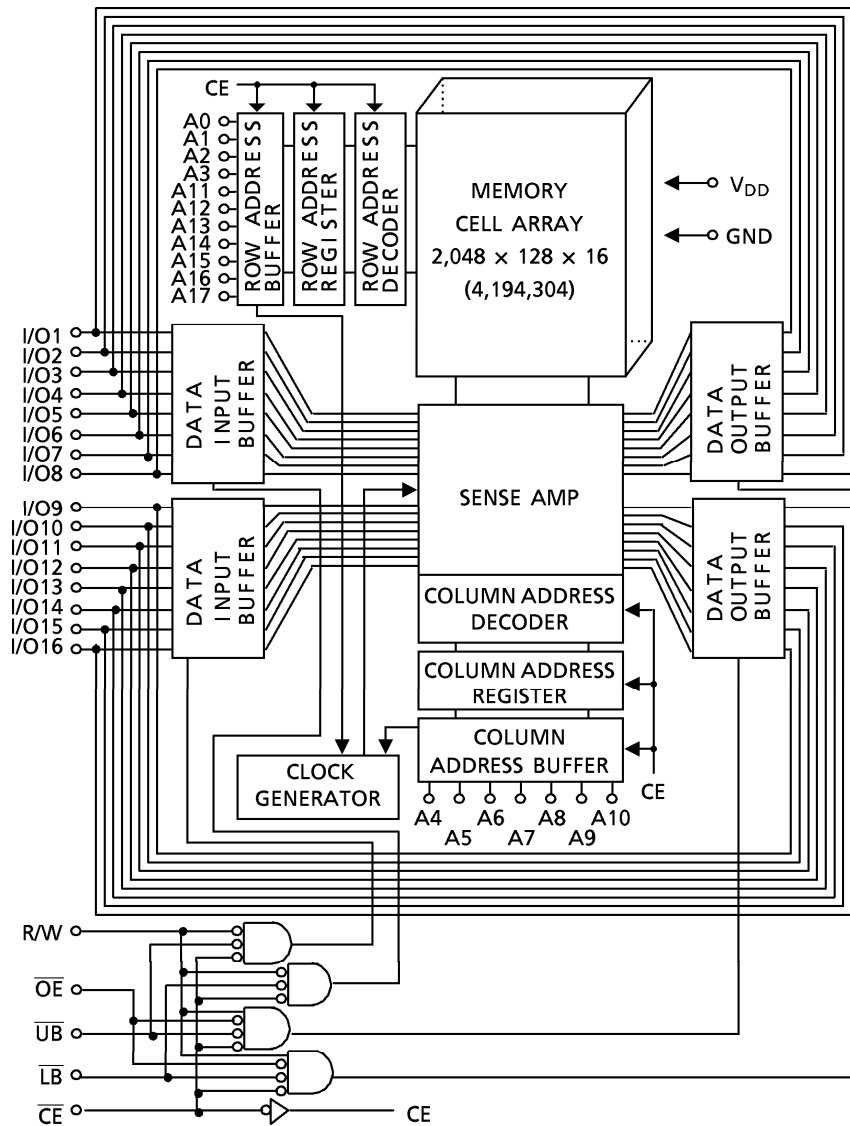
A0 to A17	Address Inputs
I/O1 to I/O16	Data Inputs/Outputs
$\overline{CE}$	Chip Enable
R/W	Read/Write Control
$\overline{OE}$	Output Enable
$\overline{LB}$ , $\overline{UB}$	Data Byte Control
V <sub>DD</sub>	Power (+ 5 V)
GND	Ground
NC	No Connection
OP*	Option

\*: OP pin must be open or connected to GND.

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**BLOCK DIAGRAM**



**MAXIMUM RATINGS**

SYMBOL	RATING	VALUE	UNIT
V <sub>DD</sub>	Power Supply Voltage	- 0.3 to 7.0	V
V <sub>IN</sub>	Input Voltage	- 0.3 * to 7.0	V
V <sub>I/O</sub>	Input/Output Voltage	- 0.5 to V <sub>DD</sub> + 0.5	V
P <sub>D</sub>	Power Dissipation	0.6	W
T <sub>solder</sub>	Soldering Temperature (10 s)	260	°C
T <sub>strg</sub>	Storage Temperature	- 55 to 150	°C
T <sub>opr</sub>	Operating Temperature	- 40 to 85	°C

\* - 3.0 V when measured at a pulse width of 30 ns

**DC RECOMMENDED OPERATING CONDITIONS (Ta = -40° to 85°C)**

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
V <sub>DD</sub>	Power Supply Voltage	4.5	5.0	5.5	V
V <sub>IH</sub>	Input High Voltage	2.4	-	V <sub>DD</sub> + 0.3	V
V <sub>IL</sub>	Input Low Voltage	- 0.3 *	-	0.6	V
V <sub>DH</sub>	Data Retention Supply Voltage	2.0	-	5.5	V

\* - 3.0 V when measured at a pulse width of 30 ns

**DC CHARACTERISTICS (Ta = -40° to 85°C, V<sub>DD</sub> = 5 V ± 10%)**

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT		
I <sub>IL</sub>	Input Leakage Current	V <sub>IN</sub> = 0 V to V <sub>DD</sub>	-	-	± 1.0	μA		
I <sub>LO</sub>	Output Leakage Current	$\overline{CE} = V_{IH}$ or R/W = V <sub>IL</sub> or $\overline{OE} = V_{IH}$ V <sub>OUT</sub> = 0 V to V <sub>DD</sub>	-	-	± 1.0	μA		
I <sub>OH</sub>	Output High Current	V <sub>OH</sub> = 2.4 V	- 1.0	-	-	mA		
I <sub>OL</sub>	Output Low Current	V <sub>OL</sub> = 0.4 V	2.1	-	-	mA		
I <sub>DDO 1</sub>	Operating Current	$\overline{CE} = V_{IL}$ R/W = V <sub>IH</sub> , I <sub>OUT</sub> = 0 mA Other Inputs = V <sub>IH</sub> /V <sub>IL</sub>	Tcycle	70 ns	-	-	110	mA
				85 ns, 100 ns	-	-	100	
				1 μs	-	15	-	
I <sub>DDO 2</sub>	Operating Current	$\overline{CE} = 0.2 V$ R/W = V <sub>DD</sub> - 0.2 V, I <sub>OUT</sub> = 0 mA Other Inputs = V <sub>DD</sub> - 0.2 V/0.2 V	Tcycle	70 ns	-	-	100	mA
				85 ns, 100 ns	-	-	90	
				1 μs	-	10	-	
I <sub>DDS 1</sub>	Standby Current	$\overline{CE} = V_{IH}$		-	-	3	μA	
I <sub>DDS 2</sub>		$\overline{CE} = V_{DD} - 0.2 V$	-70, -85, -10	Ta = 25°C	-	2		-
				Ta = -40° to 85°C	-	-		200
		V <sub>DD</sub> = 2.0 to 5.5 V	-70L, -85L, -10L	Ta = 25°C	-	2		5
			Ta = -40° to 85°C	-	-	100		

**CAPACITANCE (Ta = 25°C, f = 1 MHz)**

SYMBOL	PARAMETER	TEST CONDITION	MAX	UNIT
C <sub>IN</sub>	Input Capacitance	V <sub>IN</sub> = GND	10	pF
C <sub>OUT</sub>	Output Capacitance	V <sub>OUT</sub> = GND	10	pF

Note: This parameter is periodically sampled and is not 100% tested.

**OPERATING MODE**

MODE	$\overline{CE}$	$\overline{OE}$	R/W	LB	UB	I/O1 to I/O8	I/O9 to I/O16	POWER
Read	L	L	H	L	L	Output	Output	I <sub>DDO</sub>
				H	L	High-Z	Output	I <sub>DDO</sub>
				L	H	Output	High-Z	I <sub>DDO</sub>
Write	L	x	L	L	L	Input	Input	I <sub>DDO</sub>
				H	L	High-Z	Input	I <sub>DDO</sub>
				L	H	Input	High-Z	I <sub>DDO</sub>
Output Deselect	L	H	H	x	x	High-Z	High-Z	I <sub>DDO</sub>
	L	x	x	H	H			
Standby	H	x	x	x	x	High-Z	High-Z	I <sub>DDS</sub>

x = don't care  
H = logic high  
L = logic low

**AC CHARACTERISTICS AND OPERATING CONDITIONS (Ta = -40° to 85°C, V<sub>DD</sub> = 5 V ± 10%)**

**READ CYCLE**

SYMBOL	PARAMETER	TC554161AFTI						UNIT
		-70, -70L		-85, -85L		-10, -10L		
		MIN	MAX	MIN	MAX	MIN	MAX	
t <sub>RC</sub>	Read Cycle Time	70	-	85	-	100	-	ns
t <sub>ACC</sub>	Address Access Time	-	70	-	85	-	100	
t <sub>CO</sub>	Chip Enable Access Time	-	70	-	85	-	100	
t <sub>OE</sub>	Output Enable Access Time	-	35	-	45	-	50	
t <sub>BA</sub>	Data Byte Control Access Time	-	35	-	45	-	50	
t <sub>OH</sub>	Output Data Hold Time	10	-	10	-	10	-	
t <sub>COE</sub>	Chip Enable Low to Output Active	5	-	5	-	5	-	
t <sub>OEE</sub>	Output Enable Low to Output Active	0	-	0	-	0	-	
t <sub>BE</sub>	Data Byte Control Low to Output Active	0	-	0	-	0	-	
t <sub>OD</sub>	Chip Enable High to Output High-Z	-	30	-	35	-	40	
t <sub>ODO</sub>	Output Enable High to Output High-Z	-	30	-	35	-	40	
t <sub>BD</sub>	Data Byte Control High to Output High-Z	-	30	-	35	-	40	

**WRITE CYCLE**

SYMBOL	PARAMETER	TC554161AFTI						UNIT
		-70, -70L		-85, -85L		-10, -10L		
		MIN	MAX	MIN	MAX	MIN	MAX	
t <sub>WC</sub>	Write Cycle Time	70	-	85	-	100	-	ns
t <sub>WP</sub>	Write Pulse Width	50	-	55	-	60	-	
t <sub>CW</sub>	Chip Enable to End of Write	60	-	70	-	80	-	
t <sub>BW</sub>	Data Byte Control to End of Write	50	-	55	-	60	-	
t <sub>AS</sub>	Address Setup Time	0	-	0	-	0	-	
t <sub>WR</sub>	Write Recovery Time	0	-	0	-	0	-	
t <sub>DS</sub>	Data Setup Time	30	-	35	-	40	-	
t <sub>DH</sub>	Data Hold Time	0	-	0	-	0	-	
t <sub>OEW</sub>	R/W High to Output Active	0	-	0	-	0	-	
t <sub>ODW</sub>	R/W Low to Output High-Z	-	30	-	35	-	40	

**AC TEST CONDITIONS**

Output load: 100 pF + one TTL gate

Input pulse level: 0.4 V, 2.6 V

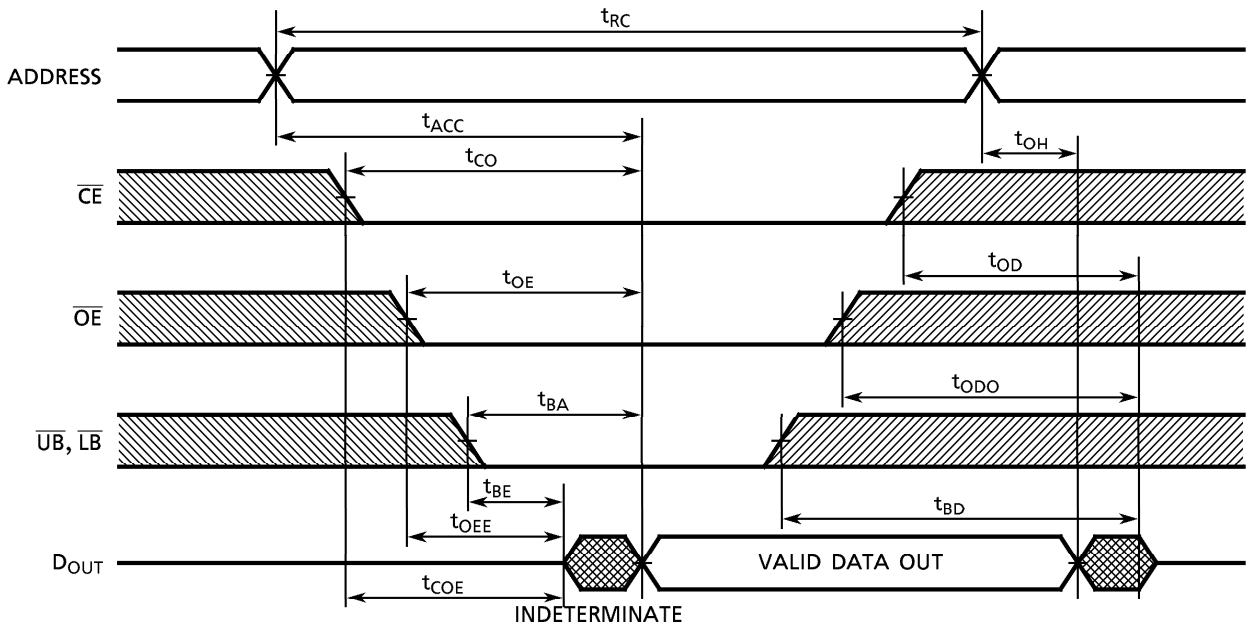
Timing measurements: 1.5 V

Reference level: 1.5 V

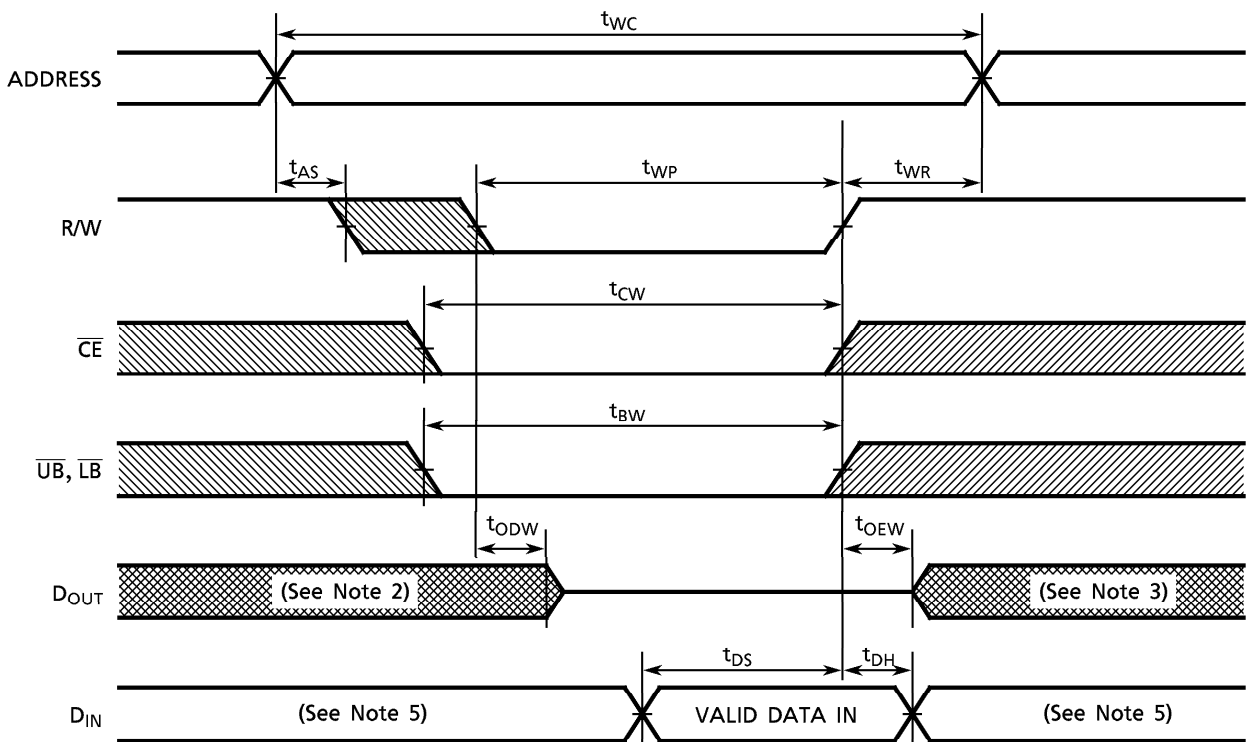
t<sub>R</sub>, t<sub>F</sub>: 5 ns

**TIMING DIAGRAMS**

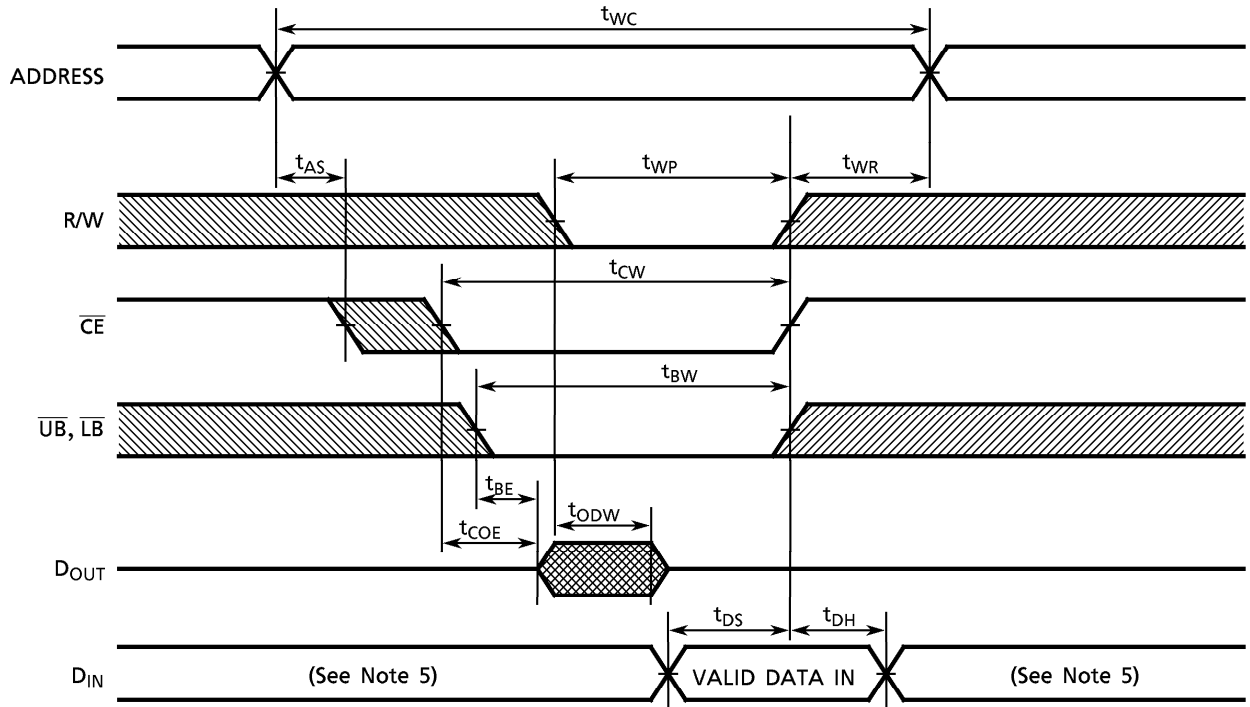
**READ CYCLE (See Note 1)**



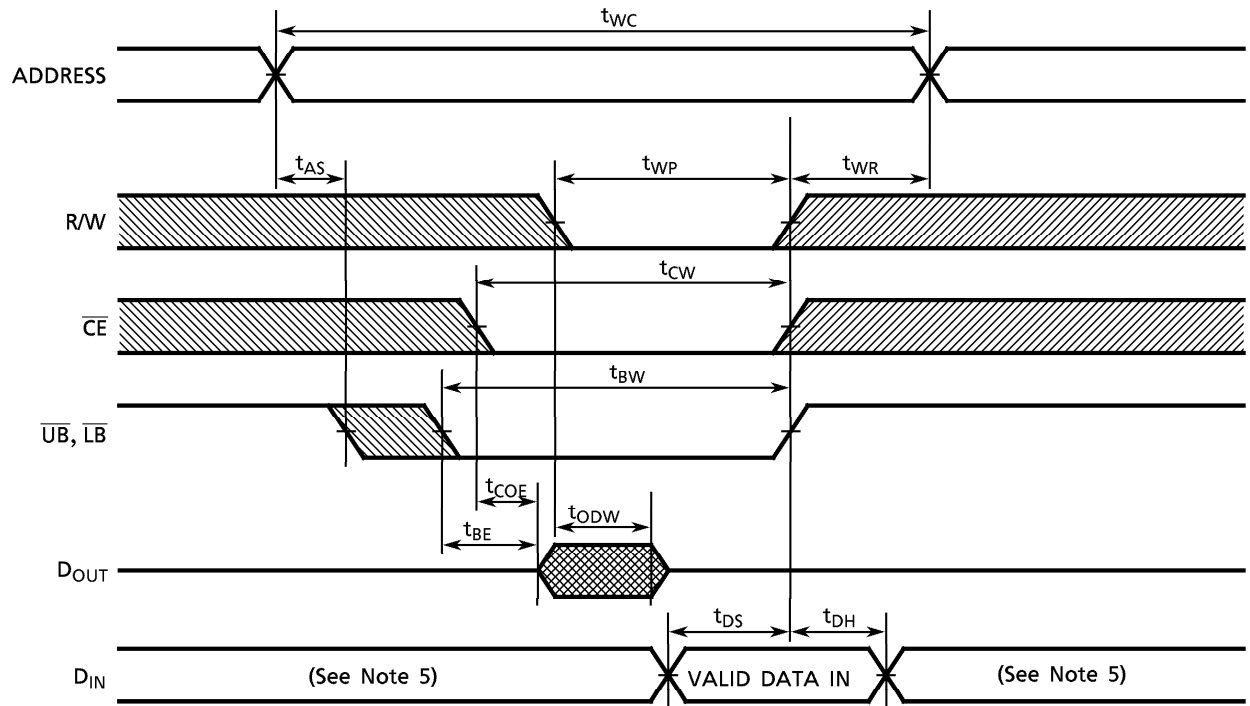
**WRITE CYCLE 1 (R/W CONTROLLED) (See Note 4)**



WRITE CYCLE 2 ( $\overline{\text{CE}}$  CONTROLLED) (See Note 4)



WRITE CYCLE 3 ( $\overline{\text{UB}}, \overline{\text{LB}}$  CONTROLLED) (See Note 4)



Note: (1) R/W remains HIGH for the read cycle.

(2) If  $\overline{CE}$  goes LOW coincident with or after R/W goes LOW, the outputs will remain at high impedance.

(3) If  $\overline{CE}$  goes HIGH coincident with or before R/W goes HIGH, the outputs will remain at high impedance.

(4) If  $\overline{OE}$  is HIGH during the write cycle, the outputs will remain at high impedance.

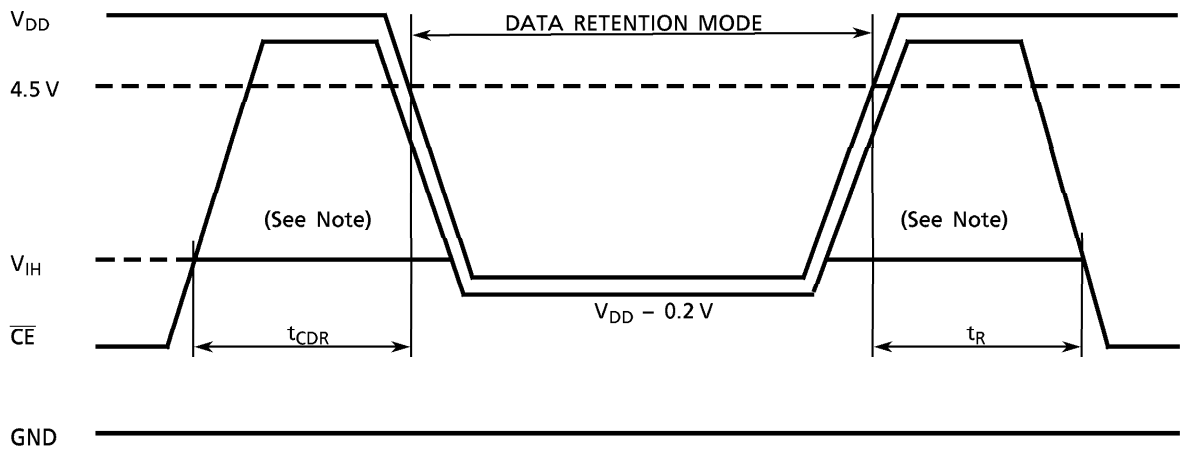
(5) Because I/O signals may be in the output state at this time, input signals of reverse polarity must not be applied.

**DATA RETENTION CHARACTERISTICS (Ta = -40° to 85°C)**

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	
V <sub>DH</sub>	Data Retention Supply Voltage	2.0	-	5.5	V	
I <sub>DDS2</sub>	Standby Current	V <sub>DH</sub> = 3.0 V	-	-	100	μA
		V <sub>DH</sub> = 5.5 V	-	-	200	
		V <sub>DH</sub> = 3.0 V	-	-	50*	
		V <sub>DH</sub> = 5.5 V	-	-	100	
t <sub>CDR</sub>	Chip Deselect to Data Retention Mode Time	0	-	-	ns	
t <sub>R</sub>	Recovery Time	5	-	-	ms	

\* 5μA (max) at Ta = -40° to 40°C

**CE CONTROLLED DATA RETENTION MODE**

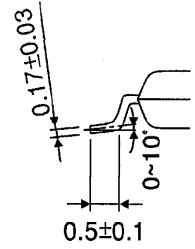
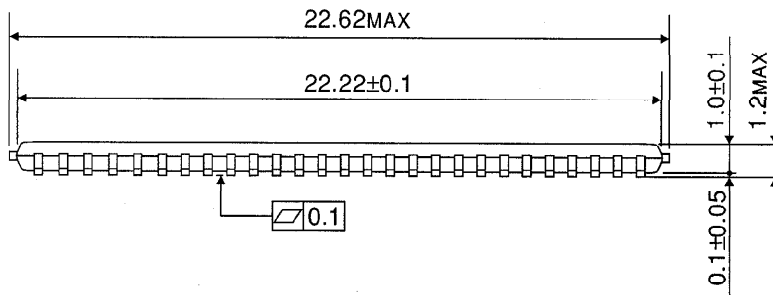
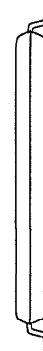
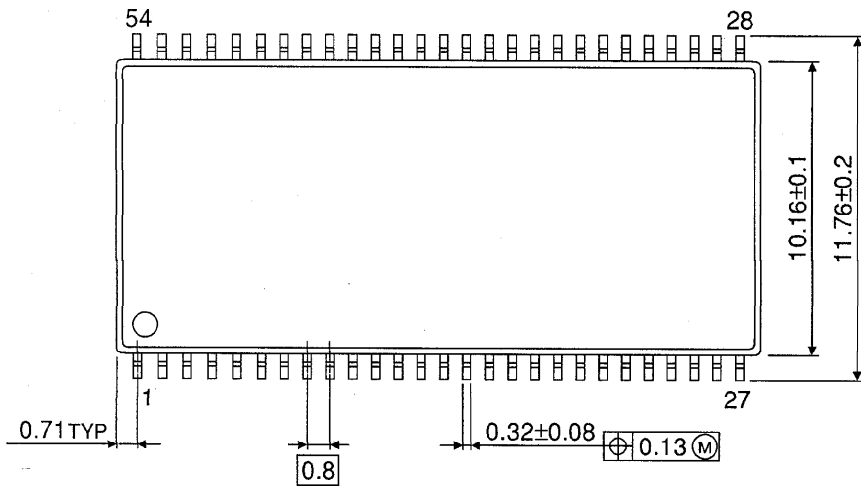


Note: When  $\overline{CE}$  is operating at the V<sub>IH</sub> level (2.4 V), the standby current is given by I<sub>DDS1</sub> during the transition of V<sub>DD</sub> from 4.5 to 2.6 V.



**PACKAGE DIMENSIONS (TSOPII 54-P-400-0.80)**

Units in mm



Weight: 0.57 g (typ)