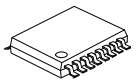
U74HCT595

CMOS IC

8-BIT SHIFT REGISTERS WITH LATCHED 3-STATE OUTPUT REGISTERS



TSSOP-16

■ DESCRIPTION

The UTC **74HCT595** contains an 8-bit register with asynchronous reset input and an 8-bit latch with output enable input. Data on the Serial Data Input (SER) will be shift into the internal shift register during every LOW-to-HIGH transition on the Shift Clock. The latch will latch the 8-bit data from the shift register during the LOW-to-HIGH transition on the Latch Clock. The shift register also provides a serial output.

■ FEATURES

* Operation Voltage Range:4.5V~5.5V
* High Noise Immunity
* Output Compatibility with CMOS and TTL
* 8-Bit Serial-In,Parallel-Out Shift
* Inputs are TTL voltage compatiable

■ ORDERING INFORMATION

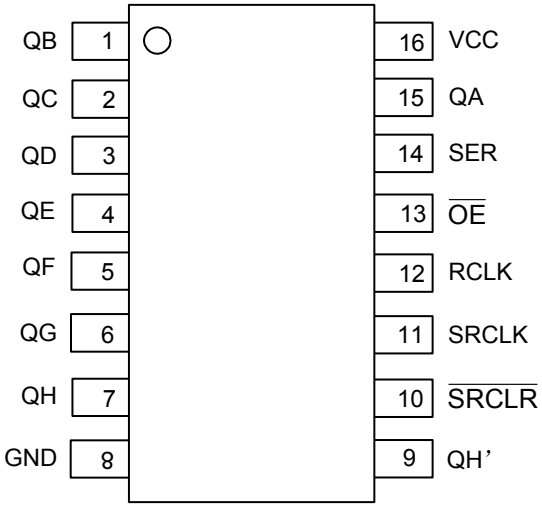
Ordering Number		Package	Packing
Lead Free	Halogen Free		
U74HCT595L-P16-R	U74HCT595G-P16-R	TSSOP-16	Tape Reel
U74HCT595L-P16-T	U74HCT595G-P16-T	TSSOP-16	Tube

U74HCT595L-P16-R

(1) Packing Type
(2) Package Type
(3) Lead Free

(1) R: Tape Reel, T: Tube
(2) P16: TSSOP-16
(3) G: Halogen Free, L: Lead Free

■ PIN CONFIGURATION

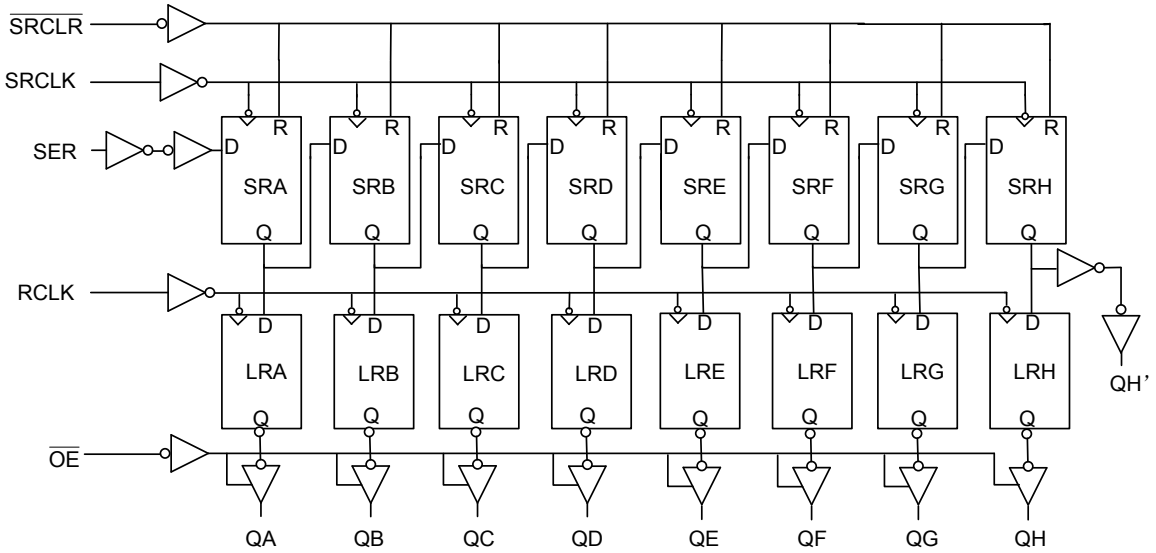


■ FUNCTION TABLE

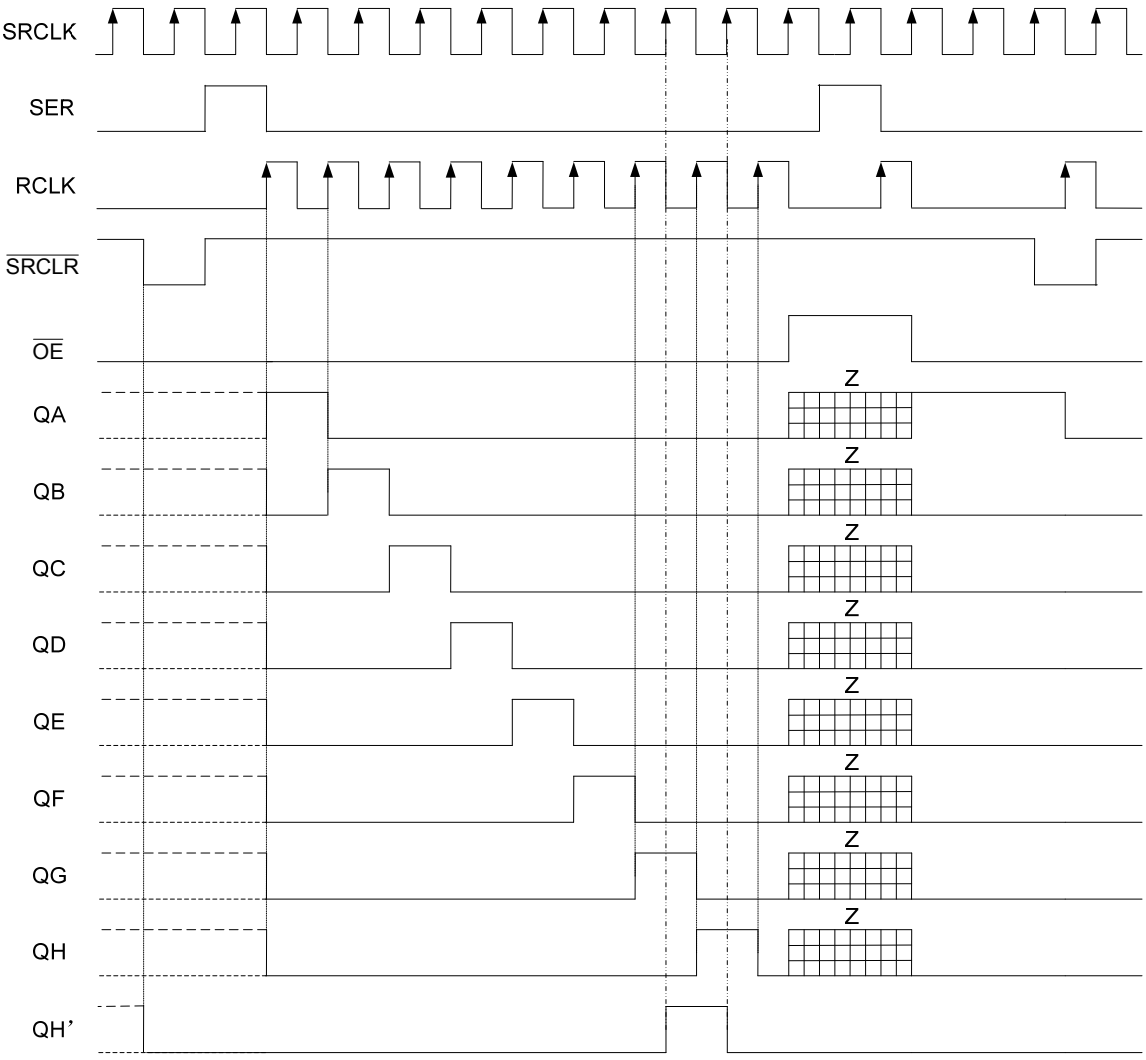
FUNCTION	INPUTS					OUTPUTS	
	SRCLK	RCLK	$\overline{OE}$	$\overline{SRCLR}$	SER	QH'	Qn
A Low-Level on $\overline{SRCLR}$ only affects the shift registers.	X	X	L	L	X	L	NC
Empty shift register loaded into storage register.	X	↑	L	L	X	L	L
Shift register clear. Parallel outputs in high-impedance OFF-state	X	X	H	L	X	L	Z
Logic high level shifted into the first shift register. Contents of all shift register stages shifted through, e.g. previous state of stage G(internal QG') appears on the serial output(QH').	↑	X	L	H	H	QG'	NC
Contents of shift register stages (internal Qn') are transferred to the storage register and parallel output stages.	X	↑	L	H	X	NC	Qn'
Contents of shift register shifted through. Previous contents of the shift register is transferred to the storage register and the parallel output stages.	↑	↑	L	H	X	QG'	Qn'

Note:H : HIGH voltage level.
L : LOW voltage level.
X : Don't care.
Z : High impedance OFF-state.
NC: No change.
↑ : Low-to-High transition.
↓ : High-to-Low transition.

■ LOGIC DIAGRAM



■ TIMING DIAGRAM



■ ABSOLUTE MAXIMUM RATING(unless otherwise specified)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V_{CC}	-0.5~7.0	V
Input Voltage	V_{IN}	-0.5~Vcc+0.5	V
Output Voltage(active mode)	V_{OUT}	-0.5~V_{CC}+0.5	V
Input Clamp Current (V_{iN}<0)	I_{IK}	±20	mA
Output Clamp Current (V_{OUT}<0)	I_{OK}	±20	mA
Output Current	I_{OUT}	±35	mA
V_{CC} or GND Current	I_{CC}	±70	mA
Storage Temperature	T_{STG}	-65 ~ +150	°C

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

■ RECOMMENDED OPERATING COMDITIONS

PARAMETER		SYMBOL	MIN	TYP	MAX	UNIT
Supply Voltage		V_{CC}	4.5	5	5.5	V
Input Voltage		V_{IN}	0		V_{CC}	V
Output Voltage		V_{OUT}	0		V_{CC}	V
Operating Temperature		T_{OPR}	-40		85	°C
Input Transition Rise or Fall Rate	V_{CC} =4.5V	t_R/t_F		6.0	500	ns

■ ELECTRICAL CHARACTERISTICS(T_a=25°C, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
High-Level input voltage	V_{IH}	V_{CC}=4.5V~5.5V	2.0	1.6		V
Low-Lever output voltage	V_{IL}	V_{CC}=4.5V~5.5V		1.2	0.8	V
High-Level Output Voltage,QA-QH	V_{OH}	V_{CC}=4.5V, I_{OH}=-20μA	4.4	4.499		V
		V_{CC}=4.5V, I_{OH}=-6mA	3.98	4.3		V
Low-Level Output Voltage,QA-QH	V_{OL}	V_{CC}=4.5V, I_{OL}=20μA		0.001	0.1	V
		V_{CC}=4.5V, I_{OH}=6mA		0.17	0.26	V
High-Level Output Voltage,QH'	V_{OH}	V_{CC}=4.5V, I_{OH}=-20μA	4.4	4.499		V
		V_{CC}=4.5V, I_{OH}=-4mA	3.98	4.3		V
Low-Level Output Voltage,QH'	V_{OL}	V_{CC}=4.5V, I_{OL}=20μA		0.001	0.1	V
		V_{CC}=4.5V, I_{OH}=4mA		0.17	0.26	V
Input Leakage Current	$I_{I(LEAK)}$	V_{CC}=5.5V, V_{IN}=V_{CC} or GND		±0.1	±100	nA
Output OFF -state current	I_{OZ}	V_{CC}=5.5V, V_{OUT}=V_{CC} or GND		±0.01	±0.5	μA
Quiescent Supply Current	I_{CC}	V_{CC}=5.5V, V_{IN}=V_{CC} or GND, I_{OUT}=0			8	μA
Additional Quiescent Supply Current	△I_{CC}	One input at V_{CC} -2.1V,other inputs at 0 or V_{CC}		100	450	uA
Input Capacitance	C_{IN}	V_{CC}=5.5V, V_{IN}=V_{CC} or GND		3	10	pF

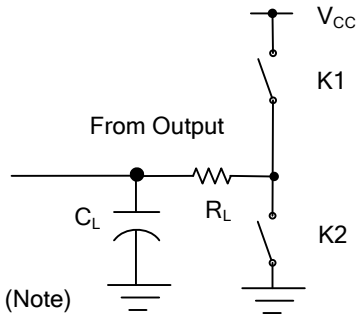
■ DYNAMIC CHARACTERISTICS(T_a=25°C, CL=50pF,RL=1kΩ,unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Maximum clock pulse frequency	$f_{(MAX)}$	V_{CC}=4.5V	30	52		MHz
Propagation delay from input (RCLK) to output(Qn)	t_{PHL}/t_{PLH}	V_{CC}=4.5V		24	40	ns
Propagation delay from input (SRCLK) to output(QH')	t_{PLH}/t_{PHL}	V_{CC}=4.5V		24	42	ns
3-state output enable time from input ($\overline{OE}$) to output(Qn)	t_{PZH}/t_{PZL}	V_{CC}=4.5V		21	35	ns
3-state output disable time from input ($\overline{OE}$) to output(Qn)	t_{PHZ}/t_{PLZ}	V_{CC}=4.5V		18	30	ns
Propagation delay from input ($\overline{SRCLR}$) to output(QH')	t_{PHL}	V_{CC}=4.5V		23	40	ns
Output transition time, QH'	t_{TLH}/t_{THL}	V_{CC}=4.5V		8	15	ns
Output transition time, Qn	t_{TLH}/t_{THL}	V_{CC}=4.5V		8	12	ns

■ OPERATING CHARACTERISTICS

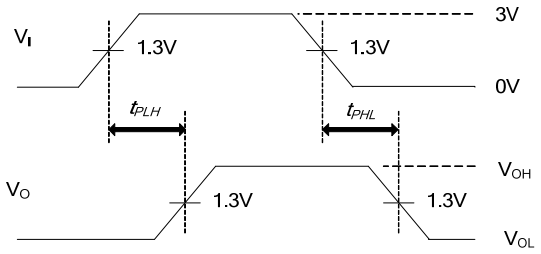
PARAMETER	SYMBOL	TEST CONDITIONS	RATINGS	UNIT
Power Dissipation Capacitance	C_{PD}	No Load	400	pF

■ TEST CIRCUIT AND WAVEFORMS

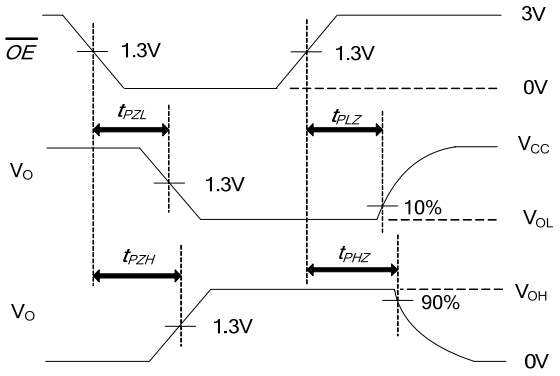


TEST	K1	K2
t_{PLH}/t_{PHL}	Open	Open
t_{PHZ}/t_{PZH}	Open	Close
t_{PLZ}/t_{PZL}	Close	Open

Note: C_L includes probe and jig capacitance.



Propagation Delay Times



Enable and Disable Times