ZARLINK
SEMICONDUCTOR ™

Features

September 2003

- Quad Band GSM (800/900/1800/1900 MHz) Compatible
- Dual Band IS136 (800/1900 MHz) Compatible
- GPRS Class 12 and EDGE Capable
- Fully Integrated Dual Band Transceiver
- Receive - IF to Baseband I and Q
- Transmit - Baseband I / Q to RF
- Integrated Filters
- FM Demodulator
- RF and IF Synthesizers
- Fully Programmable via serial bus
- 3 Volt operation
- Small scale package

Applications

- GAIT IS136/GSM/EDGE Mobile Telephones
- Dual Band (850/PCS1900) TDMA/AMPS Mobile Telephones
- Cellular 850MHz TDMA/AMPS Mobile Telephones
- PCS1900 TDMA Mobile Telephones
- 2.5G World Phones - Quad Band (850/900/1800/1900)
- Cellular Telematic Systems

Ordering Information

ZL20250/LCE (Tubes) 56 pin QFN
ZL20250/LCF (Tape and Reel) 56 pin QFN

-40°C to +85°C

Description

The ZL20250 is a fully integrated transceiver for multimode IS136/GSM/GPRS/EDGE handsets. The dual IF inputs to the receive path are amplified and down-converted to baseband I and Q signals. Gain control and baseband filtering are provided. A FM demodulator is also provided where AMPS compatibility is required.

The transmit path consists of a quadrature modulator, gain control at IF and up-conversion to RF. Dual band RF outputs are provided.

ZL20250 also includes a fractional N RF synthesizer and two IF synthesizers to provide all local oscillator signals required.

Flexible programming is provided via a 3 wire serial bus. Additional control pins allow accurate timing control when switching between modes.
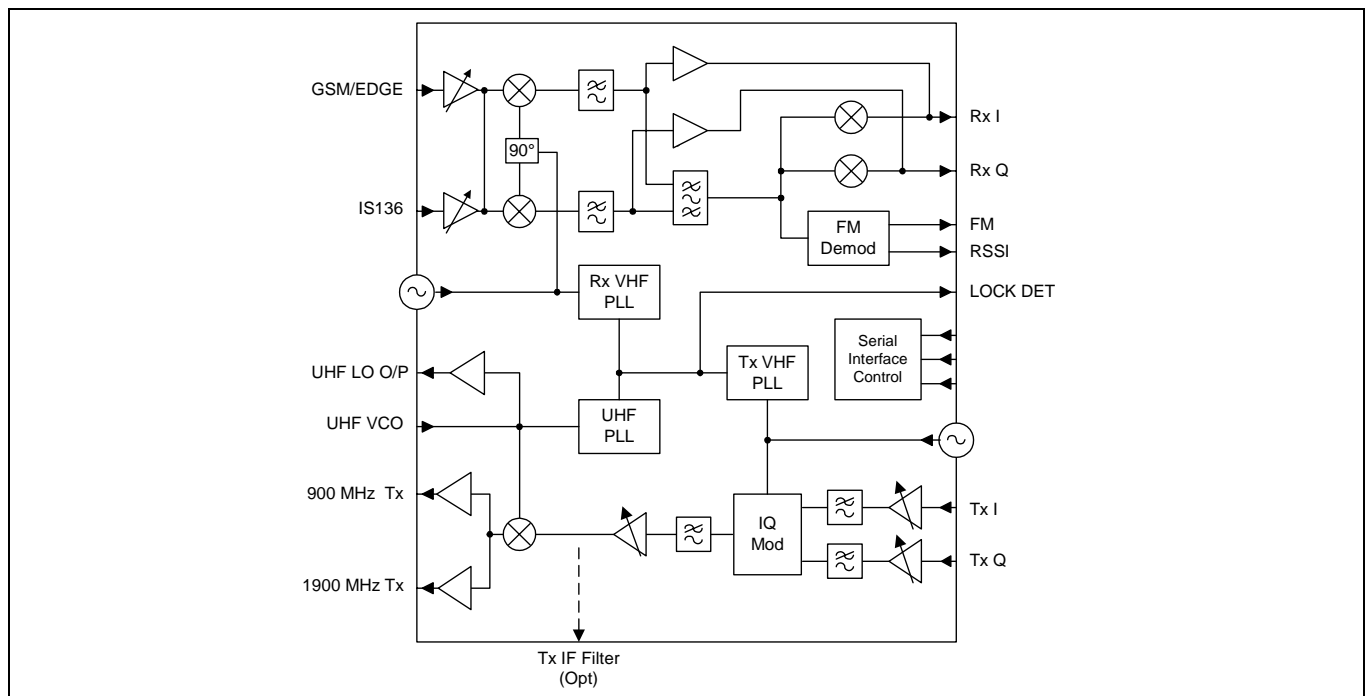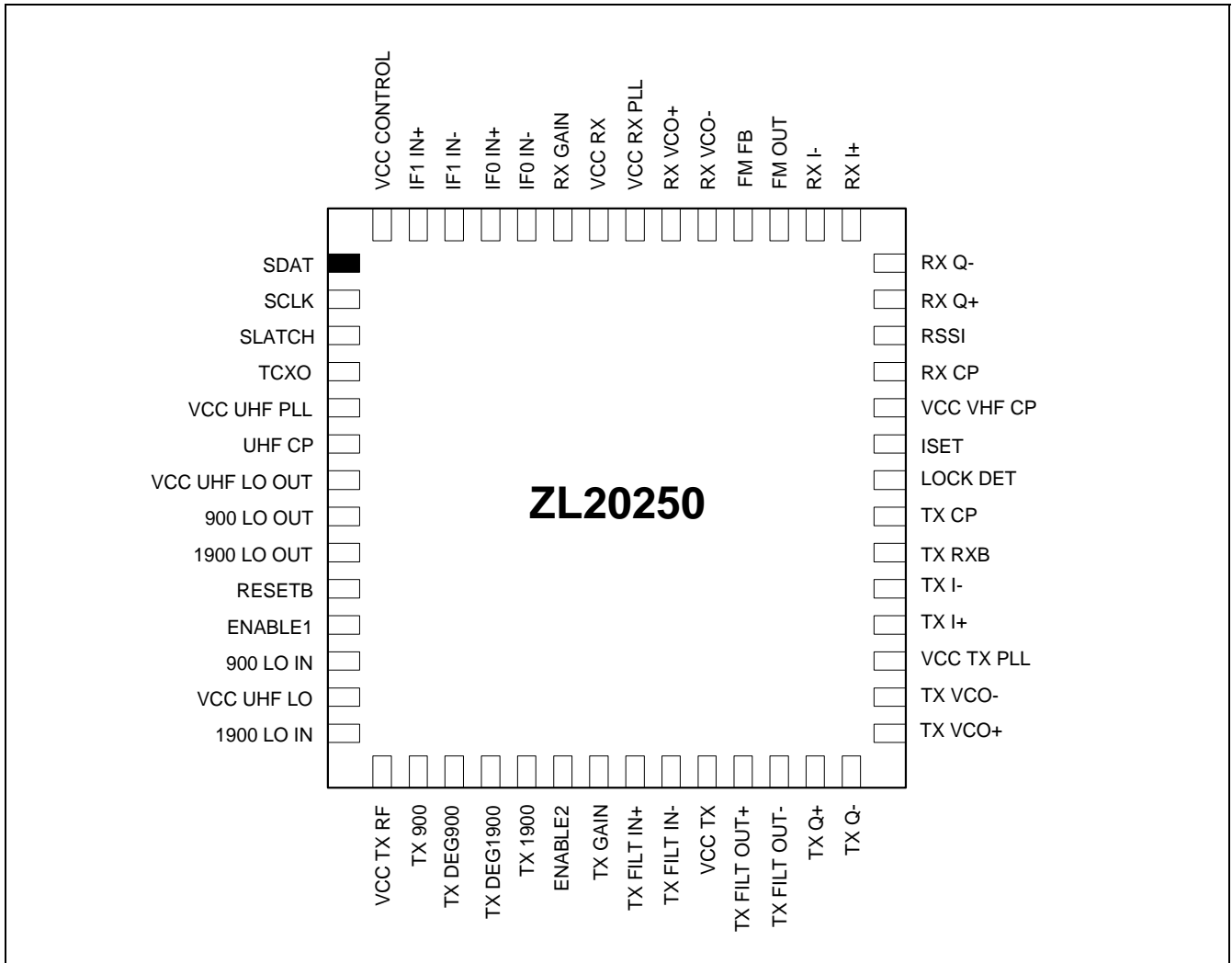

Figure 1 - Block Diagram

Package Diagram

Figure 2 - ZL20250 Package Diagram

Pin Description Table

No	Pin Name	Type	Description
1	SDAT	Input	Serial Interface - Data
2	SCLK	Input	Serial interface - Clock
3	SLATCH	Input	Serial Interface - Latch
4	TCXO	Input	Reference input from TCXO
5	VCC UHF PLL	Power	Power
6	UHF CP	Output	UHF PLL Charge Pump Output
7	VCC UHF LO OUT	Power	Power to LO output stages
8	900 LO OUT	Output	900 MHz buffered LO output to external receiver mixer
9	1900 LO OUT	Output	1900 MHz buffered LO output to external receiver mixer
10	RESETB	Input	Reset (Active low)
11	ENABLE1	Input	Mode Control
12	900 LO IN	Input	900 MHz LO input
13	VCC UHF LO	Power	Power to UHF LO input stage
14	1900 LO IN	Input	1900 MHz LO input
15	VCC TX RF	Power	Power to transmit RF output stages
16	TX 900	Output	900 MHz transmit output
17	TX DEG900		Degeneration for 900 MHz output
18	TX DEG1900		Degeneration for 1900 MHz output
19	TX 1900	Output	1900 MHz transmit output
20	ENABLE2	Input	Mode Control
21	TX GAIN	Input	Transmit gain control
22	TX FILT IN+	Input	Input from transmit IF filter (optional)
23	TX FILT IN-	Input	
24	VCC TX	Power	Power to transmit stages
25	TX FILT OUT+	Output	Output to transmit IF filter (optional)
26	TX FILT OUT-	Output	
27	TX Q+	Input	Q transmit signal from baseband
28	TX Q-	Input	
29	TX VCO+		Transmit Oscillator tank circuit
30	TX VCO-		
31	VCC TX PLL	Power	Power to Transmit VHF PLL
32	TX I+	Input	I transmit signal from baseband
33	TX I-	Input	
34	TX RXB	Input	Transmit / Receive control
35	TX CP	Output	Transmit VHF PLL charge pump output
36	LOCK DET	Output	PLL Lock Detect Output
37	ISET		Connect 50 kohm resistor to ground to set internal reference current
38	VCC VHF CP	Power	Power to VHF charge pump outputs

Pin Description Table (continued)

No	Pin Name	Type	Description
39	RX CP	Output	Receive VHF PLL charge pump output
40	RSSI	Output	RSSI Output
41	RX Q+	Output	Baseband Q signal
42	RX Q-	Output	
43	RX I+	Output	Baseband I signal
44	RX I-	Output	
45	FM OUT	Output	Demodulated FM output
46	FM FB		Feedback to FM output stage
47	RX VCO-		Receive second LO Oscillator tank circuit
48	RX VCO+		
49	VCC RX PLL	Power	Power to receive VHF PLL. Connect to VCC through 10 ohm resistor
50	VCC RX	Power	Power to receive stages
51	RX GAIN	Input	Receive gain control
52	IF0 IN-	Input	IF Input (0)
53	IF0 IN+	Input	GSM
54	IF1 IN-	Input	IF Input (1)
55	IF1 IN+	Input	IS136 Input
56	VCC CONTROL	Power	Power to serial interface logic

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1.0 General Description

A detailed block diagram is shown in Figure 3. This shows the receive and transmit paths plus the LO generation circuitry. Control is via a serial bus with the addition of direct inputs to control receive and transmit modes and optimize power consumption.
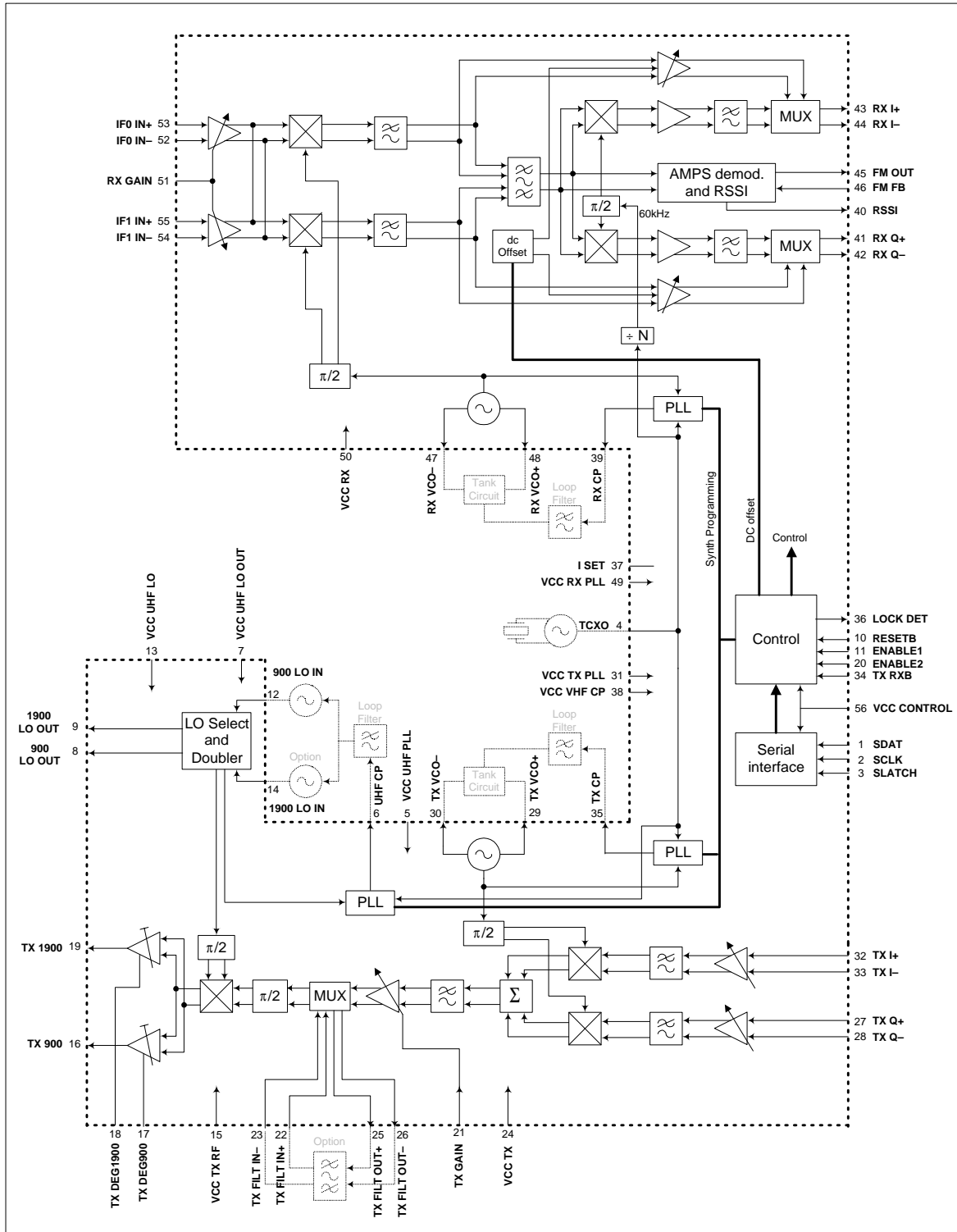

Figure 3 - ZL20250 Detailed Block Diagram

1.1 Receive Path

There are two IF inputs which will receive an input signal from IS136/AMPS and GSM IF filters. The differential input stages are identical and are followed by an agc amplifier. Gain control is provided from an external analogue voltage. After the agc amplifier the signal is then down-converted either to a low IF frequency or baseband and the signal flow then depends on the mode selected. All internal signals are differential. The LO frequency for the down conversion is derived from an on chip oscillator and PLL. The LO frequency can be programmed to be either oscillator frequency divided by 2 or 4. When in divide by 2 mode a DLL (Delay Locked Loop) circuit can be selected to maintain accurate quadrature. It is particularly important to have good quadrature in IS136/AMPS modes using a low IF frequency, to achieve the required image rejection in conjunction with the following polyphase bandpass filter. It is also possible to programme high side or low LO injection. Each receive mode will now be described in more detail

1.1.1 IS136

The IS136 receive signal path is shown in detail in Figure 4 and performance for each stage is summarized in the following table.

Circuit Block	Gain (dB)	Filter Bandwidth (If Applicable)	Description
IF Input (IF0)	26 max		Differential IF input stage
AGC Amplifier			AGC Amplifier - Gain control range 90dB
Quadrature Down-converter	47		Down-conversion to 60kHz IF
Anti-alias filter		230 kHz	Low pass Butterworth (n= 3)
Band Pass Filter		+/- 20 kHz	Switched capacitor polyphase Chebyshev. Also provides typically 30 dB image rejection. Centre frequency = 60 kHz. Clock frequencies 1.44 MHz and 720 kHz.
Gain Stage			
Baseband Down-converter	7		Down conversion to baseband I and Q signals
Baseband filter 1		37.5 kHz	Switched capacitor low pass Chebyshev. Clock frequency = 240 kHz
Baseband filter 2		60 kHz	Smoothing filter. Low pass Butterworth

Table 1 - IS136 Receive Gain and Filter Distribution

The output of the agc amplifier is down-converted using a quadrature mixer to a low IF of 60kHz. High side or low side LO injection can be selected. The In Phase (I) and Quadrature (Q) signals at 60 kHz are then passed through anti alias filter stage to remove any high frequency signals prior to subsequent sampling. The 60 kHz IF signals are then fed into a switched capacitor polyphase bandpass filter which not only provides filtering but also provides image rejection. This switched capacitor filter provides very stable performance and no calibration is required. After the bandpass filter the 60 kHz IF signal is further amplified and then mixed down to baseband I and Q signals. Additional filtering is required at baseband to remove spurii from the down-converter. This filtering is provide in two stages, the first stage is a switched capacitor filter with the second stage being a smoothing filter to remove clock breakthrough from the preceding switched capacitor filter. The differential baseband outputs can then be fed directly into analogue to digital converters on a baseband processor.
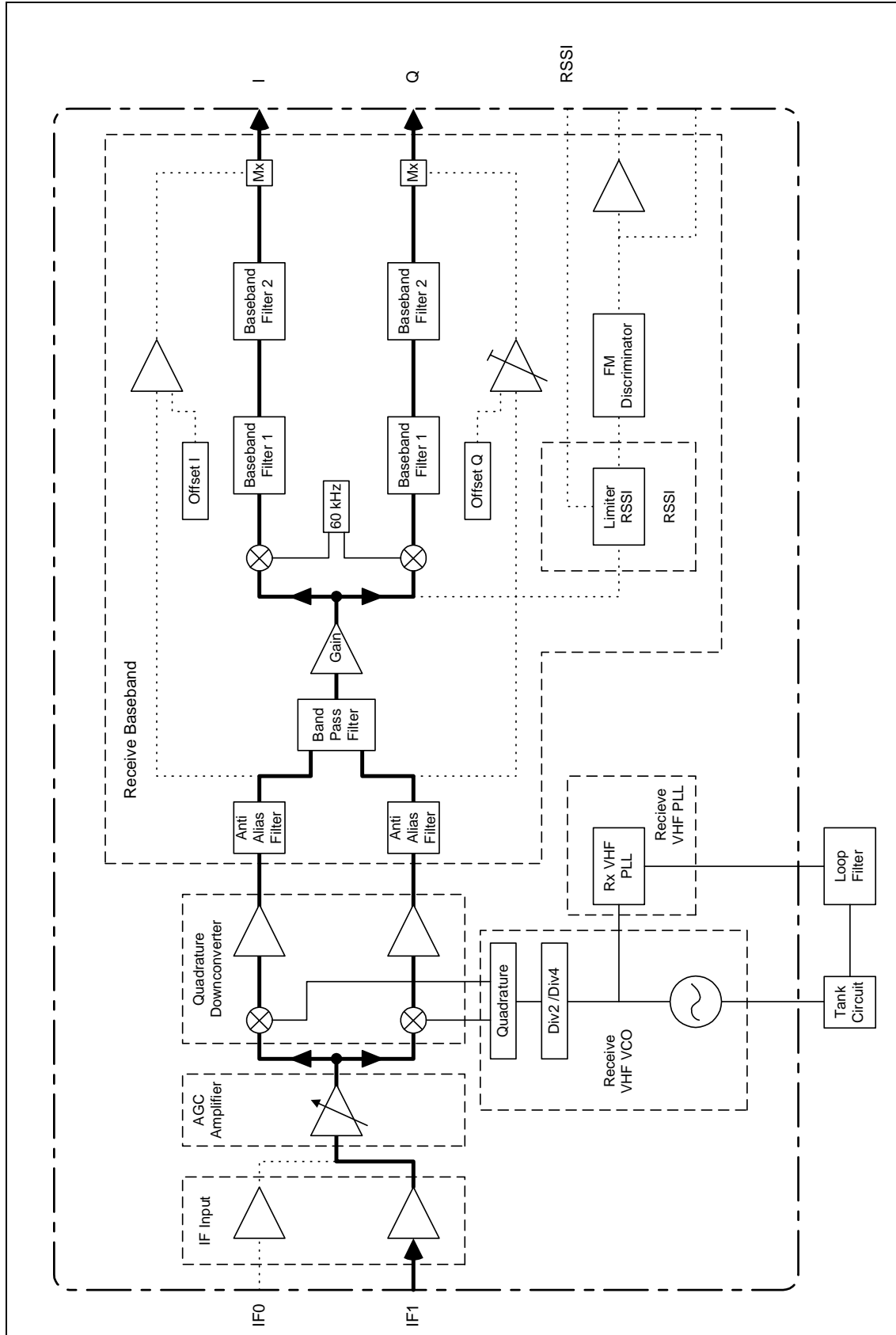
Figure 4 - IS136 Receiver Signal Flow

1.1.2   AMPS FM

FM demodulation can be performed using the I and Q baseband signals if supported by the baseband. However the ZL20250 also contains an FM demodulator, the AMPS receive signal path using this mode is shown in detail in Figure 5 and performance for each stage is summarized in the following table.

Circuit Block	Gain (dB)	Filter Bandwidth (If Applicable)	Description
IF Input (IF0)	26 max		Differential IF input stage
AGC Amplifier			AGC Amplifier - Gain control range 90dB. Includes IF input stage gain.
Quadrature Down-converter	73		Down-conversion to 60kHz IF
Anti-alias filter		230 kHz	Low pass Butterworth
Band Pass Filter		+/- 16 kHz	Switched capacitor polyphase Chebyshev. Also provides typically 30dB image rejection. Centre frequency = 60 kHz. Clock frequency 1.44 MHz and 720 kHz.
Limiter			Provides limited output to discriminator. Also provides RSSI output.
FM Discriminator			Digital FM discriminator
Baseband filter 2 (I Channel)		30 kHz	Smoothing filter. Low pass Butterworth. Provides filtering of FM discriminator output.
Baseband filter 1 (I Channel)		25 kHz	Switched capacitor low pass Chebyshev. Clock frequency = 240 kHz. Provides additional filtering of discriminator output. Selected using PDF and LPC bits
Baseband filter 1 (Q Channel)		25 kHz	Switched capacitor low pass Chebyshev. Clock frequency = 240 kHz. Provides additional filtering of discriminator output. Selected using PDF and LPC bits
Baseband filter 2 (Q Channel)		60kHz	Smoothing filter. Low pass Butterworth. Provides filtering of FM discriminator output.
FM Output		30kHz	Configured using external components as bandpass filter.

Table 2 - AMPS FM Receive Gain and Filter Distribution

The signal path is initially the same as for IS136 with the down conversion to 60 kHz and channel filtering in the bandpass filter. In FM mode however, the baseband I and Q output stages are disabled, and the 60 kHz IF signal from the bandpass filter is input to a limiting amplifier and FM discriminator. The FM discriminator consists of a shift register acting as a delay line. The output of the discriminator is a digital signal which must then be filtered to recover the audio signal. The discriminator output is therefore routed through the baseband I and Q filters. The default condition is to use the cascaded I and Q smoothing filters (baseband filter 2) with the cut-off frequency set to 30kHz. This connection is automatically selected when programming FM mode. There is an option to use the cascaded switched capacitor filters (baseband filter 1) with the cut off frequency set to 25 kHz to provide extra filtering. These filters are selected using the PDF and LPC bits in control register 6 and are inserted between the smoothing filters as shown in Figure 5. The final output stage uses external feedback components to provide a bandpass filter with a bandwidth of at least 300 Hz to 10 KHz to cover the demodulated audio and control signals. The feedback components can be modified to change the output level to optimise compatibility with baseband.

A RSSI output is provided. This is a full wave rectified output of the 60 kHz IF and therefore has a high 120 kHz content. This requires an external low pass filter - typically 10kohm and 2.7nF. There is a trade-off between settling

time and filtering. This is different to conventional RSSI circuits which operate at typically 450 kHz which is much easier to filter.

Although the AMPS receive path includes a limiting amplifier, gain control is also required. This is because the band pass filter has limited dynamic range (50dB). At low signal levels the agc should be set to 1.6 volts to set the gain 20dB below maximum to obtain optimum signal handling and noise performance. At higher signal levels the gain setting should be reduced to maintain the RSSI level approximately 10dB below maximum. Gain control would be provided by the baseband controller which would also monitor the RSSI level. Fine gain control is not required and can be implemented in large steps eg 20dB, allowing the use of a relatively slow gain control loop giving optimum performance under fading conditions.
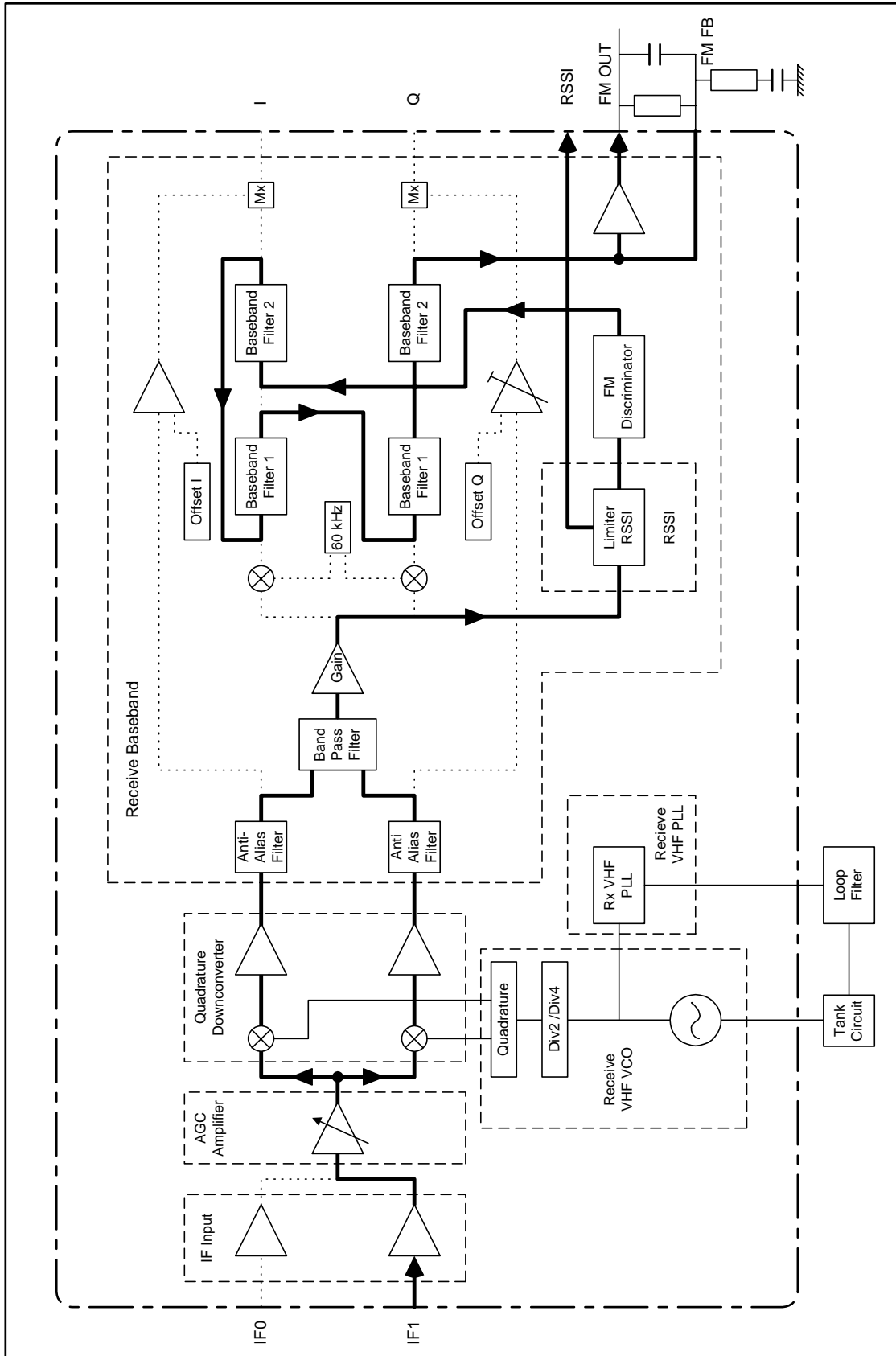
Figure 5 - AMPS Receive Signal Flow

1.1.3 GSM

The GSM receive signal path is shown in detail in Figure 6 and performance for each stage is summarized in the following table.

Circuit Block	Gain (dB)	Filter Bandwidth (If Applicable)	Description
IF Input (IF0)			Differential IF input stage
AGC Amplifier	26 max		AGC Amplifier - Gain control range 90dB. Includes IF input stage gain.
Quadrature Down-converter	54		Down-conversion to baseband
Anti-alias filter		230 kHz	Low pass Butterworth. Provides channel filtering in GSM/EDGE mode
Baseband Gain			Baseband gain with offset correction. Nominal gain is 35 dB and can be reduced in 3 dB steps to 14 dB

Table 3 - GSM Receive Gain and Filter Distribution

In GSM mode the bandpass filter and IS136 baseband stages are disabled. After passing through the agc amplifier the signal is mixed down to baseband I and Q signals rather than to a low IF. The baseband signal must be dc coupled and this can introduce a dc offset in the output, which may vary with different gain settings. The ZL20250 therefore includes the facility to correct the dc offset for each channel using an 8 bit offset correction word that must be supplied by the baseband via the serial bus.

GSM Baseband gain can be programmed via serial bus. Reducing the baseband gain can be used to improve output signal to noise ratio. The IF gain should be increased to mainatin the total overall gain. In practice a gain reduction of 6 or 9 dB would give optimum performance
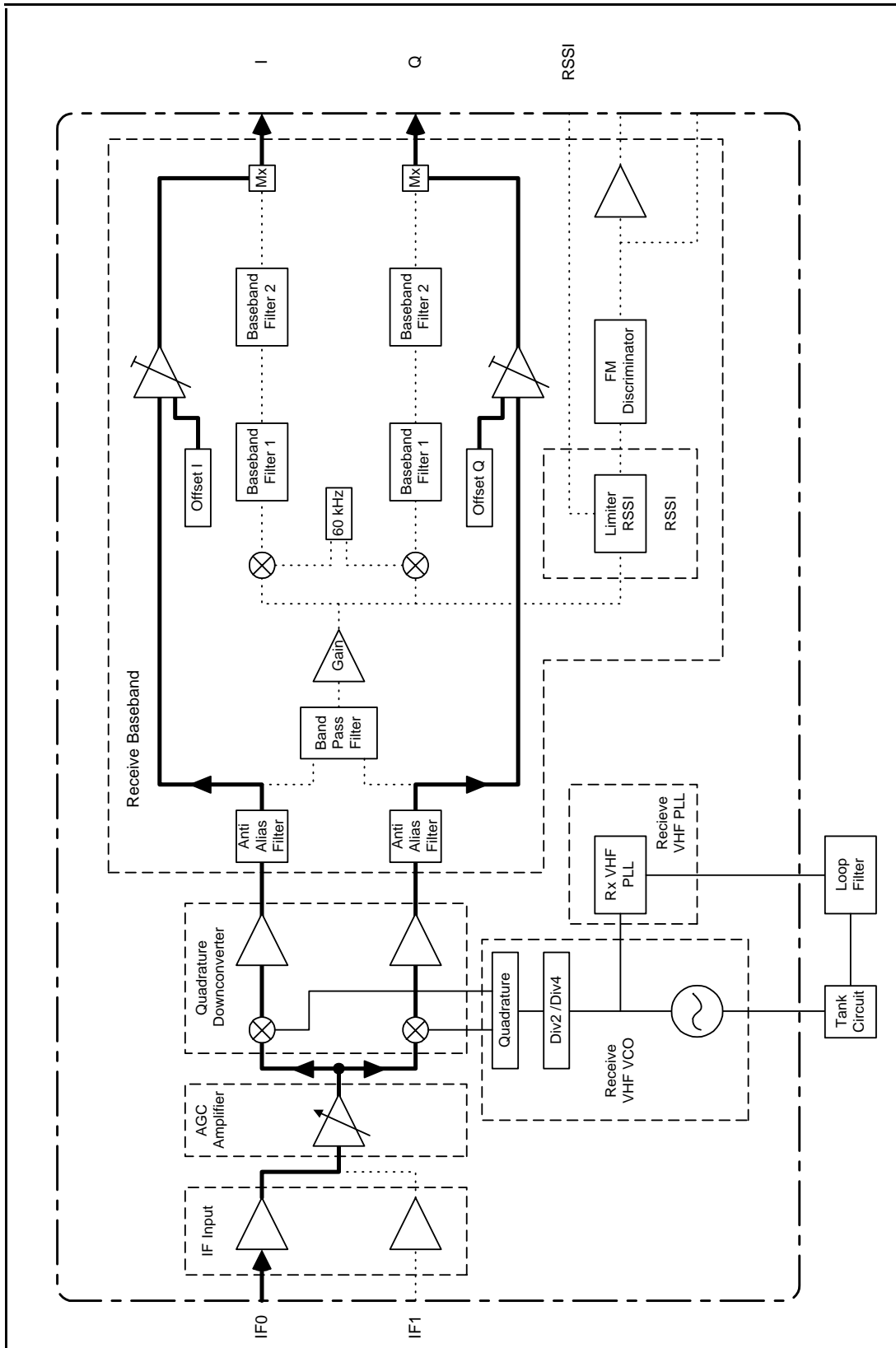
Figure 6 - GSM Receive Signal Flow

1.2 Transmit

Transmit operation is similar for all modes and a detailed diagram is shown in Figure 7. This diagram also shows the UHF LO generation circuit blocks. A summary of the characteristics of the transmit path circuit blocks are given in the table below. All circuit blocks are differential with the exception of the transmit RF outputs.

| Circuit Block	Gain (dB)	Bandwidth (If Applicable)	Description
Reconstruction Filters	0 -12	IS136/AMPS 12.5 kHz GSM 100 kHz	Baseband input stage. Gain is programmable in 3 dB steps from 0 to 12 dB. Filter bandwidth is selected for IS136/AMPS or GSM. There is also a by-pass mode so that the baseband I and Q signal can go direct to the modulator
Quadrature Modulator			Generates a modulated IF signal
Transmit IF		400 MHz	Provides gain control at IF frequency. This stage also includes a low pass filter to remove harmonics and spurii from modulator output. This stage also includes a buffered IF output which can be used with an external IF filter.
Up-converter			SSB up-converter to RF frequency. The IF path includes phase shift networks for the up-converter. This stage also includes the input circuit from the optional external IF filter
Transmit RF			The 900 MHz and 1900 MHz RF stages each consist of 2 stages. The first stage gain be set from -6 to +3 dB in 3 dB steps. Output stage current is controlled by agc signal to reduce current consumption at low output power levels. Each output stage requires an external degeneration inductor

Table 4 - Transmit Circuit blocks

Differential baseband transmit I and Q signals from a baseband processor are input to the ZL20250. The baseband signals are passed through filters - the filter bandwidth is selected for the appropriate mode i.e. IS136 or GSM. A quadrature modulator modulates these baseband signals on to the transmit IF which is typically around 200 MHz. This modulated IF signal is passed through an on chip low pass filter which removes harmonics of the IF and then into a gain controlled amplifier. This amplifier is controlled by an external analogue signal and provides greater than 60dB gain control The output of the gain controlled amplifier can then be up-converted to RF or alternatively the output can be sent to an off chip filter to provide further filtering and removal of noise before up-conversion. This filter is a parallel tuned circuit as shown in Figure 8. The choice of component values is dependent on the IF frequency being used. The filter output is then fed back on chip to the up-converter. A SSB mixer is used for the up-conversion to remove the unwanted image. High side or low side LO injection can be selected

A buffer amplifier after the up-conversion provides a further 9 dB gain control in 3 dB increments. This gain is programmable via the serial bus and can be used to optimize noise and linearity performance in particular applications. Finally there are two RF output stages for 900 MHz and 1900 MHz frequency bands. Each RF output is single ended and requires a simple matching network. The supply current of the output stages is automatically reduced at low transmit gain control voltages improving the efficiency of the output buffer at low output power levels. The supply current of the output buffer can also be controlled via the serial bus. This allows the supply current to be reduced which is particularly useful when using AMPS or GSM where the linearity performance is less critical.

The FM modulation for AMPS can be done using I,Q modulation if available. Alternatively FM modulation can be applied direct to the transmit IF VCO. The loop bandwidth for the transmit VHF PLL should be low (~100 Hz) to ensure the PLL does not remove the modulation. A dc voltage should be applied across the Tx I+, Tx I- and the Tx Q+, Tx Q- inputs to switch the modulator and generate an IF carrier signal. With a baseband gain of 0dB a dc voltage of at least 1.5 volts should be applied; a lower voltage can be used with the baseband gain increased to compensate. It is assumed that this bias can be provided by the baseband however if this is not possible then the simplest solution is to connect 200kohm resistors between I+, Q+ inputs and Vcc and 200kohm resistors between I+,Q- inputs and

ground assuming the transmit outputs from the baseband are in a high impedance state in AMPS mode. These resistors do produce a small dc offset in TDMA mode however this is insignificant if the output impedance of baseband transmit outputs is less than 1 kohm.As the FM modulation is applied direct to the VCO in this mode and is external to the ZL20250, any necessary filtering of the FM signal must be provided externally.

Figure 7 - Transmit Path
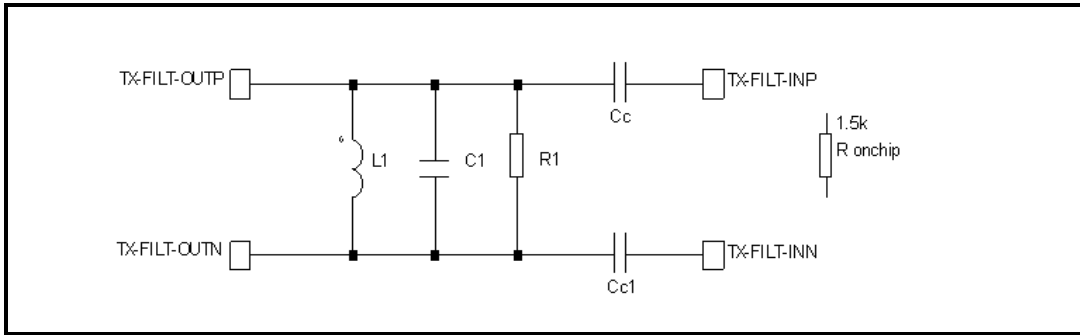
Figure 8 - External Transmit IF Filter

1.3   UHF LO and Frequency Doubler

Figure 8 also shows the UHF LO buffering and frequency doubler. The ZL20250 is designed to operate either with separate external UHF VCOs for the 900 and 1900 MHz frequency bands, or alternatively a single 900 MHz VCO can be used with the on-chip frequency doubler providing the LO for the 1900 MHz band. A UHF synthesizer is included. The input to the UHF synthesizer will normally be the active UHF LO signal, however when using the frequency doubler mode for 1900 MHz LO generation, the synthesizer input can be selected to be either the frequency doubler output or the 900 MHz input LO signal. The UHF LO input buffer minimizes any load pulling effects on the UHF VCO when internal modes are switched.

UHF LO output buffers are also provided. These can be used to drive an external mixer for the receive section. If not required these buffers can be powered down.

1.4   UHF Frequency Synthesizer

A fractional N UHF synthesizer is included on the ZL20250 to provide LO signals for the transmit up-converter and the external receive RF down-converters. The UHF synthesizer operates with an external VCO. A block diagram of the synthesizer is shown in Figure 9.
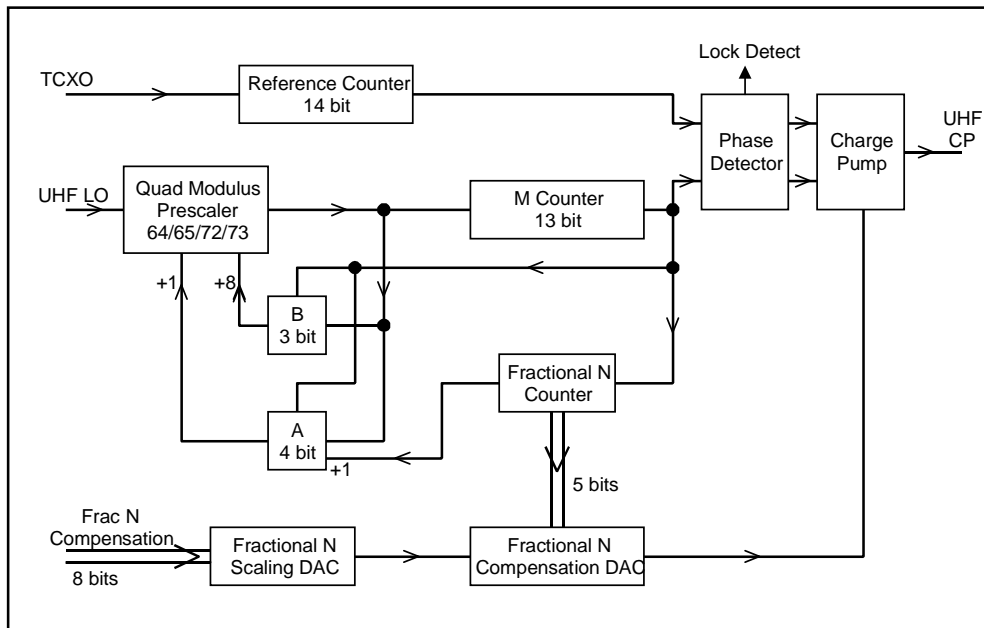
Figure 9 - UHF Synthesizer

The synthesizer uses a 4 modulus prescaler with an 'M' counter and 'A' and 'B' swallow counters together with a fractional N counter in the UHF counter allowing maximum flexibility. The reference counter is a simple 14 bit counter. All counter values are programmed via the serial bus and programming details are shown in the programming section. Each of the counters operates as count down. At the start of a count the counters are loaded with their respective values. The initial prescaler ratio is dependent on the values loaded into the A and B counters; when both the A and B counters reach zero the prescaler ratio is 64 and then remains until the M counter reaches zero. The complete process is then repeated.

This can be shown in a simple example where M = 9, A = 4 and B = 2 which gives a total divide ratio of 596. The count sequence is shown in Figure 10.
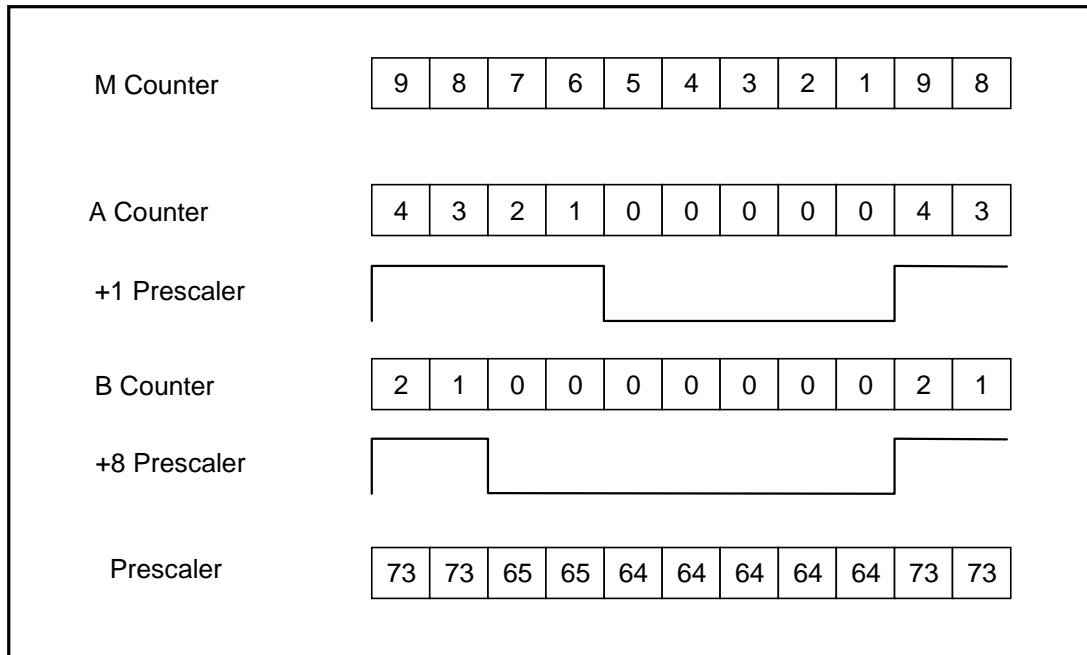
Figure 10 - Count Sequence for UHF PLL with 4 modulus prescaler

At the start of the count sequence the '+1' and '+8' controls to the prescaler are both asserted and the prescaler ratio is 73. After 2 cycles only the '+1' control is asserted and the divide ratio is 65. After a further 2 cycles the A counter reaches zero as well and the prescaler ratio is 64 for the remainder of the count sequence. At the end of the sequence all counters are reloaded and the sequence repeats.

The total divide ratio (N) for this type of counter is given by

$N = 64*M + 8*B + A$
M is always greater then A or B
A value of A = 0 does not support fractional N operation. Valid values of A are 1 to 8.

The values of M, B and A can be easily calculated from the total divide ratio as shown below.

$M = INT ((N - 1)/64)$
$B = INT (((N - 1) - 64*M)/8)$
$A = N - 64*M - 8*B$

The value of M must always be greater than A or B. The maximum value of B is 7.

The UHF synthesizer also includes a fractional N capability which allows the use of higher comparison frequencies but maintain narrow channel spacing. The use of higher comparison frequencies allows faster loop settling and reduces comparison spur level. This is particularly important in TDMA mode where settling times of < 1.5 ms are required and still obtain good spur performance.

Fractional N allows the use of non-integer divide ratios. For example if the total divide ratio is N + 1/5 the counter will divide by N for 4 count cycles and N+1 on the fifth cycle giving the required total divide ratio over five cycles. The ZL20250 can use 5,8,13 or 20 as the fractional denominator (also referred to as the fractional modulus) allowing maximum flexibility in the choice of comparison frequencies.

An extra counter - fractional N counter - is required. The input to this counter is from the M counter output. The fractional N modulus can be programmed to be 5,8,13, or 20. Each output pulse from the M counter will increment the fractional N divided by the required fractional numerator. For example if the fraction is 2/5 then the fractional N counter will increment by 2 for each output pulse from the M counter. When the fractional N counter overflows the A counter is incremented by 1, thus generating an additional '+1' count sequence.

An example is shown in Figure 11 for a divide ratio of 596+2/5. The values for M, A, B are calculated using the integer value (596) as in the previous example. The fractional denominator is programmed as 5 and the fractional numerator as 2. At the end of the first count cycle (596) the fractional counter is incremented to 2. At the end of the third count cycle the fractional N counter overflows, incrementing the A counter by 1 which gives a subsequent count cycle of 597. After five count cycles the sequence repeats with a total count of 2982 over the five count cycle giving a mean value of 596 + 2/5.

	Total Count Cycle						
Count Value	596	596	597	596	597	596	
Fractional N Counter	0	2	4	1	3	0	2
Initial A Counter Value		4	4	5	4	5	4

Figure 11 - UHF Synthesizer - Fractional N Operation

A result of this count sequence is that the output phase of the total counter changes through the count cycle, which causes the output pulse from the phase detector, and therefore the charge pump, to vary. This would cause large fractional spurs on the synthesizer output. These spurs can be compensated by applying a current pulse with the opposite polarity to the charge pump output. This compensation pulse has a fixed width of two reference clock (TCXO) periods; the amplitude is proportional to the value in the fractional N counter. The correction current is scaled by a 8 bit compensation DAC, with an externally provided input from the serial bus. This allows performance to be optimized in a given application.

The compensation value can be calculated from the following formula:

Comp Value = 255 - INT((Icp * Ftcxo)/(0.0245 * 6 * MOD *Fvco))

where

Icp   = charge pump current (uA)

Ftcxo = Reference frequency

MOD   = Fractional Modulus

Fvco   = UHF VCO Frequency

The synthesizer provides a lock detect output. When the output pulse from the phase detector is less than half a reference clock period an in-lock signal is generated. These in-lock signals then clock a 4 bit counter into which a threshold value has been programmed. When the required number of successive in-lock pulses have been generated the lock detect output is set.

The ZL20250 has a single lock detect output pin for the UHF synthesizer and VHF synthesizers. The lock detect signal is asserted when all active synthesizers are in lock. If a synthesizer has not been enabled in the power control registers then that synthesizer will be inactive and will have no effect on the lock detect output.

1.5   VHF Frequency Synthesizer

The ZL20250 includes two VHF synthesizers to generate the second LO for the receiver and the transmit IF. They operate with their respective on-chip VHF VCO's and off-chip loop filters. The tank circuits and tuning components for the VCO's are also off chip. The two synthesizers are identical and are shown in Figure 12.
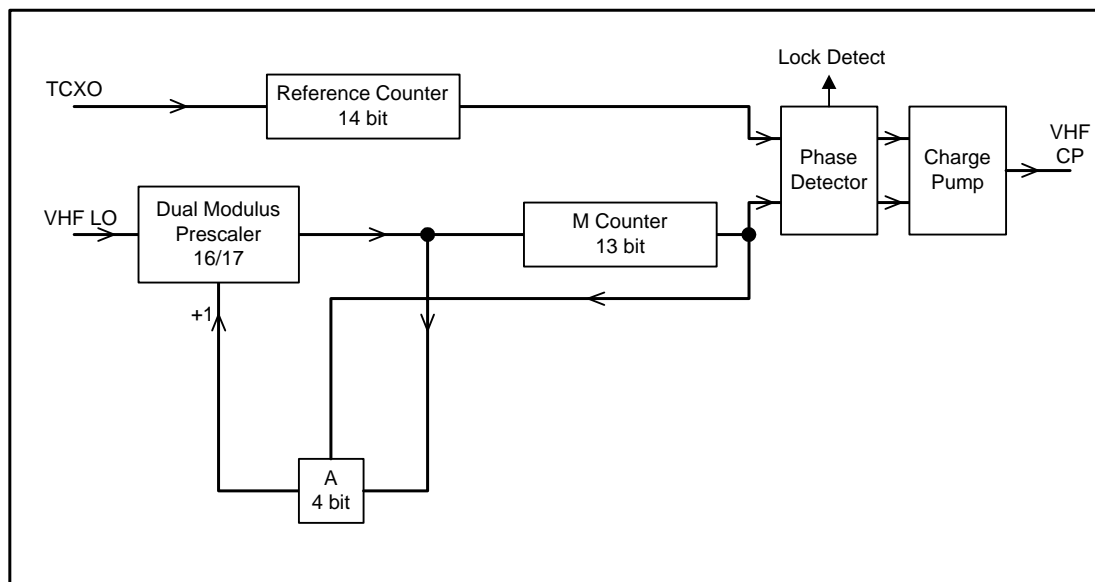
Figure 12 - VHF Frequency Synthesizer

The synthesizer uses a 2 modulus 16/17 prescaler with an 'M' counter and an 'A' swallow counter. This allows maximum flexibility when using this synthesizer. The reference counter is a simple 14 bit counter. All counter values are programmed via the serial bus and programming details are shown in the programming section. Both counters operate as count down. At the start of a count the counters are loaded with their respective values. The initial

prescaler ratio is 17 assuming A > 0; when the A counter reaches zero the prescaler ratio is 16 until the M counter reaches zero. The complete process is then repeated.

The total divide ratio (N) for this type of counter is given by

N = 16*M + A
M is always greater then A
The values of M and A can be easily calculated from the total divide ratio N.

M = INT (N/16)
A = N - 16*M
The maximum value for A is 15 and M must always be greater than A.

The VHF PLLs do not have fractional N capability however it is recommended that thay are operated at as high a comparison frequency as allowed by the chosen frequency plan to minimise spurs levels.

Both VHF synthesizers have lock detection circuits. These operate in the same way as described for the UHF synthesizer.

1.6   Internal Clock Generation

ZL20250 can use 14.4 MHz or 19.44MHz reference frequency (standard for IS136), or 13 MHz or 26 MHz (standard for GSM). The appropriate reference must be programmed via the serial bus. The clock signals for the switched capacitor filters and FM demodulator are generated from the reference TCXO signal. The internal divide ratios are switched to give the optimum ratio. For dual mode applications (GSM/IS136) a 13 MHz or 26 MHz reference should be used. This will give a small error in the switched capactor clock frequency used for IS136 but has negligible effect on performance.

1.7   VHF VCO

ZL20200 has two VHF VCOs which operate with the VHF PLLs to provide the IF LO signals for both receive and transmit IF signals. The oscillators are a differential design and require an external tank circuit. A basic circuit with varactor is shown in Figure 13. It is recommended to include series resistors (eg 43 ohms) in each arm of the tank circuit to prevent any spurious high frequency oscillation due to parasitic capacitances.
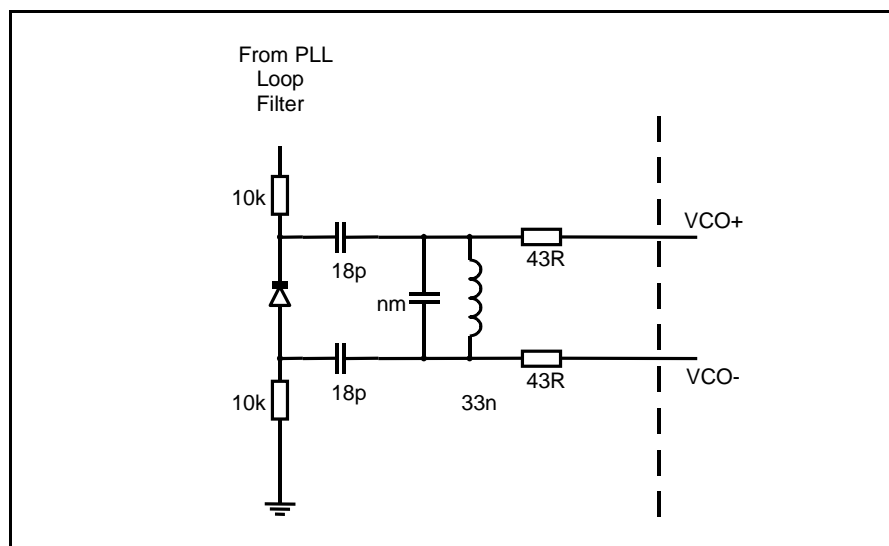
Figure 13 - Typical VCO Tank Circuit

1.8   Power Supply Connections

The circuit blocks within ZL20250 have separate supply connections to minimize interaction between circuit blocks. Details are shown in the earlier 'Pin Names' section. These supplies are also grouped to allow different groups of supply pins to be connected to separate supplies for example, receive or transmit. These groups are shown below:

VCC – Control Supply	
Pin No.	**Pin Name**
56	VCC CONTROL
VCC – TxRx Common (Synth)	
Pin No.	**Pin Name**
5	VCC UHF PLL
7	VCC UHF LO OUT
13	VCC UHF LO
38	VCC VHF CP
8	900 LO OUT
9	1900 LO OUT
VCC – Rx	
Pin No.	**Pin Name**
49	VCC RX PLL
50	VCC RX
VCC – Tx	
Pin No.	**Pin Name**
15	VCC TX RF
24	VCC TX
31	VCC TX PLL
16	TX 900
19	TX 1900

The LO OUT and TX 900/1900 pins require bias and are normally connected to VCC through an inductor.

All supply pins within a group must be powered together. Each group of pins can be powered up independent of the other groups.

2.0 Programming and Control

Programming via the serial bus is via 24 bit words with a 4 bit address as shown below

23	22	21	20	19	18	17	17	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Data																				Address			

Bit23 (MSB) is loaded first. Bits 3:0 are used as address bits for the control registers. Details of serial bus timing are shown in Figure 14.
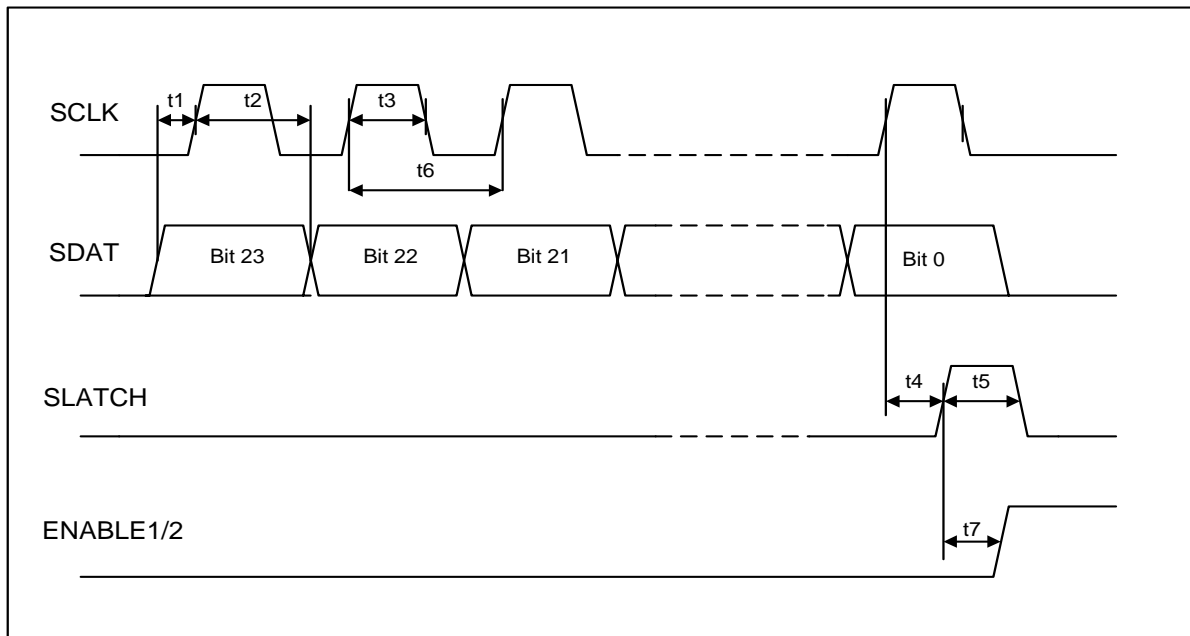
Figure 14 - Serial Bus Timing

2.1 Power Control Registers - Address 0 to 3

These registers are used in conjunction with the TX RXB and ENABLE1 and ENABLE2 control pins to power up the required sections of the device for any required mode. This enables power consumption to be optimized under all conditions. Figures 4 - 7, which show the receive and transmit paths in detail, show which sections are powered up by each control bit.

The assignment is common for each of the registers 0 to 3 and is shown below.

Bit	Circuit Section
23	Not used
22	Receive Baseband section
21	UHF LO Buffer
20	Receive VHF VCO

Bit	Circuit Section
19	UHF synthesizer
18	Receive RSSI circuit
17	Not used
16	Receive Quadrature down-converter
15	Receive VHF PLL
14	Receive IF input
13	Receive AGC amplifier
12	Transmit reconstruction filters
11	Transmit RF
10	Transmit UHF LO
9	UHF LO input buffer
8	Transmit IF
7	Transmit quadrature modulator
6	Transmit VHF PLL
5	Transmit VHF VCO
4	Transmit up-converter IF input

Note 1:   If a bit is set to logic 1 then that circuit section is powered on.
Note 2:   UHF LO input (bit 9) must be enabled for Transmit UHF LO (bit 10), UHF synthesizer (bit 19) and UHF LO Buffer (bit 21) to be active.

The 4 registers address 0 to 3 are assigned as follows:

Register Address	Register Name	Description
0	Receive	All circuit blocks required in receive mode should be set to 1. This register will be selected when TX RXB is low. No circuits will be actually powered up if ENABLE1 and ENABLE 2 are both low.
1	Transmit	Transmit register All circuit blocks required in transmit mode should be set to 1. In duplex modes e.g. AMPS then both receive and transmit circuits must be selected. This register will be selected when TX RXB is high. No circuits will be actually powered up if ENABLE1 and ENABLE 2 are both low
2	ENABLE1 Configuration	This register determines which circuit sections are powered up when ENABLE1 is high. The contents of this register are logical ANDed with the contents of the Receive or Transmit register as selected by TX RXB input.
3	ENABLE2 Configuration	This register determines which circuit sections are powered up when ENABLE2 is high. The contents of this register are logical ANDed with the contents of the Receive or Transmit register as selected by TX RXB input.

A feature of this programming approach is that once a phone operating mode has been selected and set up via the serial bus, all power control can then be via the TX RXB, ENABLE1 and ENABLE2 control pins. Alternatively full power control is possible via the 3 wire serial bus without the use of any external control pins.

If ENABLE1 and ENABLE2 are both low then the device is in Sleep mode. No circuits will be enabled unless either ENABLE1 or ENABLE2 are high regardless of the contents of the receive and transmit registers.

An example of how these control bits can be used, is that the oscillators and PLL circuits can be powered up and allowed to settle prior to powering up the complete transmit or receive path. In the case of the receive path the UHF synthesizer, UHF LO input buffer, UHF LO Buffer and Receive VHF VCO, Receive VHF PLL bits would be set in the ENABLE1 Configuration register. The ENABLE2 Configuration register would contain these bits plus the remainder of the receive path bits, Receive IF input, Receive AGC amplifier, Receive quadrature down-converter and receive baseband section.

This is demonstrated in the following examples.

2.1.1   Power Control Modes - TDMA (GSM and IS136)

In a TDMA system the transceiver will either operate in receive only, or transmit only mode. It is assumed that an interim power on state will be used during which the oscillators and PLLs will be set up, and allowed to settle prior to activating the full signal path. The suggested programming for the power control registers (0 - 3) is shown in the table below.

Bit	Circuit Section	Receive Addr 0	Transmit Addr 1	Enable 1 Config. Addr 2	Enable 2 Config. Addr 3	Comments
23	Not used	0	0	0	0	
22	Receive Baseband section	1	0	0	1	
21	UHF LO Buffer	0	0	0	0	Note 1
20	Receive VHF VCO	1	0	1	1	
19	UHF synthesizer	1	1	1	1	
18	Receive RSSI circuit	0	0	0	0	Note 2
17	Not used	0	0	0	0	
16	Receive Quadrature down-converter	1	0	0	1	
15	Receive VHF PLL	1	0	1	1	
14	Receive IF input	1	0	0	1	
13	Receive AGC amplifier	1	0	0	1	
12	Transmit reconstruction filters	0	1	0	1	
11	Transmit RF	0	1	0	1	
10	Transmit UHF LO	0	1	0	1	
9	UHF LO input buffer	1	1	1	1	
8	Transmit IF	0	1	0	1	
7	Transmit quadrature modulator	0	1	0	1	
6	Transmit VHF PLL	0	1	1	1	

Bit	Circuit Section	Receive Addr 0	Transmit Addr 1	Enable 1 Config. Addr 2	Enable 2 Config. Addr 3	Comments
5	Transmit VHF VCO	0	1	1	1	
4	Transmit up-converter IF input	0	1	0	1	

Note 1: Not required if driving external receive mixer direct from UHF VCO.
Note 2: Can be used for IS136 if required.

The receive register contains all bits required when in receive mode: the transmit register contains all bits required in transmit mode. The Enable1 configuration register contains all bits required to power up oscillators and synthesizers in both receive and transmit mode. The Enable2 configuration register contains all bits required to power up the complete receive and transmit modes (this register can be set to all '1's if preferred).

The following words should therefore be programmed on the serial bus (Hex format):

Receive register (0)   59E200
Transmit register (1)   081FF1
Enable1 Config. register (2)   188262
Enable2 Config. register (3)   59FFF3

2.1.2   Power Control Modes - AMPS

When operating in AMPS mode the ZL20250 will operate in either Receive only or Duplex. The enable registers should therefore be programmed as shown below.

Bit	Circuit Section	Receive Addr 0	Transmit Addr 1	Enable 1 Config. Addr 2	Enable 2 Config. Addr 3	Comments
23	Not used	0	0	0	0	
22	Receive Baseband section	1	1	0	1	
21	UHF LO Buffer	0	0	0	0	Note 1
20	Receive VHF VCO	1	1	1	1	
19	UHF synthesizer	1	1	1	1	
18	Receive RSSI circuit	1	1	0	1	
17	Not used	0	0	0	0	
16	Receive Quadrature down-converter	1	1	0	1	
15	Receive VHF PLL	1	1	1	1	
14	Receive IF input	1	1	0	1	
13	Receive AGC amplifier	1	1	0	1	
12	Transmit reconstruction filters	0	1	0	1	
11	Transmit RF	0	1	0	1	
10	Transmit UHF LO	0	1	0	1	
9	UHF LO input buffer	1	1	1	1	
8	Transmit IF	0	1	0	1	

Bit	Circuit Section	Receive Addr 0	Transmit Addr 1	Enable 1 Config. Addr 2	Enable 2 Config. Addr 3	Comments
7	Transmit quadrature modulator	0	1	0	1	
6	Transmit VHF PLL	0	1	1	1	
5	Transmit VHF VCO	0	1	1	1	
4	Transmit up-converter IF input	0	1	0	1	

Note 1:   Not required if driving external receive mixer direct from UHF VCO.

The receive register contains all bits required when in receive mode: the transmit register contains all bits required in duplex mode. The Enable1 configuration register contains all bits required to power up oscillators and synthesizers in both receive and duplex mode. The Enable2 configuration register contains all bits required to power up the complete receive and duplex modes (this register can be set to all '1's if preferred).

The following words should therefore be programmed on the serial bus (Hex format):

Receive register (0)   5DE200
Transmit register (1)   5DFFF1
Enable1 Config. register (2)   188262
Enable2 Config. register (3)   5DFFF3

2.2   Operating Register Address 4

This registers selects internal setups for example IS136 or GSM. The bits are assigned for control of receive and transmit bits as shown below:

23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RX<7:0>								TX <11:0>												0	1	0	0
Receive Set Up								Transmit Set Up												Address			

The function of the receive bits is shown below:

Register Bit No.	Control Bit	Action if '0'	Action if '1'
23	RX<7>	Receive DLL disabled	Receive DLL enabled
22	RX<6>	Bandpass Filter BW = +/- 20 kHz	Bandpass Filter BW = +/- 16 kHz
21	RX<5>	GSM Filters active	Receive GSM filters bypassed
20	RX<4>	LO output = 900 MHz	LO Output = 1900 MHz
19	RX<3>	Receive output dc bias (I/Q) = 1.25 V	Receive output dc bias (I/Q) = Vcc/2
18	RX<2>	IS136 Mode IF1 Input enabled	GSM Mode IF0 Input enabled
17	RX<1>	AMPS	IS136
16	RX<0>	Not used	Not used

Bit 23 RX<7> is only applicable when VCO divide by 2 mode is selected in register 5.

The function of the transmit bits is shown below:

Register Bit No.	Control Bit	Action if '0'	Action if '1'
15	TX<11>	Transmit output stage gain control	
14	TX<10>		
13	TX<9>	Control of RF Transmit output stage current with VGA control voltage. Nominal value for TX<11:4> is 101010	
12	TX<8>		
11	TX<7>		
10	TX<6>		
9	TX<5>		
8	TX<4>		
7	TX<3>	900 MHz output	1900MHz output
6	TX<2>	Internal	External transmit IF Filter
5	TX<1>	IS136 baseband filters	GSM/EDGE baseband filters
4	TX<0>	Transmit baseband filters selected	Transmit baseband filters by-passed

Control bits TX<11:4> allow optimization of the transmit output stage. This allows variation of the decrease in supply current with decreasing agc voltage and also allows optimization depending on output power and linearity requirements. Figure 15 shows the variation of output stage supply current with agc voltage and the programmable characteristics. The maximum current, agc threshold and slope can be programmed. The minimum current is not programmable.

TX<11:10> (bits 15,14) allow the gain of the transmit output stage to be varied in 3 dB steps as shown in the table below:

TX<11>	TX<10>	Gain (dB)
0	0	-6
0	1	-3
1	0	Nominal
1	1	+3
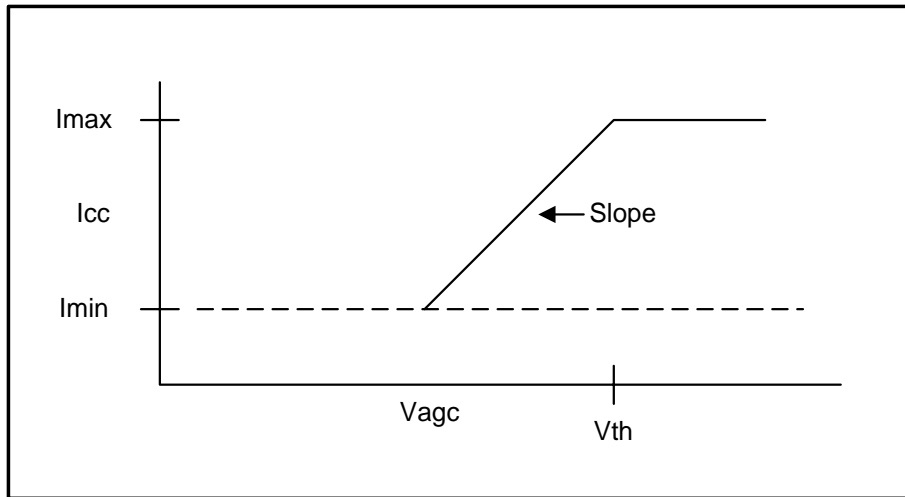
Figure 15 - Transmit Output Stage Current versus Gain Control

TX<9:8> (bits 13:12) control the agc voltage (Vth) at which the output stage current starts reducing. Typical values are shown in the table below:

TX<9>	TX<8>	Vth (V)
0	0	1.09
0	1	1.25
1	0	1.48
1	1	2.81

TX<7:6> (bits 11,10) control the rate of current reduction as shown in Figure 15. Typical vales are shown in the below:

TX<7>	TX<6>	Slope (mA/V)
0	0	8.5
0	1	10.5
1	0	12.0
1	1	14.0

TX<5:4> (bits 9:8) adjust the maximum current (Imax) of the transmit output stage. The gain of the output stage is not changed. Typical values are shown in the table below:

TX<5>	TX<4>	Current
0	0	25%
0	1	50%
1	0	Nominal
1	1	150%

Using these controls allows the performance of the output stage to be optimized under various conditions; for example, current cant can be reduced if non-linear operation is required.

The nominal value recommended for TX<11:4> is 10101010.

An example of setting up the control register (address 4) for various systems is shown below:

Bit	Name	GSM (850)	GSM (1900)	IS136 (900)	IS136 (1900)	AMPS	Comments
23	RX<7>	0	0	0	0	0	
22	RX<6>	0	0	0	0	1	
21	RX<5>	0	0	0	0	0	
20	RX<4>	0	1	0	1	0	
19	RX<3>	0	0	0	0	0	Note 1
18	RX<2>	1	1	0	0	0	
17	RX<1>	0	0	1	1	0	
16	RX<0>	0	0	1	1	1	
15	TX<11>	1	1	1	1	1	
14	TX<10>	0	0	0	0	0	
13	TX<9>	1	1	1	1	1	
12	TX<8>	0	0	0	0	0	
11	TX<7>	1	1	1	1	1	
10	TX<6>	0	0	0	0	0	
9	TX<5>	1	1	1	1	1	
8	TX<4>	0	0	0	0	0	
7	TX<3>	0	1	0	1	0	
6	TX<2>	0	1	0	1	0	Note 2

Bit	Name	GSM (850)	GSM (1900)	IS136 (900)	IS136 (1900)	AMPS	Comments
5	TX<1>	1	1	0	0	0	
4	TX<0>	0	0	0	0	0	

Note 1:   The setting for RX<3> is dependent on the optimum common mode input voltage of the analog to digital converter in the baseband.
Note 2:   Selects external transmit IF filter if used.

The following hex words are therefore recommended for the control register (address 4):

GSM (850)	04AA24
GSM (1900)	4AAE4
IS136 (900)	03AA04
IS136 (1900)	13AAC4
AMPS	41AA04

2.3   Synthesizer Register - Address 5

This register sets up LO options for receive and transmit and also UHF synthesizer set up.

23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
							0													0	1	0	1
UI	RX LO2 Set Up					UC		DL	UD	TX LO Set Up					UHF PLL Set Up					Address			

Bits 23,17,14 are also used for UHF PLL and LO set up.
Bits 16,15 are not used and should be set to zero.

2.3.1   UHF PLL and LO

Register Bit No.	Action if '0'	Action if '1'
23	UHF PLL input = 900 MHz	UHF PLL input = 1900 MHz
17		Fractional N Compensation selected
14		UHF Doubler Selected
8	Fractional N Denominator - see table below	
7		
6	Not Used - Set to 0	
5	UHF PLL Charge Pump Current - see table below	
4		

Note 1:   Bit 14 is only effective if 1900 MHz mode has been selected (register 4 Bit 7).
Note 2:   Bit 23 is only effective if 1900 MHz mode has been selected (register 4 Bit 7) and the UHF frequency doubler selected (Register 5 Bit 14). This control allows the use of the doubled frequency to be used as the input to the UHF PLL.
Note 3:   Fractional N Denominator
Note 4:   Bits 8,7 select the fractional N denominator for the UHF PLL as shown below:

<8>	<7>	Frac N Denom.
0	0	5
0	1	8
1	0	13
1	1	20

2.3.2   UHF PLL Charge Pump Current

Bits 5,4 select the charge pump current for the UHF PLL as shown below:

<5>	<4>	Current (mA)
0	0	1.00
0	1	0.50
1	0	0.25
1	1	0.125

2.3.3   Receive LO Set Up

Register Bit No.	Action if '0'	Action if '1'
22	High side Rx second LO injection	Low side Rx second LO injection
21	Rx second LO = VCO/2	Rx second LO = VCO/4
20	Rx LO phase detector polarity normal	Rx LO phase detector polarity inverted
19	Receive VHF PLL Charge Pump Current - see table below	
18		

Bits 19,18 select the charge pump current for the receive VHF PLL as shown below:

<19>	<18>	Current (mA)
0	0	1.00
0	1	0.50
1	0	0.25
1	1	0.125

2.3.4   Transmit LO Set Up

Register Bit No.	Action if '0'	Action if '1'
15	Transmit DLL disabled	Transmit DLL enabled
13	Low side Tx up-converter LO injection	High side Tx up-converter LO injection
12	Tx second LO = VCO/2	Tx second LO = VCO/4
11	Tx LO phase detector polarity normal	Tx LO phase detector polarity inverted
10	Transmit VHF PLL Charge Pump Current - see table below	
9		

Bits 10,9 select the charge pump current for the receive VHF PLL as shown below:

<10>	<9>	Current (mA)
0	0	1.00
0	1	0.50
1	0	0.25
1	1	0.125

2.4   Control Register - Address 6

23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0					0															0	1	1	0
	BBG		TCXO			PDF		LPC		Tx Gain			R	Mode Control						Address			

2.4.1   IS136 Baseband Gain

Bits 22:21 can be used to vary the gain of the baseband output stages in IS136 mode only. The gain of the 60 kHz IF stage preceding the baseband mixer is also varied so that the overall gain of the device can be maintained if required. The nominal gain is 20 dB and the recommended setting is BBG<1:0> = 11 to minimize output dc offsets.

BBG<1> Bit 22	BBG<0> Bit 21	IF Gain (dB)	Baseband Gain (dB)	Overall Gain (dB)
0	0	14	6	20
0	1	17	6	23
1	0	17	0	17
1	1	20	0	20

2.4.2   TCXO Reference Selection

Bits 20:19 are used to set the device to the required TCXO reference frequency.

TCXO<1> Bit 20	TCXO<0> Bit 19	TCXO Frequency (MHz)
0	0	13.0
0	1	14.4
1	0	19.44
1	1	26.0

2.4.3   Discriminator Output Filtering

Bits 17:14 set up on chip filtering of the FM output signal and are therefore only used in AMPS mode. Two cascaded filters can be selected and the bandwidth can be set to 25 or 37.5 kHz cut-off. Bits 17,16 (PDF) select the filters and bits 15,14 set the cutoff frequency.

<17>	<16>	<15>	<14>	Filter Selection
0	0	X	X	No filters
0	1	X	X	Filter 1 selected
1	0	X	X	Filter 2 selected
1	1	X	X	Filters 1 and 2 selected
X	X	0	0	Both filters 37.5 kHz
X	X	0	1	Filter 1 25kHz, Filter 2 37.5kHz
X	X	1	0	Filter 1 37.5 kHz, Filter 2 25 kHz
X	X	1	1	Both filters 25kHz

In GSM and IS136 modes Bits <17:14> should be set to 0000. It is recommended that if the additional discriminator filtering is required in AMPS mode then both filters should be used with 25 kHz bandwidth, i.e. Bits<17:14> should be set 1111.

2.4.4   Transmit baseband Gain

Bits 13:11 set the transmit baseband gain as shown below:

<13>	<12>	<11>	Gain (dB)
0	0	0	0
0	0	1	3
0	1	0	6
0	1	1	9
1	0	0	12

2.4.5   Mode Control

Bit 10 resets the contents of all registers to '0'. After the reset is complete bit 10 is also reset to '0'.

Bits 9:4 allow TXRXB, ENABLE1 and ENABLE2 to be programmed by either the external pins or via the serial bus. This allows mode control to be either via the external pins or the serial bus. The default state is using the external pins as this allows more accurate timing of power control.

Register Bit No.	Action if '0'	Action if '1'
9	Receive Register (0) selected	Transmit Register (1) selected
8		Enable2 Configuration Register (3) selected
7		Enable1 Configuration Register (2) selected
6	TXRXB Pin (34) selected	Serial Bus selected - Bit 9
5	Enable2 Pin (20) selected	Serial Bus selected - Bit 8
4	Enable1 Pin (11) selected	Serial Bus selected - Bit 7

Bits 9:7 can only be used if the appropriate bits 6:4 have been set to disable the external pins. If serial mode has been selected then the operation of bits 9:7 is the same as the external TX RXB, ENABLE1 and ENABLE2 pins respectively.

2.5   GSM/EDGE Baseband Control Register - Address 7

23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
																				0	1	1	1
OE	BB Gain			Q Offset								I Offset								Address			

This register is only used when in GSM/EDGE mode. The BB Gain bits enable the GSM baseband gain section to be reduced in 3 dB increments. The nominal gain is 35 dB (000). The I and Q offset bits allow the GAM baseband dc offset to be cancelled.

2.5.1   Q Channel Gain Adjust

Bits 22:20 adjust Q channel gain.

<22>	<21>	<20>	Gain Adjustment(dB)
0	0	0	0
0	0	1	-3
0	1	0	-6
0	1	1	-9
1	0	0	-12
1	0	1	-15
1	1	0	-18
1	1	1	-21

2.5.2   Baseband Offset Correction

Bits 19:12 adjust the dc offset for the Q channel. Bit 19 is the sign bit and bit 12 the LSB. Bits 11:4 adjust the dc offset for the I channel with bit 11 the sign bit and bit 4 the LSB. The coding is the same for both I and Q channels and is shown below:

00000000	**Maximum positive correction**
00000001	
01111110	
01111111	Zero positive correction
11111111	Zero negative correction
11111110	
10000001	
10000000	Maximum negative correction

Bit 23 must be set to '1' to enable dc offset correction.

2.6   Test Mode Register - Address 8

This register is used for test purposes only and should not be used.

2.7 UHF PLL Divider Programming Register - Address 9

23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
																0				1	0	0	1
M Counter Value													B Counter Value			x	A Counter Value			Address			

Bits 23:11 set M counter value (Bit 23 = MSB)
Bits 10:8 set B counter value - max value = 7 (Bit 10 = MSB)
Bits 7:4 set A counter value - max value = 7 (Bit 6 = MSB)
The A counter is a 4 bit counter to enable correct fractional N operation. Valid values of A are in the range 1 to 8.

Using the 64/65/72/73 four modulus prescaler the divide ratio (N) is given by:

$$N = 64 * M + 8 * B + A$$

Values of M, B, A can be easily calculated using the formulae in the synthesizer section.

2.8 UHF PLL Reference Divider and Fractional N Programming Register - Address 10

23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0																				1	0	1	0
X	Frac N Numerator					UHF PLL Reference Counter Value														Address			

Bit 23 is unused and should be set to '0'
Bits 22:18 set the fractional N numerator (Bit 22 = MSB)
Bits 17:4 set the Reference counter value (Bit 17 = MSB)

2.9 Receive VHF PLL Divider Programming Register - Address 11

23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0																		1	0	1	1
X	X	X	M Counter Value														A Counter Value			Address			

Bits 23:21 are unused and should be set to '0'
Bits 20:8 set M counter value (Bit 20 = MSB)
Bits 7:4 set A counter value - max value = 15 (Bit 7 = MSB)

Using the 16/17 two modulus prescaler the divide value (N) is given by:

$$N = 16 * M + A$$

Values of M, A can be easily calculated using the formulae in the synthesizer section, however the programming register has been organized to simplify this.

For example for a divide ratio of 13235, the binary equivalent is: 11001110110011. The programming values can be selected as shown below:

Bit No.	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4
Count Value	0	0	0	1	1	0	0	1	1	1	0	1	1	0	0	1	1
	M													A			

2.10 Receive VHF PLL Reference Divider Programming Register - Address 12

23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0																1	1	0	0
X	X	X	X	X	RS	Receive VHF PLL Reference Counter Value														Address			

Bits 23:19 are unused and should be set to '0'
Bit 18 selects common reference divider for VHF receive and transmit PLLs ('0' to select). If a common reference divider is selected then the transmit VHF reference divider is used which must be programmed in register 13.
Bits 17:4 set the Reference divider value (Bit 17 = MSB)

2.11 Transmit VHF PLL Divider Programming Register - Address 13

23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0																		1	1	0	1
X	X	X	M Counter Value													A Counter Value				Address			

Bits 23:21 are unused and should be set to '0'
Bits 20:8 set M counter value (Bit 20 = MSB)
Bits 7:4 set A counter value - max value = 15 (Bit 7 = MSB)

Programming is identical to that for the receive VHF PLL register 11.

2.12 Transmit VHF PLL Reference Divider Programming Register Address 14

23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0															1	1	1	0
X	X	X	X	X	X	Transmit VHF PLL Reference Counter Value														Address			

Bits 23:18 are unused and should be set to '0'
Bits 17:4 set the Reference counter value (Bit 17 = MSB)

2.13 PLL Lock Detect & Fractional N Compensation Programming Register Address 15

23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
																				1	1	1	1
Fractional N Compensation								UHF PLL Lock Count				Transmit VHF PLL Lock Count				Receive VHF PLL Lock Count				Address			

2.13.1   Fractional N Compensation

Bits 23:16 set the value for fractional N compensation in the UHF PLL with bit 23 as MSB. The value for the compensation is dependent on a number of parameters which are described in the synthesizer section.

2.13.2   PLL Lock detect counters

These 4 bit counters count the consecutive comparison cycles where the lock detect circuit gives an in-lock result. When the counter reaches its programmed count then that PLL is deemed to have achieved full lock. This prevents spurious false in-lock signals while the PLL is achieving lock up. There are separate counters for the UHF, Rx VHF and Tx VHF PLLs which are programmed as shown above. Bits 15,11,7 are the MSB's for the UHF, Rx VHF and Tx VHF PLL lock detector counters respectively. A non zero value must be programmed for the lock detect to operate correctly.

3.0   Absolute Maximum Ratings

Supply Voltage	-0.3 to 3.6V
Voltage applied to any pin	-0.3 to Vcc + 0.3 V
Operating Temperature	-40°C to 85°C
Storage Temperature	-55°C to 125°C
Max Junction Temperature	125°C

This device is sensitive to ESD. Most pins have an ESD rating greater than 2000V (Human Body Model HBM), however some pins have limited protection (800 to 2000V)in order to meet the RF performance. Anti-static precautions should be used when handling this device.

4.0   Operating Conditions

Device operation is guaranteed under the following coonditions:

Condition	Min	Value Typ	Max	Units	Comments
General					
Supply Voltage	2.7		3.3	V	
Operating Temperature	-40		+85	°C	
Logic Input Voltage High – VIH	0.8Vcc			Volts	
Logic Input Voltage Low – VIL			0.2Vcc	Volts	
TCXO Reference Frequency					
Frequency		13.0		MHz	GSM
Frequency		14.4		MHz	IS136
Frequency		19.44		MHz	IS136

Condition	Min	Value Typ	Max	Units	Comments
Receiver					
Receiver IF Frequency	70		215	MHz	
Transmitter					
Transmit IF Frequency	50		215	MHz	
I & Q common mode voltage		1.2		V	
I & Q input voltage level			1.5	V p-p	0dB input buffer gain
Cellular band LO input level	-15	-10	-5	dBm	
PCS band LO input level	-15	-10	-5	dBm	
Cellular band LO frequency	900		1100		
PCS1900 band frequency	1900		2200	MHz	
Serial Control Timing					See Figure 14
SDATA Set Up t1	20			ns	
SDATA Hold t2	20			ns	
SCLK Pulse Width t3	50			ns	
SLATCH Set up t4	20			ns	
Serial Control Timing (cont'd)					
SLATCH Pulse Width t5	50			ns	
SCLK Period t6	100			ns	
Power Control Set up t7	20			ns	

5.0　Electrical Characteristics

The electrical characteristics are guaranteed under the following conditions unless stated otherwise. Vcc =3.0 V, T = 25°C, TCXO Ref Frequency = 19.44 MHz.

Characteristics	Min	Value Typ	Max	Units	Comments
Supply Current					
Sleep		10	40	μA	Logic inputs = 0V or Vcc
Receive Operation					
AMPS		32	38	mA	Note 1, AGC = 1.6V
IS136		33	39	mA	Note 1, AGC = 1.6V
GSM/EDGE		30	36	mA	Note 1, AGC = 1.6V
Transmit Operation					
900 MHz Output		141	170	mA	VGA = 2.4V, Note 2
		106	125	mA	VGA = 1V , Note 2
1900 MHz Output		120	145	mA	VGA = 2.4V, Note 2
		102	120	mA	VGA = 1V, Note 2
Standby Operation					
UHF PLL		12.5	15.0	mA	Note 3
Receive VHF PLL		5.2	6.3	mA	
Transmit VHF PLL		4.9	6.0	mA	
Additional Circuits					
Frequency Doubler		4	5	mA	Note 4
UHF LO Output Buffer		4.5	5.5	mA	900 or 1900 Band Note 5
Logic Inputs					
Input Current			10	nA	Vin = 0 to Vcc
Input Capacitance			10	pF	
Lock Detect Output					

Characteristics	Min	Value Typ	Max	Units	Comments
Output Voltage Low			0.2Vcc	Volts	I out = 1mA
Output Voltage High	0.8Vcc			Volts	I out = -1 mA
TCXO Input					
Input Resistance	10			kΩ	
Input Capacitance			10	pF	
Input Sensitivity	0.5		2	V p-p	ac coupled
Receiver - IS136					All parameters are measured at an IF frequency of 135.06 MHz, Rx VCO = 270 MHz unless stated otherwise
Input impedance	500		1500	Ω	
Max Voltage Gain	80	91		dB	AGC = 2.4 V
Min Voltage Gain		-13	5	dB	AGC = 0.3 V
Gain slope	50	56	62	dB/V	AGC = 0.3 to 2V
NF Gainmax		8		dB	Rs =800Ω
Input V1dB Gainmin	101	104		dBμV	Minimum gain
IIP3 Gainmax		74		dBμV	Max Gain
I/Q Amplitude Matching			+/- 0.5	dB	
I/Q Quadrature Accuracy			+/- 2	°	
Output 1dB Compression	3			V p-p	
Output dc Offset			+/-20	mV	
Receiver AMPS (Fixed Gain)					All parameters are measured at an IF frequency of 135.06 MHz, Rx VCO = 270 MHz unless stated otherwise. Vagc = 1.6V (Gain 20 dB below maximum)
Input impedance	500		1500	Ω	
Input Sensitivity		14		dBμV	Note 6
Noise Figure		12		dB	
Input IP3		93		dBμV	

Characteristics	Min	Value Typ	Max	Units	Comments
Audio Output	900	1000	1100	mV	Note 7
RSSI Dynamic Range		50		dB	
Accuracy	-3		+3	dB	
RSSI Slope		16		mV/dB	
Input Signal - Min		25		dBμV	
Input Signal - Max		75		dBμV	
Min RSSI Level	0.35	0.5	0.70		
Max RSSI Level	1.45	1.55	1.65	V	
RSSI Output Impedance		1		kΩ	
Bandpass Filter IS136 and AMPS					Narrow bandwidth mode
Centre Frequency		60		kHz	
3dB Bandwidth	+/- 16		+/- 18	kHz	
Stop Band Attenuation					Relative to signal at 60kHz
0 to 3 kHz	67	69		dB	
3 kHz to 10 kHz	61	63		dB	
10 kHz to 22 kHz	48	51		dB	
38 kHz	18	20		dB	
82 kHz	18	20		dB	
98 kHz to 110 kHz	48	50		dB	
110 kHz to 117 kHz	61	63		dB	
117 kHz to 123 kHz	68	70		dB	
123 kHz to 1.36 MHz	71	73		dB	
1.36 MHz to 1.52 MHz	36	48		dB	
1.52 MHz to 10 MHz	71	73		dB	
Image Attenuation					
0 to -10kHz	61			dB	
-10 kHz to -42 kHz	40			dB	

Characteristics	Min	Value Typ	Max	Units	Comments
- 42 kHz to -78 kHz	30	40		dB	
- 78 kHz to -105 kHz	40			dB	
-105 kHz to -1.36 MHz	61			dB	
-1.36 MHz to -1.52 MHz	36	48		dB	
-1.52 MHz to -10 MHz	61			dB	
Gain Ripple		1.0	1.5	dB	60kHz +/- 12.5kHz
Receiver - GSM					All parameters are measured at an IF frequency of 135.0 MHz, Rx VCO = 270 MHz unless stated otherwise. TCXO = 13.0MHz.
IF Frequency	70		215	MHz	
Input impedance	500		1500	Ω	
Max Voltage Gain	80	91		dB	AGC = 2.4 V
Min Voltage Gain		-13	+5	dB	AGC = 0.3 V
Gain slope	50	56	62	dB/V	AGC = 0.3 to 2V
NF Gainmax		8		dB	Rs =800Ω
Input V1dB Gainmin	100	104		dBμV	Minimum gain
IIP3 Gainmax		73		dBμV	Max Gain
Baseband filter attenuation					
100kHz			1	dB	
315kHz	15			dB	
600kHz	30			dB	
10MHz	60			dB	
Filter Ripple			1	dB	0 to 100kHz
Output dc Offset		10	20	mV	After offset calibration. Maximum Base band gain
I/Q Amplitude Matching			+/- 0.5	dB	
I/Q Quadrature Accuracy			+/- 2	°	
Output 1dB Compression	3			V p-p	

Characteristics	Min	Value Typ	Max	Units	Comments
Baseband Gain Adjust	-21		0	dB	3dB steps
Baseband Gain Step Resolution		3		dB	
Transmitter					All parameters are measured at an IF frequency of 180.0 MHz, Tx VCO = 360 MHz unless stated otherwise
I & Q modulator					
I/Q Input Buffer Gain	-1	0	+1	dB	
I/Q Input Buffer Gain		3		dB	
I/Q Input Buffer Gain		6		dB	
I/Q Input Buffer Gain		9		dB	
I/Q Input Buffer Gain		12		dB	
I & Q differential input resistance	80			kΩ	
I & Q Baseband Filter Attenuation (IS136/AMPS)					
dc - 12.5 kHz			0.5	dB	
85 - 180 kHz	12	17		dB	
> 180 kHz	25	33		dB	
I & Q Baseband Filter Attenuation (GSM/EDGE)					
dc to 100kHz			1	dB	
> 4MHz	55dB			dB	
Carrier Suppression	30	40		dB	
Sideband Suppression	30	40		dB	
IF Variable gain amplifiers					
Gain control range	45	60		dB	
Control voltage for minimum gain	0.10			V	
Control voltage for maximum gain			2.4	V	
AGC control voltage slope	33	38	43	dB/V	VGA = 0.5 to 1.2V

Characteristics	Min	Value Typ	Max	Units	Comments
IF Output Filter (option)					
IF output impedance		500		Ω	To external filter
IF input impedance		1.5		kΩ	From external filter
IF output level		100		mV	
800MHz RF output stage					Specifications assume 50 ohm load driven via a matching network. Output Frequency = 836 MHz, UHF LO = -10 dBm at 1016 MHz.
RF amplifier operating frequency range	824		849	MHz	
Output power	+8	+10		dBm	
ACPR (TDMA)		-36		dBc	Pout = +8dBm, Offset = 30kHz
		-56		dBc	Pout = +8dBm, Offset = 60kHz
Output power AMPS	+10	+14		dBm	
Receive band noise (869 - 894 MHz)		-124		dBm/Hz	ftx = 849 MHz Pout = +8dBm With external IF filter
Spurious Outputs					
LO Leakage		-25	-21	dBc	Pout = +8dBm
Image Rejection		-27	-21	dBc	Pout = +8dBm
Other Spurii			-20	dBm	
1900MHz RF output stage (PCS)					Specifications assume 50 ohm load driven via a matching network Output Frequency = 1880 MHz, UHF LO = -10 dBm at 2060 MHz.
RF amplifier operating frequency range	1.88		1.91	GHz	
Output power	+8	+10		dBm	
ACPR (TDMA)		-36		dBc	Pout = +8dBm, Offset = 30kHz
		-56		dBc	Pout = +8dBm, Offset = 60kHz

Characteristics	Min	Value Typ	Max	Units	Comments
Receive band noise (1930-1990 MHz)		-128		dBm/Hz	ftx = 1910 MHz, Pout = +8dBm With external IF filter
Spurious Outputs					
LO Leakage		-30	-25	dBc	Pout = +8dBm
Image Rejection		-30	-25	dBc	Pout = +8dBm
Other Spurii			-20	dBm	
UHF Synthesiser					
Input Frequency	800		2200	MHz	
Charge Pump Current	0.9	1	1.1	mA	
	0.45	0.5	0.55	mA	
	0.22	0.25	0.28	mA	
	0.11	0.125	0.14	mA	
Charge Pump Output Compliance	0.4		Vdd - 0.4	V	Less than +/-10 % variation in Iout
Charge Pump sink/source mismatch			15	%	
Charge Pump off-state current		5		nA	
Fractional Compensation	88	98	108	µA	Full Scale
UHF Buffers					
Load Impedance		200		Ω	
Output Level (900 and 1900)		-11		dBm	Load = 200 ohms
Harmonic Level		-40		dBc	LO1900 Output
Rx and Tx IF Synthesisers					
Input Frequency	100		430	MHz	
Charge Pump Current	0.9	1	1.1	mA	
	0.45	0.5	0.55	mA	
	0.22	0.25	0.28	mA	
	0.11	0.125	0.14	mA	

Characteristics	Min	Value Typ	Max	Units	Comments
Charge Pump Output Compliance	0.4		Vcc - 0.4	V	Less than +/-10 % variation in Iout
Charge Pump sink/source mismatch			15	%	
Charge Pump off-state current		5		nA	
Rx LO Oscillator					
Frequency	140		430	MHz	
Phase Noise		-99		dBc/Hz	Freq = 270 MHz, Offset = 30 kHz
Tx LO Oscillator					
Frequency	260		430	MHz	
Phase Noise		-99		dBc/Hz	Freq = 360 MHz, Offset = 30 kHz

Note 1:　All receive currents include all receiver sections plus Rx VHF and UHF PLL's, and UHF LO input buffer circuits. The LO output buffer and frequency doubler are not included.
Note 2:　All transmit currents include all transmit sections plus Tx VHF and UHF PLL's, and UHF LO input buffer circuits. The LO output buffer and frequency doubler are not included.
Note 3:　Includes UHF LO input buffer
Note 4:　This is only applicable in 1900 MHz band
Note 5:　The UHF LO output buffer need only be powered up if required to drive an external circuit, for example, a receive front end mixer.
Note 6:　Input signal FM modulated with 8 kHz deviation by 1 kHz modulating signal. Specification is minimum input level to obtain 12 dB SINAD at FM Output (pin 45) using CCITT filter.
Note 7:　Input modulation: 1kHz modulating signal with 8 kHz deviation. Output level at FM out (pin 45) is set by external components. See application section for details.

6.0 Typical Performance Curves

6.1 Receive

Rx. RSSI

6.2 Transmit

IS136 Tx. 1900 MHz - Icc v AGC (Vcc)

IS136 Tx.1900 MHz - Icc v AGC (Temperature)

IS136 Tx. 900 MHz - Power Out v AGC (Vcc)

IS136 Tx. 900 MHz - Power Out v AGC (Temp.)

IS136 Tx. 1900 MHz - Power Out v AGC (Vcc)

IS136 Tx 1900MHz - Power Out v AGC (Temp.)

TOP VIEW

See Note 8.
INDEX AREA
(D/2 X E/2)

SEATING PLANE

BOTTOM VIEW
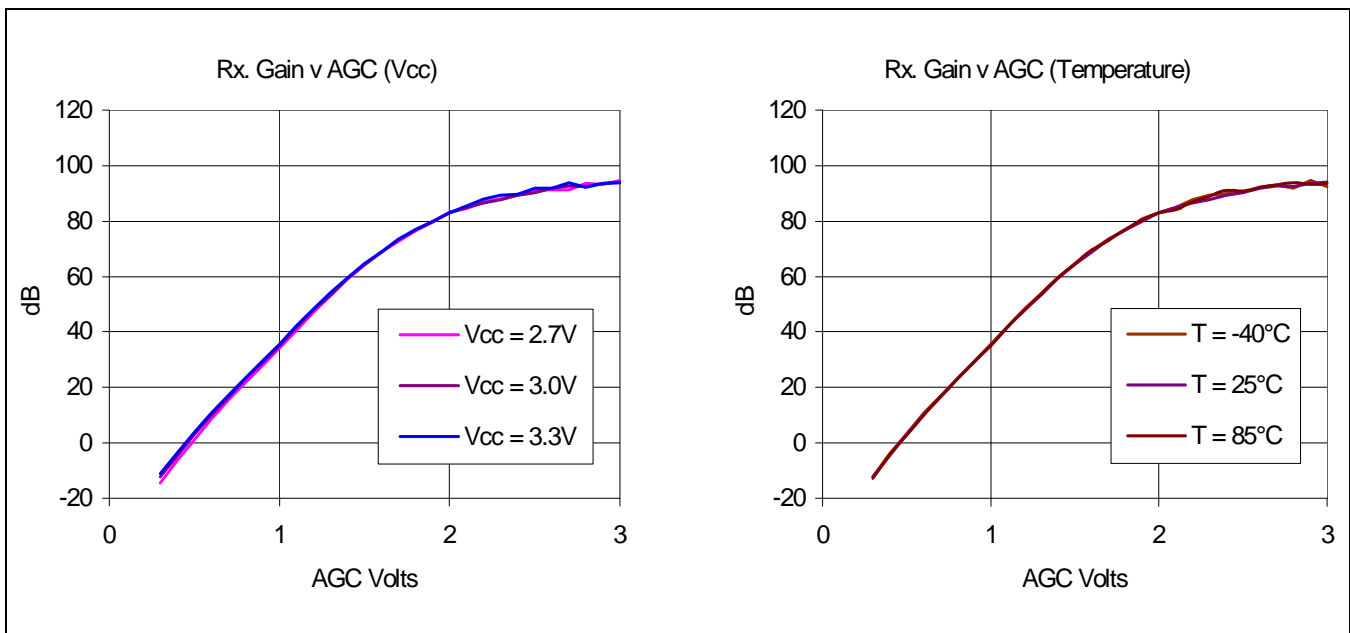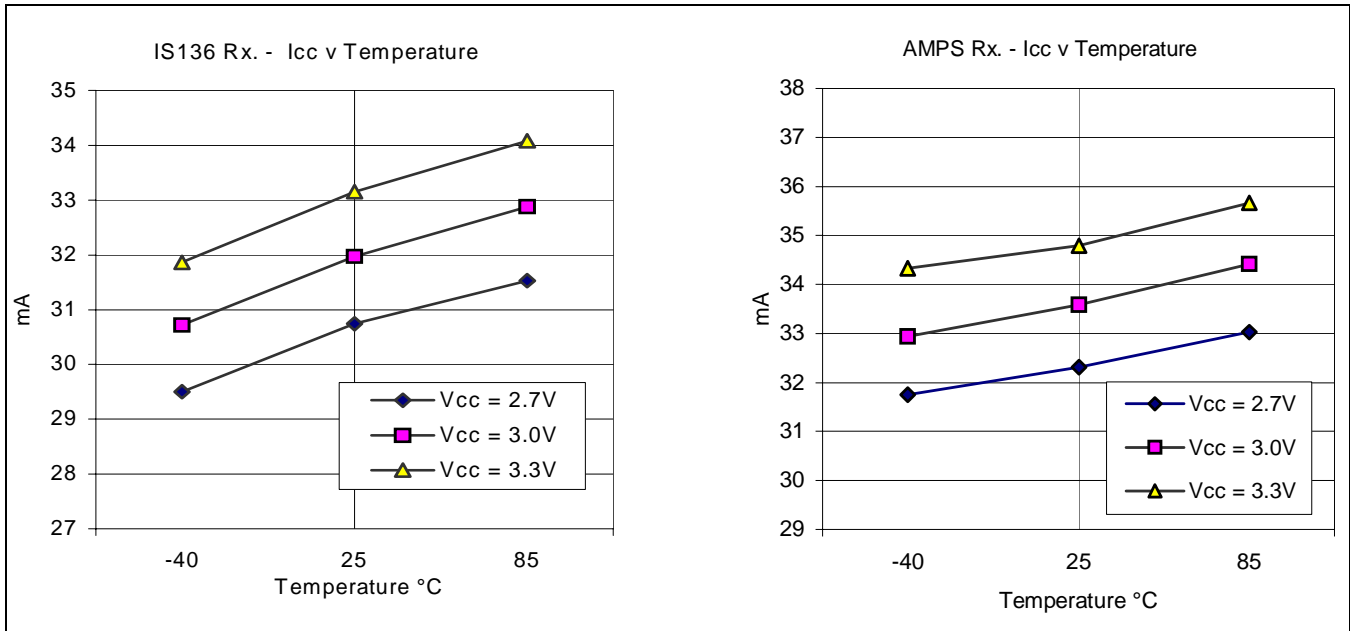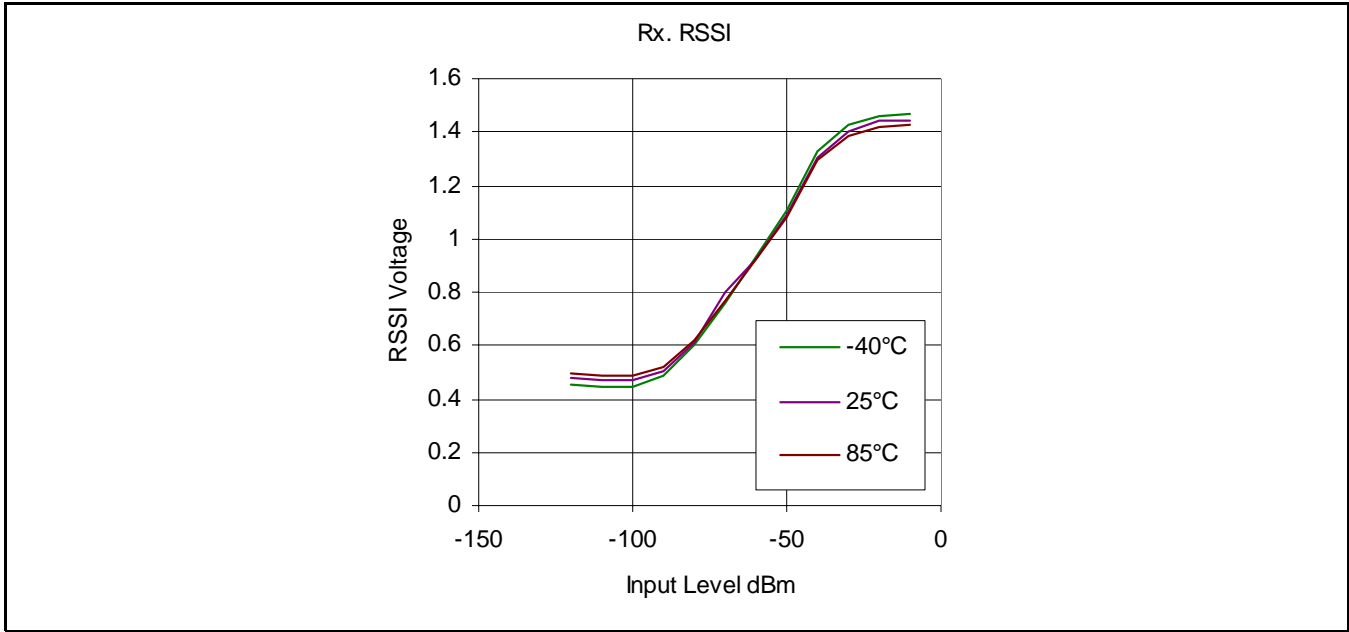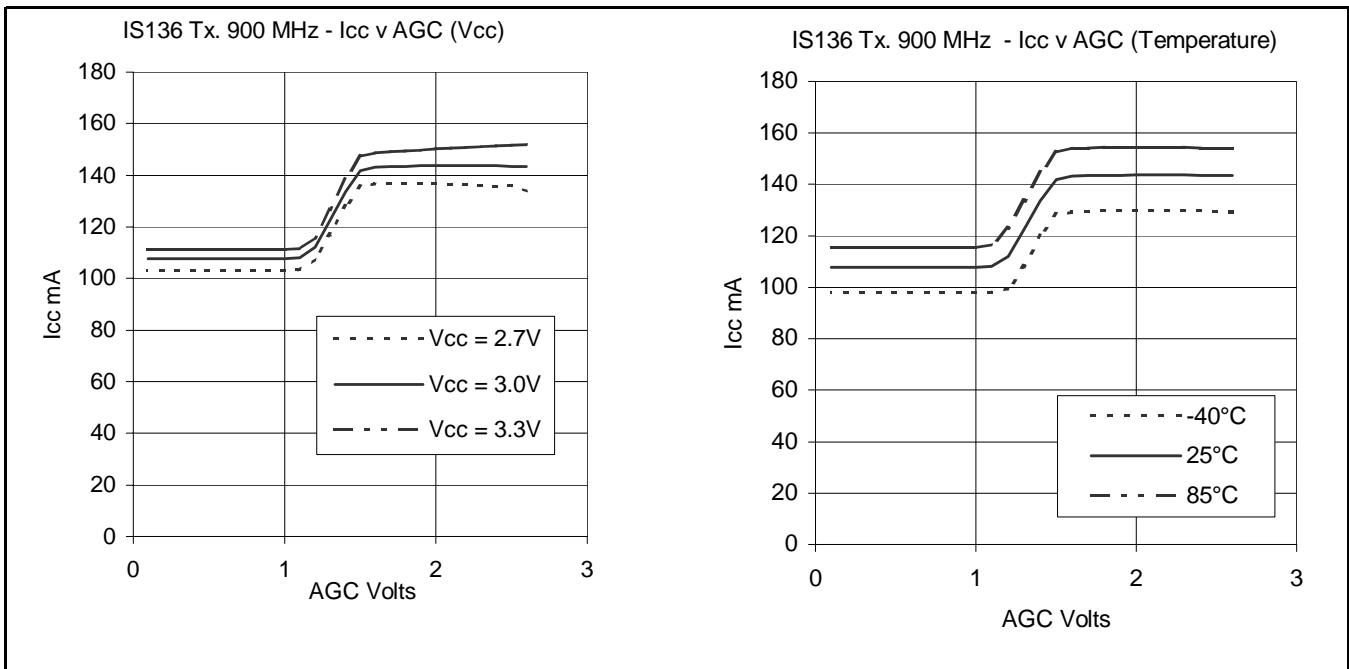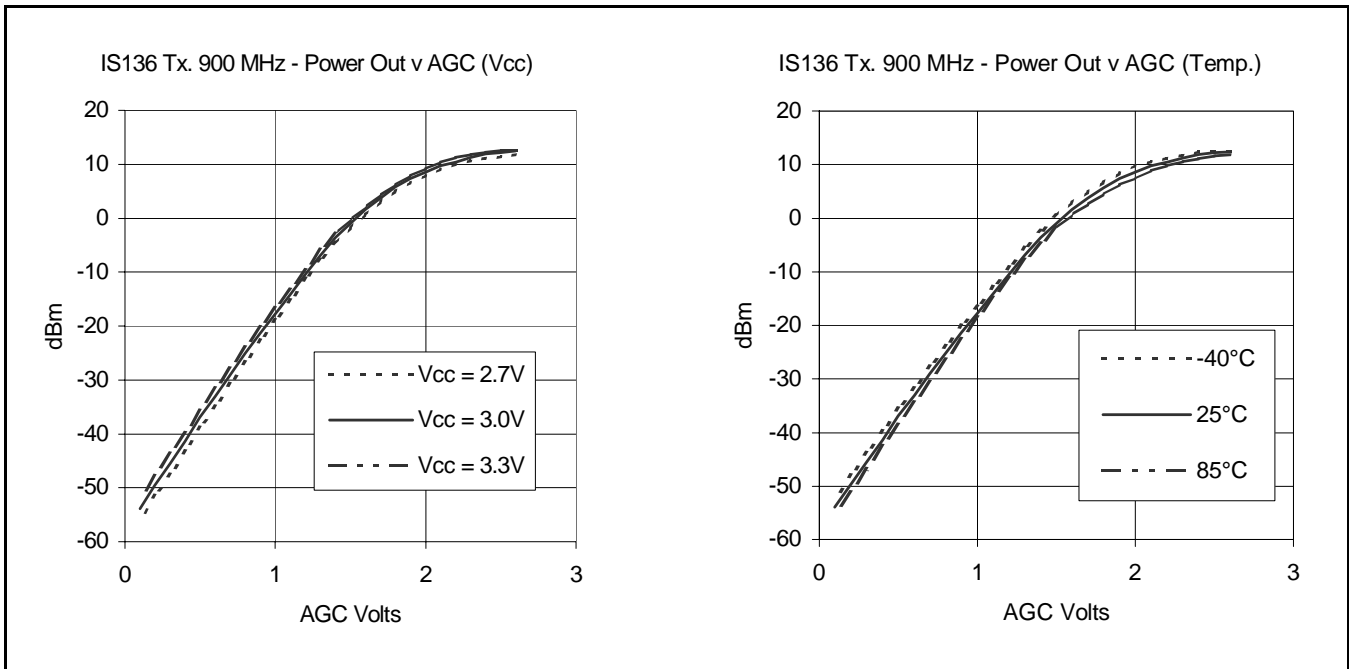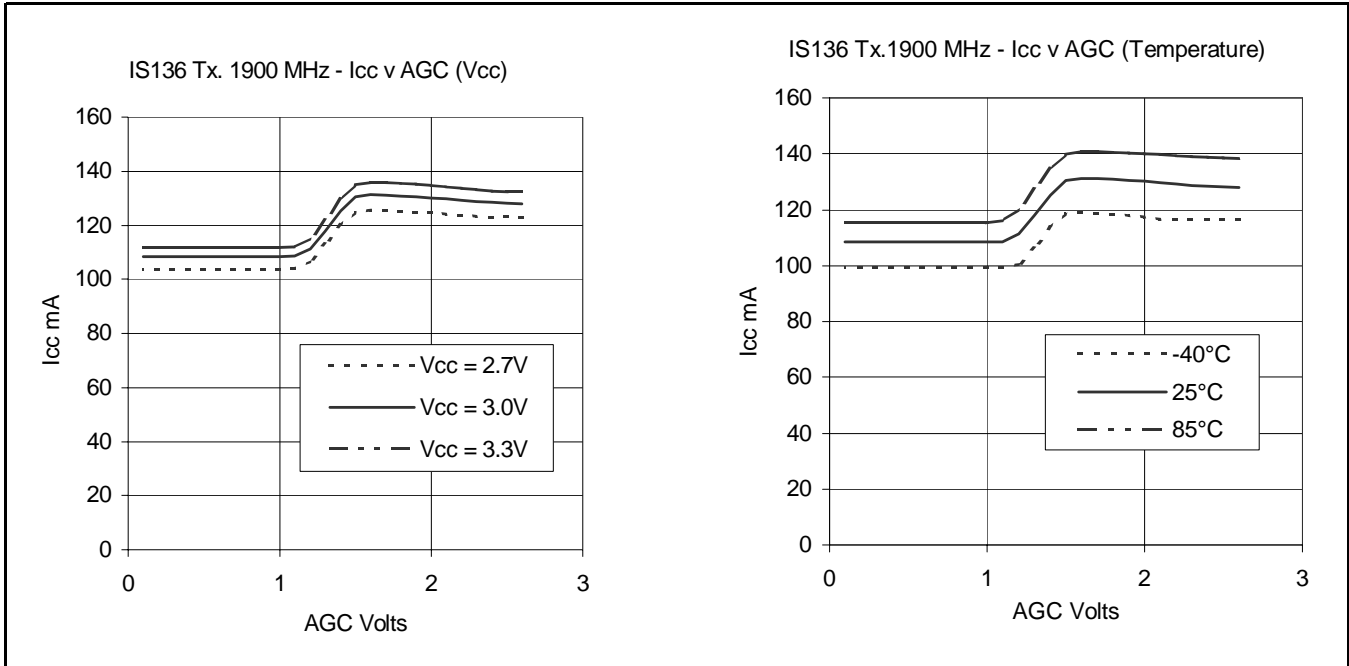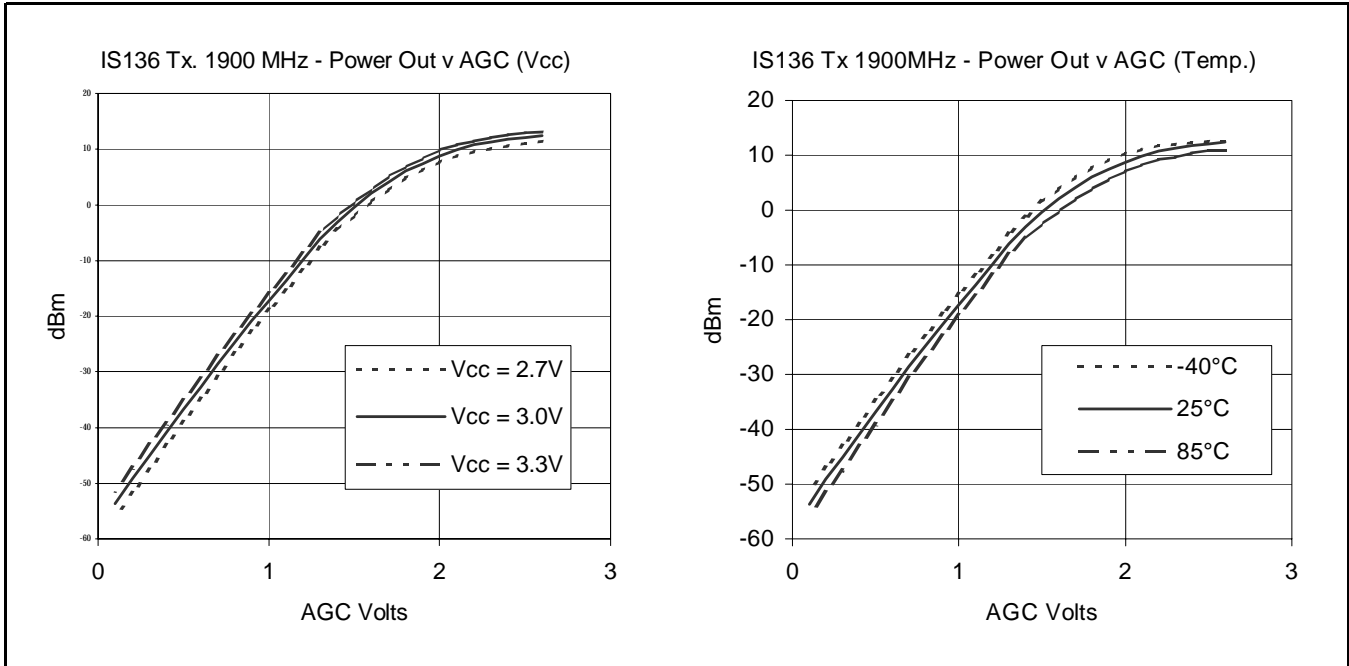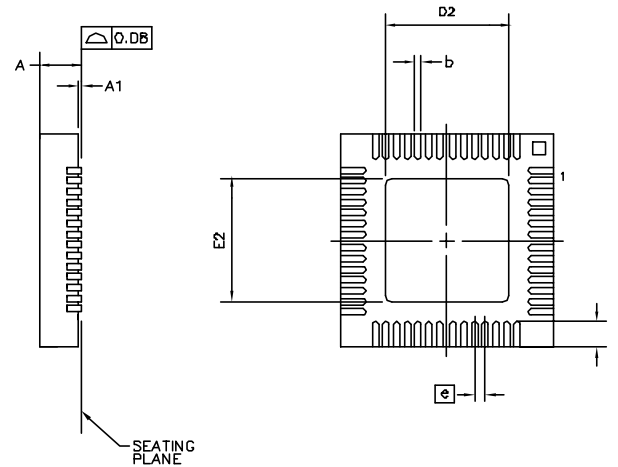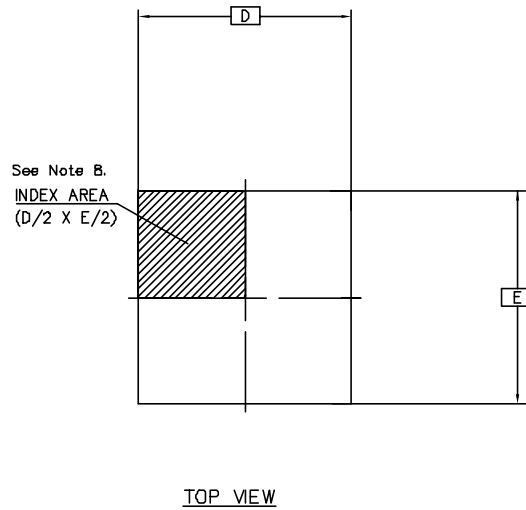
S Y M B O L	COMMON DIMENSIONS	
	MIN.	MAX.
A	0.80	1.00
A1	0.00	0.05
b	0.18	0.30
D	8.00 BSC	
D2	6.00	6.25
E	8.00 BSC	
E2	6.00	6.25
N	56	
Nd	14	
Ne	14	
e	0.50 BSC	
L	0.30	0.75

NOTES: 1. DIMENSIONING & TOLERANCES CONFORM TO ASME Y14.5M. – 1994.
2. N IS THE NUMBER OF TERMINALS.
   Nd & Ne ARE THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED
   BETWEEN 0.25 AND 0.30mm FROM TERMINAL.
4. ALL DIMENSIONS ARE IN MILLIMETERS.
5. LEAD COUNT IS 56.
6. PACKAGE WARPAGE MAX 0.08mm.
7. NOT TO SCALE.
8. TERMINAL #1 IDENTIFIER MUST BE LOCATED WITHIN THE ZONE INDICATED AND MAY BE EITHER A MOULD OR MARKED FEATURE.
   PIN # 1 IDENTIFICATION ON PACKAGE BOTTOM IS METAL TERMINAL (SHORTED TO EXPOSED PAD)

ISSUE	1	2		
ACN	211130	213841		
DATE	16Jun01	12Dec02		
APPRD.				

ZARLINK SEMICONDUCTOR

Package Code

Previous package codes
LH

Package Outline for 56 Lead (8x8)mm, (LC)

GPD00770

ZARLINK
SEMICONDUCTOR

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