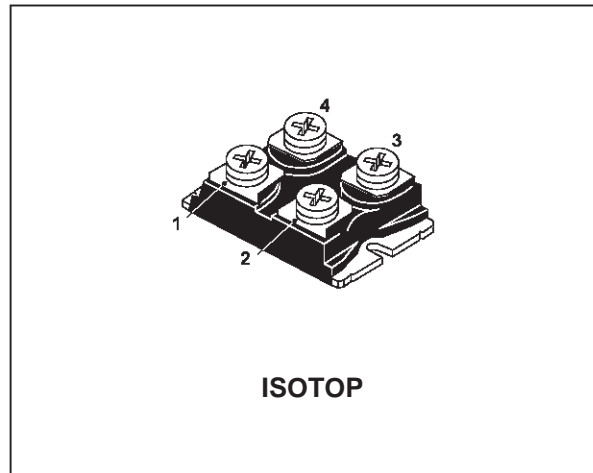


N - CHANNEL ENHANCEMENT MODE FAST POWER MOS TRANSISTOR

TYPE	V _{DSS}	R _{DS(on)}	I _D
STE53NA50	500 V	< 0.085 Ω	53 A

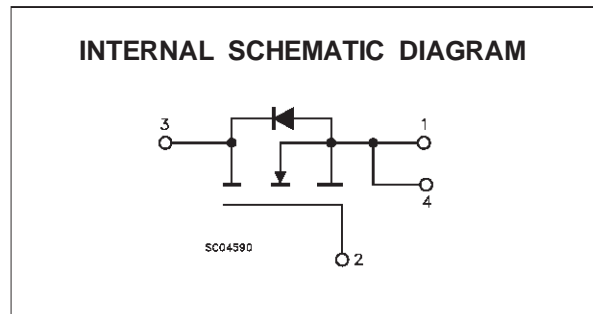
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- TYPICAL R_{DS(on)} = 0.075 Ω
- HIGH CURRENT POWER MODULE
- AVALANCHE RUGGED TECHNOLOGY
- VERY LARGE SOA - LARGE PEAK POWER CAPABILITY
- EASY TO MOUNT
- SAME CURRENT CAPABILITY FOR THE TWO SOURCE TERMINALS
- EXTREMELY LOW R_{th} (Junction to case)
- VERY LOW INTERNAL PARASITIC INDUCTANCE
- ISOLATED PACKAGE UL RECOGNIZED



APPLICATIONS

- SMPS & UPS
- MOTOR CONTROL
- WELDING EQUIPMENT
- OUTPUT STAGE FOR PWM, ULTRASONIC CIRCUITS



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V _{DS}	Drain-source Voltage (V _{GS} = 0)	500	V
V _{DGR}	Drain- gate Voltage (R _{GS} = 20 kΩ)	500	V
V _{GS}	Gate-source Voltage	± 30	V
I _D	Drain Current (continuous) at T _c = 25 °C	53	A
I _D	Drain Current (continuous) at T _c = 100 °C	33	A
I _{DM} (●)	Drain Current (pulsed)	212	A
P _{tot}	Total Dissipation at T _c = 25 °C	460	W
	Derating Factor	3.68	W/°C
T _{stg}	Storage Temperature	-55 to 150	°C
T _j	Max. Operating Junction Temperature	150	°C
V _{ISO}	Insulation Withstand Voltage (AC-RMS)	2500	V

(●) Pulse width limited by safe operating area

February 1998

1/7

STE53NA50

THERMAL DATA

$R_{thj-case}$	Thermal Resistance Junction-case	Max	0.27	$^{\circ}C/W$
R_{thc-h}	Thermal Resistance Case-heatsink With Conductive Grease Applied	Max	0.05	$^{\circ}C/W$

AVALANCHE CHARACTERISTICS

Symbol	Parameter	Max Value	Unit
I_{AR}	Avalanche Current, Repetitive or Not-Repetitive (pulse width limited by T_j max, $\delta < 1\%$)	26	A
E_{AS}	Single Pulse Avalanche Energy (starting $T_j = 25^{\circ}C$, $I_D = I_{AR}$, $V_{DD} = 50 V$)	1014	mJ

ELECTRICAL CHARACTERISTICS ($T_{case} = 25^{\circ}C$ unless otherwise specified)

OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source Breakdown Voltage	$I_D = 1 mA$ $V_{GS} = 0$	500			V
I_{DSS}	Zero Gate Voltage Drain Current ($V_{GS} = 0$)	$V_{DS} = \text{Max Rating}$ $V_{DS} = \text{Max Rating}$ $T_c = 125^{\circ}C$			100 1000	μA μA
I_{GSS}	Gate-body Leakage Current ($V_{DS} = 0$)	$V_{GS} = \pm 30 V$			± 400	nA

ON (*)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}$ $I_D = 1 mA$	2.25	3	3.75	V
$R_{DS(on)}$	Static Drain-source On Resistance	$V_{GS} = 10V$ $I_D = 27 A$		0.075	0.085	Ω
$I_{D(on)}$	On State Drain Current	$V_{DS} > I_{D(on)} \times R_{DS(on)max}$ $V_{GS} = 10 V$	53			A

DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$g_{fs} (*)$	Forward Transconductance	$V_{DS} > I_{D(on)} \times R_{DS(on)MAX}$ $I_D = 27 A$	25			S
C_{iss}	Input Capacitance	$V_{DS} = 25 V$ $f = 1 MHz$ $V_{GS} = 0$		13	16	nF
C_{oss}	Output Capacitance			1500	2000	pF
C_{rss}	Reverse Transfer Capacitance			450	650	pF

ELECTRICAL CHARACTERISTICS (continued)

SWITCHING ON

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on Time	$V_{DD} = 250\text{ V}$ $I_D = 27\text{ A}$		57	80	ns
t_r	Rise Time	$R_G = 4.7\ \Omega$ $V_{GS} = 10\text{ V}$ (see test circuit, figure 1)		92	130	ns
Q_g	Total Gate Charge	$V_{DD} = 400\text{ V}$ $I_D = 53\text{ A}$ $V_{GS} = 10\text{ V}$		470	658	nC
Q_{gs}	Gate-Source Charge			54		nC
Q_{gd}	Gate-Drain Charge			219		nC

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SWITCHING OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{r(Voff)}$	Off-voltage Rise Time	$V_{DD} = 400\text{ V}$ $I_D = 53\text{ A}$		105	145	ns
t_f	Fall Time	$R_G = 4.7\ \Omega$ $V_{GS} = 10\text{ V}$		36	50	ns
t_c	Cross-over Time	(see test circuit, figure 3)		145	205	ns

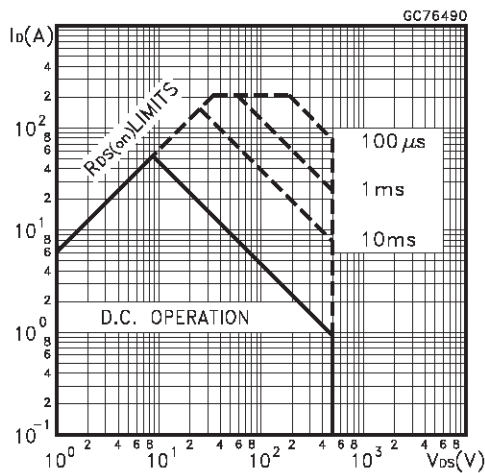
SOURCE DRAIN DIODE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain Current				53	A
$I_{SDM}(\bullet)$	Source-drain Current (pulsed)				212	A
$V_{SD} (*)$	Forward On Voltage	$I_{SD} = 53\text{ A}$ $V_{GS} = 0$			1.6	V
t_{rr}	Reverse Recovery Time	$I_{SD} = 53\text{ A}$ $di/dt = 100\text{ A}/\mu\text{s}$ $V_R = 100\text{ V}$ $T_j = 150\text{ }^\circ\text{C}$ (see test circuit, figure 3)		1000		ns
Q_{rr}	Reverse Recovery Charge			31.5		μC
I_{RRM}	Reverse Recovery Current			63		A

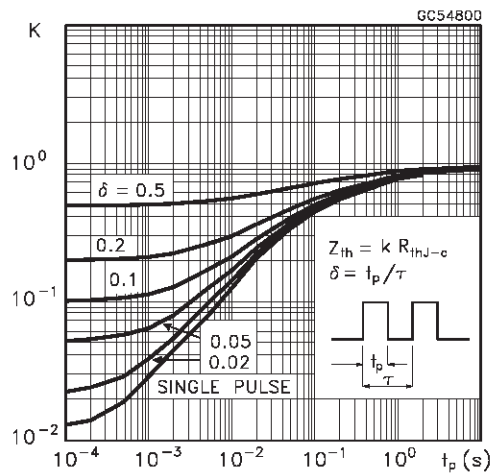
(*) Pulsed: Pulse duration = 300 μs , duty cycle 1.5 %

(\bullet) Pulse width limited by safe operating area

Safe Operating Area for

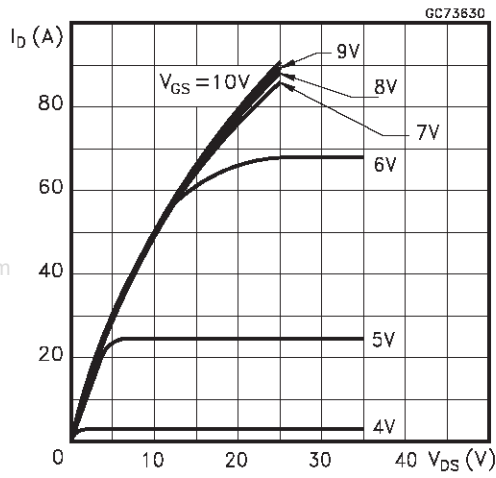


Thermal Impedance

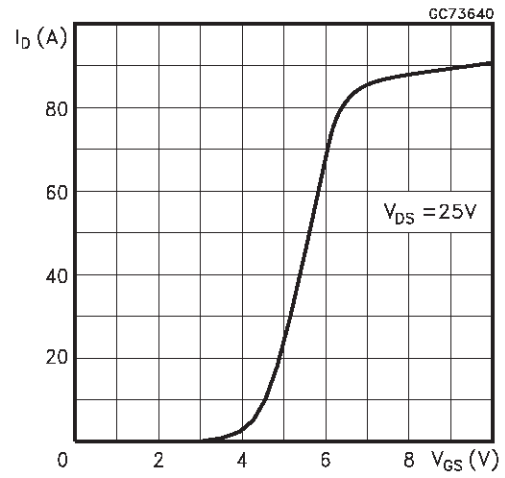


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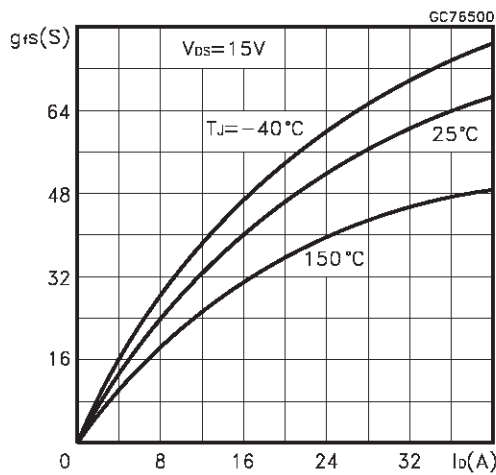
Output Characteristics



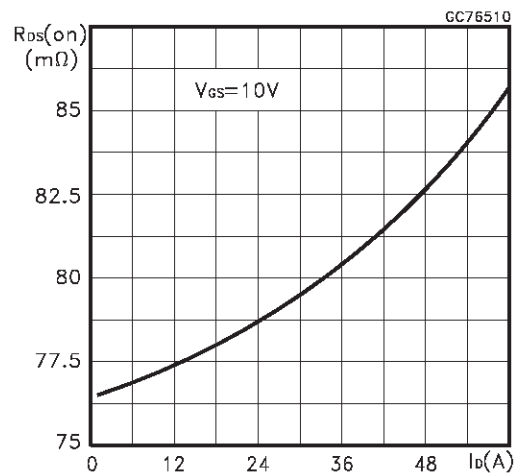
Transfer Characteristics



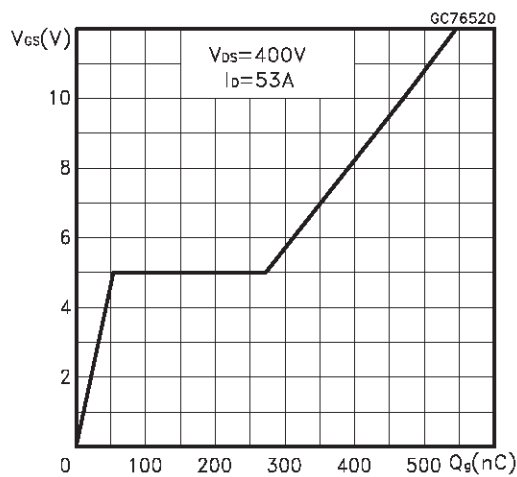
Transconductance



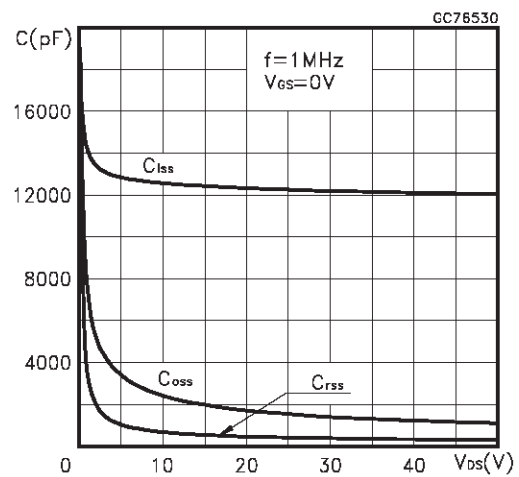
Static Drain-source On Resistance



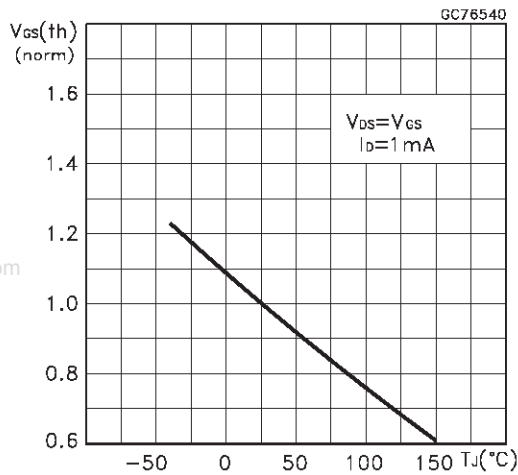
Gate Charge vs Gate-source Voltage



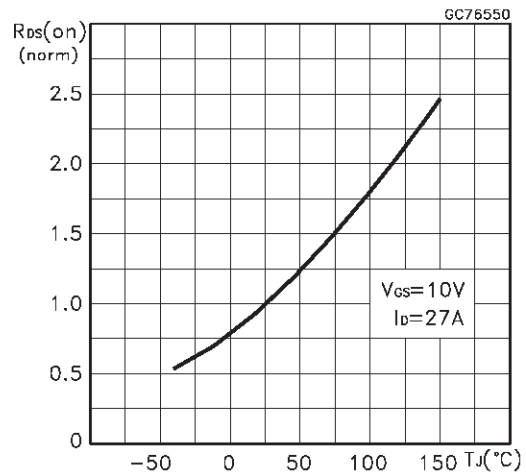
Capacitance Variations



Normalized Gate Threshold Voltage vs Temperature



Normalized On Resistance vs Temperature



Source-drain Diode Forward Characteristics

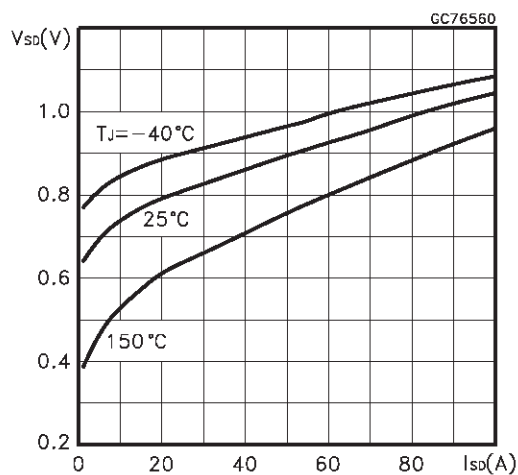


Fig. 1: Switching Times Test Circuits For Resistive Load

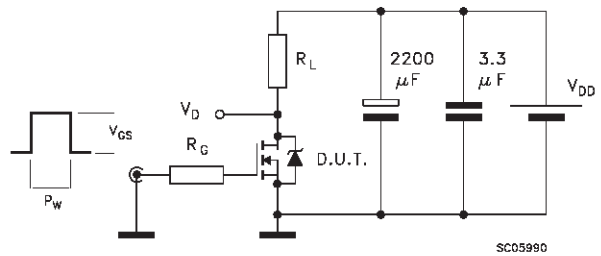


Fig. 2: Gate Charge test Circuit

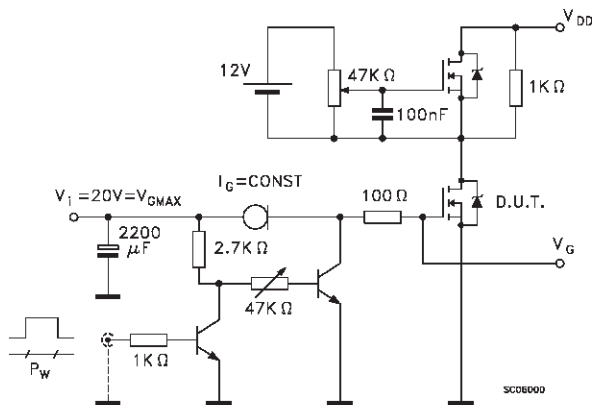
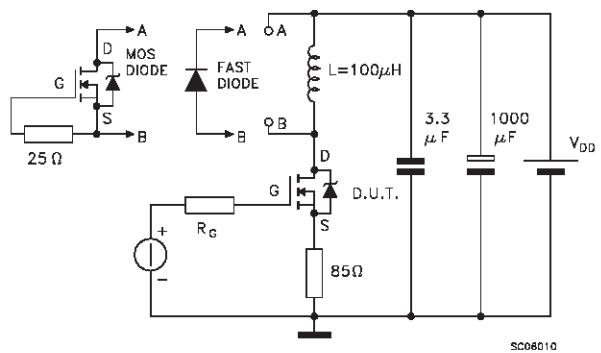
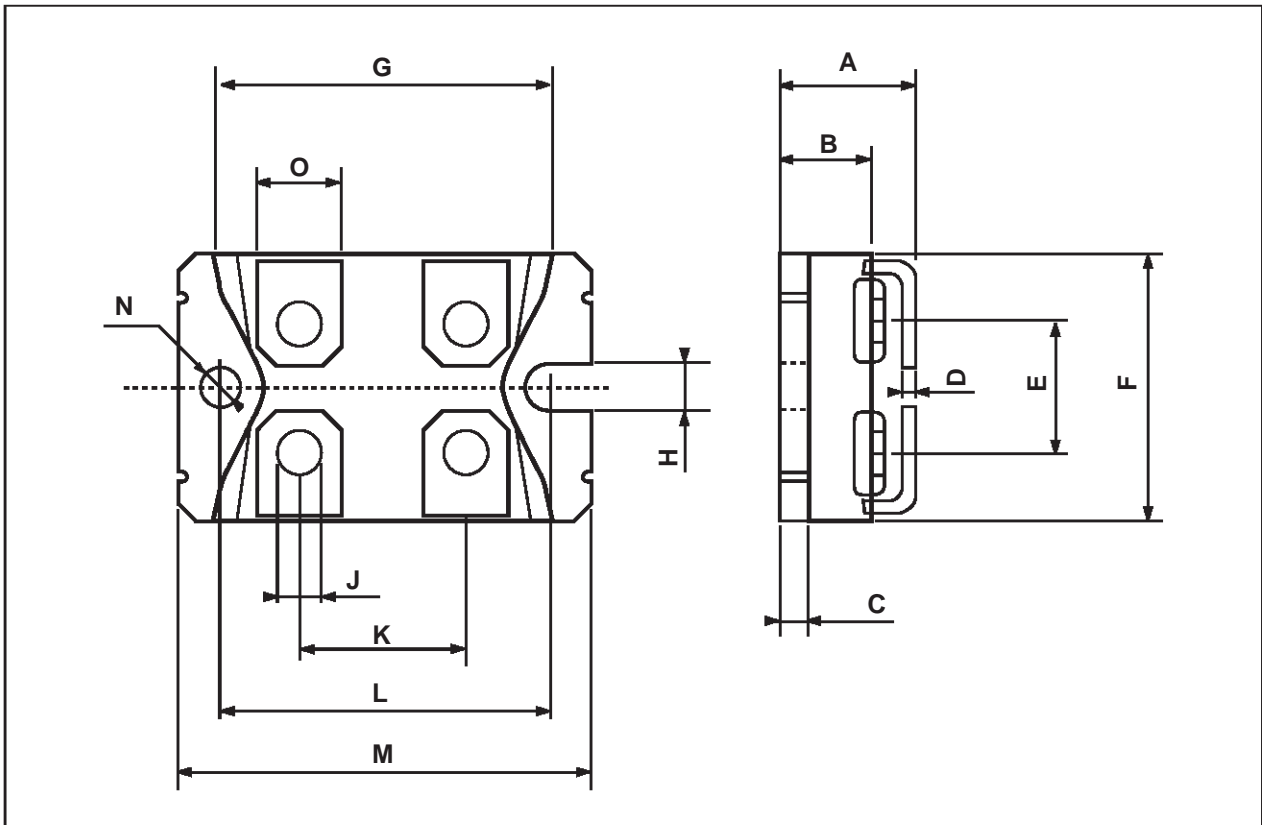


Fig. 3: Test Circuit For Inductive Load Switching And Diode Recovery Times



ISOTOP MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	11.8		12.2	0.466		0.480
B	8.9		9.1	0.350		0.358
C	1.95		2.05	0.076		0.080
D	0.75		0.85	0.029		0.033
E	12.6		12.8	0.496		0.503
F	25.15		25.5	0.990		1.003
G	31.5		31.7	1.240		1.248
H	4			0.157		
J	4.1		4.3	0.161		0.169
K	14.9		15.1	0.586		0.594
L	30.1		30.3	1.185		1.193
M	37.8		38.2	1.488		1.503
N	4			0.157		
O	7.8		8.2	0.307		0.322



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