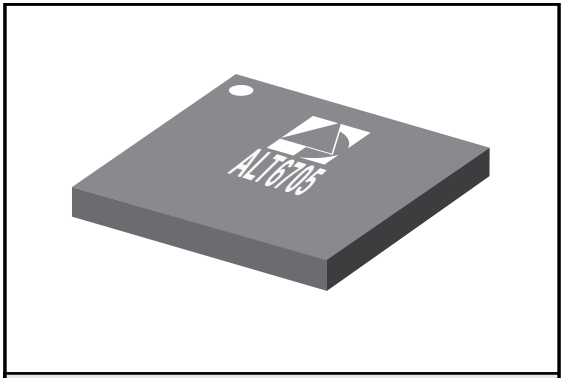
ALT6705

HELP4™ UMTS800 (Bands 5, 6, 18, 19, & 26)
LTE, WCDMA, CDMA Multimode PAM

Data Sheet - Rev 2.5

FEATURES

- Multimode (LTE, HSPA, EV-DO Compliant)
- 4th Generation HELP™ technology
- High Efficiency (R99 waveform):
  - 40 % @ POUT = +28.4 dBm
  - 27 % @ POUT = +17 dBm
  - 18 % @ POUT = +13.5 dBm
  - 20 % @ POUT = +8 dBm
  - 11 % @ POUT = +3.5 dBm
- Low Quiescent Current: 3 mA
- Low Leakage Current in Shutdown Mode: <5 μA
- Internal Voltage Regulator
- Integrated "daisy chainable" directional coupler with CPLIN and CPLOUT port
- Internal DC Blocks on all RF ports
- Optimized for a 50 Ω System
- 1.8V Control Logic
- RoHS Compliant Package, 260 °C MSL-3



M45 Package
10 Pin 3 mm x 3 mm x 1 mm
Surface Mount Module

APPLICATIONS

- Bands 5, 6, 18, 19, & 26 LTE Wireless Devices
- Bands 5, 6, 18, 19, & 26 WCDMA/HSPA Wireless Devices
- Band Class 0 CDMA/EVDO Wireless Devices

PRODUCT DESCRIPTION

The ALT6705 HELP4™ PA is the 4th generation HELP™ product for LTE and WCDMA devices operating in UMTS800 (Bands 5, 6, 18,19, & 26) and for CDMA devices operating in Cell-band. This PA incorporates ANADIGICS' HELP4™ technology to deliver exceptional efficiency at low power levels and low quiescent current without the need for external voltage regulators or converters. The device is manufactured using advanced InGaP-*Plus*™ HBT technology offering state-of-the-art reliability, temperature stability, and ruggedness. Three selectable bias modes that optimize efficiency for different output power levels and a shutdown mode with low leakage current increase handset talk and standby time. A "daisy chainable" directional coupler is integrated in the module thus eliminating the need of an external coupler. The self-contained 3 mm x 3 mm x 1 mm surface mount package incorporates matching networks optimized for output power, efficiency, and linearity in a 50 Ω system.

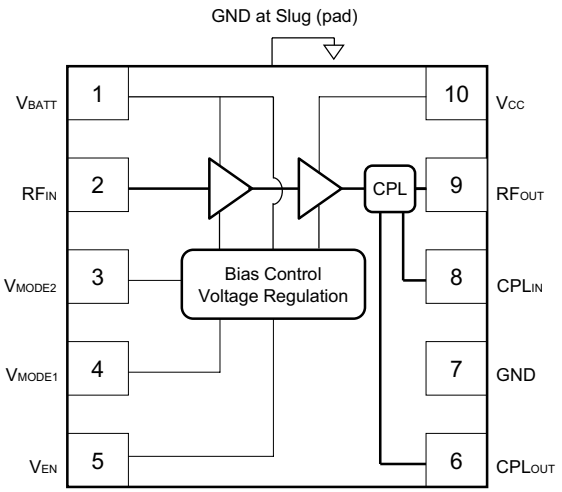


Figure 1: Block Diagram

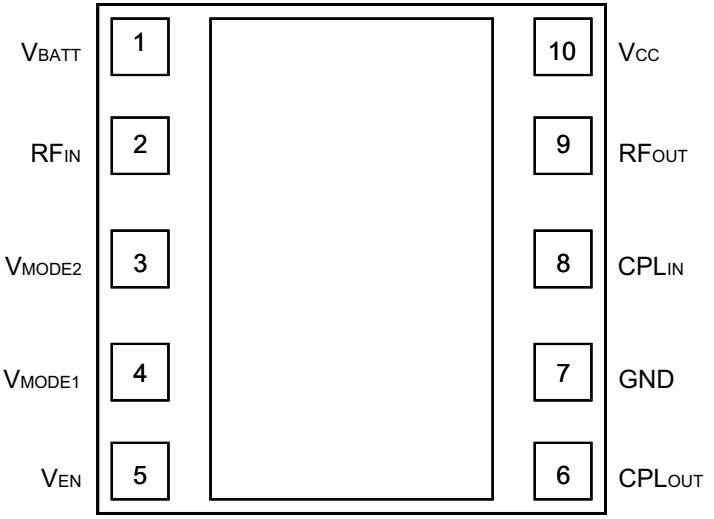


Figure 2: Pinout (X-ray Top View)

Table 1: Pin Description

PIN	NAME	DESCRIPTION
1	V_{BATT}	Battery Voltage
2	RF_{IN}	RF Input
3	V_{MODE2}	Mode Control Voltage 2
4	V_{MODE1}	Mode Control Voltage 1
5	V_{EN}	PA Enable Voltage
6	CPL_{OUT}	Coupler Output
7	GND	Ground
8	CPL_{IN}	Coupler Input
9	RF_{OUT}	RF Output
10	V_{CC}	Supply Voltage

ELECTRICAL CHARACTERISTICS

Table 2: Absolute Minimum and Maximum Ratings

PARAMETER	MIN	MAX	UNIT
Supply Voltage (V_{CC})	0	+5	V
Battery Voltage (V_{BATT})	0	+6	V
Control Voltages (V_{MODE1}, V_{MODE2}, V_{EN})	0	+3.5	V
RF Input Power (P_{IN})	-	+10	dBm
Storage Temperature (T_{STG})	-40	+150	°C

Stresses in excess of the absolute ratings may cause permanent damage. Functional operation is not implied under these conditions. Exposure to absolute ratings for extended periods of time may adversely affect reliability.

Table 3: Operating Ranges

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
Operating Frequency (f)	814	-	849	MHz	
Supply Voltage (V_{CC})	+3.1	+3.4	+4.35	V	P_{OUT} ≤ +28.4 dBm
Enable Voltage (V_{EN})	+1.35 0	+1.8 -	+3.1 +0.5	V	PA “on” PA “shut down”
Mode Control Voltage (V_{MODE1}, V_{MODE2})	+1.35 0	+1.8 -	+3.1 +0.5	V	Low Bias Mode High Bias Mode
WCDMA/UMTS Output Power (1, 3) R99, HPM HSPA (MPR = 0), HPM LTE(2) (MPR = 0), HPM R99, MPM LTE(2) & HSPA (MPR = 0), MPM R99, LPM LTE(2) & HSPA (MPR = 0), LPM	 27.6 26.6 26.4 - - - -	 28.4 27.4 27.2 17.0 16.0 8.0 7.0	 - - - - - - -	dBm	 3GPP TS 34.121-1, Rel 8 Table C.11.1.3 for WCDMA SUBTEST 1 TS 36.101 Rel 8 for LTE
CDMA Output Power (1, 3) HPM MPM LPM	 26.9 - -	 27.7 16.0 7.0	 - - -	dBm	 CDMA 2000, RC1
Case Temperature (T_C)	-40	-	+90	°C	

The device may be operated safely over these conditions; however, parametric performance is guaranteed only over the conditions defined in the electrical specifications.

Notes:

(1) For operation at 3.1 V, P_{OUT} is derated by 0.8 dB.

(2) LTE waveform characteristics: up to 15 MHz, QPSK, RB = 16.

(3) For operation at +105 °C, P_{OUT} is derated by 1.0 dB.

Table 4: Electrical Specifications - LTE Operation (RB = 12, START = 0, QPSK)
(T_C = +25 °C, V_{BATT} = V_{CC} = +3.4 V, V_{EN} = +1.8 V, 50 Ω system)

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS		
					P_{OUT}	V_{MODE1}	V_{MODE2}
Gain	26 16 10	29 19 13.5	32 22 16	dB	P_{OUT} = +27.2 dBm P_{OUT} = +16 dBm P_{OUT} = +7 dBm	0 V 1.8 V 1.8 V	0 V 0 V 1.8 V
ACLR E-UTRA at ± 10 MHz offset	- - -	-41 -40 -40	-35 -35 -35	dBc	P_{OUT} = +27.2 dBm P_{OUT} = +16 dBm P_{OUT} = +7 dBm	0 V 1.8 V 1.8 V	0 V 0 V 1.8 V
ACLR UTRA at ± 7.5 MHz offset	- - -	-40 -39 -40	-36 -36 -36	dBc	P_{OUT} = +27.2 dBm P_{OUT} = +16 dBm P_{OUT} = +7 dBm	0 V 1.8 V 1.8 V	0 V 0 V 1.8 V
ACLR UTRA at ± 12.5 MHz offset	- - -	-60 -58 -57	-40 -40 -40	dBc	P_{OUT} = +27.2 dBm P_{OUT} = +16 dBm P_{OUT} = +7 dBm	0 V 1.8 V 1.8 V	0 V 0 V 1.8 V
Power-Added Efficiency (1)	31 20 14	36 24 18	- - -	% % %	P_{OUT} = +27.2 dBm P_{OUT} = +16 dBm P_{OUT} = +7 dBm	0 V 1.8 V 1.8 V	0 V 0 V 1.8 V
Quiescent Current (Icq) Low Bias Mode	-	3	4.0	mA	through V_{CC} pin	1.8 V	1.8 V
Mode Control Current	-	0.06	0.15	mA	through V_{MODE} pins, V_{MODE} = 1.8 V		
Enable Current	-	0.04	0.12	mA	through V_{EN} pin		
BATT Current	-	0.7	1.2	mA	through V_{BATT} pin, V_{MODE1} = +1.8 V, V_{MODE2} = +1.8 V		
Leakage Current	-	<5	10	µA	V_{BATT} = +4.35 V, V_{CC} = +4.35 V, V_{EN} =0 V, V_{MODE} = 0 V, V_{MODE1} = 0 V		
Noise in Receive Band	-	-134	-	dBm/Hz	869 MHz to 894 MHz		
Harmonic 2fo 3fo, 4fo	- -	-48 -60	-35 -42	dBc	P_{OUT} ≤ 27.2 dBm		
Coupling Factor	-	20	-	dB			
Directivity	-	20	-	dB			
Coupler IN_OUT Daisy Chain Insertion Loss	-	<0.3	-	dB	698 MHz to 2620 MHz Pin 8 - 6, Shutdown Mode		
Spurious Output Level (all spurious outputs)	-	-	<-70	dBc	P_{OUT} < +27.2 dBm In-band Load VSWR < 5:1 Out-of-band Load VSWR < 10:1 Applies over all operating conditions		
Load mismatch stress with no permanent degradation or failure	8:1	-	-	VSWR	Applies over all operating conditions		

Notes:
(1) ACLR and Efficiency measured at 832 MHz.

Table 5: Electrical Specifications - WCDMA Operation (R99 Modulation)
(T_C = +25 °C, V_{CC} = +3.4 V, V_{BATT} = +3.4 V, V_{EN} = +1.8 V, 50 Ω system)

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS		
					P_{OUT}	V_{MODE1}	V_{MODE2}
Gain	26 16 10	29 19 13.5	32 22 16	dB	P_{OUT} = +28.4 dBm P_{OUT} = +17 dBm P_{OUT} = +8 dBm	0 V 1.8 V 1.8 V	0 V 0 V 1.8 V
ACLR1 at 5 MHz offset (1)	- - -	-41 -42 -40	-37 -37 -37	dBc	P_{OUT} = +28.4 dBm P_{OUT} = +17 dBm P_{OUT} = +8 dBm	0 V 1.8 V 1.8 V	0 V 0 V 1.8 V
ACLR2 at 10 MHz offset	- - -	-57 -58 -59	-48 -48 -48	dBc	P_{OUT} = +28.4 dBm P_{OUT} = +17 dBm P_{OUT} = +8 dBm	0 V 1.8 V 1.8 V	0 V 0 V 1.8 V
Power-Added Efficiency (1)	36 23 - 16 -	40 27 18 20 11	- - - - -	%	P_{OUT} = +28.4 dBm P_{OUT} = +17 dBm P_{OUT} = +13.5 dBm P_{OUT} = +8 dBm P_{OUT} = +3.5 dBm	0 V 1.8 V 1.8 V 1.8 V 1.8 V	0 V 0 V 0 V 1.8 V 1.8 V
Spurious Output Level (all spurious outputs)	-	-	-70	dBc	P_{OUT} < +28.4 dBm In-band load VSWR < 5:1 Out-of-band load VSWR < 10:1 Applies over all operating conditions		
Load mismatch stress with no permanent degradation or failure	8:1	-	-	VSWR	Applies over full operating range		

Notes:
(1) ACLR and Efficiency measured at 832 MHz.

Table 6: Electrical Specifications - CDMA2000 Operation (RC-1 waveform)
(T_C = +25 °C, V_{BATT} = V_{CC} = +3.4 V, V_{ENABLE} = +1.8 V, 50 Ω system)

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS		
					P_{OUT}	V_{MODE1}	V_{MODE2}
Gain	26 16 10	29 19 13.5	32 22 16	dB	P_{OUT} = +27.7 dBm P_{OUT} = +16 dBm P_{OUT} = +7 dBm	0 V 1.8 V 1.8 V	0 V 0 V 1.8 V
Adjacent Channel Power at ±885 kHz offset (1) Primary Channel BW = 1.23 MHz Adjacent Channel BW = 30 kHz	- - -	-50 -50 -50	-46.5 -46.5 -46.5	dBc	P_{OUT} = +27.7 dBm P_{OUT} = +16 dBm P_{OUT} = +7 dBm	0 V 1.8 V 1.8 V	0 V 0 V 1.8 V
Adjacent Channel Power at ±1.98 MHz offset (1) Primary Channel BW = 1.23 MHz Adjacent Channel BW = 30 kHz	- - -	-59 -60 -60	-56 -56 -56	dBc	P_{OUT} = +27.7 dBm P_{OUT} = +16 dBm P_{OUT} = +7 dBm	0 V 1.8 V 1.8 V	0 V 0 V 1.8 V
Power-Added Efficiency (1)	33 20 13	37 23 17	- - -	%	P_{OUT} = +27.7 dBm P_{OUT} = +16 dBm P_{OUT} = +7 dBm	0 V 1.8 V 1.8 V	0 V 0 V 1.8 V
Spurious Output Level (all spurious outputs)	-	-	-70	dBc	P_{OUT} < +27.7 dBm In-band Load VSWR < 5:1 Out-of-band Load VSWR < 10:1 Applies over all operating conditions		
Load mismatch stress with no permanent degradation or failure	8:1	-	-	VSWR	Applies over all operating conditions		

Notes:
(1) ACLR and Efficiency measured at 832 MHz.

APPLICATION INFORMATION

To ensure proper performance, refer to all related Application Notes on the ANADIGICS web site: http://www.anadigics.com

Shutdown Mode

The power amplifier may be placed in a shutdown mode by applying logic low levels (see Operating Ranges table) to the V_{EN}, V_{MODE1} and V_{MODE2} voltages.

Bias Modes

The power amplifier may be placed in either Low, Medium or High Bias modes by applying the appropriate logic level (see Operating Ranges table) to the V_{MODE} voltages. The Bias Control table below lists the recommended modes of operation for various applications.

Three operating modes are recommended to optimize current consumption. High Bias/High Power operating mode is for P_{OUT} levels $\geq$ 17 dBm. At ~17dBm - 8 dBm, the PA should be "Mode Switched" to Medium Power Mode. For P_{OUT} levels $\leq$ ~7 dBm, the PA can be switched to Low Power Mode for even lower quiescent current consumption.

Table 7: Bias Control

APPLICATION	P_{OUT} LEVELS	BIAS MODE	V_{EN}	V_{MODE1}	V_{MODE2}	V_{CC}	V_{BATT}
Low power (Low Bias Mode)	≤ +7 dBm	Low	+1.8 V	+1.8 V	+1.8 V	3.1 - 4.35 V	> 3.1 V
Med power (Medium Bias Mode)	> 7 dBm ≤ +17 dBm	Low	+1.8 V	+1.8 V	0 V	3.1 - 4.35 V	> 3.1 V
High power (High Bias Mode)	> +17 dBm	High	+1.8 V	0 V	0 V	3.1 - 4.35 V	> 3.1 V
Shutdown	-	Shutdown	0 V	0 V	0 V	3.1 - 4.35 V	> 3.1 V

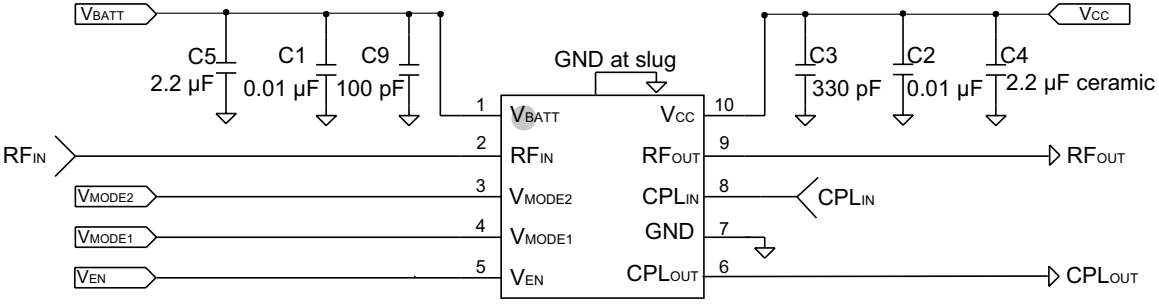


Figure 3: Evaluation Board Schematic

Performance Data Plots:

Figure 4: LTE Gain (dB) over Temperature (V_{BATT} = V_{CC} = 3.4 V)

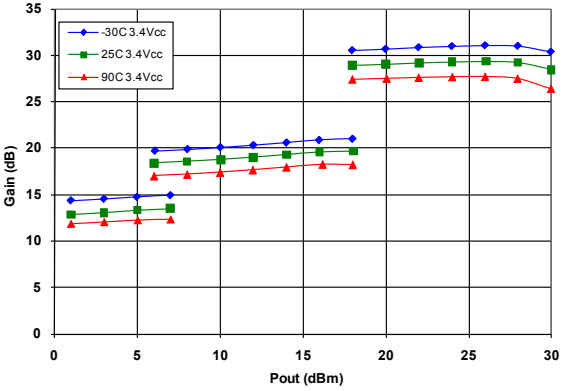


Figure 5: LTE Gain (dB) over Voltage (T_C = 25 °C)

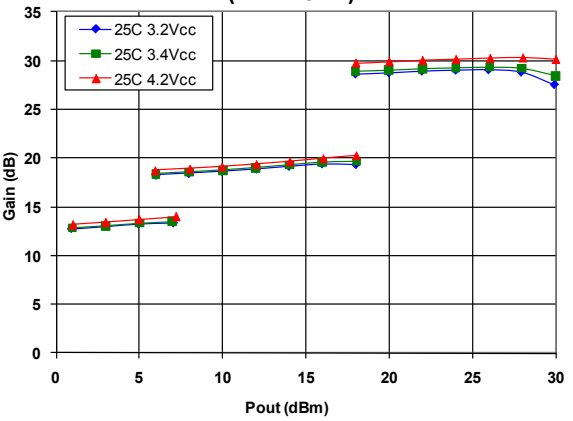


Figure 6: LTE PAE (%) over Temperature (V_{BATT} = V_{CC} = 3.4 V)

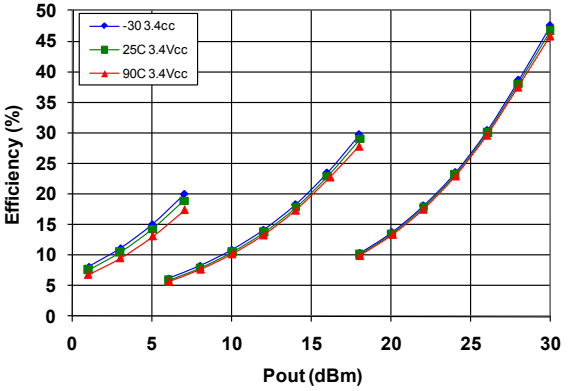


Figure 7: LTE PAE (%) over Voltage (T_C = 25 °C)

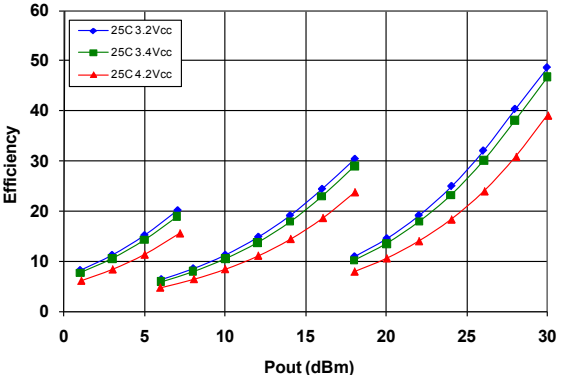


Figure 8: LTE ACLR1 (dBc) over Temperature (V_{BATT} = V_{CC} = 3.4 V)

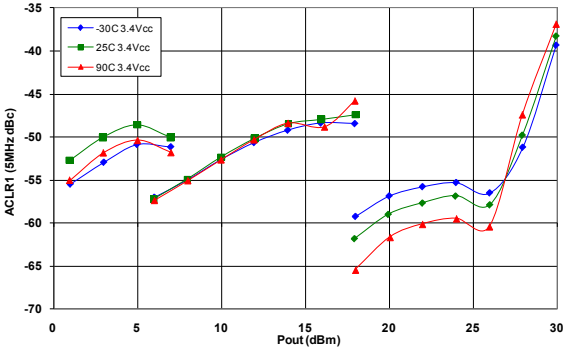
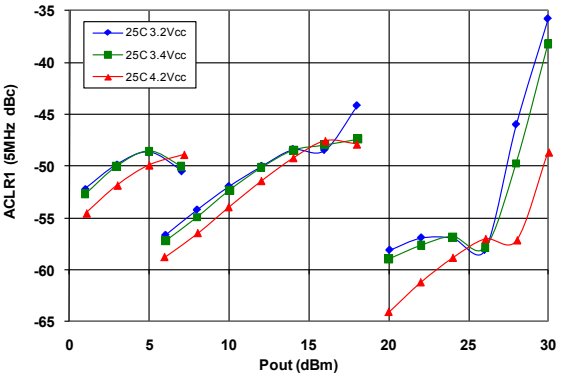
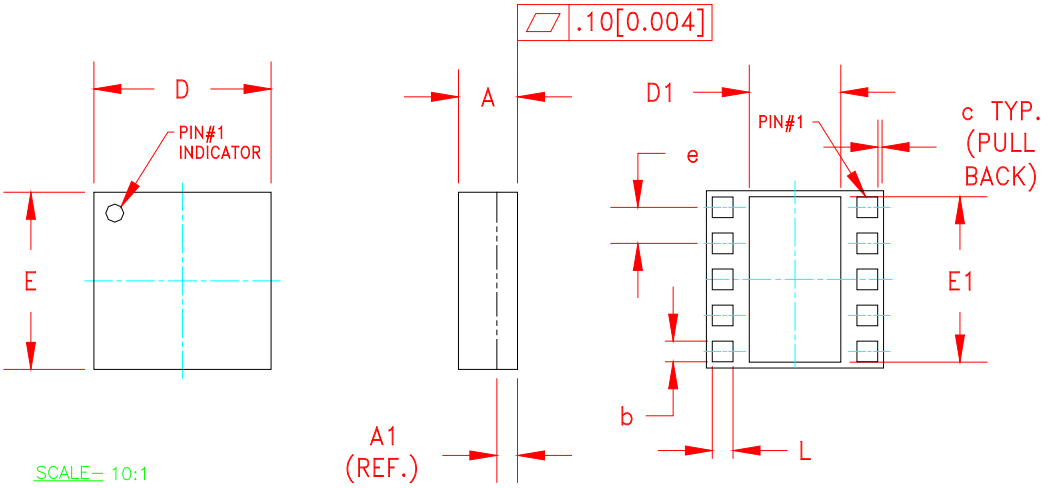


Figure 9: LTE ACLR1 (dBc) over Voltage (T_C = 25 °C)



PACKAGE OUTLINE



SYMBOL	MILLIMETERS			INCHES			NOTE
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	
A	0.91	1.03	1.13	0.035	0.041	0.044	–
A1	PLEASE REFER TO LAMINATE CONTROL DRAWING						–
b	0.32	0.35	0.40	0.013	0.014	0.016	3
c	–	0.10	–	–	0.004	–	–
D	2.88	3.00	3.12	0.113	0.118	0.123	–
D1	1.45	1.50	1.57	0.057	0.059	0.062	3
E	2.88	3.00	3.12	0.113	0.118	0.123	–
E1	2.70	2.75	2.85	0.106	0.108	0.112	3
e		0.60			0.024		3
L	0.32	0.35	0.40	0.013	0.014	0.016	3

NOTES:

1. CONTROLLING DIMENSIONS: MILLIMETERS
2. UNLESS SPECIFIED TOLERANCE=±0.076[0.003].
3. PADS (INCLUDING CENTER) SHOWN UNIFORM SIZE FOR REFERENCE ONLY. ACTUAL PAD SIZE AND LOCATION WILL VARY WITHIN MIN. AND MAX. DIMENSIONS ACCORDING TO SPECIFIC LAMINATE DESIGN.
4. UNLESS SPECIFIED DIMENSIONS ARE SYMMETRICAL ABOUT CENTER LINES SHOWN.
5. LAMINATE CONTROL DRAWING SPECIFIED BY PART NUMBER.

Figure 10: M45 Package Outline - 10 Pin 3 mm x 3 mm x 1 mm Surface Mount Module

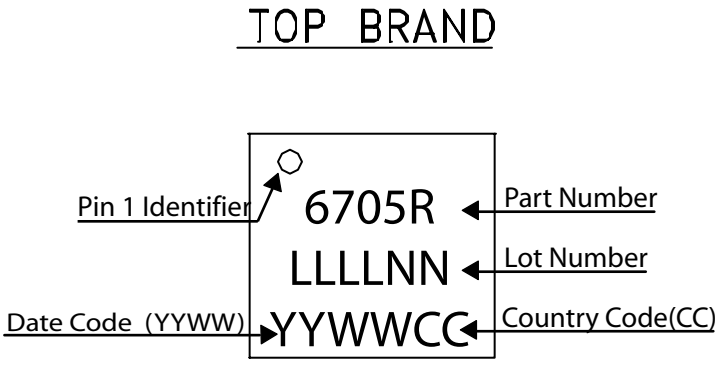
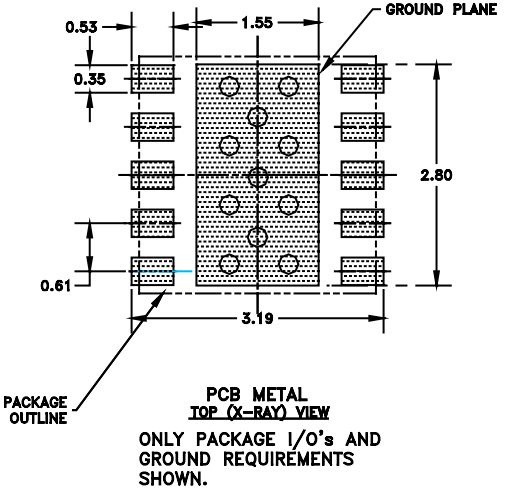


Figure 11: Branding Specification - M45 Package

PCB AND STENCIL DESIGN GUIDELINE



NOTES:

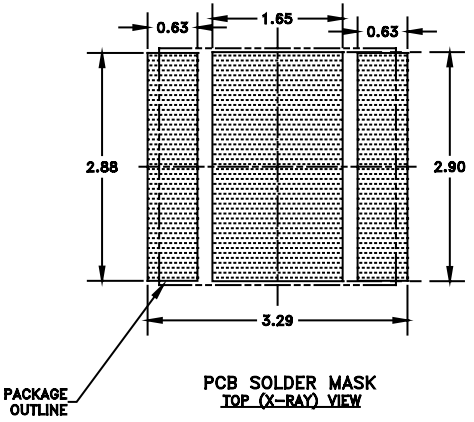
(1) OUTLINE DRAWING REFERENCE: P8002478_E

(2) UNLESS SPECIFIED DIMENSIONS ARE SYMMETRICAL ABOUT CENTER LINES SHOWN.

(3) DIMENSIONS IN MILLIMETERS.

(4) VIAS SHOWN IN PCB METAL VIEW ARE FOR REFERENCE ONLY. NUMBER & SIZE OF THERMAL VIAS REQUIRED DEPENDENT ON HEAT DISSIPATION REQUIREMENT AND THE PCB PROCESS CAPABILITY.

(5) RECOMMENDED STENCIL THICKNESS: APPROX. 0.150mm (6 Mils)



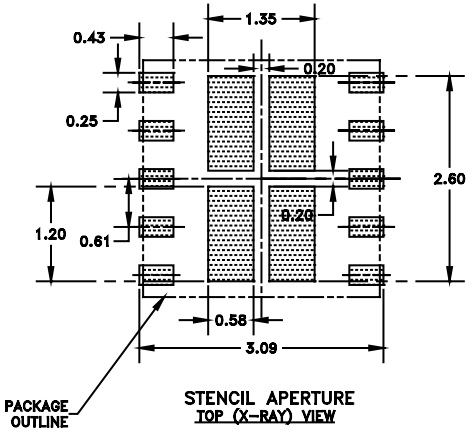
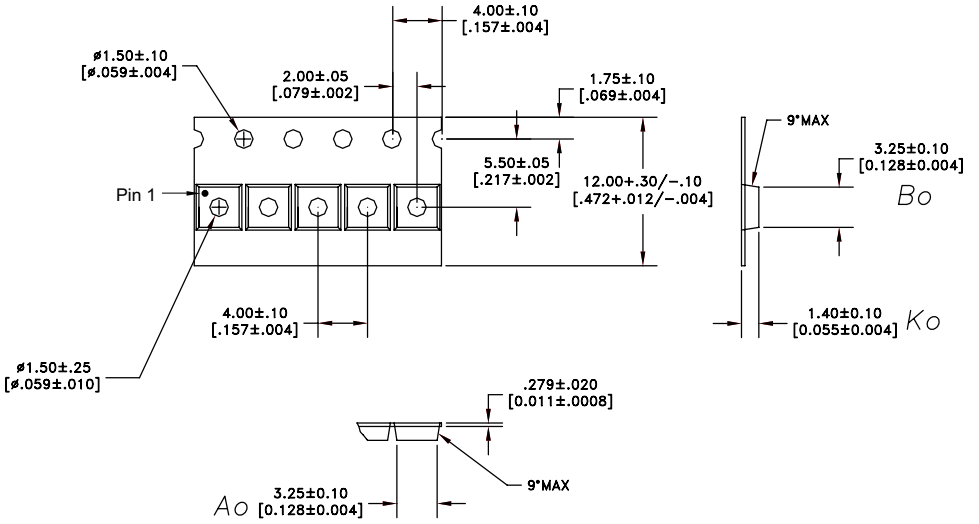


Figure 12: Recommended PCB Layout Information

COMPONENT PACKAGING



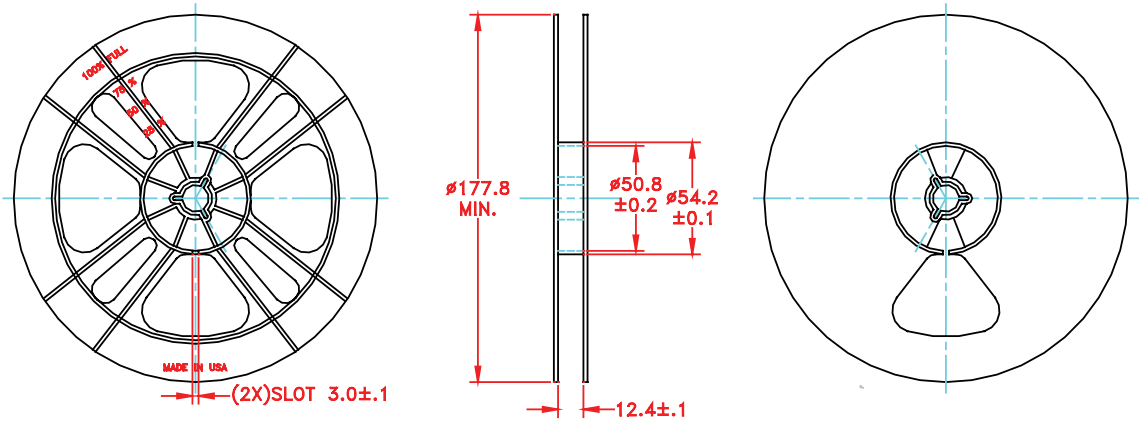
NOTES:

1. MATERIAL: 3000 (CARBON FILLED POLYCARBONATE)
100% RECYCLABLE.

DIMENSIONS ARE IN MILLIMETERS [INCHES]

DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994

Figure 13: Carrier Tape



DIMENSIONS ARE IN MILLIMETERS

NOTES:

1. MATERIAL: BLACK CARBON POLYSTYRENE
SURFACE RESISTIVITY: $1X10^4$ TO $1X10^5$ ohms/square

DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994

Figure 14: Reel

ORDERING INFORMATION

ORDER NUMBER	TEMPERATURE RANGE	PACKAGE DESCRIPTION	COMPONENT PACKAGING
ALT6705RM45Q7	-40 °C to +90 °C	RoHS Compliant 10 Pin 3 mm x 3 mm x 1 mm Surface Mount Module	Tape and Reel, 2500 pieces per Reel
ALT6705RM45P9	-40 °C to +90 °C	RoHS Compliant 10 Pin 3 mm x 3 mm x 1 mm Surface Mount Module	Partial Tape and Reel

ANADIGICS
141 Mount Bethel Road
Warren, New Jersey 07059, U.S.A.
Tel: +1 (908) 668-5000
Fax: +1 (908) 668-5132

URL: http://www.anadigics.com